Calibration-Kit Design for Millimeter-Wave Silicon Integrated Circuits*

Dylan F. Williams, *Fellow*, *IEEE*, Phillip Corson, Jahnavi Sharma, Harish Krishnaswamy, Wei Tai, Zacharias George, David Ricketts, Paul Watson, Eric Dacquay, Sorin Voinigescu

***Abstract*—We study and present design guidelines for thru-reflect-line vector-network-analyzer calibration kits used for characterizing circuits and transistors fabricated on silicon integrated circuits at millimeter-wave frequencies. We compare contact-pad designs and develop fixed-fill contacts that achieve both repeatable and low contact-pad capacitances. We develop a fill-free and mesh-free transmission line structure for the calibration kit and compare it to similar transmission lines with meshed ground plane. We also develop a gold plating process that greatly improves contact repeatability, permitting the use of redundant multiline calibrations. This in turn simplifies the development of an error analysis. Finally, we apply the technique to state-of-the-art transistor characterization, and present measured results with uncertainties.**

***Index Terms*—Calibration, measurement, millimeter-wave, scattering parameters, silicon, transistor, uncertainty, vector network analyzer.**

I. Introduction

We study the contact pads, ground-plane meshes, and number of transmission lines used in millimeter-wave thru-reflect-line (TRL) vector-network-analyzer calibration kits fabricated in the IBM 45-nm complementary metal-oxide-semiconductor (CMOS) silicon-on-insulator SOI12S0 integrated-circuit process.[1] This leads to straight-forward guidelines for calibration-kit design. We then apply the calibration kits to transistor characterization and explore their frequency limitations.

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[1] We use brand names only to better specify the experimental conditions. The National Institute of Standards and Technology does not endorse commercial products. Other products may work as well or better.

Vector-network-analyzer calibrations used to characterize silicon transistors are usually performed on commercial impedance-standard substrates fabricated on an alumina substrate with an SOLT, line-reflect-match (LRM) [1], line-reflect-reflect-match (LRRM) [2], or similar calibration algorithm. This first tier calibration moves the calibration reference plane "to the probe tips." The first-tier probe-tip calibration is then often followed by a second-tier calibration intended to move the calibration reference plane from the probe tips to the transistor terminals [3-5]. These second tier calibrations are used to subtract out the electrical parasitics associated with contact pads, short transmission lines in the interconnect stack separating the contact pads from the transistors, and access vias connecting those transmission lines to transistors fabricated in the silicon substrate.

The TRL calibration method avoids calibrating at the probe tip, where the lack of a transmission line makes it difficult to rigorously define voltages, currents, and wave parameters. The TRL calibration is unique in that it puts the calibration reference plane directly in a transmission line where wave parameters, voltages, and currents can be rigourously defined. The TRL calibration does this by measuring traveling-wave amplitudes in a single-mode transmission line at the center of a thru with no recourse to any assumptions with respect to symmetry, loss, or the lumped-element nature of the standards [6]. For this reason, the TRL calibration has been adopted as the calibration of reference for coaxial measurements at microwave frequencies.

References [7] and [8] introduced an accurate approach for determining the characteristic impedance of small printed transmission lines from the propagation constant measured by the TRL calibration. This advance allows the reference impedance of on-wafer TRL calibrations to be accurately set to 50 Ω when the lines are quasi-TEM and employ low-loss dielectrics, and has led to the TRL calibration also being adopted as the calibration of reference for on-wafer measurements at microwave frequencies [2;9-11]. Furthermore, approaches that make use of redundant calibration standards [12-15] have overcome the bandwidth limitations of the early TRL algorithms.

Because the TRL calibration makes few assumptions about the calibration standards, it is particularly well suited to performing measurements at millimeter-wave frequencies and beyond, and recent work has demonstrated accurate transistor characterization to 750 GHz with the TRL approach [16]. The fundamental nature of the TRL calibration also simplifies the

development of error analyses, and reasonable error estimates can be obtained simply with the use of the same redundant calibration standards used to extend the bandwidth of the calibrations [13-15].

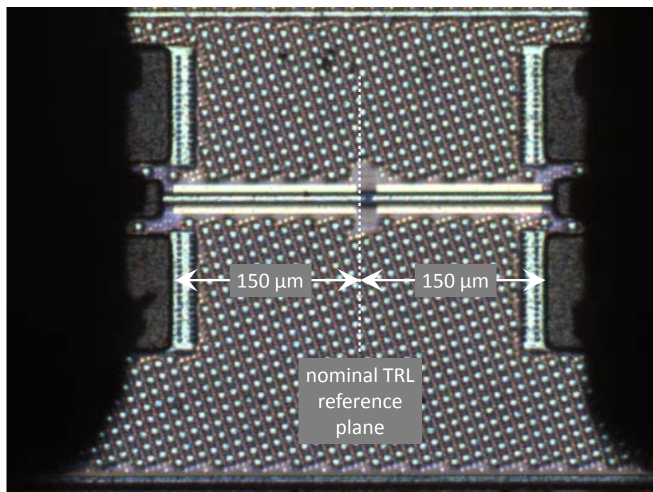
TRL calibrations are not typically used to characterize silicon transistors in part because of the expense of fabricating the TRL standards on the silicon die, the difficulty of repeatedly forming good contacts with the aluminum or copper contact pads on the silicon die, the difficulty of performing accurate measurements at very low frequencies with TRL calibrations, and the availability of commercial impedance-standard substrates supporting short-open-load, line-reflect-match, and similar lumped-element-based calibrations with good accuracy at frequencies suitable for characterizing slower silicon devices. Layout and automated testing is also complicated by the need for transmission lines of different lengths. As a result, most silicon transistors are characterized by building microstrip lines, or closely related conductor-backed coplanar lines, in the metal interconnect stack, typically using multilayered grounds stitched together with vias, and off-wafer lumped-element calibrations with easy-to-contact gold-plated contact pads.

However, as the speed of silicon transistors has improved, so has the need for accurate high-frequency vector-network-analyzer calibrations for characterizing transistors fabricated on silicon. In this paper, we examine the fundamental limitations of TRL calibrations performed in the interconnect stack of the SOI12S0 integrated-circuit process. We show that gold plating can be used to improve the repeatability of contacts to transmission lines fabricated on silicon die. This greatly improves the accuracy and reliability of TRL calibrations performed directly on silicon wafers. We also show that field penetration into the silicon is low, allowing the methods described in [7;8] to be used to set the reference impedance of the TRL calibration accurately, and that the loss of the small microstrip lines fabricated in the interconnect stack is not too large to prevent the algorithm from converging. We demonstrate the TRL calibration in the SOI12S0 integrated-circuit process with transistor measurements at millimeter wavelengths, and show that the calibration continues to behave well far into the sub-millimeter wavelength region.

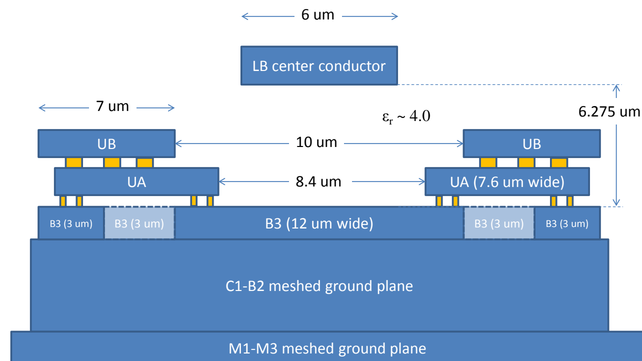
II. TRL Calibration Kit

Figure 1 shows a photograph of a typical test structure we fabricated with its contact pads and 150 µm long microstrip access lines, as well as a sketch of the cross section of the microstrip transmission lines we used. We used contact pads and access lines of the same design for the test structures, devices under test, and in the calibration kit to minimize calibration and measurement errors.

We supplemented the 300 µm long thru line in the TRL calibration kit with a pair of symmetric shorts offset by 150 µm from the contact pads, and four transmission lines of additional length 200 µm, 300 µm, 800 µm, and 2000 µm. This design sets the initial reference plane of the TRL calibration 150 µm from the contact pads in the center of the thru line. This position corresponds to the input at the left of the transistor, as shown in the figure. The multiple lines allow us to perform broadband TRL calibration.



(a) Photograph of a test structure showing the contact pads, access lines, and device under test. The signal contact pads are 40-µm-long and 30-µm-wide, and are separated from the ground contact pads by 15 µm. Some of the automated fill on the top metal layers can be seen in the photograph. The photograph also shows some inadvertent top-metal-level fill directly around the contact pads that we could have eliminated with an additional exclusion layer.



(b) Cross-section of the transmission line.

Fig. 1. The transmission-line calibration artifacts and test structures we employed. The interconnect stack supports 11 levels of metal:

We fabricated the access lines and transmission lines used in the TRL calibration kit in the interconnect stack of the IBM 45-nm CMOS silicon-on-insulator SOI12S0 integrated-circuit process (see Fig. 1). That technology supports three thick metal and dielectric layers at the top of the interconnect stack. We fabricated our transmission-line center conductor in the top-most LB layer, and were able to completely suppress metal fill in the two UA and UB layers below this top-most LB layer over a 24 µm width while adhering to the design

rules. The center conductor was 6 μm wide and supported by approximately 6.275 μm of dielectric with a relative dielectric constant of about 4.0. This put the nominal characteristic impedance of the transmission lines at about 75 Ω, a reasonable match to our nominally 50 Ω probes.

To set the reference impedance of the TRL calibration to 50 Ω, we first determined the capacitance per unit length of the line at low frequencies with the load method of [8]. However, as we did not have an on-wafer load, we used an off-wafer load instead, potentially adding some error into the overall reference impedance of the calibration. Then we determined the actual characteristic impedance of the lines from the measured propagation constant with the method of [7], which works well in low-loss dielectrics. This provided us with the information needed to account for the complex characteristic impedance of these transmission lines and to transform the reference impedance of the TRL calibration to 50 Ω. This correction is important even when nominally 50 Ω transmission lines are used in the calibration, because the actual characteristic impedance of printed lines becomes large at low frequencies as the resistance per unit length of the lines becomes comparable to the inductive reactance per unit length of the lines.

We formed the ground plane from the fourth level of metal (B3) from the top of the interconnect stack. This solid level of metal was 12 μm wide and approximately 255 nm thick. To meet the design rules for the IBM process, we added 3 μm wide strips of B3 metal spaced 3 μm from these 12 μm wide ground lines and tied the ground plane together with 7.6 μm and 7.0 μm wide strips in the next two higher levels of metal UB and UA, as shown in Fig. 1. We also meshed together all of the lower levels of metal below the B3 ground plane.

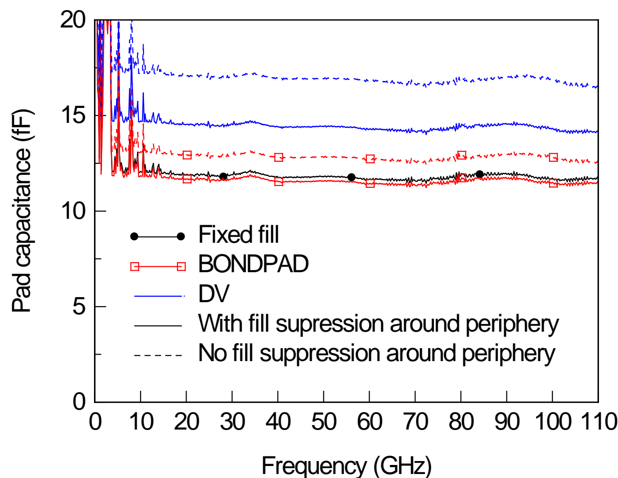


Fig. 2. Measured capacitances of contact pads of the same area but with different fill. Only one version of the fixed-fill design was fabricated, and that design had fill suppression around the periphery.

III. Contact-Pad Design

We optimized our calibration-kit design to reduce contact-pad capacitance and improve contact resistance.

A. *Contact-pad capacitance*

The TRL calibration corrects for the electrical behavior of the vector network analyzer, probes, contact pads, and accesses lines. After the calibration is performed, the measurement reference plane is set in the center of the thru, and the initial reference impedance of the calibration is transformed to 50 Ω.

Although the calibration corrects for the capacitance of the contact pads, the capacitance of the pads is large enough at millimeter-wave frequencies to adversely impact measurements. For example, a contact-pad capacitance of 17 fF corresponds to a shunt impedance of less than 100 Ω at 100 GHz, a parasitic that is of the same order of magnitude as the impedance of the measurement system. Equally important, the calibration does not correct for differences in contact-pad capacitance from calibration artifact to calibration artifact and from calibration artifact to device under test.

Reference [17] suggests opening windows under contact pads to reduce pad capacitance. However, this approach was developed for interconnect stacks with only a few metal layers and thinner dielectrics than in the IBM technology, and our electromagnetic simulations indicated that this approach does little to reduce contact-pad capacitance in this technology.

To minimize the impact of contact-pad capacitance in our technology, following [17], we first selected a 40-μm-long by 30-μm-wide contact-pad. This was the smallest size we felt that we could make these contact pads without adversely impacting contact reliability.

We then investigated the impact of fill strategy on the capacitance of the contact pad. Figure 2 shows the measured capacitance of several contact pads with this geometry as a function of the type of fill used under the contact pads. The dashed curve marked with hollow circles and labeled "DV" corresponds to opening a hole in the passivation over a 40-μm-long by 30-μm-wide contact pad and allowing the automated IBM routines to place fill under and around the pad. The solid curve marked with hollow circles corresponds to the same pad, except that fill was suppressed around its periphery. The figure shows that suppressing the fill around the pad significantly reduces contact-pad capacitance.

The curve labeled "BONDPAD" corresponds to the same contact pad, but uses fill automatically generated by IBM to reduce the capacitance of wire-bond pads. Using this special fill pattern further reduces the capacitance of the contact pad. The figure also shows that eliminating the fill around the periphery reduces the capacitance of these contact pads even further.

While the capacitance of contact pads using fill automatically generated by IBM to reduce the capacitance of wire-bond pads is low, the actual placement of the fill depends on nearby structures, potentially changing the capacitance of the pad. Because the calibration does not correct for changing pad capacitances, we took extra steps to ensure the uniformity of the contact-pad capacitance over the die by replacing the automatically generated IBM fill with a fixed fill pattern. This fixed fill pattern is similar to the actual automated fill patterns generated by the IBM fill software. The capacitance of this contact pad is labeled "Fixed fill" in Fig. 2, and is nearly equal to that of the low-capacitance IBM "BONDPAD" fill with fill suppression around the pad periphery. However, it has the additional advantage that the fill pattern is independent of position on the die. For this reason, we used this fixed fill pattern under the contact pads that we used in our TRL calibration kit and test structures.

B. *Contact-pad metallization*

The IBM process we used employs aluminum for the top-metal level. However, obtaining reliable probe connections to aluminum contact pads, which oxidize quickly, is very challenging, and can depend both on the type of probe employed, the number of previous contacts on the pad, and the skill of the operator. For example, [4] showed that errors due to contact-pad repeatability dominate over errors due to test-set drift over an eight-hour period. To remedy this, we developed a process based on [18;19] for gold-plating the aluminum contact pads fabricated at IBM.

Figure 3 compares measurements of the total resistance of the bias tee, probe, contact, line, and via of six offset shorts using a standard microwave probe with beryllium-copper tips. Two of the offset shorts had pads that were plated with gold, and four of the offset shorts had bare aluminum pads. Figure 3 shows clearly that the gold-plated pads improve the DC contact resistance significantly.

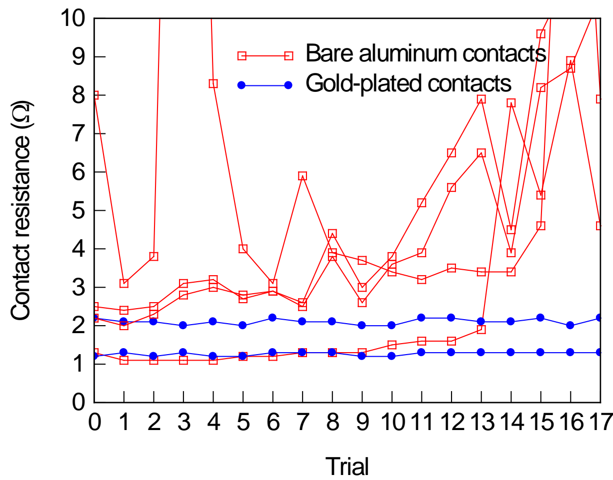
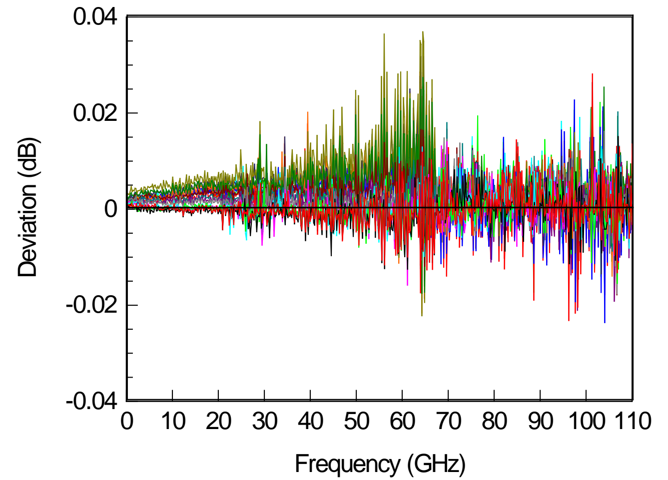


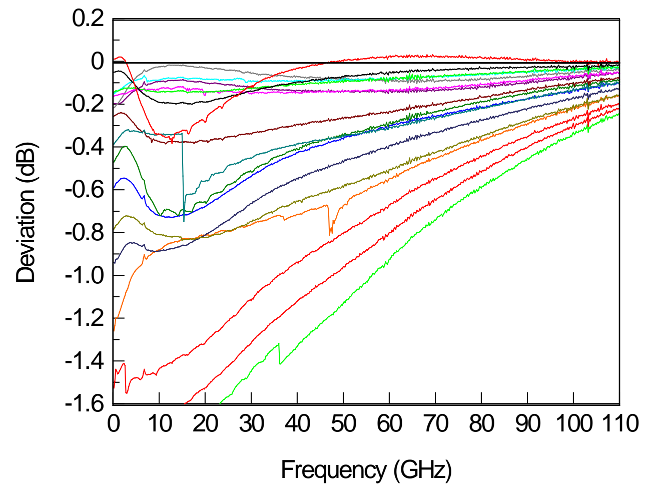
Fig. 3. Measured contact resistances.

Figures 4a and 4b compare repeated measurements of the reflection coefficient of a short with and without gold-plated contact pads using the same probes and operator. Again, the improvement in contact repeatability is evident. These observations are consistent with those of [4], which also demonstrated that contact-pad resistance is more difficult to control on aluminum pads than on gold pads.

Of course, we might have obtained better results on the bare aluminum pads had we used probes designed specifically for that purpose. Nevertheless, the improvement we obtained in contact repeatability by gold-plating our contact pads with our probes designed with beryllium-copper tips was fairly dramatic, and might expect benefits even with probes developed specifically for aluminum pads as well. Finally, we noted a strong correlation between the RF repeatability of our probes and the DC repeatability. This suggests that monitoring DC resistance during microwave measurements as a tool for detecting poor contact repeatability at microwave frequencies.



(a) Repeatability of the reflection coefficient of a short measured with gold-plated aluminum contacts.



(b) Repeatability of the reflection coefficient of a short measured with standard aluminum contacts

Fig. 4. Comparison of measurements of offset shorts made with bare and gold-plated aluminum contact pads.

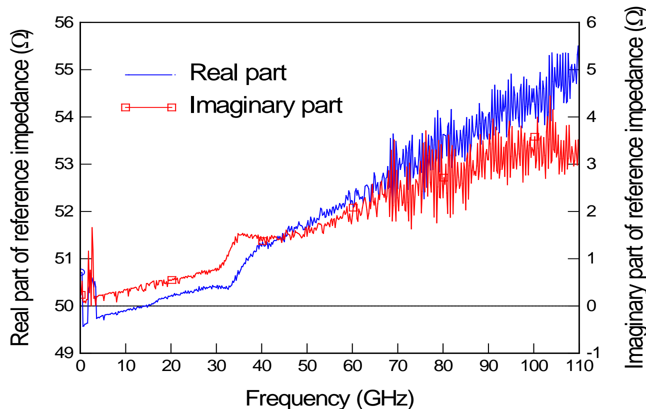


Fig. 5. Reference impedance of our TRL calibration determined by comparison to a probe-tip SOLT calibration.

IV. Reference Impedance

We mentioned above that we set the reference impedance of the TRL calibration to 50 Ω with the capacitance per unit length of the line at low frequencies determined from the load method of [8] and the measured propagation constant [7]. This procedure requires a constant capacitance C per unit length of transmission line and a small $G/\omega C$, where G is the conductance per unit length of the transmission line. These conditions are usually satisfied when low-loss dielectrics are used in the construction of the transmission lines, and previous comparisons to calibrations on an impedance-standard substrate indicate that most transmission lines in a silicon interconnect stack meet these criteria [5].

We used an approximate SOLT probe-tip calibration performed on a commercial calibration substrate and the calibration comparison method of [20] to verify, to the extent possible, the accuracy of the reference impedance of our TRL calibration, and thus our assumption of constant capacitance C per unit length of transmission line and a small $G/\omega C$ in our transmission lines. This approach is similar to that employed in [21]. As we cannot expect the SOLT calibration to be accurate at high frequencies, and the TRL calibration fails at very low frequencies, we only expect this comparison between the two calibrations to work well only at moderate microwave frequencies.

Figure 5 shows the reference impedance of the TRL calibration that we estimated from this approach. Most importantly, the imaginary part of the reference impedance appears linear. This is more likely due to an error in the inductance of the resistor suggested by the manufacturer for use in the SOLT calibration, than to loss in the dielectric material in the interconnect stack, which would typically manifest itself as a constant loss tangent, and thus, a constant offset in the imaginary component of the TRL reference impedance.

The half ohm offset in the low-frequency limit of the real part of the reference impedance of the TRL calibration indicates an error in setting the DC value of the capacitance C in the TRL algorithm [7;8]. This offset is not surprising, given that we did not have an on-wafer resistor with which to estimate the capacitance per unit length of our transmission lines.

Finally, the figure shows a weak resonance in the reference impedance at about 35 GHz. It may be due to a problem with the SOLT calibration, with the approximations involved in the calibration comparison method itself [20], or a manifestation of unexpected behavior in the dielectrics in the interconnect stack in which we built our transmission lines. Without further information, we are unable to identify the source of this behavior.

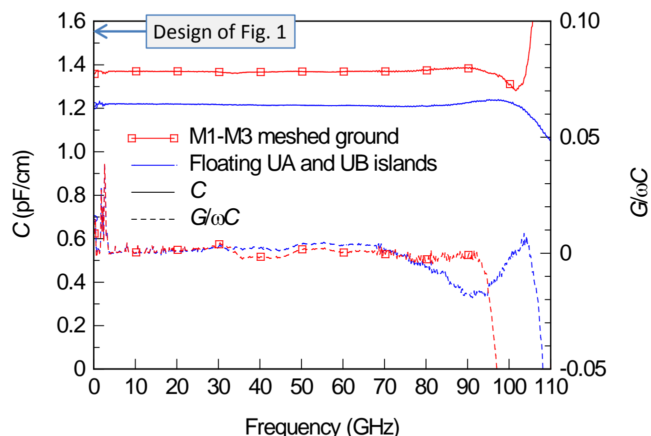
V. Ground-Plane Design

The transmission lines we employed were fabricated on top of a lossy doped silicon substrate. Furthermore, ground planes in this technology are often meshed, raising the possibility that fields might penetrate through them and into the silicon substrate, and potentially violate the key assumptions of constant capacitance and zero conductance used to set the reference impedance to 50 Ω. While we did not see evidence of this in the reference impedance we estimated in the last section from the calibration-comparison method, we further searched for evidence of field penetration through our ground planes by constructing transmission lines with thinner ground planes and constructing transmission lines with floating fill, and comparing them to our nominal transmission lines. Our intent was to try to detect any issues with field penetration or fill by exaggerating them in these additional transmission lines, and then comparing them to our nominal transmission lines.

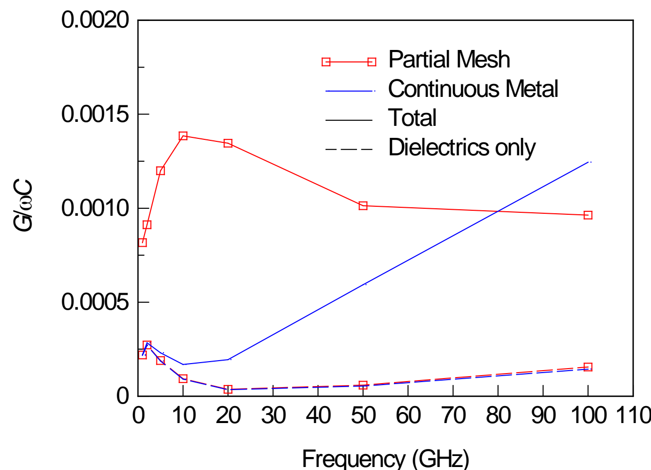
As indicated in Fig. 1, the IBM technology we used affords a great deal of flexibility in the construction of the ground plane. We chose B3, the fourth level of metal from the top, for the nominal ground planes we used in our TRL calibrations. We chose B3 in part because the IBM design rules do not require this metal level to be meshed over a 12 μm width, and in part because the lower levels of metal and dielectrics are so thin that using B3 for the ground does not significantly decrease the overall dielectric thickness. Furthermore, we meshed all of the lower levels of metal available to us together, and attached them to B3 with periodic vias, limiting field penetration through the metals to the greatest extent possible. Thus, our nominal approach should minimize field penetration into the substrate, and best satisfy the conditions of constant capacitance and small conductance required by the calibration, while keeping the impedance of the lines high.

To verify the conditions C constant and $G/\omega C$ are also small when the ground planes are thinner, contain floating fill, or are meshed, we fabricated two additional TRL calibration kits comprised of a thru line and an additional 650 μm long line. The first calibration kit used the ground-plane design shown in Fig. 1 except that the grounded UA and UB strips were replaced with floating islands. The second calibration kit used a meshed ground plane in the bottom three levels of metal M1, M2, and M3 in the interconnect stack. These three lowest metal levels are approximately 140 nm thick, meshed, and tied together with arrays of vias.

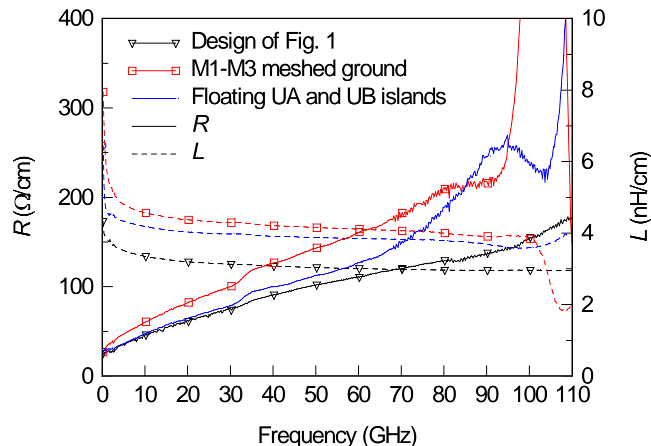
We used the calibration-comparison method of [2] with the recommended algorithm of [20] to compare these two transmission lines to our nominal transmission line shown in Fig. 1. This allowed us to estimate the characteristic impedance of these transmission lines from the characteristic impedance of our nominal lines calculated from the constant-capacitance assumption of [7]. We then used the propagation constants of these lines estimated from the TRL calibrations to estimate the capacitance and conductance per unit length of the lines shown in Fig. 6. The curve labeled “Floating UA and UB islands” correspond to the configuration of Fig. 1 with



(a) Measured capacitance and conductance.



(b) Simulated conductance.



(c) Resistance and inductance.

Fig. 6. Comparison of measured and simulated transmission-line parameters.

floating UA and UB islands instead of strips tied to ground with arrays of vias, and the curve labeled "M1-M3 meshed ground" corresponds to our meshed ground plane in the lowest three metal levels M1, M2, and M3.

A. Capacitance and conductance per unit length

First, we note from that the measured capacitances per unit length of the transmission lines in Fig. 6a compare well with the fixed capacitance of 1.55 pF/cm we estimated for our nominal transmission lines shown in Fig. 1 with the load method of [8] below 50 GHz. While we must treat the measurements above 50 GHz with some caution, as the approximations that we employed to estimate the parameters plotted in Fig. 6 begin to fail at higher frequencies [20] and the larger deviations above 90 GHz may be due to instrumentation errors, these measurements are a good indication that the capacitances of all of the lines are roughly constant below 50 GHz.

We also conclude from Fig. 6a that the meshed ground plane fabricated on the lowest metal levels does not allow significant energy to leak through the ground plane and into the lossy silicon beneath at frequencies below 50 GHz, which would be evidenced by significant values of $G/\omega C$. This is extremely significant from the point of view of calibration-kit design, because the skin depth prevents field penetration through the ground plane at higher frequencies. Thus, we expect field penetration into the lossy silicon substrate to be a low-frequency phenomenon, and a lack of measured low-frequency field penetration indicates that we should not have field penetration at higher frequencies either.

Figure 6b shows results of HFSS simulations we performed to further verify our conclusions regarding the behavior of $G/\omega C$. To increase accuracy, we substituted the fields from our HFSS simulations into the perturbation expressions in equations (33)-(36) in [6] for the capacitance C, inductance L, conductance G, and resistance R per unit length of the rectangular waveguide. These expressions are

$$\begin{aligned}
C &= \frac{1}{|v_0|^2}\left[\int_S \varepsilon' |e_t|^2 \,\mathrm{d}S - \int_S \mu' |h_z|^2 \,\mathrm{d}S\right] \\
L &= \frac{1}{|i_0|^2}\left[\int_S \mu' |h_t|^2 \,\mathrm{d}S - \int_S \varepsilon' |e_z|^2 \,\mathrm{d}S\right] \\
G &= \frac{\omega}{|v_0|^2}\left[\int_S \varepsilon'' |e_t|^2 \,\mathrm{d}S + \int_S \mu'' |h_z|^2 \,\mathrm{d}S\right] \\
R &= \frac{\omega}{|i_0|^2}\left[\int_S \mu'' |h_t|^2 \,\mathrm{d}S + \int_S \varepsilon'' |e_z|^2 \,\mathrm{d}S\right],
\end{aligned} \qquad (3)$$

where the integrals are performed over the cross section of the guide, i_0 is defined by $v_0 i_0^* = p_0$, $\varepsilon = \varepsilon' - j\varepsilon''$ and $\mu = \mu' - j\mu''$.

The solid curves in Fig. 6b show the total value of $G/\omega C$ we calculated for a microstrip line fabricated in this technology with solid metal or meshed M1-M3 ground planes, while the dashed curves in Fig. 6b exclude the fields in the metals from the expressions in (3) and show only the component of $G/\omega C$ due to the field that penetrates into the silicon dielectric. The dashed lines show that the component of $G/\omega C$ due to field penetration into the silicon is very small, confirming our measured results and giving us confidence in the reference-impedance transformation we must apply in our TRL calibration.

The solid lines also indicate that the total value of $G/\omega C$ including transverse currents in the metals is small as well. However, the total values of $G/\omega C$ in Fig. 6b should be treated with caution, as we found it difficult to obtain good convergence for the transverse currents in the metal, particularly when the metal was meshed. Thus, while these results further support our measurements by indicating that the total values of $G/\omega C$ are small in these lines, it would not be appropriate to draw further conclusions regarding the actual magnitudes of $G/\omega C$ in these lines.

B. Inductance and resistance per unit length

Finally, Fig. 6c shows modest increases in the inductance L and resistance R per unit length of our two transmission lines when compared to the nominal design of Fig. 1 below 50 GHz, where the frequencies are low enough that we can have confidence in the measured estimates in Fig. 6. However, these modest increases in R and L are not particularly significant from a calibration point of view, as they are estimated in our calibration procedure from our measured the propagation constant [7]. In fact, the modest increase in the resistance R per unit length when the metal is meshed gives us greater confidence that $G/\omega C$ should not increase greatly when the metal ground plane is meshed.

Thus, we see that, while we choose a very conservative approach to ground-plane design that backs a solid metal B3 ground with a stack of meshed grounds underneath to minimize field penetration into the silicon substrate, our results indicate that even designs with only a few meshed metal levels in the ground should prevent significant field penetration into the silicon substrate.

Finally, due to the inherent errors in our estimates of the transmission-line parameters of the transmission lines employing floating islands and M1-M3 meshed ground planes outlined in [20], it is difficult to draw conclusions about the behavior of these transmission lines above 80 GHz from the data plotted in Fig. 6. Nevertheless, the data below 50 GHz are quite comforting, and a good indication that TRL calibration kits based on any of these lines should perform well over the entire band.

VI. Transistor Measurements

We applied our calibration to the characterization of a silicon nFET power transistor with 40 fingers of width 770 nm and a minimum length of 40 nm designed for use at millimeter-wave frequencies. The gate was contacted on a single side, while the source and drain both exit on the opposite side of the gate in order to reduce parasitic capacitance. The sources connect directly to the ground plane. The drains are tapered while moving up through the metal stack to make contact with the signal line of the microstrip feeds.

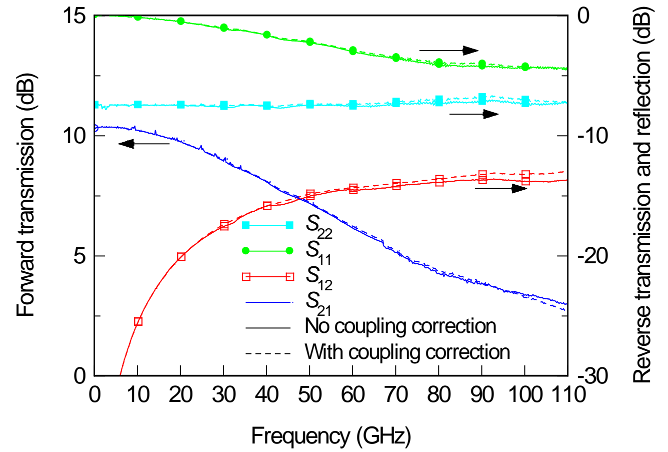
A. *Coupling corrections*

We first investigated the impact of the coupling corrections investigated in [16] because that reference showed significant improvements in millimeter-wave transistor scattering-parameter measurements of hetero-junction bipolar transistors designed for use at terahertz frequencies. Figure 7 compares the magnitude and phase of scattering-parameter measurements of a power transistor we designed for use at millimeter-wave frequencies with and without coupling corrections. These measurements were corrected to the initial reference plane of the TRL calibration, and we did not attempt to move that reference plane to the transistor contacts. The figure shows that the differences are very much smaller than those observed in [16]. This could be due to the larger size of the transistors we designed for this IBM technology, or to differences in contact pads, access lines or probes.

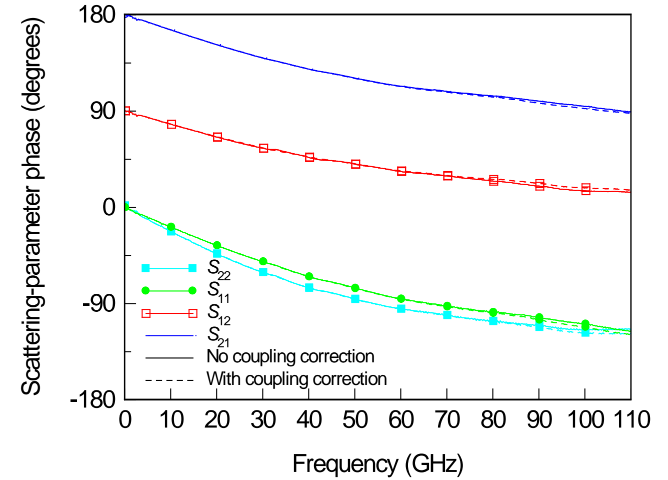
B. *Uncertainties*

We also performed an uncertainty analysis to assess the overall accuracy of our measurement and calibration procedures. We used the orthogonal-distance regression algorithms of ODRPACK [22] as implemented in [13;14] to estimate the uncertainty in our TRL calibration from the lack of fit of the over-determined measurements of the TRL calibration standards to the VNA calibration model. To capture drift in the VNA and the cables, we included calibration measurements performed both before and after the transistor measurements.

We added estimates of the uncertainty in the crosstalk corrections to these errors. As we have found that corrections due to crosstalk are unreliable, we estimated the standard uncertainty in our crosstalk corrections as equal to half of the values of the corrections themselves. We also assumed a coverage factor of two for the uncertainty in the crosstalk terms. We then propagated these errors through the de-embedding procedure to assess its impact on the transistor parameters.



(a) Magnitude comparison.



(b) Phase comparison.

Fig. 7. Comparison of transistor scattering parameters with and without coupling corrections.

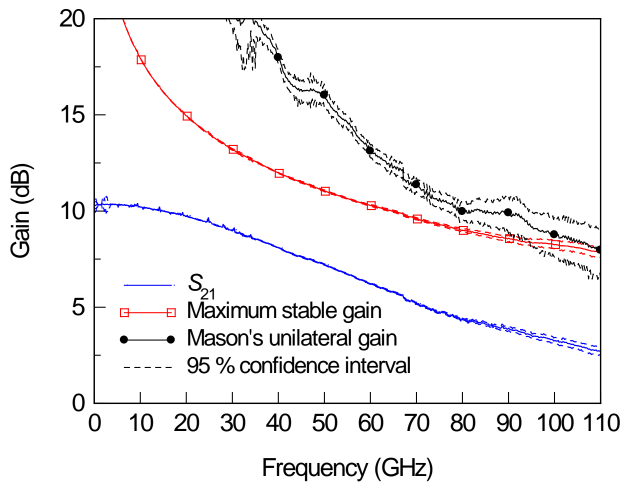


Fig. 8. Measurements of transistor gain with 95 % confidence limits.

Figure 8 shows measurements of the gain of our transistor and 95 % confidence intervals. As we did not attenuate the signals from the vector network analyzer for these measurements, the response of our transistors was not quite linear, which may explain in part why some of the variation in our measurements may seem somewhat large compared to our 95 % confidence intervals. For example, the uncertainty analysis does not account for a jump in power level at 67 GHz from approximately -17 dBm to about +5 dBm where the test-set configuration changes automatically inside our vector network analyzer. Nevertheless, our 95 % confidence intervals do seem representative of our actual uncertainties.

VII. Frequency Limitations

The lateral dimensions of the transmission lines we used in our calibration kits are small enough, and the dielectrics are of high-enough quality, that it seemed possible that our transmission lines might be useful not just for calibrations at millimeter-wave frequencies, but also in the sub-millimeter-wave region. Figure 9 shows the measured effective dielectric constant, which is a normalized form of the propagation constant [6], and the attenuation of transmission lines fabricated in the IBM technology with a 4 µm wide center conductor and the same meshed M1-M3 ground-plane design we discussed earlier. This curve is dashed in the figure and labeled "IBM 45 nm SOI." The contact pads on this wafer were also gold plated. We compared these measurements to measurements performed on 22-µm-wide gold microstrip lines fabricated on a 8-µm-thick bisbenzocyclobutene-based (BCB) monomers film designed for measurements at terahertz frequencies [16], which are labeled "THz BCB."

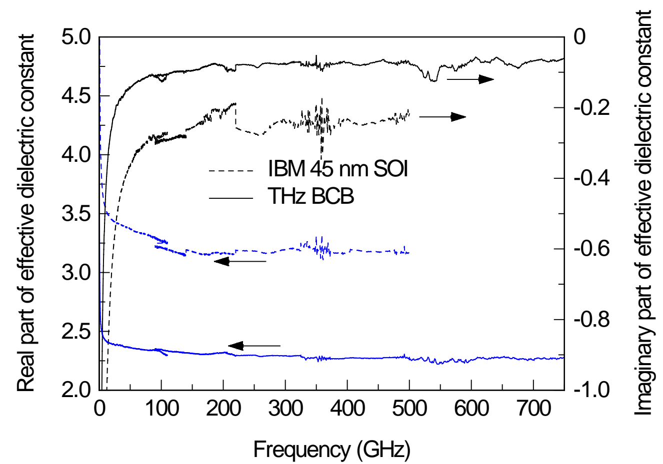
The propagation constants determined by TRL calibrations in the two technologies are remarkably similar. While the loss (as reflected by the imaginary part of the effective dielectric constant) and real part of the effective dielectric constant of the transmission lines in the IBM technology are greater than those of the BCB based microstrip lines, they were not lossy enough to prevent TRL calibration from failing at these sub-millimeter wavelengths.

More importantly, at high frequencies the effective dielectric constant is smooth and well behaved, and does not display resonances of other characteristics that might indicate radiation, multimode propagation, or other problems in the transmission lines at these frequencies. While the attenuation of our silicon transmission lines in Fig. 9b is much higher than that of the terahertz lines, they are both still well behaved below 325 GHz, and reasonably well behaved in the 325-500 GHz band. Furthermore, we note that the most significant noise in the measurements between 325 GHz and 400 GHz are present in both the terahertz BCB and the IBM 45 nm SOI measurements, an indication that the root cause of this noise is more likely due to instrumentation problems than the calibration artifacts.

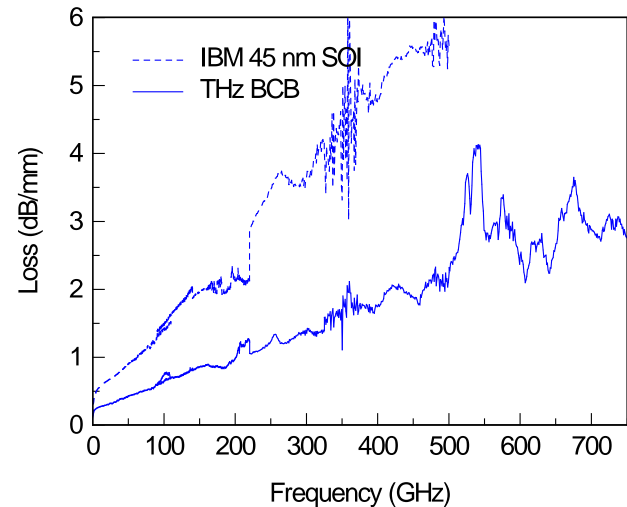
Figure 10 shows measurements of two Beatty standards that are a half wavelength long at about 420 GHz. Here again, the measurements, while not as accurate at submillimeter wavelengths as in the millimeter-wave region, are quite well behaved below 325 GHz, and reasonably well behaved in the 325-500 GHz band.

A. *Multiline calibrations*

Single-line TRL calibrations typically fail whenever the length of the transmission line reaches a multiple of a half-wavelength long. This happens because the scattering parameters of the line in the calibration kit cannot be distinguished from the scattering parameters of the thru when the line is a multiple of a half wavelength longer. However, this is not true if the transmission lines are so lossy that the



(a) Effective dielectric constant.



(b) Attenuation.

Fig. 9. Comparison of measured propagation constants and attenuation.

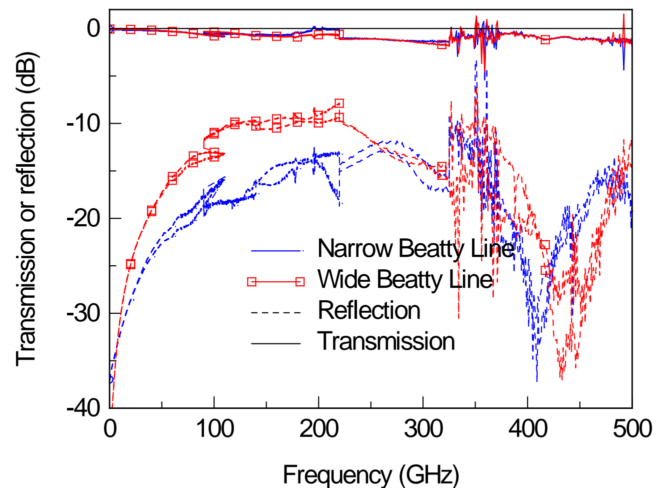


Fig. 10. Magnitude and phase of the scattering parameters of two Beatty standards.

attenuation of the line is significantly greater than the attenuation of the thru due to the line's additional length.

We performed a short investigation to see if the high loss of our silicon transmission lines could be actually used to reduce the number of transmission lines in our calibration kit, and thus reduce its size. Figure 11 shows a typical comparison of reflection coefficients of one of our Beatty lines measured with a TRL calibration kit using a thru, reflect and all of the lines, and a thru, reflect, and 1 mm line. The arrows at the bottom of the graph indicate the locations where the 1 mm line is an integer multiple of a half-wavelength long. It is clear from the figure that the calibration using only the 1 mm line fails these locations, indicating that the loss in our transmission lines fabricated in the IBM technology was not large enough to allow us to accurately calibrate our vector network analyzer when the line was a multiple of a half wavelength longer that the thru line. Thus we conclude that obtaining accurate TRL calibrations in the transmission lines we used at sub-millimeter wavelengths will require multiline calibrations.

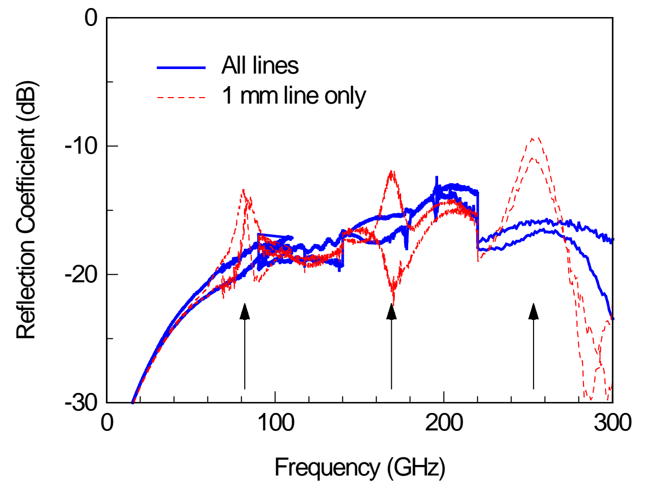


Fig. 11. Comparison of reflection coefficients of a Beatty line calibrated with a thru, reflect, and 1 mm line, and with a thru, reflect, and all lines.

VIII. Conclusion

We showed that the TRL calibration algorithm provides an accurate alternative to lumped-element calibrations that is well suited to measurements at millimeter and sub-millimeter wavelengths. We investigated possible sources of error, including field penetration through meshed ground planes, metal contact repeatability, and contact-pad capacitance. We showed that contact repeatability can be improved by plating the aluminum pads with gold and developed a pad design that reduces the magnitude and variation of contact-pad capacitances. Finally, we applied the approach to transistor characterization and presented uncertainties for those measurements.

IX. Acknowledgements

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