NOTICE OF FUNDING OPPORTUNITY (NOFO)

CHIPS Manufacturing USA Institute Competition

Executive Summary

Federal Agency Name: National Institute of Standards and Technology (NIST), United States Department of Commerce

Funding Opportunity Announcement Title: FY2024 CHIPS Manufacturing USA Institute Competition

Funding Opportunity Announcement Type: Initial

Funding Opportunity Announcement Number: 2024-NIST-CHIPS-MFGUSA-01

Assistance Listing Number(s): 11.042 – CHIPS R&D

Funding Opportunity Description: This NOFO seeks proposals from eligible applicants for activities to establish and operate a CHIPS Manufacturing USA Institute focused on digital twins with integrated physical assets and computational capabilities (digital assets) to tackle important semiconductor-industry manufacturing challenges. The CHIPS Manufacturing USA Institute will join an existing network of seventeen Institutes designed to increase U.S. manufacturing competitiveness and promote a robust R&D infrastructure. The Institute will manage a portfolio of Institute-led projects and competitively funded Member-led projects, including Education and Workforce Development (EWD) activities, basic and applied research, and technology demonstrations.

Dates: Relevant dates in the application process are listed in Table 1 and described in the text that follows.

Table 1. Chips Digital Twin Manufacturing USA Institute NOFO Key Dates	
Webinar Information Session	May 8, 2024
Proposers Day	May 16, 2024
Concept Paper Due	June 20, 2024
Invited Full Applications Due	September 9, 2024

The Department of Commerce may amend this NOFO at any time. It may also close the NOFO with at least 60 days' notice. Changes will be communicated via https://www.grants.gov and https://www.chips.gov.

Webinar Information Session: The National Institute of Standards and Technology (NIST) CHIPS Research and Development Office (CHIPS R&D) will host an informational webinar on May 8, 2024, to provide general information regarding this NOFO, offer general guidance on preparing applications, and answer questions. Proprietary technical discussions about specific project ideas will not be permitted during the webinar, and CHIPS R&D staff will not critique or provide feedback on specific project ideas while they are being developed by an applicant, brought forth during the webinar, or at any time before the deadline for all applications. However, questions about the NOFO, eligibility requirements, evaluation and award criteria, selection process, and the general characteristics of a competitive application will be addressed at the webinar and by e-mail to askchips@chips.gov with "2024-NIST-CHIPS-MFGUSA-01 Questions" in the subject line. There is no cost to attend the webinar, but participants must register in advance. Participation in the webinar is not required and will not be considered in the review and selection process.

Proposers Day and Teaming Meetings: In addition to the informational webinar described above, CHIPS R&D plans to host a Proposers Day on May 16, 2024 to promote awareness of this NOFO and provide a forum for organizations to identify prospective partners. Information about the event can be found on the CHIPS for America events website.

Public Website, and Frequently Asked Questions (FAQs): CHIPS R&D has a public website with a "Frequently Asked Questions" page and other information pertaining to this NOFO.

Concept Papers: The submission of a concept paper is required. Concept papers will only be accepted through Grants.gov. The deadline for receipt of concept papers is 11:59 p.m. Eastern Time, June 20, 2024. Concept papers received after this deadline will not be reviewed or considered. Please note that an active SAM.gov registration is required to submit application materials through Grants.gov.

Full Applications: Full applications will be accepted only from those applicants invited after concept paper evaluation. Full applications must be received at Grants.gov no later than 11:59 p.m. Eastern Time, September 9, 2024. Applications received after this deadline will not be reviewed or considered.

Anticipated Amounts: NIST anticipates awarding up to approximately $285M in Federal funding for a single Institute award, with a performance period of up to five years.

Funding Instrument: Awards in this program will be made as other transaction agreements for the selected project, as provided in 15 U.S.C. § 4659(a)(1). See Section 2 of this document for additional information regarding the type of award agreement.

Eligibility: Eligible applicants for the Institute award are non-profit organizations; accredited institutions of higher education; State, local, and Tribal governments; and for-profit organizations that are domestic entities. A domestic entity is one incorporated within the United States (including U.S. territories) with its principal place of business in the United States (including U.S. territories). Eligible applicants may only submit one concept paper for the Institute award under this NOFO. See Section 3 regarding eligibility requirements. Eligible entities may participate in multiple concept papers and applications as a subrecipient. Applicants and recipients are required to have an active registration in SAM.gov and are encouraged to begin the process of registering as early as possible.

Cost Share Requirements: Non-Federal cost share is required for an award issued pursuant to this NOFO. Specifically, this program requires cost share in an amount equal to at least the total amount of Federal funding over the lifetime of the award *(i.e.,* 50% or more of the total funding for the Institute must come from non-Federal sources). Cost share is that portion of the project costs not borne by the Federal government. See Sections 1.2, 1.8, and 3.2 of this document for definitions, additional information, and expectations regarding cost share requirements and optional co-investment.

Agency Points of Contact (POC): Section 7 identifies Agency Points of Contact. Applicants must submit all questions in writing to the appropriate agency point of contact with "2024-NIST-CHIPS-MFGUSA-01" in the subject line. All inquiries regarding this NOFO must be submitted to the email addresses in that section.

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1 PROGRAM DESCRIPTION

The statutory authority for the CHIPS[1] Manufacturing USA Institute is 15 U.S.C. § 4656(f). This competition seeks to establish one (1) Manufacturing USA Institute (the Institute) focused on the development, validation, and use of digital twins for semiconductor manufacturing, advanced packaging, assembly, and test processes. This CHIPS Manufacturing USA Institute will be established and operated consistent with the requirements of 15 U.S.C. § 278s(e), as amended.

1.1 CHIPS MANUFACTURING USA INSTITUTE OVERVIEW

The CHIPS and Science Act of 2022 appropriated $50 billion to the U.S. Department of Commerce's (the Department) CHIPS for America program to strengthen semiconductor manufacturing in the United States. This amount includes $39 billion for the Department to onshore semiconductor manufacturing through an incentives program and $11 billion to advance U.S. leadership in semiconductor research and development (R&D). These R&D advances will be realized through four programs: the CHIPS National Semiconductor Technology Center (NSTC), the CHIPS National Advanced Packaging Manufacturing Program (NAPMP), the CHIPS Metrology Program, and the CHIPS Manufacturing USA Program. These investments, across both the R&D and incentives programs, seek to strengthen U.S. competitiveness, support domestic production and innovation, create good jobs across the country—with working conditions consistent with the Good Jobs Principles published by the Department and the U.S. Department of Labor—and advance U.S. economic and national security.

1.1.1 CHIPS R&D Mission and Goals

Within the CHIPS for America program, the mission of the National Institute of Standards and Technology (NIST) CHIPS Research and Development Office (CHIPS R&D) is to accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic research efforts, tools, resources, workers, and facilities. CHIPS R&D aims to achieve the following goals by 2030:

- ***U.S. Technology Leadership***: The United States establishes the capacity to invent, develop, prototype, manufacture, and deploy the foundational semiconductor technologies of the future.
- ***Accelerated Ideas to Market***: The best ideas achieve commercial scale as quickly and cost effectively as possible.
- ***Robust Semiconductor Workforce***: Inventors, designers, researchers, developers, engineers, technicians, and staff meet evolving domestic government and commercial sector needs.

[1] DOC CHIPS activities were authorized by Title XCIX—Creating Helpful Incentives to Produce Semiconductors for America of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Pub. L. 116-283, often referred to as the CHIPS Act), codified at 15 U.S.C. 4651 *et seq.*, as amended.

1.1.2 The Manufacturing USA Network

The CHIPS Manufacturing USA Institute will join an existing network of seventeen Institutes designed to increase U.S. manufacturing competitiveness and promote a robust R&D infrastructure. Institutes are public-private partnerships that convene members[2] in industry; academia (e.g., research universities, community colleges, and career and technical education schools); non-profit groups; Federal laboratories; and State, local, and Tribal governments to focus on priorities that

(1) address challenges in advanced manufacturing;
(2) assist manufacturers in retaining or expanding domestic industrial production;
(3) reduce the cost, time, or risk of commercializing new technologies; and
(4) develop and implement improvements in education and workforce development.

NIST further expects that Institutes will work to improve the competitiveness of U.S. manufacturing, help fill the gap between basic research and commercialization, accelerate non-Federal investment in advanced domestic manufacturing production capacity, and enable the commercial application of new technologies.

Within NIST's Office of Advanced Manufacturing (OAM), the Advanced Manufacturing National Program Office is tasked with coordinating the activities of the Manufacturing USA network. The Institute will be required to engage with the network, as described in Section 1.6.2. More information about Manufacturing USA, including published reports documenting program design and performance, can be found online at https://manufacturingusa.com.

1.1.3 CHIPS Manufacturing USA Institute Description

Semiconductors are arguably the smallest, most complex products ever made in one of the world's most sophisticated manufacturing environments. Although U.S. innovation created the sector, domestic manufacturing currently accounts for about 12% of global production, compared to 37% approximately thirty years ago.[3] To improve its manufacturing competitiveness, the United States must address key challenges, such as the time and cost of chip development and manufacturing processes, as well as talent shortages.

1.1.3.1 Background on Digital Twins

Digital twins offer a critical tool for the United States to achieve technology leadership and accelerate ideas to market across the semiconductor sector. As recently defined by the National Academies of Sciences, Engineering, and Medicine:

[2] The business model for institutes relies on a group of persons and/or organizations coming together for a common purpose. This model generally results in a membership structure and an associated agreement that formalizes the relationship between a stakeholder organization and the institute entity itself. Stakeholder organizations that establish this type of relationship with an institute are generally referred to as members.

[3] See https://www.whitehouse.gov/briefing-room/statements-releases/2022/01/21/fact-sheet-biden-harris-administration-bringing-semiconductor-manufacturing-back-to-america-2/.

> A digital twin is a set of virtual information constructs that mimics the structure, context, and behavior of a natural, engineered, or social system (or system-of-systems), is dynamically updated with data from its physical twin, has a predictive capability, and informs decisions that realize value. The bidirectional interaction between the virtual and the physical is central to the digital twin.[4]

Digital twin technologies can significantly impact both current and future semiconductor manufacturing, advanced packaging, assembly, and test processes. Leading companies have therefore developed and deployed proprietary digital twins and resources to optimize key process steps and increase throughput. However, despite substantial investments in proprietary semiconductor digital twin technologies, multiple challenges hinder the development of breakthrough innovations using digital twins, including:

- ***Fragmentation***, where companies each develop separate digital twins, limiting process optimization to a single tool or suite of tools rather than across the full manufacturing flow.
- ***Lack of transparency and trust***, where companies are unwilling to share critical assets (e.g., models, data, and best practices related to their digital twins) outside of their supply chain.
- ***High barriers to entry***, where high equipment and facilities costs, along with the difficulty of testing and validating digital twins in a full process flow, limit small business participation.

1.1.3.2 CHIPS Manufacturing USA Institute Vision, Mission, and Objectives

By convening the manufacturing ecosystem to solve shared technology challenges, a new Manufacturing USA Institute aims to unlock the full potential of digital twins for the semiconductor industry and benefit manufacturers of all sizes. The CHIPS Manufacturing USA Program therefore seeks to establish an Institute with the following vision and mission:

> ***Vision****: The CHIPS Manufacturing USA Institute will enable seamless integration of digital twin models into the U.S. semiconductor manufacturing, advanced packaging, assembly, and test industry, enabling the rapid development and adoption of innovations and enhancing domestic competitiveness for decades.*

> ***Mission:*** *The CHIPS Manufacturing USA Institute will foster a collaborative environment within the domestic semiconductor industry, enabled by shared facilities; support industry-led solutions through funded research projects; accelerate technology towards commercialization through significant co-investment; and enable digital-twin workforce training.*

To facilitate the creation of the CHIPS Manufacturing USA Institute, this NOFO seeks proposals from eligible applicants for activities to establish and operate the Institute, consistent with the mission and vision, to achieve the following specific objectives:

(1) Convene stakeholders across the semiconductor manufacturing, advanced packaging, assembly, and test industry to address shared challenges relevant to digital twins, in a collaborative environment.

[4] National Academies of Sciences, Engineering, and Medicine. 2023. *Foundational Research Gaps and Future Directions for Digital Twins*. Washington, DC: The National Academies Press. See https://doi.org/10.17226/26894

(2) Improve the state of the art in manufacturing-relevant digital twins, for both unit-level digital twins and the combination of multiple digital twins.
(3) Significantly reduce U.S. chip development and manufacturing costs by improving capacity planning, production optimization, facility upgrades, and real-time process adjustments using digital twins.
(4) Improve development cycle times of semiconductor manufacturing, advanced packaging, assembly, and test and accelerate the development and adoption of relevant innovative technologies, including breakthrough tools, materials, and manufacturing processes.
(5) Advance digital twin-enabled curricula, best practices, and hands-on opportunities for training the next generation of the domestic semiconductor workforce.
(6) Create a digital twin marketplace for industry to access digital models and manufacturing process flows and to de-risk digital twin development and implementation.

1.2 DEFINITIONS

This section provides definitions for purposes of this NOFO.

(1) **Advanced packaging** – A subset of packaging technologies that uses novel techniques and materials to increase the performance, power, modularity, and/or durability of an integrated circuit. Advanced packaging technologies include flip-chip, 2D, 2.5D, and 3D integration, fan-out and fan-in, and embedded die/system-in-package (SiP).
(2) **Applied Research** – "Original investigation undertaken in order to acquire new knowledge. Applied research is, however, directed primarily towards a specific practical aim or objective."[5]
(3) **API** –A set of interfaces for the Digital Twin Backbone that allow human developers to access the data of a digital twin. The API may also allow different digital twins to communicate, exchanging data and functionalities seamlessly.
(4) **Basic Research** – "Experimental or theoretical work undertaken primarily to acquire new knowledge of the underlying foundations of phenomena and observable facts. Basic research may include activities with broad or general applications in mind, such as the study of how plant genomes change, but should exclude research directed towards a specific application or requirement, such as the optimization of the genome of a specific crop species." [6]
(5) **Co-investment** – Commitments made by Institute members to advance potential innovations from projects to higher Manufacturing Readiness Levels (MRLs). Examples of co-investment may include those commitments required to enable the scale-up, commercialization, and transition to domestic production of Institute-funded innovations. Co-investment is described further in Section 1.8. MRLs are described further in Section 1.5.
(6) **Cost Share** – The portion of the costs of a Federally assisted project or program not borne by the Federal Government. The required cost share must, at a minimum, be equal to the total amount of Federal funding provided through the lifetime of an award (i.e., 50% or more of the total funding for the Institute must come from non-Federal sources). Examples of cost share are to be reported in the Research and Related Budget. Cost share is described further in Section 3.2.
(7) **Design Technology Co-Optimization** – The concurrent development of design and manufacturing processes to optimize chip performance, power efficiency, area utilization, and manufacturability.

[5] Office of Management and Budget Circular A-11 (2023).
[6] *Id.*

(8) **Digital Twin –** A set of virtual information constructs that mimics the structure, context, and behavior of a natural, engineered, or social system (or system-of-systems), is dynamically updated with data from its physical twin, has a predictive capability, and informs decisions that realize value.[7]

(9) **Digital Twin Backbone** – Interconnected digital twins as well as the standards, software, connection pathways, and protocols for data and IP protection required to provide a 2-way or networked path of exchange of information between them. The Digital Twin Backbone provides a means to form an end-to-end aggregated Digital Twin model of a process or system.

(10) **Full Flow** – The entire sequence of steps required for semiconductor manufacturing, from initial wafer preparation to final packaging, assembly, and test, or a subset of such steps as defined by the proposed Institute scope.

(11) **Governing Council** – The advisory body, consisting of representation from Institute membership, the Federal government, and others, that provides strategic advice to the CHIPS Manufacturing USA Institute, technical oversight of the Institute, and performance oversight of the Institute director and staff.

(12) **Institute award** – The award, granted under this NOFO, for the establishment and operation of the CHIPS Manufacturing USA Institute.

(13) **Institute team** – Together with the applicant, any proposed subrecipients, contractors, and/or unfunded collaborators listed on the application, which may include potential Institute members.

(14) **Institute-led projects** – Research, development, demonstration, or education and workforce development activities carried out by Institute staff. Institute-led projects can also support the shared capabilities, as outlined in Section 1.4.2, independent of Member-led projects. Institute-led projects must support Institute goals.

(15) **Institute-level targets** – Specific, measurable, achievable, relevant, and time-bound (SMART) technical or non-technical metrics proposed by the applicant, consistent with the mission and relevant objectives in Section 1.1.3.2, for the Institute to achieve by the end of the period of performance. Institute-level technical targets should seek to aggressively advance the current state of the art in digital twins or in semiconductor manufacturing.

(16) **Institute staff** – Individuals who may be direct Institute employees, contractors, or contracted staff at member organizations. The composition is proposed by the applicant to maximize the impact of the program.

(17) **Interoperability** – The capability of two or more networks, systems, devices, applications, or components to work together, and to exchange and readily use information — securely, effectively, and with little or no inconvenience to the user.[8]

(18) **Member-led projects** – Research, development, demonstration, or education and workforce development activities carried out by Institute members, funded via competitive Project Calls.

(19) **Milestones** – Actions or events marking a significant change or stage in developments in a project.

(20) **Phase-Specific Project Plan –** Description of the scope of technical work to be performed for a particular stage of the period of performance, what is expected to be accomplished, including SMART project-specific targets, milestones, deliverables, and budgets for Institute-led and Member-led projects.

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[7] See https://nap.nationalacademies.org/catalog/26894/foundational-research-gaps-and-future-directions-for-digital-twins.

[8] See NIST Special Publication 1108r4. "NIST Framework and Roadmap for Smart Grid Interoperability Standards, Release 4.0" February 2021. https://doi.org/10.6028/NIST.SP.1108r4

(21) **Phase-specific targets –**Technical and non-technical targets, derived from applicant-specified milestones, to inform go/revise/no-go points for the transition from one phase to the next.

(22) **Project award –** An award, granted by the Institute, for the conduct of a Member-led or Institute-led project.

(23) **Project Call** – The mechanism by which the Institute will solicit proposals for competitively awarded projects.

(24) **Semiconductor** – An integrated electronic device or system, most commonly manufactured using materials such as, but not limited to, silicon, silicon carbide, or III-V compounds, and processes such as, but not limited to, lithography, deposition, and etching. Such devices and systems include but are not limited to analog and digital electronics, power electronics, and photonics, for memory, processing, sensing, actuation, and communications applications.

(25) **Semiconductor manufacturing –** All activities encompassed by the semiconductor fabrication, advanced packaging, assembly, and test processes.

(26) **Shared capabilities model** – A federated model where the Institute and members contribute funds and resources for facilities, physical equipment, computation and data resources, and technical staff.

(27) **Short Loop** – A simplified or truncated version of the typical semiconductor manufacturing flow, typically involving fewer steps and less complexity. Short-loop processing is commonly used in research, prototyping, or when simpler devices don't require the full-scale semiconductor manufacturing process.

(28) **SMART** – Specific, measurable, achievable, relevant, and time-bound (SMART). Acronym to describe goals, targets, or objectives.

(29) **System Technology Co-Optimization** – The process of developing semiconductor technologies in tandem with system-level requirements to optimize performance, power efficiency, integration, reliability, cost, and manufacturing processes.

(30) **Technology Demonstrations** – Industry-led solutions may include technology demonstrations that validate the digital twin for manufacturing solutions. Project funding for the technology demonstration must be limited to the physical substantiation of the technology and focused on the digital twin for manufacturing outcomes.

(31) **Test Vehicle** – An article designed for physical validation of digital twins. It will contain structures, circuits or integrated circuits that can be measured and/or tested. The test vehicle will be defined for a process module or short loop and have a plan for characterization and data generation.

1.3 FUNDING OPPORTUNITY DETAILED DESCRIPTION

1.3.1 Institute Activities

Applicants to this NOFO must propose to establish a CHIPS Manufacturing USA Institute with integrated physical assets and computational capabilities (digital assets) to tackle important semiconductor-industry manufacturing challenges. The Institute will manage a portfolio of Institute-led projects and competitively funded Member-led projects, including Education and Workforce Development (EWD) activities. Projects also may include basic and applied research and technology demonstrations.[9]

[9] For more information on Manufacturing USA Institute activities, see 15 U.S.C. § 278s, as amended.

CHIPS R&D encourages collaborative proposals under this NOFO, as significant partnership will likely be required to meet the CHIPS Manufacturing USA Program objectives. Consistent with the statute, effective Institutes will likely include the active participation of expert representatives from for-profit and non-profit organizations (including industry-led consortia); covered entities; research universities; community colleges; career and technical education (CTE) schools; Federal laboratories; and State, local, and Tribal governments. As defined in 42 U.S.C. 18971(b), covered entities include Historically Black College or Universities (HBCUs), Tribal Colleges or Universities, Minority Serving Institutions, a minority business enterprise (as defined in 15 C.F.R. § 1400.2), or a rural-serving institution of higher education (as defined in 20 U.S.C. § 1161q). Further, CHIPS R&D encourages outreach and engagement with government agencies, labor organizations, public workforce systems,[10] community-based organizations, and small and medium-sized manufacturing enterprises,[11] including women-owned, minority-owned, and veteran-owned manufacturing enterprises.

1.3.2 Institute-level Targets

Consistent with the mission and objectives under Section 1.1.3.2, applicants must propose specific Institute-level technical targets, representing significant improvements over the current state of the art for semiconductor-industry digital twins and real-world semiconductor manufacturing. For example, SMART Institute-level technical targets and milestones could, but are not required to, include—

(1) A substantial decrease in the time required to develop a specific new capability (e.g., a material, process, or tool) for semiconductor manufacturing, within two years of award;

(2) A specific increase in the accuracy of a short loop of digital twins, leveraging artificial intelligence, within two years of award;

(3) Establishing a production-representative digital twin of an end-to-end flow between semiconductor fabrication and advanced packaging, consisting of multiple interoperable digital twins validated with a pre-determined test vehicle, within five years of award; or

(4) Demonstrate the applicability of one digital twin to another end-to-end flow, leveraging standards, within five years of award.

Applications should also propose Institute-level non-technical targets, representing significant advances in the operation of the Institute, addressing issues such as technology transition and financial sustainability. For example, SMART Institute-level non-technical targets and milestones could, but are not required to, include—

(1) Achieving cost share and co-investment commitments of more than three times the level of Federal investment, within two years of award; or

(2) Enabling the hiring or reskilling of a specific number of semiconductor industry workers, via EWD projects focused on credentialing, within five years of award.

1.3.3 Operational Areas

Consistent with the mission and objectives specified in Section 1.1.3.2, responsive applications to this NOFO must address each Operational Area (OA) described in Section 1.4. Briefly, the OAs are:

[10] The public workforce system is comprised of state and local workforce boards, American Job Centers, Registered Apprenticeship Programs, Eligible Training Providers, and other Federal, state, and local government-funded or overseen programs that provide training and other workforce services.
[11] See https://www.nist.gov/mep.

(1) ***OA1: Institute Operations.*** Establishing an Institute management and governance strategy, to include plans for outreach to a broad group of potential members.

(2) ***OA2: Shared Physical and Computational Capabilities.*** Operating or providing member access to physical and virtual facilities, as appropriate.

(3) ***OA3: Industry-led Solutions.*** Developing and supporting an Institute-funded portfolio of projects, to either improve the capabilities of digital twins or to impact real-world operations.

(4) ***OA4: Education and Workforce Development.*** Developing and supporting projects to either train the workforce to use digital twins or to leverage digital twin technology to deliver EWD services to diverse audiences of trainees.

1.3.4 Phases and Milestones

Consistent with the mission and objectives specified in Section 1.1.3.2, responsive applications to this NOFO must propose 4 phases of work, with each phase ranging in length from 3 months to 18 months. The total period of performance may not exceed five years.

Responsive applications must further define, within each phase, milestones marking measurable progress towards the Institute-level technical targets and other CHIPS Manufacturing USA objectives. If an application stands a reasonable chance of being funded, CHIPS R&D may negotiate with the applicant (1) to refine the proposed milestones and (2) to define phase-specific targets derived from the proposed milestones. These phase-specific targets will inform go/revise/no-go decision points for the transition from one phase to the next.

Upon approval and selection of an application, CHIPS R&D intends to award funding for Phase 1 activities across all operational areas; additional phases will be funded incrementally. CHIPS R&D retains sole discretion to determine whether a recipient has met the requirements for each Institute-level target, phase-specific target, and deliverable.

1.4 MILESTONES AND DELIVERABLES

1.4.1 Operational Area 1 (OA1): Institute Operations

The CHIPS Manufacturing USA Institute must lead a national effort to research, develop, test, and demonstrate industry-relevant, high-impact technologies relevant to the development or application of semiconductor industry digital twins. The Institute must therefore enable research collaboration among multiple parties while protecting intellectual property (IP) and advancing the vision, mission, and objectives specified in Section 1.1.3.2.

To demonstrate capabilities relevant to OA1, full applications must include an Institute Management and Governance Strategy, Institute Investment Strategy, and draft Institute Transition and Sustainability Plan.

1.4.1.1 Activities

CHIPS R&D expects activities under OA1 to include (1) attracting and serving a membership of diverse stakeholders from industry, academia, non-governmental organizations, national labs, and other groups; (2) creating and implementing clear governance and operating structures and strategies for member participation, to include policies to protect member IP and Federally funded research products; (3) creating and maintaining the Institute Investment Strategy for technical roadmaps that identify the technical and non-technical challenges across OA2, OA3, and OA4; and (4) developing and executing a financial management strategy that enables the long-term sustainability of the Institute, including after the expiration of CHIPS R&D funding.

Membership. The Institute must build, provide value to, and facilitate engagement and collaboration among a diverse membership, consistent with meeting the Institute-level targets and ensuring representation from across the relevant portions of the semiconductor manufacturing industry. Effective Institutes will likely include the members as referenced in Section 1.3.1.

Governance. CHIPS R&D expects that the key Institute leadership, including the executive director, will be 100% dedicated to the Institute.[12] The Institute must establish governance structures such as a Board of Directors, Governing Council, and advisory committees, to provide strategic direction and ensure alignment with Institute-level targets. The Institute must establish policies, consistent with governing areas such as research security, IP rights, and enterprise risk management. These structures and policies should facilitate stakeholder engagement, uphold transparency, protect research security and IP, and enable prudent and effective management of Institute resources.

Financial Management. The Institute must develop annual budgets aligned with Institute-level targets. Financial stewardship includes budget monitoring, compliance with Federal award agreement terms, transparent reporting to stakeholders, and planning for long-term sustainability once Federal support ends.

1.4.1.2 Milestones and Deliverables by Phase

Applicants must propose SMART Institute-level targets related to, at a minimum, each of the activities listed in Section 1.4.1.1. Applications must further identify SMART milestones describing measurable steps toward achieving the proposed Institute-level targets.

OA 1 Phase 1 milestones must include, at a minimum—

(1) Hiring the full Institute leadership team;
(2) Hiring or contracting other key personnel critical to OA1 operations;
(3) Finalizing the Institute Management and Governance Strategy, including a membership agreement, Intellectual Property Rights Management Plan, and Research Security Plan;
(4) Convening the Institute membership to refine the Institute Investment Strategy;

[12] Meaning that the Institute provides their full-time employment, and their appointment is not split between the Institute and other functions.

(5) Within six months of award, work towards coordination agreements with other relevant external CHIPS R&D-funded programs and entities (see Section 1.6.5), including but not necessarily limited to the CHIPS NSTC;
(6) Enrolling a diverse set of members, as required to accomplish the Institute-level targets; and
(7) Securing required cost share and any additional in-kind co-investment from Institute members or other sources.

OA 1 Phase 1, Phase 2, Phase 3, and Phase 4 deliverables must include, at a minimum—

(1) Updates to the Intellectual Property Rights Management Plan, as described in Section 4.6.1.6 and pursuant to 15 U.S.C. §4656(g) and Section 2.9;
(2) New or updated Phase-specific Project Plans, as described in Section 4.6.1.6;
(3) Reports of any significant incidents impacting research security or enterprise risk; and
(4) Additional updates to the Institute Management and Governance Strategy or Institute Investment Strategy, in the event of significant changes.

Additional deliverables may include updates to the Institute Transition and Sustainability Plan and the Market Transformation Plan, as described in Section 4.6.1.6, and information required to evaluate the potential renewal of the Institute's award, consistent with Section 2.4. The updated Institute Transition and Sustainability Plan, as practicable, should address plans to ensure Institute-owned IP compliance with Section 2.9.

1.4.2 Operational Area 2 (OA2): Shared Physical and Computational Capabilities

Digital twins offer a transformative tool to accelerate the pace of technological innovation. However, high barriers to entry, such as the costs of equipment and protections on proprietary IP, limit critical participation from academia and small businesses. Consistent with the mission, vision, and objectives under Section 1.1.3.2, the CHIPS Manufacturing USA Institute must enable innovation by providing a wide range of stakeholders with access, at low cost and with reasonable IP protections, to the equipment, facilities, licenses, staff, and digital infrastructure required for digital twin testing and validation. OA2 therefore seeks to establish a network of facilities, equipment, and tools that meet the broad requirements of Institute members. To accomplish this goal, the applicant and its partners may contribute funds and resources for physical facilities and equipment, computation and data resources, and technical staff towards a shared capabilities model that best meets members' needs.

To demonstrate capabilities relevant to OA2, applications must include, within the Institute Investment Strategy, a Shared Capabilities Infrastructure Plan to include applicant-proposed milestones and deliverables, as appropriate.

1.4.2.1 Activities

Under OA2, activities must include (1) acquiring access to physical assets, at not less than two physical locations within the United States in order to establish a network, representing key processes within the semiconductor manufacturing, advanced packaging, assembly, and test industry; (2) establishing a computational capability to provide access to and improve an interconnected network of digital twins representing tools and other necessary physical assets; (3) providing access to the human expertise required for the Institute and its members to innovate using the physical assets and Digital Twin

Backbone; and (4) establishing a digital marketplace to provide members with access to digital twins and related IP. Each of these activities must align with achieving the Institute-level technical targets.

Physical Assets. To ensure the applicability of the Institute to current and future domestic semiconductor manufacturing, applicants must propose to provide Institute members with access to industry-relevant physical assets (e.g., commercially relevant semiconductor manufacturing tools). This access must be sufficient to enable the development and testing of digital twin models, which will likely require member access to staff trained on the use of the relevant physical asset. CHIPS R&D expects a significant portion of the physical assets and staff, or access to such assets and staff, will be provided to the Institute as part of the required cost share and/or the optional co-investment.

***Computational Capability*.** To ensure that Institute activities are not limited to advancing only small subsets of digital twins, applicants must propose to establish a computational capability to build, improve, and provide Institute members with access to an interconnected network of digital twins. The resulting interconnected network (or "Digital Twin Backbone") must include not only multiple digital twins but also the computational and information technology (IT) infrastructure connecting them. The interconnected network must further include any sensors or additional infrastructure allowing for communication between physical assets and their respective digital twins. Applicants should also demonstrate how Institute governance and policies—such as data sharing standards and IP protection requirements—enable interoperability between digital twins, leading to data and model standards, data protection, and accuracy standards. CHIPS R&D expects a significant portion of the computational capability as well as the digital twins, or access to such digital twins, will be provided to the Institute as part of the required cost share and/or optional co-investment.

***Institute Expertise*.** To ensure that Institute activities are not limited to advancing the digital twin capabilities of any single member or group of members, applicants must propose to provide Institute members with access to independent technical staff responsible for supporting, maintaining, and improving the Digital Twin Backbone, including computational engineers. Independent technical staff may also include individuals with direct access to and expertise relevant to the physical assets. Institute staff—who may be direct Institute employees, contractors, or contracted staff at member organizations—may support Member-led projects and conduct Institute-led projects, among other activities, at the discretion of the Institute.

***Digital Marketplace*.** To facilitate Institute member access to digital twins and the licenses required to conduct R&D activities, applicants should propose to establish a Digital Marketplace as a resource to provide members access to Institute and member IP and other products (e.g., software licenses, other research-use licenses, Federally funded and donated IP). The marketplace may provide, based on agreed-upon terms and conditions and with appropriate IP protections, access to items available to all members as a benefit of membership. The marketplace may also provide, with appropriate IP protections, access to items available from members or other sources at a cost. CHIPS R&D invites alternative proposals as to the structure of the Digital Marketplace.

1.4.2.2 Milestones and Deliverables

Applicants must propose SMART Institute-level targets related to, at a minimum, each of the required activities listed in Section 1.4.2.1. Applicants should further identify SMART milestones describing measurable steps toward achieving the proposed Institute-level targets.

Deliverables for each phase must include, at a minimum, within the Institute Investment Strategy, providing an updated Shared Capabilities Infrastructure Plan, as described in Section 4.6.1.6.

OA2 Phase 1 milestones must include, at a minimum—

(1) Acquiring consistent access to physical assets based on member needs, at not less than two domestic locations;
(2) Establishing the computational capability and providing member access to a functional Digital Twin Backbone, with connectivity between multiple digital twins (for example data and model standards, data protection, and accuracy); and
(3) Hiring or contracting Institute expertise to support the physical assets, computational capability, Institute-led projects, and Member-led projects.

OA2 Phase 2, Phase 3, and Phase 4 milestones must include, at a minimum—

(1) Demonstrating use of the physical assets, computational capability, and functional Digital Twin Backbone to conduct projects in service to the Institute-level technical targets;
(2) Within two years of award, executing a significant demonstration of the Digital Twin Backbone, across multiple industry-relevant digital twins in a short loop (e.g., a short loop modeling front-end-of-line fabrication, advanced packaging, or assembly into printed circuit boards) and in service to the Institute-level technical targets;
(3) Increases in the quantity and quality of the physical assets;
(4) Improvements in the performance of the Digital Twin Backbone (e.g., digital twin operability and the accuracy of the digital process flow);
(5) A reduction in the time required to introduce new digital twin tools into the Digital Twin Backbone; and
(6) Additional demonstrations of the Digital Twin Backbone, sufficient to indicate the full technical scope of the Institute.

1.4.3 Operational Area 3 (OA3): Industry-led Solutions

To accomplish the mission, vision, and objectives specified in Section 1.1.3.2, the CHIPS Manufacturing USA Institute must provide "industry-led solutions" via research, development, and demonstration projects that both develop improved digital twins and translate digital twin innovations into the real world. Project Calls for Member-led projects and Institute-led projects should be consistent with the Institute Investment Strategy and developed and executed through a transparent, member-driven process.

1.4.3.1 Activities

Described below, CHIPS R&D expects activities under OA3 to include (1) issuing Project Calls to improve digital twin capabilities through competitively funded Member-led projects and Institute-led projects; and (2) issuing Project Calls to address real-world challenges in semiconductor manufacturing (including fabrication, advanced packaging, assembly, and test) through competitively funded Member-led projects and Institute-led projects. As described in Section 4.6.1.6, Project Calls should be consistent with the Institute Investment Strategy and Phase-Specific Project Plan. Each of these activities must align with achieving Institute-level technical targets.

***Improving Digital Twin Capabilities*.** Some projects should seek to produce and demonstrate innovations and measurable improvements both in individual digital twins and in the integration and interoperability of multiple digital twins in short loops and full flows. These projects, for example, could:

(1) Reduce the time required to develop and demonstrate digital twin short- and long-loops, verified and validated through the shared capabilities model; and

(2) Improve the performance of the Digital Twin Backbone or of other elements of the shared capabilities model, for instance by leveraging artificial intelligence.

***Applying Digital Twins to Real-World Challenges*.** Some projects should seek to use digital twins, or a combination of multiple digital twins, to optimize physical process flows, such as for semiconductor design, fabrication, advanced packaging, assembly, and test. These projects, for example, could:

(1) Reduce the time required for semiconductor product development and deployment;

(2) Enable integration of new materials into manufacturing;

(3) Reduce the need for physical experimentation by enabling digital experimentation; and

(4) Improve the yield, operational efficiency, sustainability, or other key performance indicators through Design Technology Co-Optimization/System Technology Co-Optimization (see Section 1.2).

1.4.3.2 Milestones and Deliverables by Phase

Applications under this NOFO must propose SMART Institute-level targets related to, at a minimum, each of the required activities listed in Section 1.4.3.1. Applications must further identify SMART milestones describing measurable steps toward achieving the proposed Institute-level targets.

Deliverables for each phase must include, at a minimum, within the Institute Investment Strategy, an updated Phase-Specific Project Plan, as described in Section 4.6.1.6, including regular updates on project progress against Institute level technical targets and project adherence to the CHIPS R&D commercial viability and domestic production requirements.

OA3 Phase 1 milestones must include, at a minimum—

(1) Initiating at least one Project Call requesting proposals for Member-led projects; and

(2) Initiating Institute-led projects.

OA3 Phase 2 and Phase 3 milestones must include, at a minimum—

(1) Initiating multiple Project Calls per phase requesting proposals for Member-led projects;

(2) Initiating additional Institute-led projects; and

(3) Within two years of award, demonstrating the application of at least one significant Institute-funded innovation in a real-world system.

OA3 Phase 4 milestones must include the conclusion of Member-led and Institute-led projects, absent an agreement with CHIPS R&D for further Institute operations.

1.4.4 Operational Area 4 (OA4): Education and Workforce Development

A skilled and diverse pipeline of workers is critical to building a sustainable domestic semiconductor industry and achieving the CHIPS for America economic and national security goals. According to one estimate, the U.S. semiconductor sector may have roughly 67,000 unfilled jobs at the end of the decade.[13]

CHIPS R&D therefore expects the CHIPS Manufacturing USA Institute to support EWD projects that foster a diverse and capable domestic workforce with access to good jobs, such as those consistent with the Departments of Commerce and Labor Good Jobs Principles. The combination of expertise, facilities, equipment, and membership required to execute the Institute should provide exceptional opportunities for tailored EWD activities, which are developed to be consistent with the Department of Commerce Workforce Development Strategy Principles.

To complement the activities described in Section 1.4.4.1 and to accomplish the mission, vision, and objectives specified in Section 1.1.3.2, the CHIPS Manufacturing USA Institute must work with employer partners and engage educational institutions, to support the creation and widespread adoption of training materials and curricula. Such an approach (1) complements the strong emphasis on sectoral partnerships described in the Department of Commerce Workforce Development Strategy Principles, (2) is essential to ensure that Education and Workforce Activities address the needs of the sector and especially the Institutes' members, and (3) supports the development of a skilled and diverse workforce.

CHIPS R&D further believes that, in order to advance best practices and hands-on opportunities for training (as expressed in the Institute objectives), strong applications should provide for outreach and engagement with additional partner institutions key to the delivery of quality employment and training pathways, such as labor organizations, government agencies, and industry organizations. CHIPS R&D is especially interested in programs focused on training for underserved communities, as defined by Executive Order 13985, *Advancing Racial Equity and Support for Underserved Communities Through the Federal Government* (Jan. 20, 2021) and Executive Order 14091, *Further Advancing Racial Equity and Support for Underserved Communities Through the Federal Government* (Feb. 16, 2023).

To demonstrate capabilities relevant to OA4, applicants must provide, within their Institute Investment Strategy, an Education and Workforce Development Plan with SMART Institute-level targets. The initial Phase-Specific Project Plan should also detail proposed EWD projects. CHIPS R&D encourages applicants, in providing an EWD plan, to describe any efforts to attract and retain a diverse student and trainee population and demonstrate that the EWD efforts that involve employer partners, are worker centered, industry-aligned, and promote high-quality jobs. For instance, EWD plans should:

- Provide evidence of alignment with U.S. industry needs, such as demonstrated linkages between the skills to be developed and available jobs or to industry-recognized curriculum, credentials, or certifications; and
- Describe any efforts to maximize access to and participation in the semiconductor workforce, including efforts to attract and retain a diverse student and trainee population such as supportive services and outreach to underserved communities.

Following the release of a Project Call, Institutes should further request that applicants seeking funding for Member-led or Institute-led EWD projects describe alignment with the EWD Institute-

[13] See https://www.commerce.gov/news/blog/2024/03/women-stem-representation-matters.

level targets, including any targets relevant to industry alignment and maximizing participation in the semiconductor workforce.

1.4.4.1 Activities

Described below, CHIPS R&D expects activities under OA4 to include developing and supporting EWD projects that (1) create a Digital Twin-capable workforce; and (2) leverage digital twin technologies to train the manufacturing workforce. EWD projects should include Member-led projects and, at the discretion of the Institute, Institute-led projects.

Digital Twin-capable Workforce. In addition to the skilled workforce required to design and manufacture chips, growth in the digital twin market will also require workers capable of building, maintaining, and operating digital twin models and their physical counterparts. Relevant EWD projects may include paid research internships and fellowships focused on digital twin activities, paid research experiences for undergraduates, pre-apprenticeships, registered apprenticeships, and partnerships with employers, labor organizations, community-based organizations, and workforce development boards.[14]

Leveraging Digital Twins for the Semiconductor Manufacturing Workforce. Digital twins, when integrated into tools such as augmented or virtual reality, can help increase access to industry-relevant curriculum and training, including certifications and credentials. For instance, digital twins could enable individuals without physical access to a particular manufacturing tool to train on the tool virtually. As a result, projects funded by the Institute can support technical and career development for the current and future workforce, such as in-school and opportunity youth, and help ensure equitable access to manufacturing careers, including partnerships with K-12, CTE programs, and community colleges.

1.4.4.2 Milestones and Deliverables by Phase

Applicants under this NOFO must, at a minimum, propose SMART Institute-level targets related to each of the required activities listed in Section 1.4.4.1. Applications should further identify SMART milestones describing measurable steps toward achieving the proposed Institute-level EWD targets, such as the number of students trained or engaged in research and subsequently placed in good jobs in the domestic semiconductor industry.

Deliverables for each phase must include, at a minimum, within the Institute Investment Strategy, updates to the Education and Workforce Development Plan and EWD-specific updates to the Phase-Specific Project Plan, including regular updates on EWD project progress against relevant Institute-level targets.

OA4 Phase 1, Phase 2, and Phase 3 milestones must include, at a minimum—

(1) Initiating at least one Project Call requesting proposals for EWD-relevant Member-led projects.

[14] See https://www.careeronestop.org/LocalHelp/WorkforceDevelopment/find-workforce-development-boards.aspx.

OA4 Phase 4 milestones must include, at a minimum—

(1) The conclusion of Member-led and Institute-led projects, absent an agreement with CHIPS R&D for further Institute operations.

In each case, the Project Call for EWD projects may occur simultaneous to or within any OA3 Project Call. Project progress updates may be included in OA3 progress updates.

1.5 MANUFACTURING READINESS LEVELS

To ensure that Member-led and Institute-led projects lead to real-world industry solutions, CHIPS R&D envisions the CHIPS Manufacturing USA Institute addressing technologies at varying Manufacturing Readiness Levels (MRLs),[15] in accordance with the following guidelines:

MRL 1-3: The Institute may invest limited Federal funds, dependent on the degree of interest from members, in MRL 1-3 projects that involve early-stage technology development, including activities that typically occur at academic institutions. Substantial additional investment may come from industry or other sources of non-Federal funds. Such projects may, for instance, support workforce development and workforce opportunities to students as a substantial outcome. Such projects may be coordinated with Institute projects at MRL 4-7.

MRL 4-7: CHIPS R&D expects that the most substantial portion of Institute investments into Member-led and Institute-led projects will support MRL 4-7 activities.

MRL 8-9: The Institute may invest, dependent on the degree of interest from members, in MRL 8-9 projects that involve late-stage pre-competitive technology development to commercialize digital twins or the application of digital twins to semiconductor manufacturing. CHIPS R&D encourages the Institute Management and Governance Strategy to require, for these projects, cost share or co-investment significantly greater than the Federal investment, if any. Applicants should further indicate how support for projects at MRL 8-9 may impact Institute membership and whether such projects require different Project Call processes, membership, and IP policies.

1.6 GENERAL ROLES OF THE INSTITUTE AWARD RECIPIENT AND NIST

1.6.1 Substantial Involvement

CHIPS R&D will have ongoing and substantial programmatic involvement with the Institute award recipient throughout the award period of performance, aimed at supporting the recipient's activities and working jointly with the recipient in a partnership role. Primary responsibility for the operation and management of the Institute will reside with the Institute award recipient; however, responsibility for specific tasks and activities may be shared between the recipient and CHIPS R&D, or between the recipient and other NIST organizations, as defined below.

[15] Explanations of the MRLs are available at https://dodmrl.com/ and https://acqnotes.com/acqnote/careerfields/manufacturing-readiness-levelmanufact.

1.6.2 Responsibilities of Recipient

CHIPS R&D will require the Institute award recipient to:

(1) Assume primary responsibility for coordination, day-to-day management, and oversight of program activities, financial transactions, reporting obligations, and convening and governing the CHIPS Manufacturing USA Institute and its members.

(2) Attend a kick-off conference, which will be held at the beginning of the performance period, to help ensure that the CHIPS R&D and Manufacturing USA leadership teams have a clear understanding of the program and its components.

   a. The kick-off conference will take place at NIST (Washington, DC area) if the award recipient does not have a facility. It will take place at the award recipient's site if they do have a facility of sufficient size to host the kick-off conference.

   b. Applicants should include travel and related costs for the kick-off conference as part of the budget for year one, and these costs must be reflected in the SF-424 R&R and the budget narrative for year one (Section 4.6.1.8).

(3) Be a collaborative partner within the network of Manufacturing USA Institutes by participating to the extent possible in:

   a. Activities that inform policies and implementation of national strategies for advanced manufacturing innovation, roundtables and summits convened by other Federal agencies, the White House, or non-profit entities such as the National Academies of Sciences, Engineering, and Medicine;

   b. The Manufacturing USA Leaders Council convened by NIST's Office of Advanced Manufacturing (OAM) and the Institute Directors' Council, convened by the elected chairperson of that Council; and

   c. The NIST OAM-convened annual Manufacturing USA network meeting and Education and Workforce Development working groups.

(4) If applicable, coordinate with NIST in the development of collaborations with other Federal agencies, including NIST laboratory programs.

(5) Encourage work environments to implement safety policies, such as NIST's policy for Occupational Safety and Health at Institute- and Member-operated facilities.

1.6.3 Involvement of NIST and CHIPS R&D

NIST / CHIPS R&D may provide, as appropriate:

(1) Programmatic and financial oversight of the Institute award;

(2) Input relevant to the design and development of Institute-led projects and Member-led projects, including EWD projects;

(3) Subject matter experts to support collaborative research conducted within the Institute;

(4) Coordination and engagement with other Federal agencies;

(5) Guidance and support related to approvals for membership of foreign-owned organizations; and

(6) Research security and other relevant support, as described in Section 2.8 and Section 3.1.6.

In an award agreement issued under this NOFO, NIST and potentially other Federal agencies may have access to research material and data, and other outcomes of the Manufacturing USA Institute, in accordance with the member agreements, as applicable.

1.6.4 Joint Activities Between Recipient and NIST and CHIPS R&D

When the technical activities of the Institute align with NIST measurement science priorities, NIST may work collaboratively with the Institute (e.g., through a Cooperative Research and Development Agreement, or CRADA), including by organizing workshops or other conferences or partnering with project teams.

1.6.5 Coordination with other Federal R&D Programs

Realizing the full potential of the CHIPS and Science Act requires alignment across programs towards a common strategy and vision. The CHIPS Manufacturing USA Institute, as a critical element of the broader CHIPS R&D mission, will coordinate closely with other CHIPS R&D programs (NSTC, NAPMP, and CHIPS Metrology).

The following principles guide each program to meet CHIPS R&D's mission:

(1) CHIPS R&D programs and funding should address problems that are of the greatest relevance to the semiconductor industry and align research investments with knowledge gaps, opportunities, and customer demand.
(2) CHIPS R&D programs and funding must prioritize pathways from research to commercialization to ensure long-term U.S. economic competitiveness of the domestic semiconductor industry.
(3) CHIPS R&D programs and funding will avoid unnecessary duplication and competition with each other and with other Federal programs.
(4) CHIPS R&D programs and funding should enable coordination rather than competition among the programs to the greatest extent possible, to leverage activities for maximum impact and long-term sustainability.
(5) CHIPS R&D programs and funding must contribute to a skilled, diverse semiconductor workforce.

In coordination with CHIPS R&D, the Institute is expected to coordinate and work towards agreements with specific Federally funded entities, as applicable and mutually agreed upon, addressing coordination of facilities, data sharing, membership, and research activities. Examples may include agreements covering:

(1) Within six months of award, developing simplified or joint membership processes, with the goal of minimizing burden and friction to research participants to the extent possible.
(2) Within six months of award, participating in the development, review, or selection of research and EWD activities.
(3) Within twelve months of award, towards the validation of digital twins, establishing protocols for access to physical and digital assets (e.g., tools, equipment, standards, and sensor data).
(4) By the end of the first phase, integrating digital twin innovations into Federally funded research and manufacturing.

In addition to the above agreements and consistent with transition and impact strategy evaluation criterion (see Section 5.3.4), CHIPS R&D will favorably consider applications that commit to collaborate with other Manufacturing USA Institutes and support other Federally funded semiconductor-related R&D initiatives. These initiatives may include but are not limited to the U.S. Department of Defense (DoD) National Network for Microelectronics Research and Development, also known as the Microelectronics

Commons; Defense Advanced Research Projects Agency (DARPA) Electronics Resurgence Initiative (ERI) and Next Generation Microelectronics Manufacturing (NGMM); National Science Foundation (NSF) Designing Materials to Revolutionize and Engineer our Future (DMREF); semiconductor education activities at NSF and other agencies; as well as other efforts established by the CHIPS and Science Act of 2022 (P.L. 117-167). Further details will become available as these organizations develop their operational plans and membership programs.

1.7 BROADER IMPACTS

CHIPS R&D is committed to building strong communities that share in the prosperity of the semiconductor industry, as well as ensuring that taxpayer investments maximize benefits for the U.S. economy. CHIPS R&D also strongly supports inclusion, diversity, equity, and access, and firmly believes that the semiconductor industry cannot succeed unless all Americans have an equal opportunity to fully participate, including individuals from underserved communities. In its evaluation and selection processes, CHIPS R&D will consider how proposed Institutes will create broader impacts across the following dimensions.

1.7.1 Commitments to Future Investment

Ensuring U.S. leadership in semiconductor technology and the security and resilience of the domestic semiconductor supply chain will require sustained capital, R&D, and workforce investments. In addition to the projects funded under this NOFO, significant investment will be required to enable the seamless integration of digital twin models into the U.S. semiconductor manufacturing industry and the rapid adoption of Institute-funded innovations. CHIPS R&D therefore encourages applications likely to induce non-Federal investment, beyond what would have occurred absent a CHIPS R&D award, into integrating these innovations into domestic manufacturing facilities and equipment. In selecting applications for award, CHIPS R&D will prioritize applications that include credible commitments (e.g., letters of commitment from potential members highlighting potential financial support or contributions of physical/computational capabilities or follow-on funding) to rapidly move innovations to higher MRL levels, including to production and deployment.

1.7.2 Creating Inclusive Opportunities

CHIPS for America strives for the inclusion of a broad array of partners,[16] as referenced in Section 1.3.1. Consistent with transition and impact strategy evaluation criterion (see Section 5.3.4), CHIPS R&D will favorably consider applications that address the following, for instance:

(1) Outline robust outreach plans and demonstrate the inclusion of a broad array of partners in the funded activities. From the entities consistent with the statute, effective Institutes will likely include the active participation of expert representatives from for-profit and non-profit organizations (including industry-led consortia), covered entities, research universities, community colleges, career and technical education (CTE) schools, Federal laboratories, and State, local, and Tribal governments. As defined in 42 U.S.C. § 18971(b), covered entities include Historically Black College or Universities (HBCUs), Tribal Colleges or Universities, Minority Serving Institutions, a minority business enterprise (as such term is defined in 15 C.F.R. § 1400.2), or a rural-serving institution of higher education (as such term is defined 20 U.S.C. § 1161q). CHIPS R&D further encourages outreach and engagement with government agencies;

[16] See Exec. Order No. 14080, 87 Fed. Reg. 52,847 (Aug. 25, 2022).

labor organizations; public workforce systems;[17] community-based organization; and small and medium-sized manufacturing enterprises,[18] including women-owned, minority-owned, and veteran-owned manufacturing enterprises;

(2) Include meaningful leadership opportunities for early career researchers, including individuals from underserved communities, and emerging research institutions; and

(3) Provide specific plans for training programs that expand opportunities for participation, including for underserved communities such as veterans and individuals with disabilities. Plans could include investing in pre-apprenticeship programs or building recruitment partnerships with community-based organizations that have a track record of serving underserved communities, as demonstrated within the proposal. Plans could also include the Institute or its members, investing in supportive services such as childcare, transportation, and housing, and promoting a safe and respectful workforce culture that prevents harassment and discrimination.

1.7.3 Environmental Responsibility

CHIPS R&D understands that semiconductor companies can reduce their environmental impact, improve the potential for domestic manufacturing, and further their competitive advantage by helping their customers meet environmental goals. Consistent with the transition and impact strategy evaluation criterion (see Section 5.3.4), CHIPS R&D will favorably consider applications that identify, among their Institute-level targets, metrics and milestones that demonstrate the capability of funded technologies to improve upon environmental outcomes of current semiconductor manufacturing methodologies. Such improvements, for instance, could help minimize the potential for adverse impacts on health, the environment, and the local community, including communities with environmental justice concerns[19], by reducing or eliminating the use of per- and polyfluoroalkyl substances (PFAS) or reducing greenhouse gas (GHG) emissions. All applicants are further encouraged to incorporate strategies for pollution prevention, energy efficiency, water efficiency, and renewable energy use in their project approach.

1.7.4 Community Impact and Support

CHIPS for America aims to ensure that its semiconductor manufacturing incentives build strong communities that participate in the prosperity of the semiconductor industry, grow the U.S. economy, and support the creation of good jobs with working conditions consistent with the Good Jobs Principles. CHIPS R&D efforts can complement these goals by further strengthening or expanding regional semiconductor manufacturing and innovation ecosystems, including by facilitating the development of new or existing regional semiconductor industry clusters.[20] Consistent with the transition and impact strategy evaluation criterion (see Section 5.3.4), CHIPS R&D will favorably consider applications that demonstrate the impact of the project on regional ecosystems —such as through their creation of Good Jobs, including for individuals from underserved communities— either as a direct consequence of the project or by virtue of the anticipated research results. Project activities do not necessarily need to be completed within a specific geographic area to demonstrate an impact on a regional semiconductor industry cluster.

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[17] See https://www.dol.gov/agencies/eta/employers/workforce-development-solutions.
[18] See https://www.nist.gov/mep.
[19] See EO 14096: Revitalizing Our Nation's Commitment to Environmental Justice for All.
[20] See https://www.whitehouse.gov/briefing-room/presidential-actions/2022/08/25/executive-order-on-the-implementation-of-the-chips-act-of-2022/.

Applicants or members of Institute teams seeking to demonstrate community impact and support, including impacts on a new or existing regional semiconductor industry cluster, can do so in a variety of ways, as relevant to the objectives and funded activities stated in this NOFO, including through:

(1) Letters of commitment or interest submitted by community-based organizations and local officials;
(2) Letters of commitment or interest submitted by semiconductor and/or supply chain companies with operations or facilities in the selected region or in a relevant regional semiconductor industry cluster;
(3) Letters of commitment or interest submitted by potential customers and/or other stakeholders;
(4) Letters of commitment or interest submitted by labor organizations;
(5) Cost share or co-investment from third parties and philanthropies;
(6) Partnerships with entities focused on innovation, entrepreneurship, access to capital, and technology commercialization in the selected region;
(7) Participation as referenced in Section 1.3.1 and Section 1.7.2; or
(8) Alignment with regional, state, or local economic development strategies, such as relevant Comprehensive Economic Development Strategies, regional or cluster-based growth efforts, or other complementary Federal investments under programs such as the DOC Build Back Better Regional Challenge (BBBRC), DOC Regional Technology and Innovation Hub (Tech Hubs) program, Manufacturing Extension Partnership, or NSF Regional Innovation Engines program, including through strong, concrete commitments to such programs' consortia and participation in consortium/coalition governance.

1.8 OPTIONAL CO-INVESTMENTS

A key goal of the CHIPS Manufacturing USA Institute is to have a significant impact on the semiconductor industry. To fully achieve that goal, CHIPS R&D will prioritize applicants able to secure additional co-investments from members so that they can further develop their technologies and ultimately deploy game-changing technologies.

As part of the Market Transformation Plan (Section 4.6.1.6), applicants should provide commitments from members to advance potential innovations from projects to higher MRLs. These commitments may involve late-stage technology development to commercialize digital twins or the application of digital twins to semiconductor manufacturing. Examples of co-investments may include those commitments required to enable the scale-up, commercialization, and transition to domestic production of Institute-funded innovations.

During the period of performance under the award, CHIPS R&D will work collaboratively with the recipient and Institute members to capture the outcomes and impacts of co-investments while protecting IP and proprietary information, subject to Section 1.6 and Section 2.9.

1.9 GOVERNMENT-FURNISHED PROPERTY (GFP) AND GOVERNMENT FURNISHED INFORMATION (GFI)

Under this NOFO, no GFP or GFI is identified to be provided at this time. Further availability of GFP or GFI may be determined at the time of award or during the award period of performance.

2 FEDERAL AWARD INFORMATION

2.1 FUNDING INSTRUMENT AND PAYMENTS

The Institute award issued under this NOFO will be made be made in the form of an "other transaction" (OT) agreement, as provided in 15 U.S.C. § 4659(a)(1). NIST may issue award payments as advance payments, reimbursements, or a combination of both. The payment method may be negotiated during pre-award negotiations and will be specified in the terms and conditions of an award.

2.2 FUNDING AVAILABILITY UNDER THIS ANNOUNCEMENT

The funding amounts referenced in this NOFO are subject to the availability of funds and the Department's priorities at the time of award. The Department is not responsible for application preparation costs. Publication of this announcement does not obligate the Department to make any specific award or to obligate any available funds. Subject to the availability of funding and based on applications received, CHIPS R&D anticipates making one Institute award for up to approximately $285 million, with a period of performance of up to five years. CHIPS R&D reserves the right not to make any award under this NOFO, based on the quality of applications received, program priorities, and the availability of funds.

2.2.1 Eligible Uses of Funds

Eligible uses of Federal funds under this NOFO include operational activities to run the Institute; basic and applied research related to semiconductor digital twin development; establishing and supporting shared physical and digital facilities; industry-relevant demonstration projects; and digital twin-related workforce training. Where consistent with the objectives of the CHIPS Manufacturing USA Program, applicants may also propose to expend limited funds to protect innovations developed under this NOFO, including to cover fees for patent protection or to enhance research security.

2.2.2 Construction

Construction activities are not an allowable cost with Federal funds under this NOFO. However, costs related to internal modifications of existing buildings that would be necessary to carry out the proposed research tasks may be allowed, at NIST discretion. Construction activities may be permitted when carried out exclusively with optional, non-Federal co-investment funds.

The Department expects applicants to design the Institute and any funded projects so as to avoid, minimize, and mitigate the potential for significant effects on the human environment. While construction activities are not an eligible use of funds under this NOFO, certain activities may be subject to various Federal, state, and local environmental and permitting requirements, such as under the National Environmental Policy Act (NEPA), National Historic Preservation Act (NHPA), Endangered Species Act, Clean Water Act, Clean Air Act, Resource Conservation and Recovery Act, and related Executive Orders. Applicants must assist the Department with compliance with the above requirements and, where applicable, are responsible for obtaining and complying with Federal, state, and local permits.

CHIPS R&D will review full applications to determine whether they provide sufficient information to support NEPA and NHPA reviews, and may, at its sole discretion, request the applicant to provide additional information. The Department may request that an applicant prepare draft environmental analyses, which it will review to determine the potential environmental impacts and consultation needs of proposed activities under consideration for CHIPS R&D funds. CHIPS R&D may also request further supplementary written information or may ask questions during pre-selection interviews and/or site visits. CHIPS R&D will not issue any award until any required environmental review under NEPA for that award has been completed.

2.3 MULTI-YEAR FUNDING POLICY

If an application for a multi-year award is approved, funding will be provided only for the first phase of Institute operations; additional phases will be funded incrementally. Funding for subsequent phases will be contingent upon satisfactory performance; continued relevance to the CHIPS R&D mission, goals, and priorities; and the availability of funds.

CHIPS R&D reserves the right to suspend or terminate an award if phase-specific targets, milestones, and deliverables are not met, or for non-performance under the award agreement, as applicable.

2.4 POSSIBILITY OF AWARD RENEWAL

As described above, any award issued pursuant to this NOFO is expected to have a period of performance of up to five years. In 2019, the Department received authority to non-competitively renew funding for its sponsored Institutes, subject to a rigorous merit review.[21] This merit review would assess whether the Institute has made progress during the initial award period towards a set of performance standards established by NIST.[22]

Approximately one year before the end of the award's period of performance, if funding is anticipated to be available for a renewal award, CHIPS R&D will initiate the required rigorous merit review to determine whether the Institute is eligible for a renewal award. Any renewal award would be issued at the sole discretion of NIST and subject to the availability of funds at the time of the potential renewal.

2.5 INDIRECT (F&A) COSTS

CHIPS R&D will reimburse applicants for proposed indirect costs, commonly referred to as Facilities & Administrative (F&A) Costs, similar to those described at 2 C.F.R. § 200.414. Applicants proposing indirect costs must follow the application requirements set forth in Section 4.6.1.

2.6 PUBLIC ACCESS TO CHIPS R&D RESEARCH

NIST is committed to the principle that the results of Federally funded research are a valuable national resource and a strategic asset. To the extent feasible and consistent with law, agency mission, resource constraints, and U.S. national, homeland, and economic security, NIST will promote the deposit of

[21] See 15 U.S.C. § 278s(e)(2)(B)(i), as amended.
[22] Manufacturing USA Institute Evaluation: Renewal Process and Performance Standards (https://doi.org/10.6028/NIST.AMS.600-8), July 2021.

scientific data arising from unclassified research and programs, funded wholly or in part by NIST, except for Standard Reference Data, free of charge in publicly accessible databases. Subject to the same conditions and constraints listed above, NIST also intends to make freely available to the public, in publicly accessible repositories, all peer-reviewed scholarly publications arising from unclassified research and programs funded wholly or in part by CHIPS R&D.

All applications for activities that will generate research data[23] using funding under this NOFO are required to adhere to a Data Management Plan (DMP) or explain why data sharing and/or preservation are not within the scope of the project (see Section 4.6.1.12).

2.7 FUNDAMENTAL RESEARCH

The National Security Decision Directive (NSDD) 189 defines "fundamental research" as follows:

> *'Fundamental research' means basic and applied research in science and engineering, the results of which ordinarily are published and shared broadly within the scientific community, as distinguished from proprietary research and from industrial development, design, production, and product utilization, the results of which ordinarily are restricted for proprietary or national security reasons.*

Funded activities under this NOFO may include efforts categorized as fundamental research. In submitting an application, the applicant acknowledges that research activities considered to be fundamental research may include or produce IP with relevance to U.S. national or economic security and that requires protection against foreign interference and exploitation. As such, the applicant and any subrecipients agree to comply with the research security requirements described in Section 2.8 of this NOFO.

2.7.1 Fundamental Research Declaration

Institute activities include issuing Project Calls for competitively funded Member-led projects and executing Institute-led projects, both of which may include fundamental research. While NIST/CHIPS R&D reserves sole discretion to determine which elements of a proposed project shall be considered fundamental research, applicants must indicate in the Institute Narrative (see Section 4.6.1.6) specific elements of the initially proposed Institute-sponsored Project Calls and activities or tasks within selected projects that may include fundamental research based on the applicant's understanding at the time of application.

[23] Research data means the recorded factual material commonly accepted in the scientific community as necessary to validate research findings, but not any of the following: Preliminary analyses, drafts of scientific papers, plans for future research, peer reviews, or communications with colleagues. This "recorded" material excludes physical objects (e.g., laboratory samples). Research data also do not include: (i) Trade secrets, commercial information, materials necessary to be held confidential by a researcher until they are published, or similar information which is protected under law; and (ii) Personnel and medical information and similar information the disclosure of which would constitute a clearly unwarranted invasion of personal privacy, such as information that could be used to identify a particular person in a research study.

The Institute award recipient will have an ongoing obligation to inform CHIPS R&D which elements of subsequent Project Calls, selected projects, or tasks within projects (including individual Member-led and Institute-led projects) may include fundamental research.

2.7.2 On-Campus Research

Wherever feasible, the Institute award recipient shall, subject to concurrence by NIST/CHIPS R&D, seek to consider basic or applied research conducted on campus at a university as fundamental research.

2.7.3 Pre-Publication Reviews

The Institute is responsible for ensuring that any Institute activities (e.g., Institute-led or Member-led projects) that include fundamental research will include appropriate language reaffirming the ability of the applicant and members of the project team to publish and broadly disseminate the results of such fundamental research.

For activities that include research not deemed fundamental, the Institute may prescribe, with concurrence from NIST, pre-publication review requirements and other restrictions, as appropriate, for such research. This may require the Institute or the recipient of project awards to submit publications describing work carried out under this NOFO for an efficient pre-publication review, which may include pre-publication review by NIST. The pre-publication review may result in a request for revisions to address national security concerns, including an assessment of whether information disclosed in the publication could negatively impact the patent or proprietary interests of the Institute, the recipient of the project award, other Institute members, or the Federal government.

2.8 RESEARCH SECURITY

It is NIST policy to create a culture of personal and organizational responsibility where the practice and management of research and its products are free from undue influence and interference not essential to the practice of science, such as personal or social allegiances, beliefs, or interests. NIST adheres to the principle that U.S. research leadership benefits from mutually beneficial international collaborations, including welcoming international scientists, and that U.S. national and economic security depends on effective risk management practices for all research organizations to protect against foreign interference and exploitation.

Founded on the NIST core values of perseverance, integrity, inclusivity, and excellence, the NIST Research Security and Safeguarding International Science Team promotes mutually beneficial international engagement using a risk-based methodology to safeguard NIST research programs and intellectual property.

2.8.1 Research Security Definitions

Unless otherwise noted, the definitions for terms used in this section are found in the Appendix to *Guidance for Implementing National Security Memorandum 33 (NSPM-33) on National Security Strategy for United States Government-Supported Research and Development* issued by the National Science and Technology Council in January 2022 (NSTC NSPM-33 Guidance).

2.8.2 Authorities

In recent years, both Congress and the Executive Branch have focused on protecting the security of R&D conducted or funded by Federal agencies. On January 14, 2021, National Security Presidential Memorandum-33 (NSPM-33) was issued to "strengthen protections of United States Government-supported R&D against foreign government interference and exploitation." NSPM-33 requires U.S. agencies that fund R&D to require the disclosure of information related to potential conflicts of interest and commitment from participants in the Federal R&D enterprise.

Under Section 223 of Division A, Title II of the William M. (Mac) Thornberry National Defense Authorization Act (NDAA) for Fiscal Year 2021 (FY21), (Pub. L. No 116–283, codified at 42 U.S.C. § 6605), "covered individuals" (see Section 2.8.4) must disclose the amount, type and source of all current and pending research support, which includes both monetary and non-monetary support, and certify that the disclosure is current, accurate, and complete as part of the application for an R&D award. In addition, covered individuals must agree to update disclosures, as required, before and during the term of the award.

Subtitle D of Title VI of the Research and Development, Competition, and Innovation Act, enacted along with the CHIPS and Science Act of 2022, codified at 42 U.S.C. § 19231 – 19237, also contained research security requirements. On February 14, 2024, the Office of Science and Technology Policy (OSTP) defined the term "foreign talent recruitment program" in issuing *Guidelines for Federal Research Agencies Regarding Foreign Talent Recruitment Programs* required under 42 U.S.C. § 19231(b).

2.8.3 Requirement to Establish a Research Security Program

Pursuant to the authorities described above, applicants under this NOFO must submit a plan to establish a Research Security Program (see Section 4.6.1.6). The plan should identify a member of applicant's leadership team to serve as the point of contact responsible for coordinating with NIST on research security issues. The plan should further describe the Institute's proposed internal processes or procedures to address cybersecurity, foreign talent recruitment programs (as referenced in Section 2.8.2), conflicts of commitment, conflicts of interest, research security training, and research integrity.

In August 2023, NIST published the *Safeguarding International Science: Research Security Framework (NIST IR 8484)*, which provides (1) guidance on establishing a successful research security program; (2) background information related to research security generally; and (3) methodologies and requirements for an integrated, mission-focused, risk-balanced approach for safeguarding international science and technology from undue foreign interference while protecting the openness and integrity of the U.S. research ecosystem. CHIPS R&D has further published a companion document, the CHIPS Technology Protection Guidebook, as a resource for implementing applicant and performer research security requirements.

Upon review of the Research Security Program Plan, NIST may provide the applicant with feedback and an opportunity to refine the plan, as described in Section 2.8.8.

2.8.4 Covered Individuals

For the purposes here, the term "covered individual" is defined as "an individual who (1) contributes in a substantive, meaningful way to the scientific development or execution of a research and development project proposed to be carried out with a research and development award from a Federal research agency; and (2) is designated as a covered individual by the Federal research agency concerned," as under 42 U.S.C. § 6605(d)(1).

In developing the Institute Narrative required under Section 4.6.1.6, the applicant must determine and identify which individuals are covered individuals and provide a brief description (title or one-sentence summary) of the role to be served by each covered individual. Applicants must also complete the Current and Pending Support Forms required under Section 4.6.1.13.

Covered individuals should include the Institute Director, any identified principal investigators, co-investigators, and associate investigators and any individual listed under Section 4.6.1 by the applicant as "key personnel" or as a "Senior/Key Person" or for whom a resume or CV is provided. Personnel who participate only through isolated tasks that are incidental to the research (for example, setting up equipment or performing administrative functions), and those individuals who support research by executing discrete tasks as directed are not covered individuals. Consistent with guidance for implementing NSPM-33, disclosures from broader classes of individuals (e.g., certain graduate students and undergraduate students) will generally be unnecessary, except when the activities of such an individual in a specific proposal rise to the level of meeting the definition of a "covered individual" under 42 U.S.C. § 6605(d)(1).

For awards for Member-led or Institute-led projects, the Institute must further identify to NIST additional covered individuals, specific to the project.

2.8.5 Foreign Entities of Concern

Pursuant to 15 U.S.C. § 4657, none of the funds awarded under this NOFO may be provided to a foreign entity of concern, as defined in 15 U.S.C. § 4651(8) and implemented by the final rule entitled Preventing the Improper Use of CHIPS Act Funding, 88 FR 65600[24] (Sept. 25, 2023), codified at 15 C.F.R. § 231.104. Foreign entities of concern are also ineligible to participate in this NOFO as members or unfunded collaborators.

2.8.6 Research Security Review and Risk Determination

The NIST Research Security and Safeguarding International Science Team will conduct a research security review and a risk determination of applications likely to be selected for award. During the review of the application, NIST will use NIST IR 8484 as the basis for reviewing and assessing research security risks. In conducting this review, NIST will review available information, (e.g., the Current and Pending Support Form and Resume or CV), to assess whether the applicant or any covered individuals, including foreign nationals who are not lawful permanent residents or protected persons as defined in 8 U.S.C. § 1324b(a)(3), are subject to any undue foreign influence or interference through conflicts of interest or

[24] See https://www.federalregister.gov/documents/2023/09/25/2023-20471/preventing-the-improper-use-of-chips-act-funding

conflicts of commitment. Undue foreign influence or interference may include, but is not limited to, associations or affiliations with foreign strategic competitors or governments of countries that have a history of intellectual property theft, research misconduct, or targeting U.S. technology for unauthorized transfer. Affiliations include any past or present organization (foreign and domestic) with whom the applicant has a formal relationship or obligation (e.g., universities, scholarships, professional societies, foreign talent recruitment programs).[25] NIST will examine associations or affiliations during the ten-year period immediately preceding the application submission.

At the conclusion of the research security review for the application, NIST will issue a risk determination of a low, medium, or high risk of potential foreign interference or exploitation.

NIST will base its risk determination of the proposal and covered individuals on a totality of information, which may include but is not limited to:

(1) The ownership structure, subsidiaries, and obligations of the applicant, the Institute team (including subrecipients, contractors, and/or unfunded collaborators);
(2) Conflicts of interest and conflicts of commitment of covered individuals;
(3) Participation of covered individuals in a foreign talent recruitment programs; and
(4) Any military-civil applications of the funded research, as applicable.

If the research security review results in a medium- or high-risk determination, NIST may provide the applicant an opportunity to mitigate the assessed risk, or it may work with the applicant to discuss mitigation strategies (see Section 2.8.8).

NIST or the Institute must also conduct a research security review and a risk determination, as described above, of applications likely to be selected for an Institute-led or Member-led project award.

2.8.7 Non-Discrimination

Consistent with Section 10637 of the CHIPS and Science Act of 2022 and Executive Orders 13985 and 14031, NIST activities that implement NSPM-33 and 42 U.S.C. § 6605 are carried out in a manner that does not inadvertently target, stigmatize, or discriminate against individuals on the basis of race, color, ethnicity, religion, sex (including pregnancy, sexual orientation, or gender identity), national origin, age (40 or older), disability, and genetic information (including family medical history), consistent with Title VI of the Civil Rights Act of 1964 (42 U.S.C. § 2000d et seq.).

2.8.8 Potential for Mitigation

If the NIST Research Security and Safeguarding International Science Team issues a risk determination that an application is high risk, NIST may, at its sole discretion, provide the applicant an opportunity to mitigate the assessed risk prior to CHIPS R&D making a final funding determination. NIST/CHIPS R&D reserves the right to request specific mitigation actions, including but not limited to, requiring additional training for project participants or segmentation of certain tasks of the proposed work, and any follow-up information needed to assess risk or mitigation strategies. CHIPS R&D may determine not to make an award for an application, despite any proposed mitigation terms.

[25] See OSTP *Guidelines for Federal Research Agencies Regarding Foreign Talent Recruitment* Programs.

2.8.9 Requirement for Recipients to Update Research Security-Related Information

Pursuant to 42 U.S.C. § 6605(a)(1)(C), applicants have an ongoing duty to update the NIST Agreements Officer of any changes made to the list of covered individuals or to the foreign affiliations and research financial and in-kind support of such individuals or of the applicant and subrecipients. Prior to NIST making an award under this NOFO, applicants must update the NIST Agreements Officer of any such changes immediately; during the project period of performance, the award recipient must update the NIST Agreements Officer within five (5) business days of such changes being made or of becoming aware of such changes.

Applicants and subrecipients are expected to reasonably exercise due diligence to ensure that covered individuals involved in the subject award are not subject to foreign interference or exploitation.

2.9 INTELLECTUAL PROPERTY (IP) AND DOMESTIC PRODUCTION

As set forth in 15 U.S.C. § 4656(g), the Department must develop policies for the domestic production, to the extent possible, of intellectual property resulting from R&D conducted under this NOFO. Further, 15 U.S.C. § 4656(g) requires CHIPS R&D to develop domestic control requirements to protect such IP (which may include software) from foreign adversaries. For the purposes of 15 U.S.C. § 4656(g), "intellectual property" means any invention that is or may be patentable under U.S. law; and "foreign adversaries" include but are not necessarily limited to any "foreign entity of concern" and "foreign country of concern," as those terms are defined in 15 U.S.C. § 4651(7)-(8) and 15 C.F.R. §§ 231.102 and 231.104.

Both Institute-led and Member-led projects are subject to 15 U.S.C. §4656(g). CHIPS R&D will include special award terms and conditions in the Institute award related to intellectual property and domestic production and control, to meet the requirements of 15 U.S.C. § 4656(g). The Institute may further require, including in coordination with CHIPS R&D, special award terms and conditions in individual project awards, including to address national security concerns.

2.9.1 Domestic Production

For the purposes of 15 U.S.C. § 4656(g), "production" includes the manufacture, integration, assembly, testing, and packaging of semiconductors, materials used to manufacture semiconductors, or semiconductor manufacturing equipment developed or improved as a result of CHIPS-funded intellectual property. CHIPS R&D does not require the covered "production" to occur exclusively within the United States. However, applicants that are unable to conduct certain "production" activities in the United States should explain, to the extent practicable at the current level of technology development, why such production may not be possible, considering the following factors:

(1) The availability or lack of availability of domestic production capabilities, which may consider:
   a. Planned or previous efforts made to locate, develop, or contract for the production of the CHIPS R&D-funded technology, or relevant similar technologies, in the United States;
   b. Access to resources and other material inputs required for production; and
   c. The expected additional product development time or cost required to make U.S. production of the CHIPS R&D-funded technology commercially feasible.

(2) The relative costs of domestic versus foreign production of the CHIPS R&D-funded technology, at relevant production volumes;

(3) Commercial adoption risks and benefits, such as:

   a. Risks to the market acceptance and to the value proposition for the CHIPS-funded technology, resulting from U.S. production; and

   b. Expected commercial, economic, or national security benefits to the United States resulting from distributed production among U.S. and overseas sites; and

(4) Any other factors that are important to the success of the CHIPS R&D-funded technology.

Applicants for an Institute award should describe their intent to maximize domestic production in the Market Transformation Plan and Intellectual Property Rights Management Plan. To the extent applicants are not able to engage in domestic production, applicants should provide reasoning, with reference to the above factors in the Market Transformation Plan. Applicants should be aware that this assessment of domestic production may be an initial assessment, with updates occurring across the award period.

In addition to applying CHIPS R&D's domestic production policies pursuant to 15 U.S.C. 4656(g) as outlined above, CHIPS R&D will also implement the specific domestic production policies explained in 42 U.S.C. 18972(a)(1)(A)-(B) and, if applicable, any waiver process provided in 42 U.S.C. 18972(a)(1)(C).

2.9.2 Domestic Control

To meet the requirements of 15 U.S.C. § 4656(g), CHIPS R&D will include special award terms and conditions related to intellectual property and domestic control, applicable both to the Institute and Institute Members. The relevant terms and conditions will include, at a minimum, the following:

(1) At least one domestic entity must own or co-own any intellectual property resulting from R&D (e.g., Institute-led and Member-led projects) conducted under this NOFO ("resulting intellectual property") and must have full rights to enforce the applicable intellectual property rights, at least for a period of years to be determined prior to the final award.

(2) At the conclusion of the period of years, ownership of the resulting intellectual property may generally be sold, transferred, or assigned to a foreign entity that is not a foreign adversary.

(3) In the event a domestic entity sells, transfers, or assigns ownership of the resulting intellectual property, the entity must promptly disclose such transaction to NIST prior to such transaction.

(4) Any owner or co-owner of the resulting intellectual property (including successors in interest) may not sell, transfer, or assign ownership of such intellectual property to a foreign adversary.

(5) Any owner of the resulting intellectual property may not license such intellectual property to a foreign adversary, subject to the following specific exceptions.

   a. This restriction is not applicable to the following specific exceptions, provided that an owner or co-owner of any patent or patent application resulting from R&D conducted under this NOFO satisfies the notification requirement specified in 5.a.iii below.

      i. This restriction is not applicable to any patent(s) or published patent application(s) (i) declared and/or determined to be essential to a technical standard and (ii) under an obligation that the owner of the patent or published patent application license such rights pursuant to the terms of a standards development organization's Intellectual Property Rights policy.

ii. This restriction is not applicable to any license(s) of patent(s) or published patent application(s), including cross-licenses, resulting from settling an actual case or controversy, including patent infringement or validity disputes, whether part of a formal proceeding or not.

iii. In the event an owner or co-owner of the patent(s) resulting from R&D conducted under this NOFO determines that any of the specific exceptions above applies and plans to license such patent(s) to a foreign adversary pursuant to the exception(s), the owner or co-owner must promptly disclose such action for NIST review.

b. This restriction is not applicable to the sale of a product by a funding recipient (or any other lawful owner, assignee, transferee or licensee of the IP) and any accompanying implied or explicit intellectual property license relating to the use of the product that is sold.

2.9.3 Requirements at the Institute Level

Applicants to this NOFO will be expected to submit an Intellectual Property Rights Management Plan as part of the Project Management and Governance Plan, pursuant to 15 U.S.C. § 4656(g) and as outlined in Section 2.9 and Section 4.6.1.6. The Institute will be required to provide regular updates to the plan to report any new or changed intellectual property or intellectual property governance structures, as described in Section 1.4.1.2.

Applicants to this NOFO are also expected to submit a Market Transformation Plan as part of the Institute Investment Strategy, pursuant to 15 USC 4656(g) and as outlined in Section 2.9.1, Section 2.9.2, and Section 4.6.1.6. The Institute will be required to provide regular updates to the plan as the portfolio of Institute-funded innovations evolves. The Market Transformation Plan should address commercial viability and domestic production and domestic control requirements, as described above in Section 2.9.1, Section 2.9.2, and in the CHIPS R&D Commercial Viability and Domestic Production (CVDP) Plan Guidebook.

2.9.4 Project Level Requirements: Commercial Viability and Domestic Production Plans

Applicants to this NOFO are expected to draft a Phase-Specific Project Plan, as described in Section 4.6.1.6, that addresses the domestic production and domestic control requirements under Sections 2.9.1 and 2.9.2. Applicants to this NOFO are also expected to draft and issue Project Calls for Institute-led and Member-led projects, as outlined in Section 1.4.3 and Section 1.4.4. The Institute will be required to provide regular updates to the Phase-Specific Project Plan, describing progress of Project Call awards.

Consistent with the applicant-submitted Market Transformation Plan and in keeping with the provisions of Executive Order 14104 and the CHIPS Act domestic production requirements (15 U.S.C. §4656(g)), CHIPS R&D may require applicants for Member-Led or Institute-Led projects (i.e., applicants responding to the above Project Calls) to develop and provide a Commercial Viability and Domestic Production (CVDP) Plan describing activities to be funded as part of the project. Applicants should be aware that the CVDP Plan is often intended to be an initial assessment, with updates occurring across the award period.

Depending on the size and scope of the project award, a strong CVDP plan should include a realistic business model for the funded innovations (which may include software), include a technology transition plan, and describe pathways to benefitting national and economic security, such as through the domestic availability of the technology and successful adoption by commercial or defense partners. Applicants for

an Institute-led or Member-led project should propose measurable CVDP targets that demonstrate the viability of the proposed business model and of domestic production. Where relevant, CVDP milestones should complement technical milestones.

Strong applications for Member-led or Institute-led funding should present evidence of existing or potential demand for the funded innovations; identify existing or potential customers, or categories of customers, at volumes necessary for commercial viability; provide an initial assessment of marketability in terms of cost and value proposition that can be updated as the project advances; describe existing or potential competitors and competing technologies; and demonstrate the potential to attract private capital, such as venture capital.

CHIPS R&D strongly encourages applicants for Member-led or Institute-led funding to identify approaches to maximizing market advantages of the funded innovation, such as by reducing manufacturing costs and improving yields (e.g., optimizing process times and achieving economies of scale through increasing volume). Other approaches could include addressing performance, availability, conformance to technical standards, and environmental sustainability. CHIPS R&D further encourages applicants for Member-led or Institute-led funding to outline mechanisms (which may include licensing strategies) to encourage domestic adoption, deployment, and integration of the funded innovation into domestic manufacturing processes and supply chains. Additionally, applicants should address any barriers or challenges that may impede U.S. manufacturer access or utilization of the funded innovation and propose strategies to overcome them.

Finally, CHIPS R&D recognizes the importance of preventing the illicit exfiltration of funded innovations, including software, in order to protect competitive advantage. Successful CVDP plans may therefore also consider security and compliance measures to mitigate risks associated with the unauthorized access to the funded innovation, which may include encryption, access controls, authentication mechanisms, and adherence to relevant cybersecurity standards and regulations.

To assist in the development of Phase-Specific Project Plans, which must address commercial viability and domestic production requirements, and the development of individual project-level CVDP plans, CHIPS R&D has published a CHIPS R&D Commercial Viability and Domestic Production (CVDP) Plan Guidebook.

3 ELIGIBILITY INFORMATION

3.1 ELIGIBLE APPLICANTS

Eligible applicants for the Institute award are non-profit organizations; accredited institutions of higher education; State, local, and Tribal governments; and for-profit organizations that are domestic entities. A domestic entity is one incorporated within the United States (including U.S. territories) with its principal place of business in the United States (including U.S. territories). Eligible applicants may only submit one concept paper for the Institute award under this NOFO. Eligible entities may participate in multiple concept papers and applications as a subrecipient.

3.1.1 Institute Teams

CHIPS R&D encourages collaborative proposals under this NOFO, as significant partnership will likely be required to meet the CHIPS Manufacturing USA Program objectives. An eligible applicant may work

individually or include proposed subrecipients, contractors, and/or unfunded collaborators in its application, effectively forming a collaborative Institute team. In an Institute team, eligible subrecipients at the application phase must meet the applicant eligibility requirements stated above. Organizations that are ineligible to apply because they are majority foreign-owned or foreign-controlled may be included in an Institute team as an unfunded collaborator, provided that they are organized and operated in the United States and not subject to the restriction in Section 2.8.5. After an Institute award has been issued, majority foreign-owned or foreign-controlled entities organized and operated in the United States may be allowed as subrecipients or contractors, subject to Section 3.1.6.

3.1.2 Existing Manufacturing USA Institutes

The Manufacturing USA statute prohibits the creation of new Manufacturing USA institutes that substantially duplicate the technical scope and programs of existing Manufacturing USA institutes. Given its specific focus on digital twins for semiconductor manufacturing, CHIPS R&D does not expect this NOFO to solicit applications that duplicate the technical scope and programs of existing institutes. Applications that deviate from these objectives to propose an Institute that substantially overlaps the technical scope of another institute will therefore not be considered.

Organizations executing existing Manufacturing USA institutes, Federally funded centers, consortia, Microelectronics Commons, or other Federally supported membership-based programs are eligible to apply to this NOFO, with the understanding that the Institute must be operationally separate and distinct from other supported efforts. Further, CHIPS R&D strongly encourages the CHIPS Manufacturing USA Institute to build substantive collaborations with other Federally funded activities.

3.1.3 Federally Funded Research and Development Centers

Federally Funded Research and Development Centers (FFRDCs) may participate in awards as subrecipients or contractors, to the extent allowed by law, based on the unique and specific needs of the proposed Institute.

Applicants must identify the FFRDC(s) in the Institute Narrative and provide documentation, attached to the required letter of commitment (see Section4.6.1.11), establishing that FFRDC subrecipients and contractors are able to participate in the proposed work, including:

(1) Documentation demonstrating that the proposed work does not compete with the private sector; and

(2) Documentation from the FFRDC's sponsoring agency citing the FFRDC's eligibility to participate in competitive funding programs of the Federal government; the FFRDC's compliance with the sponsor agreement; and confirmation from the sponsoring agency that they can receive Federal funds from NIST.

FFRDCs interested in participating in this NOFO should first contact their sponsoring agency to discuss their eligibility to receive Federal funds under this NOFO.

3.1.4 Federal Entities

Federal Entities (e.g., Federal departments and agencies, military services educational institutions, etc.) are eligible to participate in Institute activities as subrecipients or contractors, to the extent allowed by

law and subject to applicable direct competition limitations. Federal Entities must clearly demonstrate that the work is not otherwise available from the private sector and provide written documentation citing the specific statutory authority and contractual authority, if relevant, establishing their ability to receive Federal award funds and compete with industry.

In its application, the applicant must identify the inclusion of any Federal entity in the Institute Narrative and provide documentation attached to the required letter of commitment (see Section 4.6.1.11 establishing that Federal entity is able to participate in the proposed work.

3.1.5 Individuals and Unincorporated Sole Proprietors

Individuals and unincorporated sole proprietors are not eligible to receive funding under this NOFO.

3.1.6 Foreign Entities and Foreign Research Activities

Foreign entities are eligible to join an Institute team, a project team, or the membership of the Institute, provided that they are not a foreign entity of concern, subject to CHIPS R&D review and approval. In each case, the applicant leading an Institute award or project award must be a domestic entity.

3.1.6.1 Foreign Entity Justification

CHIPS R&D must provide written approval for a foreign entity's participation in the Institute as a member, unfunded collaborator, funded Institute award, or project award (e.g., Institute-led or Member-led award) prior to the foreign entity's engaging in any Institute-related work The applicant must provide CHIPS R&D with a written justification demonstrating:

(1) That the foreign entity's involvement is essential to advancing Institute objectives, such as by offering access to unique facilities, IP, or expertise that is otherwise not readily available in the United States;
(2) The adequacy of any agreements and protocols between the applicant and foreign entity regarding IP protection and data protection;
(3) The partnership does not jeopardize the soundness of the project's proposed pathway to domestic manufacturing;
(4) As applicable, the foreign entity will comply with any necessary nondisclosure agreements, security regulations, export control laws, audit requirements, and other governing statutes, regulations, and policies;
(5) The foreign entity is not based in a foreign country of concern as defined at 15 U.S.C. § 4651(7) and implemented by the final rule entitled Preventing the Improper Use of CHIPS Act Funding, 88 FR 65600 (Sept. 25, 2023), codified at 15 C.F.R. § 231.104; and
(6) The foreign entity agrees to be subject to a national security review by CHIPS R&D, which may include a risk assessment of IP leakage, if appropriate.

3.1.6.2 Location of funded activity

While the work funded under this NOFO is to be conducted within the United States, certain tasks outside the United States may be allowed based on the unique and specific capabilities of the foreign entity, their relevance to the Institute objectives, and the lack of comparable capabilities in the United States. CHIPS R&D's determination regarding the performance of project tasks outside the United States will be based on information provided by the applicant and by other Federal agencies.

CHIPS R&D will only approve work outside of the United States if it is in the best interest of CHIPS R&D and the United States, including the domestic economy generally, U.S. national security, U.S. industry, and U.S. manufacturing competitiveness.

3.1.6.3 Transferring funding to a foreign entity

While applicants may invite eligible foreign entities to join Institute-led or Member-led project awards as subrecipients or contractors, any disbursement of funds outside the United States, whether by an award recipient, subrecipient, or contractor, must be approved by CHIPS R&D prior to the commencement of the project.

In making such a determination, CHIPS R&D will consider whether the disbursement of funds as proposed advances the economic or national security interests of the United States and the justification described in Section 2.9.

CHIPS R&D will not approve the disbursement of funds to an entity in or under the control of a foreign country of concern under any circumstances.

3.2 COST SHARE REQUIREMENTS

Non-Federal cost share is required for an award issued pursuant to this NOFO. Specifically, this program requires non-Federal cost share in an amount equal to at least the total amount of federal funding over the lifetime of the award (i.e., 50% or more of the total funding for the Institute must come from non-Federal sources).

The cost share may include cash, services, contributions or donations of equipment or other property for use in the project, and third-party in-kind contributions, similar to those described at 2 C.F.R. § 200.306. In addition, the applicant may propose different types of cost share for evaluation other than those described at 2 C.F.R. § 200.306, provided that the proposed cost share is allocable and necessary for the success of the project and approved in writing by the NIST Agreements Officer. The value of cost share to be provided by any subrecipients may be determined using Generally Acceptable Accounting Principles (GAAP).

A proposed and well-supported cost share ratio of significantly more than 1:1 that increases the capability of the Institute will be considered favorably, consistent with the evaluation criteria (see Section 5.3.2). However, the applicant should not include cost share to match or exceed the required minimum equal non-federal cost share if that cost share will not reasonably and realistically contribute to the success of the project during the period of award. NIST reserves the right to disallow any proposed cost share that

NIST determines is unallowable pursuant to this NOFO or otherwise does not contribute to the success of the project.

The applicant must document in the Budget Narrative and Justification (see Section 4.6.1.2 and Section 4.6.1.8) the source and detailed rationale of any proposed cost share, including cash, full- and part-time personnel, and in-kind donations, which will be considered as part of the review under the evaluation criteria. The recipient must provide a budget that meets the minimum cost share requirements by the end of the award. For instructions on incorporating cost share into the Research and Related Budget (Total Fed + Non-Fed) form and the Budget Narrative and Justification, see Section 4.6.1.

3.3 ALLOWABLE COSTS

An award under this program will be made in the form of an other transaction (OT) agreement. The OT agreement will generally use the cost principles set out at 2 C.F.R. Part 200, Subpart E – Cost Principles and 48 C.F.R. Part 31.2 – Contracts with Commercial Organizations, as a guide for determining the terms and conditions of an award issued under this NOFO. As the final awards will not be directly subject to the requirements of 2 C.F.R. Part 200 or 48 C.F.R. Part 31.2, adjustments to the proposed costs may be required at NIST's sole discretion.

4 APPLICATION AND SUBMISSION INFORMATION

4.1 OVERVIEW

The Institute application process consists of a mandatory concept paper and a full application. Full applications will only be accepted from applicants invited after the concept paper stage.

Eligible applicants may only submit one concept paper under this NOFO.

CHIPS R&D may make changes or additions to this NOFO at any time, including, for example, adjustments to submission dates, times, or requirements. All changes will be communicated on Grants.gov. CHIPS R&D may also close the NOFO with at least 60 days' notice and is not obligated to make any federal award or commitment as a result of publishing this announcement.

All submissions must be unclassified. The Department will not reimburse applicants for any costs associated with participation in this NOFO process. Likewise, the cost of preparing concept papers and full applications in response to this NOFO is not an allowable charge (direct or indirect) under any Federal award.

4.2 ADDRESS TO REQUEST APPLICATIONS PACKAGE

The application package for full proposals is available at Grants.gov under Funding Opportunity Number 2024-NIST-CHIPS-MFGUSA-01.

4.3 PAGE COUNT GUIDANCE

This NOFO identifies strict limitations on page counts for the concept paper and the full application. As part of its initial administrative review, CHIPS R&D will redact any pages received in excess of the stated page limits prior to beginning the merit review. The applicant should refer to Tables 2 and 3 to determine which documents and forms are included and excluded in the page count limits for concept papers and full applications, respectively.

4.4 SUBMISSION FORMAT

Applicants should follow the guidance on Grants.gov and the information provided in Section 4.5 and Section 4.6 for concept paper and full application submissions, respectively. This includes requirements for uploading specific required forms and plans. A concept paper or full application received after the due date and time will NOT be evaluated or considered for an award.

Applicants should carefully follow specific Grants.gov instructions to ensure that all attachments will be accepted by the Grants.gov system. A receipt from Grants.gov indicating an application is received does not provide information about whether attachments have been received. For further information or questions regarding applying electronically for the 2024-NIST-CHIPS-MFGUSA-01 NOFO, contact the Grants.gov Help Desk at 800-518-4726.

Document formatting requirements are specified to ensure the readability of the documents by reviewers. Neither the concept paper nor application should contain any hyperlink references used solely to circumvent any page restrictions. All information critical for the application must be contained within the page limits provided in Tables 2 and 3 below for the concept papers and applications.

4.4.1 Amendments

Any amendments to this NOFO will be announced through Grants.gov. Applicants may sign up on Grants.gov to receive amendments by e-mail.

4.4.2 Proprietary and Sensitive Business Information

Applicants must clearly identify proprietary information in their concept papers and full applications. Submissions containing proprietary or sensitive business information must have the cover page and each page containing such information clearly marked with a label such as “Proprietary” or “Sensitive Business Information” and provide an indication as to what specific information is proprietary or sensitive.

Applicants must not submit classified information.

4.5 CONCEPT PAPER INSTRUCTIONS

The content and form of concept papers required pursuant to this NOFO are set forth below.

4.5.1 Required Forms and Documents

4.5.1.1 SF-424 (R&R), Application for Federal Assistance.

Instructions for filling in the SF-424 (R&R) can be found on www.grants.gov, as well as at the NIST Grants Management Division SF-424 Research & Related (R&R) Application Package Guidance.

The SF-424 (R&R) must be signed by an authorized representative of the applicant organization.

For SF-424 (R&R), Items 5, 14, and 19, use the Zip Code + 4 format (##### - ####) when addresses are called for.

The list of certifications and assurances referenced in Item 17 of the SF-424 (R&R) is contained in the Federal Financial Assistance Certifications and Representations (Certs and Reps) as part of the SAM.gov entity registration.

4.5.1.2 Cover sheet and additional items

Items a. through d. below must be completed and attached as a single document to Item 20. Pre-application on the SF-424 (R&R).

Applicants should carefully follow specific Grants.gov instructions at www.grants.gov to ensure the attachment will be accepted by the Grants.gov system. A receipt from Grants.gov does not provide details concerning whether all attachments (or how many attachments) transferred successfully. Applicants will receive a series of e-mail messages over a period of up to two business days before learning whether a federal agency's electronic system has received its application.

The concept paper submission must contain the following materials.

a. **Cover Sheet.** The cover sheet is a one-page document providing:
   - NOFO Name and Reference Number (2024-NIST-CHIPS-MFGUSA-01)
   - Concept paper submission date
   - Name of the applicant organization
   - Name of the Institute Director
   - Major collaborating institutions that the applicant seeks to highlight
   - Proposal title
   - Point of Contact for the applicant, to include name, address, telephone number, and business e-mail address
   - Total funds requested and total proposed cost share and co-investment components, respectively (rough order of magnitude)
   - Any statement regarding confidentiality, including proprietary or sensitive business information, if applicable

   The cover sheet does not contribute to the Concept Paper Narrative page limit.

b. **Concept Paper Executive Summary**

   The Concept Paper Executive Summary is a two-page summary/abstract suitable for

dissemination to the public and must not include any classified information or proprietary or sensitive business information. It should be a self-contained document that identifies the name of the applicant, the Institute Director/principal investigator(s), the application title, the objectives of the proposed Institute, a description of the proposed Institute, the potential impact of the proposed Institute (i.e., benefits, outcomes) including Institute-level targets, and major participants (for collaborative Institute activities). The executive summary does not contribute to the Concept Paper Narrative page limit.

c. **Table of Contents** (This does not contribute to the Concept Paper Narrative page limit.)

d. **Concept Paper Narrative**

The Concept Paper Narrative is a word-processed document of no more than twenty (20) pages with a description of the proposed Institute sufficient to permit evaluation of the concept paper accordance with the Evaluation Criteria.

Submissions containing proprietary or sensitive business information must have the cover page and each page containing such information clearly marked with a label such as "Proprietary" or "Sensitive Business Information" and provide an indication as to what specific information is proprietary or sensitive. Concept papers must not include any classified information.

The Concept Paper Narrative must contain the following:

i. Institute Impact Statement – Provide a clear problem statement and explain how Institute activities are relevant to the CHIPS R&D mission and goals (see Section 1.1.1) and the mission and objectives of the CHIPS Manufacturing USA Program, as expressed in Section 1.1.3.2. Further describe the Institute's contribution to economic and national security, as expressed in the evaluation criteria in Section 5.1.1.

ii. Institute Management and Governance Strategy – Provide an overview of a robust project management plan and governance structure that will engage industry for the most impactful projects, incorporate academic and Federal laboratory research for technical solutions, and integrate CHIPS R&D programs, other Manufacturing USA Institutes, and other U.S. Government funded microelectronics programs (see Section 1.6.5). The strategy must, at a minimum, address:

- *OA1 Institute-level targets.* Provide SMART OA1 Institute-level targets and milestones.
- *Leadership roles and responsibilities*. Describe the key leadership positions within the Institute and the functions of those positions, with an organization chart showing reporting relationships, as applicable. Provide the names of any individuals in key leadership positions, if known. CHIPS R&D will consider each of these individuals as Key Personnel and therefore "covered individuals."
- *Project Solicitation and Selection Process*. Describe the Institute's process for developing and executing roadmaps and Project Calls. Include details for the transparent evaluation, selection, and award of Member-led and Institute-led projects.
- *Membership Model*. Describe the different tiers of membership and the benefits of each tier, including strategies for member outreach and to stimulate sharing of physical and digital capabilities.

iii. Institute Investment Strategy – Consistent with the overall scientific and technical merit evaluation criterion in Section 5.1.3, provide an assessment of the current technological state of the art and the projected state of art resulting from Institute activities. The investment strategy must, at a minimum, address:

- *OA2, OA3, and OA4 Institute-level targets.* Provide SMART Institute-level targets and milestones, noting the feasibility and innovativeness of the required actions and any gaps, constraints, and challenges to address.
- *Education and Workforce Development Plan*. Describe how the Institute will develop, manage, and execute its EWD portfolio to train a diverse and skilled manufacturing workforce and create a Digital Twin-capable workforce, enabling trainees, including individuals from underserved communities, to access good job and career opportunities across the semiconductor industry and meet the needs of members. Provide evidence of alignment with U.S. semiconductor industry needs, such as demonstrated linkages between the skills to be developed and in-demand high quality jobs or to industry-recognized curriculum, credentials, or certifications.
- *Market Transformation Plan*. Describe how the Institute will support advancing CHIPS-funded technologies towards commercialization and adoption with the goal of strengthening U.S. manufacturing competitiveness.
- *Shared Capabilities Infrastructure Plan*. Provide a written plan that describes how the Institute will develop, acquire, manage, operate, and provide access to shared physical assets, computational capabilities, and Institute expertise to achieve the Institute-level targets. The plan should describe—
    - The computational capabilities shared or made available for Institute efforts, including the physical location(s) of such capabilities;
    - The physical assets shared or made available for Institute and member efforts, such as for the verification and validation of digital twins, including the physical location(s) of such assets;
    - The Institute expertise shared or made available for Institute and member efforts, including the physical location(s) of such expertise;
    - A digital marketplace or similar mechanism to enable access to the licenses required to conduct R&D activities; and
    - The process for selecting and adding physical and/or computational capabilities from a diverse set of organizations.

iv. **Table of Funded Participants and Unfunded Collaborators.** Provide a table that identifies all organizations that will participate in and collaborate with the awarded Institute (the Institute team), known at the time of the concept paper submission. The table should consist of an alphabetically ordered list, by organization, of all known Funded Participants[26] and Unfunded Collaborators.[27] The table should include each organization's name, address, Congressional District, the country of incorporation, Dun and Bradstreet number or Federal Unique Entity Identifier, administrative role,

[26] A Funded Participant is an organization or person who receives funds (money) from an Institute as part of their participation. This includes all subrecipients and contractors.

[27] An Unfunded Collaborator is any organization or person who will not receive funds (money) from an Institute as a part of their collaborative relationship with the Institute.

organization type,[28] scope of work (funded participants only) and proposed total funding amount to the participant (funded participants only). Administrative roles are subrecipient or contractor for funded participants; or unfunded collaborator if they will not receive funding. This table does not contribute to the total number of pages.

v. **Table of Required Cost Share and Optional Co-investment Components and Contributors.** Provide a table detailing all sources of required cost share and optional co-investment, both cash and in-kind. This table does not contribute to the total number of pages.

vi. **Letters of Commitment**. Provide, as an appendix to the concept paper, a letter of commitment from each planned Institute team member indicating their intention to participate in the Institute and the capabilities they expect to provide to the proposed project. This appendix does not contribute to the total number of pages.

Table 1. Concept Paper Format and Guidelines

Paper, Email, and Facsimile (fax) Submissions	Will not be accepted
Figures, Graphs, Images, and Pictures	Should be of a size that is easily readable or viewable and may be displayed in landscape orientation. Any figures, graphs, images, or pictures will count toward the page limits for the Concept Paper Narrative.
Font	Use one of the following fonts: • Arial (not Arial Narrow), Courier New, or Palatino Linotype at a font size of 10 points or larger; • Calibri at a font size of 11 points or larger; • Times New Roman at a font size of 11 points or larger; or • Computer Modern family of fonts at a font size of 11 points or larger.
Page Limit	A portion of the Concept Paper Narrative, as described in Section 4.5.1, is limited to 20 pages. A summary of those components and subcomponents is given below: Institute Impact Statement; Institute Management and Governance Strategy; Membership Model; Institute Investment Strategy; Education Workforce Development Plan; Market Transformation Plan; and Shared Capabilities Infrastructure Plan.
Page Limit Exclusions	Additional materials are required in the Concept Paper (Section 4.5) and are not subject to page limits: Cover Sheet (1 page limit); Concept Paper Executive Summary (2 page limit);

[28] The organization type is selected from the list that is used to complete SF-424 R&R, Item 7.

	Table of Contents; Table of Funded Participants and Unfunded Collaborators; Table of Cost Share and Optional Co-investment Components and Contributors; and Letters of Commitment.
Page Layout	The Concept Paper Narrative must be in portrait orientation.
Page size	21.6 centimeters by 27.9 centimeters (8 ½ inches by 11 inches)
Page numbering	Number all pages sequentially within each section of the application, in a format that is clear and consistent. CHIPS R&D suggests formatting such as 'Concept Paper Narrative page 1 of 10' for ease of reference.
Application language	All documents must be in English, including but not limited to the initial application, any additional documents submitted in response to a CHIPS R&D request, all reports, and any correspondence with CHIPS R&D.
Typed document	All applications, including forms, must be typed.

4.6 FULL APPLICATION INSTRUCTIONS

Full applications will only be accepted from applicants invited after the concept paper stage. Submissions from entities other than those specifically invited to submit a full application will not be reviewed or considered.

4.6.1 Required Forms and Documents

The full application must contain the following:

4.6.1.1 SF-424 (R&R), Application for Federal Assistance

The SF-424 (R&R) must be signed by an authorized representative of the applicant organization.

For SF-424 (R&R), Items 5, 14, and 19, use the Zip Code + 4 format (##### - ####) when addresses are called for.

The list of certifications and assurances referenced in Item 17 of the SF-424 (R&R) is contained in the Federal Financial Assistance Certifications and Representations (Certs and Reps) as part of the SAM.gov entity registration.

SF-424 (R&R), Item 18. If the SF-LLL, Disclosure of Lobbying Activities form (item (4.6.1.5) below) is applicable, attach it to field 18.

Instructions for filling in the SF-424 (R&R) can be found on Grants.gov, as well as at the NIST Grants Office SF-424 Research & Related (R&R) Application Package Guidance.

4.6.1.2 Research & Related Budget (Total Fed + Non-Fed)

The budget should reflect anticipated expenses for the full term of the project (5 years), considering all potential cost increases, including cost of living adjustments.

The budget should be detailed in these categories:

A. Senior/Key Person;
B. Other Personnel;
C. Equipment Description;
D. Travel;
E. Participant/Trainee Support Costs;
F. Other Direct Costs;
G. Direct Costs (automatically generated);
H. Indirect Costs;
I. Total Direct and Indirect Costs (automatically generated);
J. Fee (not relevant to this competition);
K. Total Costs and Fee (automatically generated);
L. Budget Narrative and Justification document (Item 4.6.1.8 below) should be attached to field L.

A separate detailed R&R Budget must be completed for each budget period during the proposed award (e.g., annual basis or by phase). To add additional budget periods (e.g., year 2), click "Add Period" embedded at the end of the form. Information regarding the Research & Related Budget (Total Fed + Non-Fed) is available in the R&R Family Section of Grants.gov, as well as at the NIST Grants Management Division SF-424 Research & Related (R&R) Application Package Guidance.

4.6.1.3 CD-511, Certification Regarding Lobbying

Enter "2024-NIST-MFGUSA-01" in the Award Number field. Enter the title of the application, or an abbreviation of that title, in the Project Name field.

4.6.1.4 Research and Related Other Project Information

Answer the highlighted questions and use this form to attach the Project Narrative (named as Institute Narrative in this NOFO, Section 4.6.1.6**.** below); the Indirect Cost Rate Agreement (Section 4.6.1.9); the Letters of Commitment and Interest, if applicable, (Section 4.6.1.11), the Data Management Plan (Section 4.6.1.12), and the Current and Pending Support Form (Section 4.6.1.13). Instructions for completing the Research and Related Other Project Information form can be found in the Grants.gov R&R Forms Repository by scrolling down to Research And Related Other Project Information and clicking the Instructions link, as well as in the NIST Grants Management Division SF-424 Research & Related (R&R) Application Package Guidance.

Please note that the Project Summary/Abstract is not relevant to this competition. However, Grants.gov requires an attachment to field 7 of the Research and Related Other Project Information form to successfully pass through Grants.gov. Please attach a document to field 7 stating, "A Project Summary/Abstract is not relevant to this competition."

4.6.1.5 SF-LLL, Disclosure of Lobbying Activities

Complete this form if applicable.

4.6.1.6 Institute Narrative

The Institute Narrative is a word-processed document of no more than ninety (90) pages (single-spaced between lines), which is responsive to the program description and the evaluation criteria. The Institute Narrative must contain the following information and elements:

a. **Cover Sheet.** The cover sheet is a one-page document providing:
   - NOFO Name and Reference Number (2024-NIST-CHIPS-MFGUSA-01)
   - Full Application submission date
   - Name of the applicant organization
   - Name of the Institute Director
   - Major collaborating institutions that the applicant seeks to highlight
   - Proposal title
   - Point of Contact for the applicant, to include name, address, telephone number, and business e-mail address
   - Total funds requested and the total proposed cost share and co-investment components, respectively
   - Any statement regarding confidentiality, including with respect to proprietary or sensitive business information, if applicable

   The cover sheet does not contribute to the Institute Narrative page limit.

b. **Executive Summary.** A concise summary/abstract of the proposed effort. The summary/abstract must contain a summary of the proposed activity suitable for dissemination to the public. It should be a self-contained document that identifies the name of the applicant, the Institute Director/principal investigator(s), the application title, the objectives of the proposed Institute, a description of the proposed Institute, methods to be employed, the potential impact of the proposed Institute (i.e., benefits, outcomes), and major participants (for collaborative Institute activities). This document must not include any proprietary or sensitive business information as NIST may make it available to the public after awards are issued. A table can be helpful in providing this information. The executive summary should not exceed two (2) pages. The executive summary does not contribute to the Institute Narrative page limit.

c. **Table of Contents.** This does not contribute to the Institute Narrative page limit.

d. **Institute Description**. A description of the proposed Institute covering items e.-h. below and sufficient to permit evaluation of the application in accordance with the evaluation criteria (see Section 5.3). The Institute Description must not include any classified information. Applicants must clearly identify proprietary information in their Institute Description. Submissions containing proprietary or sensitive business information must have the cover page and each page containing such information clearly marked with a label such as “Proprietary” or “Sensitive Business Information” and provide an indication as to what specific information is proprietary or sensitive.

e. Institute Impact Statement.

- Provide a clear problem statement and explain how Institute activities are relevant to the CHIPS R&D mission and goals (see Section 1.1.1) and the mission and objectives of the CHIPS Manufacturing USA Program, as expressed in Section 1.1.3.2.
- Describe the Institute's contribution to economic and national security, as expressed in the evaluation criteria in Section 5.3.1. Provide, if applicable, evidence of known or expected impacts to the U.S. Department of Defense, other government systems, critical infrastructure, and/or to advancing domestic production.

f. Broader Impacts Statement. Provide an overview of the proposed Institute's broader impacts, consistent with Section 1.7. If relevant, identify impacts on a new or existing regional semiconductor industry cluster.

While construction activities are not an allowable cost under this program, costs related to internal modifications of existing buildings may be allowed, at NIST discretion. Where such costs are proposed, provide a description of whether and how the applicant intends to utilize domestically produced iron, steel, and construction materials as part of their projects, including, for non-Federal entities,[29] how they plan to meet any applicable legal requirements pursuant to the Build America, Buy America Act.

g. **Institute Management and Governance Strategy.** Provide an overview of a robust project management plan and governance structure that will engage industry for the most impactful projects, incorporate academic and Federal laboratory research for technical solutions, and integrate CHIPS R&D programs, other Manufacturing USA Institutes, and other U.S. Government funded microelectronics programs (see Section 1.6.5). The strategy must, at a minimum, address:

i. **OA1 Institute-level targets.** Provide OA1 Institute-level targets and milestones.

ii. **Leadership roles and responsibilities**. Describe the key leadership positions within the Institute and the functions of those positions. Provide:

- An organization chart showing key management positions and reporting relationships, as applicable;
- The names of any such key leaders or key personnel, if known, as well as their roles and responsibilities. CHIPS R&D will consider each of these individuals as "covered individuals;
- The organizational structure, including relationships among the fiduciary Board of Directors/Trustees, technical advisory and strategic governance councils, and other similar bodies of both the Institute award recipient and specific to the Institute; and
- The functions and authorities of any relevant Boards and councils, and how decisions will be made, and disputes will be resolved.

iii. **Business Operations**. Describe the Institute's plan to manage and track the Institute's financial status and compliance with Federal award agreement terms.

iv. **Project Solicitation and Selection Process**. Describe the Institute's proposed process for developing and executing roadmaps and Project Calls. Include details for the open and transparent evaluation, selection, and award of Member-led and Institute-led projects. Include plans to update the roadmap periodically.

[29] Non-Federal entity (NFE) means a State, local government, Indian tribe, Institution of Higher Education (IHE), or nonprofit organization that carries out a Federal award as a recipient or subrecipient (see M-24-02).

v. **Membership Model and Draft Agreement**. This does not contribute to the Institute Narrative page limit. Describe the membership structure, including different tiers of membership and the benefits of each tier. Provide:

- Expected strategies for member outreach, including plans to encourage participation by small and medium-sized enterprises (SMEs), women-owned, minority-owned, and veteran-owned manufacturing enterprises, and if applicable other organizations that serve underserved communities as described in Section 1.3.1;
- Expected strategies to stimulate the sharing of physical and digital capabilities; and
- A draft member agreement, to include any initial **Intellectual Property Rights Management Plan** of IP or physical and computational capabilities.

vi. **Intellectual Property Rights Management Plan**. Provide a written plan that –

- Describes how Applicant(s) plan to manage IP that may be developed as a result of research and development conducted at the Institute (e.g., through Institute-led or Member-led projects), including provisions for Foreground IP, Background IP, commercial and non-commercial licensing of IP, data sharing, and publication;
- Describes how Applicant(s) plan to manage background technology, the use of which may be necessary for research and development in Institute-led projects or Member-led projects, and/or which may be necessary for commercialization of IP developed in Institute-led or Member-led projects. Describe how Background technology will be managed with respect to Institute members' access to such IP (e.g., through a Digital Twin Marketplace);
- Describes the proposed management and ownership of IP and any existing or planned protocols to ensure domestic control and domestic production of CHIPS R&D-funded intellectual property, including to protect such IP (which may include software) from foreign adversaries, pursuant to 15 U.S.C. § 4656(g) and Section 2.9;
- Describes any desired deviations from standard regulations and terms, such as 2 C.F.R. § 200.315 and Section C.03 of the Department of Commerce Financial Assistance Standard Terms and Conditions;
- Describes any additional licensing provisions to protect IP rights, as relevant to the activities to be carried out in the operational areas described in Section 1.4.

vii. **Research Security Plan**. Provide a written plan that–

- Provides a point of contact on research security issues within the Institute leadership team;
- Describes internal processes or procedures to address foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity for both application team personnel and Institute members for the life of the Institute;
- Addresses cybersecurity in the planning, design, and project oversight phases for the Institute, describing measures taken to ensure that appropriate practices for cybersecurity—such as the NIST Cybersecurity Framework and Cybersecurity and Infrastructure Security Agency (CISA) Cybersecurity Performance Goals (CPGs)—are incorporated; and
- Lists any relevant certifications in place or plans to obtain such certifications (e.g., FCL, CMMC) and standards they follow (e.g. ISO/IEC 27001, ISO 8000-51).

viii. **Enterprise Risk Management Plan.** Provide a written plan that–

- Details an enterprise risk assessment and risk mitigation plan covering the technical, economic, and operational aspects of the proposed Institute; and
- Addresses Intellectual property (IP) management; strengthening U.S. manufacturing competitiveness; identifying, handling, and managing sensitive information within the Institute and outside the Institute; and vetting of Institute staff working on projects. It should also address how risks will be re-evaluated periodically and how the Enterprise Risk Management Plan will be updated in response to changes in policy and the identification of emerging risks.

ix. **Institute Transition and Sustainability Plan.** The applicant should describe how the proposed Institute will move towards financial self-sustainability beyond the 5-year award period, including:

- Proposed sources of funding/revenue and the model to support Institute operations;
- A strategy to keep the Institute relevant to industry;
- What resources will be dedicated or otherwise available to support Institute operations beyond the Institute award period;
- How manufacturing professionals will be recruited and trained over time to support the Institute, for both technical operations and EWD programs; and
- A vision for the role that other entities, including other Federally supported research organizations and if applicable, other industry cluster partners, will play in the transition and sustainability of Institute capabilities.

h. **Institute Investment Strategy.** Provide an initial roadmap that identifies the technical and non-technical challenges across OA2, OA3, and OA4. Consistent with the overall scientific and technical merit evaluation criterion in Section 5.3.3, provide an assessment of the current technological state of the art and the projected state of art resulting from Institute activities. The strategy must, at a minimum, address:

i. **OA2, OA3, and OA4 Institute-level targets.** Provide SMART Institute-level targets and milestones, noting the feasibility and innovativeness of the required actions and any gaps, constraints, and challenges that need to be addressed.

ii. **Education and Workforce Development Plan.** Describe how the Institute will develop, manage, and execute its EWD portfolio to achieve the goals and objectives described in Section 1.4.4 The EWD plan should:

- Identify targeted educational or professional levels, support mechanisms (e.g., paid internships, registered apprenticeships, and pre-apprenticeships with direct links to registered apprenticeship programs, and traineeships), and the roles and responsibilities of relevant participating organizations, such as members, accredited educational institutions, including community and technical colleges, state and local education agencies, labor organizations, or other workforce training organizations;
- Explain how Institute efforts will leverage digital twins (1) to train the manufacturing workforce and (2) to create a Digital Twin-capable workforce, enabling trainees to access job opportunities across the semiconductor industry;
- Provide evidence of alignment with U.S. industry needs, such as demonstrated linkages between the skills to be developed and available jobs or to industry-recognized curriculum, credentials, or certifications. Other evidence may include letters of interest from members, other potential employers and labor organizations;

- Describe how the Institute research and development activities will be leveraged to support education and workforce training programs, including the engagement and training of students in research;
- Describe any efforts to maximize access to and participation in the semiconductor workforce, including efforts to attract and retain a diverse student and trainee population such as supportive services and outreach to underserved communities.
- Describe any physical or virtual infrastructure that will be made available to support education and workforce training programs; and
- Describe how programmatic outcomes will be disseminated across the CHIPS R&D programs and other R&D programs including the Manufacturing USA network (see Section 1.6.5).

iii. **Market Transformation Plan**. Provide a written plan describing the pathway to transition Institute-funded innovations to commercial viability and domestic production, where applicable, considering factors such as cost competitiveness, value proposition, and the impact of competitor products. CHIPS R&D has provided a Commercial Viability and Domestic Production Guide to assist in the development of similar plans. Where feasible, the plan should address topics relevant to:

- Market analysis and competitor identification;
- Customer analysis, including perceived barriers to market penetration and any mitigations;
- Financial plans for a sustainable business;
- Commitments from members to advance potential innovations from projects to higher MRLs, including the commercialization of digital twins or the application of digital twins to semiconductor manufacturing (see Section 1.8);
- Domestic production and manufacturing scale-up strategy, including distribution channels;
- Any known factors requiring production outside of the United States, as detailed in Section 2.9.1; and
- Collaborative partnerships with government agencies, industry partners, research institutions, and standards bodies, as required to promote knowledge sharing or consensus building to support the adoption of innovations funded under this NOFO.

iv. **Shared Capabilities Infrastructure Plan.** Provide a written plan that describes how the Institute will develop, acquire, manage, and operate shared physical assets and computational capabilities, to achieve the Institute-level targets. The plan should describe:

- The computational capabilities shared or made available across project team members that will be accessible for Institute efforts, including the physical location(s) of such capabilities;
- The physical assets that will initially be shared or made available across project team members and accessible for Institute efforts such as the verification and validation of digital twins, including the physical location(s) of such assets;
- The physical location(s) of project team members; and
- The process for selecting and adding physical and computational capabilities from a diverse set of organizations.

v. **Phase-Specific Project Plan.** Provide a written plan that describes for Phase 1, at a minimum—

- An organized representation of the Institute's anticipated scope of technical work to be performed and what is expected to be accomplished;
- A draft version of the first Project Call, including both Institute-led and Member-led projects;
- SMART project-specific targets, milestones, and deliverables for Institute-led projects, noting the feasibility and innovativeness of the required actions and any gaps, constraints, and challenges to address;
- Anticipated SMART project-specific targets, milestones, and deliverables for Member-led projects, noting the feasibility and innovativeness of the required actions and any gaps, constraints, and challenges to address;
- An outline of plans for transitioning the above Institute-led or Member-led project technologies to commercial deployment (e.g., summary of commercial viability and domestic production plans); and
- Rough Order of Magnitude (ROM) research and related budgets for each Institute-led and Member-led project.

vi. **Fundamental Research Declaration.** Provide an initial assessment as to which of the Member-led and Institute-led projects identified in the Phase-Specific Project Plan, if any, the applicant believes NIST/CHIPS R&D should consider as fundamental research and the rationale for that determination. Note that NIST/CHIPS R&D reserves sole discretion to determine which elements of a proposed research project shall be considered fundamental.

i. **Gantt Chart/Timeline.** Provide a Gantt Chart/timeline showing achievement of Institute-level targets and corresponding milestones. This does not contribute to the total number of pages.

j. **Table of Abbreviations and Acronyms.** Provide an alphabetical list of all abbreviations, acronyms, and their meanings. This does not contribute to the total number of pages.

k. **Bibliographic List of References.** Provide a complete bibliographic listing of all references used within the application. This does not contribute to the total number of pages.

l. **Compliance Matrix.** Provide a compliance matrix in table format that explains how and where each merit review criterion is addressed in the Institute Narrative or associated application documentation. The table's format is at the discretion of the applicant. This does not contribute to the total number of pages.

m. **Table of Funded Participants and Unfunded Collaborators.** Provide a table that identifies all organizations that will participate in and collaborate with the awarded Institute (the Institute team), known at the time of the application submission. The table should consist of an alphabetically ordered list, by organization, of all Funded Participants and all Unfunded Collaborators. The table should include the organization's name, address, Congressional District, the country of incorporation, Dun and Bradstreet number or Federal Unique Entity Identifier,

administrative role, organization type,[30] scope of work (funded participants only) and proposed total funding amount to the participant (funded participants only). Administrative roles are subrecipient or contractor for funded participants; or unfunded collaborator if they will not receive funding. This does not contribute to the total number of pages.

n. **Table of Required Cost Share and Optional Components and Contributors.** Provide a table listing, in sufficient detail, all contributing sources with respect to the required cost share and optional co-investment, both cash and in-kind contributions.

o. **Estimated Funding by Work Breakdown Structure (WBS)**. The WBS is a tool to organize and describe the work to be performed during all Phases of the Institute. Each WBS divides the work into manageable segments to facilitate program management, schedule management, cost estimating and budgeting, and reporting for the Institute's operations. The WBS is composed of tasks, sub-tasks, and task descriptions. Estimated funding[31] should be listed by uniquely numbered Tasks (i.e., a high-level aggregation of the task's subtasks that have cost that can be easily updated as a group on an annual basis). The tasks named in the WBS should correspond to those listed in the Gantt Chart/Timeline. This does not contribute to the total number of pages.

4.6.1.7 Resume(s) or CV(s)

The submission of resumes or CVs do not contribute to the ninety (90) page limit on the Institute Narrative. Resumes or CVs are required for all key personnel, including the Institute Director and any identified principal investigator(s). For purposes of research security reviews, any individual whose resume is included will be deemed a covered individual. Resumes and CVs must be no longer than two (2) pages. The resumes should highlight experience relevant to the proposed work and should provide sufficient detail for CHIPS R&D to make determinations regarding covered individuals in accordance with 42 U.S.C. § 6605.

4.6.1.8 Budget Narrative and Justification

The Budget Narrative and Justification does not count against the ninety (90) page limit of the Institute Narrative. There is no set format for the Budget Narrative and Justification; however, the written justification must clearly describe the necessity and the basis for the cost, as described below. The written justification must also identify the Federal and non-Federal portion of each cost, to include indirect costs, as applicable. (See Section 3.2 of this NOFO for cost share requirements.). Proposed funding levels must be consistent with the project scope, and only allowable costs should be included in the budget.

In addition, the proposed budget must adhere to Federal cost principles (such as those in 2 C.F.R. Part 200, Subpart E for state/local governments and non-profit organizations, including institutions of higher education or 48 C.F.R. Part 31, Subpart 31.2 for-profit/commercial organizations) for determining allowable costs under this program, for both the Federal share and for the required cost share contribution to be provided by the applicant.

The applicant may propose different types of cost share contributions for evaluation other than those described at 2 C.F.R. § 200.306, provided that the proposed contribution is allocable and necessary for the success of the project and approved in writing by the NIST Agreements Officer. The value of a

[30] The organization type is selected from the list that is used to complete SF-424 R&R, Item 7.
[31] Funding should reflect the total award costs and per year costs composed of both the Federal funds that will be requested and the co-investment or matching that is planned.

contribution to be provided by any subrecipients may be determined using Generally Acceptable Accounting Principles (GAAP). Any cost share contribution incorporated into the budget of an award agreement is legally binding on the recipient and is subject to Federal oversight and audit requirements in the same general manner as Federal award funds, which will be specified in the award agreement to be entered into by NIST and the recipient.

The applicant must document, in the budget table and Budget Narrative, the source and detailed rationale of any cost share contributions, including cash, full- and part-time personnel, and in-kind donations, which will be evaluated in accordance with the Project Management, Resources, and Budget evaluation criteria (Section 5.3.2)**.** Applicants must provide a detailed budget table and budget narrative for Phase 1 of Institute Operations, fully explaining and justifying all proposed expenditures in accordance with applicable Federal cost principles, incorporating both Federal and non-Federal sources of funds. Applicants must also provide a budget table for the remaining years of the award, where budget table shows accounting information broken out by budget form object class categories in rows and summarized by performance year(s) and Federal award total in the columns. The table will also be reviewed to determine if all costs are generally reasonable, allocable, and allowable under cost principles as a guide. A detailed budget narrative for these subsequent years is not required as part of the application but will be required prior to the release of funding for each year. However, any large year-to-year variation should be described in the budget narrative and justification. For example, if funds are set aside for consultants only in the final year of your budget, be sure to explain the rationale (e.g., consultants are intended to support the statistical interpretation of the data and therefore are not needed before the final year).

Information needed for each category is as follows (categories not listed are automatically generated by the form or are not relevant to this competition):

A. **Senior/Key Person** – At a minimum, the budget justification should include the following: name, job title, commitment of effort on the proposed project in terms of average number of hours per week or percentage of time, salary rate, total direct charges on the proposed project, description of the role of the individual on the proposed project and the work to be performed. Fringe benefits should be identified separately from salaries and wages and based on rates determined by organizational policy. The items included in the fringe benefit rate (e.g., health insurance, parking, etc.) should not be charged under another cost category.

B. **Other Personnel** – Data is requested at the project role level, and not at the individual level for Other Personnel. The budget justification should include the following: job title, commitment of effort on the proposed project in terms of average number of hours per week or percentage of time, salary rate, total direct charges on the proposed project, description of the role of the position on the proposed project and the work to be performed.

   Fringe benefits should be identified separately from salaries and wages and based on rates determined by organizational policy. The items included in the fringe benefit rate (e.g., health insurance, parking, etc.) should not be charged under another cost category.

C. **Equipment Description** – Equipment is defined as an item of property that has an acquisition cost of $5,000 or more (unless the organization has established lower levels) and an expected service life of more than one year. The budget justification should list each piece of equipment, the cost, and a description of how it will be used and why it is necessary to the successful completion of the proposed project. Please note that any general use equipment (computers, etc.)

charged directly to the award should be allocated to the award according to expected usage on the project. Any items that do not meet the threshold for equipment can be included under the Materials and Supplies line item in Section F, Other Direct Costs.

D. **Travel** – For all travel costs, required by the recipient to complete the project, including attendance at any relevant conferences and/or meetings, the budget justification for travel should include the following: destination; names or number of people traveling; dates and/or duration; mode of transportation, lodging and subsistence rates; and description of how the travel is directly related to the proposed project. For travel that is yet to be determined, please provide best estimates based on prior experience. If a destination is not known, an approximate amount may be used with the assumptions given for the location of the meeting. Applicants should build into travel budgets anticipated travel and related costs for planned Institute meetings such as an award kick-off conference in year one (1) and an annual Manufacturing USA network meeting, two semiannual Institute Directors Council meetings, and two semiannual Manufacturing USA Council meetings in each of the five (5) performance years.

E. **Participant/Trainee Support Costs** – Participant support costs are stipends, subsistence allowances, travel, and registration fees paid to or on behalf of participants or trainees, who are not employees of your organization, for conferences or training projects. The budget justification should indicate the names or number of participants or trainees, a description and calculation of costs per person, a description and date of the event, and a description of why the cost is necessary for the successful completion of the proposed project.

F. **Other Direct Costs** – For costs that do not easily fit into the other cost categories, please list the cost, and the breakdown of the total costs by quantity or unit of cost. Include the necessity of the cost for the completion of the proposed project. Only allowable costs can be charged to the award.

   Each subaward or contractual cost should be treated as a separate item in the Other Direct Costs category. Describe the services to be provided and the necessity of the subaward or contract to the successful performance of the proposed project. Contracts are for obtaining goods and services. Subrecipients perform part of the project scope of work. For each subaward, applicants must provide budget detail justifying the cost of the work performed on the project.

G. **Indirect Costs** – Commonly referred to as Facilities & Administrative (F&A) Costs, Indirect Costs are defined as costs incurred by the applicant organization that cannot otherwise be directly assigned or attributed to a specific project. For more details, see Section 4.6.1.9 of this NOFO.

4.6.1.9 Indirect Cost Rate Agreement

If indirect costs are included in the proposed budget, provide a copy of the approved negotiated agreement if this rate was negotiated with a cognizant Federal audit agency. If the rate was not established by a cognizant Federal audit agency provide a statement to this effect. If the successful applicant includes indirect costs in the budget and has not established an indirect cost rate with a cognizant Federal audit agency, the applicant may be required to obtain such a rate upon award.

Alternatively, applicants that do not have a current negotiated (including provisional) indirect cost rate may elect to charge a de minimis rate of 10 percent of modified total direct costs (MTDC). Applicants proposing a 10 percent de minimis rate should note this election as part of the budget portion of the application.

4.6.1.10 Subaward Budget Form

The Research & Related Subaward Budget Attachment Form is required if sub-recipients and contractors are included in the application budget.

Instructions for completing subaward budget forms are available by visiting the R & R Family section of the Grants.gov Forms Repository and scrolling down to the R & R Subaward Budget Attachment(s) Form and selecting "Instructions."

4.6.1.11 Letters of Commitment and Interest

(1) **Letters of Commitment**. Letters that commit specific resources or funding to the proposed Institute—in the event the application is funded—are required from all of the following that apply:

a. If the application includes subawards or contracts to known third parties, in some cases effectively forming a team, as described in Section 3.1.1. of this NOFO, a Letter of Commitment from an authorized representative of each known proposed subrecipient and contractor organization must be included. Each letter should indicate the submitting organization's willingness to participate as a contractor or subrecipient, as applicable, describe what work they will do in relation to the Institute Narrative, and specify the associated cost of the proposed subaward or contract to the applicant.

b. If key personnel who are willing to fill vacancies on the applicant's or a subrecipient's staff are identified by the applicant, a Letter of Commitment from each identified person should be included. The letter from each such individual, or group of individuals, should indicate the relationship of the writer to the applicant and the role the individual will play in the Institute's operations.

c. Applicant and Third-Party Non-Federal Cost share and Co-investment: Letters of commitment for all sources of non-Federal co-investment must be included.

i. Applicant Non-Federal Cost share and Co-investment (Cash and In-kind): A letter of commitment is required from an authorized representative of the applicant, stating the total amount of cost share and co-investment to be contributed by the applicant towards the proposed Institute. This letter includes a per year break-out of cash cost share and co-investment and in-kind (non-cash) contributions for the duration of the award.

ii. Third Party Cost share and Co-investment (Cash and In-kind): The applicant must include in its application a letter of commitment from an authorized representative of each third-party organization providing cash or in-kind contributions that are to be used as cost share and co-investment under the proposed Institute. These letters should clearly state whether the third-party contribution will consist of cash contributions, in-kind contributions, or a combination thereof; the total amount or value of the contribution, including a break-out of cash versus in-kind contributions (as applicable); the time period over which the third-party contribution will be made; any interim performance requirements for phased contributions; and all contingencies or pre-conditions to which the contribution is subject.

Letters of Commitment do not contribute to the total number of pages. Letters of Commitment should not be letters submitted by non-proposing entities wishing to vouch for the applicant's (or entities associated with the applicant) knowledge, skills, and abilities or entities to conduct the proposed work. These letters should be in the form of a Letter of Interest.

(2) **Letters of Interest**. Optional letters that indicate willingness from any third party to support this proposed effort. Letters of Interest should outline the nature and importance of the collaboration or involvement being offered. Letters of Interest may also be from non-proposing entities wishing to vouch for the applicant's knowledge, skills, and abilities or entities to conduct the proposed work. Letters of Interest do not contribute to the total number of pages.

4.6.1.12 Data Management Plan

Consistent with NIST Policy 5700.00, *Managing Public Access to Results of Federally Funded Research,* and NIST Order 5701.00, *Managing Public Access to Results of Federally Funded Research*", applicants must include a Data Management Plan (DMP).

All applications for activities that will generate scientific data using NIST funding are required to adhere to a DMP or explain why data sharing and/or preservation are not within the scope of the project. For the purposes of the DMP, NIST adopted the definition of "research data" at 2 C.F.R. § 200.315(e)(3).

The DMP must include, at a minimum, a summary of proposed activities that are expected to generate data; a summary of the types of data expected to be generated by the identified activities; a plan for storage and maintenance of the data expected to be generated by the identified activities, including after the end of the award's period of performance; and a plan describing whether and how data generated by the identified activities will be reviewed and made available to the public.

A template for the DMP, an example DMP, and the rubric against which the DMP will be evaluated for sufficiency are available online.[32] An applicant is not required to use the template as long as the DMP contains the required information.

If an application stands a reasonable chance of being funded and the DMP is determined during the review process to be insufficient, the program office may reach out to the applicant to resolve deficiencies in the DMP. If an award is issued prior to the deficiencies being fully rectified, the award will include a term and condition stating that no research activities shall be initiated or costs incurred for those activities under the award until the NIST Agreements Officer amends the award to indicate the term and condition has been satisfied. Reasonable costs for data preservation and access may be included in the application.

4.6.1.13 Current and Pending Support Form

Applicants must identify all sources of current and potential funding, including this proposal, for all investigators, researchers, and key personnel. Any current project support (e.g., Federal, state, local, public, or private foundations, etc.) must be listed on this form. The proposed project and all other projects or activities requiring a portion of time of the Principal Investigator(s) (PI), co-PI (s), and key personnel must be included, even if no salary support is received. The total award amount for the entire award period covered, including indirect costs, must be shown as well as the number of person-months per year to be devoted to the project, regardless of the source of support. Similar information must be provided for all proposals already submitted or that are being submitted concurrently to other potential funders.

[32] See https://www.nist.gov/open/information-awardees

Applicants must complete the Current and Pending Support Form, using multiple forms as necessary to account for all activity for each individual identified in the PI, co-PI and key personnel roles. A separate form should be used for each identified individual.

Applicants must download the Current and Pending Support Form from the NIST website and reference the guidance provided as it contains information to assist with accurately completing the form.

4.6.1.14 Attachment of Required Documents

Items 4.6.1.1 through 4.6.1.4 above are part of the standard application package in Grants.gov and can be completed through the download application process.

Item 4.6.1.5, the SF-LLL, Disclosure of Lobbying Activities form, is an optional application form which is part of the standard application package in Grants.gov. If item 4.6.1.5, the SF-LLL, Disclosure of Lobbying Activities form is applicable to this proposal, attach it to field 18 of the SF-424 (R&R), Application for Federal Assistance.

Item 4.6.1.6, the Institute Narrative, should be attached to field 8 (Project Narrative) of the Research and Related Other Project Information form by clicking on "Add Attachment".

Item 4.6.1.8, the Budget Narrative and Justification, should be attached to field L (Budget Justification) of the Research & Related Budget (Total Fed + Total Non-Fed) form by clicking on "Add Attachment".

Items 4.6.1.7, Resume(s) or CV(s); 4.6.1.9, the Indirect Cost Rate Agreement; 4.6.1.11, Letters of Commitment if applicable to the submission; 4.6.1.12, the Data Management Plan; and 4.6.1.13, the Current and Pending Support Form, must be completed and attached by clicking on "Add Attachments" found in item 12 (Other Attachments) of the Research and Related Other Project Information form.

Item 4.6.1.10, the Subaward Budget Form(s), if applicable to the submission, should be attached to the Research & Related Subaward Budget (Total Fed + Non-Fed) Attachment(s) Form in the application package.

Following these directions will create zip files which permit transmittal of the documents electronically via Grants.gov.

Applicants should carefully follow specific Grants.gov instructions to ensure the attachments will be accepted by the Grants.gov system. A receipt from Grants.gov indicates only that an application was transferred to a system. It does not provide details concerning whether all attachments (or how many attachments) transferred successfully. Applicants will receive a series of e-mail messages over a period of up to two business days before learning whether a Federal agency's electronic system has received its application.

Applicants are strongly advised to use Grants.gov to access the "Download Submitted Forms and Applications" option to check that their application's required attachments were contained in their submission.

After submitting the application, check the status of your application.[33] If any, or all, of the required attachments are absent from the submission, follow the attachment directions found above, resubmit the application, and check again for the presence of the required attachments.

If the directions at https://www.nist.gov/oaam/grants-management-division/current-and-pending-support are not effective, please contact the Grants.gov Help Desk immediately. If calling from within the United States or from a U.S. territory, please call 800-518-4726. If calling from a place outside the United States or a U.S. territory, please call 606-545-5035. E-mails should be addressed to support@grants.gov. Assistance from the Grants.gov Help Desk will be available around the clock every day, with the exception of Federal holidays. Help Desk service will resume at 7:00 a.m. Eastern Time the day after Federal holidays.

Applicants can track their submission in the Grants.gov system by following the procedures at the Grants.gov site. It can take up to two business days for an application to fully move through the Grants.gov system to NIST.

CHIPS R&D uses the Tracking Numbers assigned by Grants.gov and does not issue Agency Tracking Numbers.

Table 2. Full Application Proposal Format and Guidelines

Paper, Email, and Facsimile (fax) Submissions	Will not be accepted
Figures, Graphs, Images, and Pictures	Should be of a size that is easily readable or viewable and may be displayed in landscape orientation. Any figures, graphs, images, or pictures will count toward the page limits for the Institute Narrative.
Font	Use one of the following fonts: • Arial (not Arial Narrow), Courier New, or Palatino Linotype at a font size of 10 points or larger; • Calibri at a font size of 11 points or larger; • Times New Roman at a font size of 11 points or larger; or • Computer Modern family of fonts at a font size of 11 points or larger.
Page Limit	A portion of the Institute Narrative, as described in Section 4.6.1.6, is limited to 90 pages. A summary of those components and subcomponents is given below: Institute Description; Institute Impact Statement; Broader Impacts Statement; Project Team and Shared Capabilities;

[33] See https://www.grants.gov/help/html/help/index.htm#t=Applicants%2FCheckApplicationStatus%2FCheckApplicationStatus.htm.

	Institute Management and Governance Strategy; Membership Model and Draft Agreement; Intellectual Proper Rights Management Plan; Research Security Plan; Enterprise Risk Management Plan; Institute Transition and Sustainability Plan; Institute Investment Strategy; Education Workforce Development Plan; Market Transformation Plan; Shared Capabilities Infrastructure Plan; Phase-Specific Project Plan; and Fundamental Research Declaration
Page Limit Exclusions	A portion of the Institute Narrative, as described in Section 4.6.1.6, is **not** limited to 90 pages. A summary of those components is given below: Membership Model and Draft Agreement; Cover Sheet (1 page limit); Executive Summary (2 page limit); Gantt Chart/Timeline; Table of Abbreviations and Acronyms; Bibliographic List of References; Compliance Matrix; Table of Funded Participants and Unfunded Collaborators; Table of Cost Share and Optional Co-investment Components and Contributors; and Estimated Funding by Work Breakdown Structure
Page Limit Exclusions	Additional materials are required in the Full Application (Section 4.6) and are not subject to page limits: SF-424 (R&R), Application for Federal Assistance; Research & Related Budget (Total Fed + Non-Fed); CD-511, Certification Regarding Lobbying; Research and Related Other Project Information; SF-LLL, Disclosure of Lobbying Activities; Table of Contents; Resume(s) or CV(s); Budget Narrative and Justification; Indirect Cost Rate Agreement; Subaward Budget Form; Letters of Commitment and/or Interest;

	Data Management Plan; Project Performance/Site Locations(s); and Current and Pending Support Form
Page Layout	The Institute Narrative must be in portrait orientation.
Page size	21.6 centimeters by 27.9 centimeters (8 ½ inches by 11 inches)
Page numbering	Number all pages sequentially within each section of the application, in a format that is clear and consistent. CHIPS R&D suggests formatting such as 'Institute Narrative page 1 of 10' for ease of reference.
Application language	All documents must be in English, including but not limited to the initial application, any additional documents submitted in response to a CHIPS R&D request, all reports, and any correspondence with CHIPS R&D.
Typed document	All applications, including forms, must be typed.

4.6.1.15 Application Replacement Pages

Applicants may not submit replacement pages and/or missing documents once a concept paper or full application has been submitted. Any revisions must be made by submission of a new concept paper or full application that must be received by NIST by the submission deadline.

4.6.2 Unique Entity Identifier and System for Award Management (SAM)

Pursuant to 2 C.F.R. § 25, applicants and recipients are required to (i) be registered in SAM before submitting its concept paper or full application; (ii) provide a valid unique entity identifier in its concept paper or full application; and (iii) continue to maintain an active SAM registration with current information at all times during which it has an active Federal award or an application or plan under consideration by a Federal awarding agency, unless otherwise excepted from these requirements pursuant to 2 C.F.R. § 25.110.

NIST will not make a Federal award to an applicant until the applicant has complied with all applicable unique entity identifier and SAM requirements and, if an applicant has not fully complied with the requirements by the time that NIST is ready to make a Federal award pursuant to this NOFO, NIST may determine that the applicant is not qualified to receive a Federal award and use that determination as a basis for making a Federal award to another applicant.

4.7 SUBMISSION DATES AND TIMES

4.7.1 Concept Papers

Concept papers must be received through Grants.gov no later than 11:59 p.m. Eastern Time, June 20, 2024. Review of the concept papers, selection, and notification to applicants is expected to be complete on or about July 18, 2024.

4.7.2 Full Application

Full applications (by invitations only) must be submitted via Grants.gov no later than 11:59 p.m. Eastern Time, September 9, 2024. Applications received after this deadline will not be reviewed or considered. Paper applications will not be accepted.

CHIPS R&D strongly encourages applicants to begin the process of registering for SAM.gov as early as possible. While this process ordinarily takes between three days and two weeks, in some circumstances it can take six or more weeks to complete due to information verification requirements.

Applicants should be aware, and factor in their application submission planning, that the Grants.gov system closes periodically for routine maintenance. Applicants should visit Grants.gov for information on any scheduled closures.

Please note that an award cannot be issued if the designated recipient's registration in the System for Award Management (SAM.gov) is not current at the time of the award.

4.8 INTERGOVERNMENTAL REVIEW

Applications under this Program are not subject to Executive Order 12372.

4.9 FUNDING RESTRICTIONS

Construction activities are not an allowable cost under this program. However, costs related to internal modifications of existing buildings that would be necessary to carry out the proposed research tasks may be allowed, at NIST discretion. See Section 2.2.2.

In addition, a recipient or a subrecipient may not charge profits, fees, or other increments above cost to an award issued pursuant to this NOFO.

5 APPLICATION REVIEW INFORMATION

5.1 CONCEPT PAPER EVALUATION CRITERIA

The CHIPS R&D merit review process will assess concept papers against the following five technical criteria: relevance to economic and national security; project management, resources, and budget; overall scientific and technical merit; transition and impact strategy; and education and workforce development. The first two criteria—relevance to economic and national security and project management, resources, and budget—will receive the greatest and approximately equal weight. The remaining criteria will receive approximately equal weight to each other. The evaluation will be qualitative, not numerical.

5.1.1 Relevance to economic and national security

This criterion addresses relevance of the proposal to enhancing U.S. economic and national security competitiveness and achieving the CHIPS R&D mission and goals (see Section 1.1.1). Specifically, the applicant must clearly demonstrate its plans and capabilities to enable domestic invention, development, prototyping, manufacture, and deployment of digital twins and other foundational semiconductor technologies. Reviewers will therefore evaluate the extent to which the overall strategy for and design of the proposed Institute is likely to:

(1) Advance domestic semiconductor-related research and development capabilities in the field of digital twins; and

(2) Generate substantial economic benefits to the Nation that extend beyond the direct return to the Institute and its members, including the creation or preservation of jobs.

5.1.2 Project Management, Resources, and Budget

This criterion addresses the reasonableness, appropriateness, and cost-effectiveness of the proposed budget, management strategy, and resources, relative to the work and objectives of the CHIPS Manufacturing USA Program. Reviewers will therefore evaluate the extent to which the concept paper:

(1) Identifies well-defined, aggressive targets and milestones that support the objectives of the CHIPS Manufacturing USA Program;
(2) Demonstrates a robust participation structure for members;
(3) Demonstrates well-defined roles and responsibilities for leadership;
(4) Identifies equipment, facilities, staff, and other shared physical and computational capabilities required to support the Institute and demonstrates either current access to or a clear plan to obtain access to needed items, as detailed in the Shared Capabilities Infrastructure Plan; and
(5) Demonstrates a proposed Federal budget and non-Federal co-investment of sufficient magnitude, quality, and reasonableness to support the objectives of this NOFO.

5.1.3 Overall Scientific and Technical Merit

This criterion addresses the quality, innovativeness, and feasibility of the Concept Paper Narrative and the potential for meeting the mission and objectives of the CHIPS Manufacturing USA Program, as expressed in Section 1.1.3.2. Reviewers will therefore evaluate the extent to which:

(1) The proposed Institute Investment Strategy is well-reasoned, well-organized, and likely to achieve CHIPS Manufacturing USA Program goals; and
(2) The concept paper demonstrates knowledge of the current state of the art in relevant fields and the feasibility of the proposed Institute-level targets to be achieved, considering gaps, constraints, and significant challenges that must be addressed.

5.1.4 Transition and Impact Strategy

This criterion addresses the project's potential for supporting the commercialization and domestic production of funded innovations, as well as beneficial impacts to the broader domestic research, development, and innovation ecosystem. Reviewers will consider the extent to which the proposal:

(1) Demonstrates an understanding of relevant competing commercial and emerging technologies and how the proposed Institute would provide a significant, marketable improvement over these competing technologies.

The evaluation may also consider the applicant's history of transitioning (or plans to transition) technologies to foreign governments or to companies that are foreign owned, controlled, or influenced.

5.1.5 Education and Workforce Development

Concept papers will be evaluated for the quality, completeness, rationality, and feasibility of the proposed Institute's EWD models and plans. Reviewers will therefore evaluate the overall EWD approach and the extent to which the EWD plan:

(1) Includes rational and feasible targets, milestones, and metrics (e.g., students trained, graduated, hired, and retained), appropriate to developing a diverse and skilled workforce;
(2) Provides evidence of alignment with U.S. industry needs; and

(3) Encourages participation by underserved communities, including the education and training of veterans and individuals with disabilities.

5.2 CONCEPT PAPER SELECTION FACTORS

The selection factors for concept papers in this competition are:

(1) Merit Review. Results of the merit reviewers' evaluations, including technical comments, and the evaluation panel's evaluations and adjectival rankings.

(2) Relevance to Program and Mission. Alignment with the objectives and priorities of the CHIPS Manufacturing USA Program and the mission, goals, and priorities of CHIPS R&D.

(3) Non-Duplication. The degree to which the proposed project duplicates other projects funded by NIST or other Federal sources.

(4) Diversity of Projects and Participants. The degree to which the proposed team and project provides for a diversity of proposed project topics, regional diversity, and institutional diversity.

(5) Broader Impacts and Workforce Development. The potential for the proposed project to contribute to broader U.S. research, development, innovation, manufacturing, education, workforce development, and regional economic development goals — including plans for broader impact consistent with Section 1.6.5 and Section 1.7 of this NOFO.

5.3 FULL APPLICATION EVALUATION CRITERIA

The CHIPS R&D merit review process will assess full applications against the following five technical criteria: relevance to economic and national security; overall scientific and technical merit; project management, resources, and budget; transition and impact strategy; and workforce development. The first two criteria—relevance to economic and national security and project management, resources, and budget —will receive the greatest and approximately equal weight. The remaining criteria will receive approximately equal weight to each other. The evaluation will be qualitative, not numerical. Applications will only be recommended for award if each criterion is adequately addressed in the application materials.

5.3.1 Relevance to economic and national security

This criterion addresses relevance of the proposal to enhancing U.S. economic and national security competitiveness and achieving the CHIPS R&D mission and goals (see Section 1.1.1). Specifically, the applicant must clearly demonstrate its plans and capabilities to enable domestic invention, development, prototyping, manufacture, and deployment of digital twins and other foundational semiconductor technologies. Reviewers will therefore evaluate the extent to which the overall strategy for and design of the proposed Institute is likely to:

(1) Advance domestic semiconductor-related research and development capabilities in the field of digital twins;

(2) Create a more resilient U.S. semiconductor supply chain, such as by addressing the risks associated with geographic concentration of current semiconductor production;

(3) Generate substantial economic benefits to the Nation that extend beyond the direct return to the Institute and its members, including the creation or preservation of jobs; and

(4) Support the production of semiconductors necessary to the U.S. Department of Defense, other government systems, or critical infrastructure.

5.3.2 Project Management, Resources, and Budget

This criterion addresses the reasonableness, appropriateness, and cost-effectiveness of the proposed budget, management strategy, and resources, relative to the work and objectives of the Institute. Applicants must demonstrate that they have the appropriate personnel and management structure to complete the work, access to the required capabilities, and that the budget requested matches the need and is reasonable. Reviewers will therefore evaluate the extent to which the proposal:

(1) Clearly describes targets, milestones, and a realistic Institute Management and Governance Strategy that supports the objectives of the CHIPS Manufacturing USA Program;
(2) Identifies key staff, leadership, and technical experts with qualifications and experience appropriate to the proposed work, including prior experience and results in efforts similar in nature, purpose, or scope of proposed activities;
(3) Identifies equipment, facilities, staff, and other shared physical and computational capabilities required to support the Institute and demonstrates either current access to or a clear plan to obtain access to needed items, as detailed in the Shared Capabilities Infrastructure Plan; and
(4) Involves active participation from a broad array of stakeholders, such as industry, small- and medium-sized businesses, academia, and labor and workforce training organizations, as appropriate to meet the objectives of the CHIPS Manufacturing USA Program.

Reviewers will further evaluate the magnitude, evidence, quality, and reasonableness of the proposed Federal budget, non-Federal cost share, and non-Federal co-investment, to include:

(1) The extent to which the proposal provides a clear picture of annual expenditures and a budget that is cost-effective, reasonable, and consistent with the proposed scope of work;
(2) The extent to which the proposed non-Federal cost share provided to the Institute is rational in magnitude and nature, from specific known and anticipated sources, and will exceed the statutory requirement for the proposed Institute;
(3) The extent to which the proposed non-Federal co-investment is rational in magnitude and nature, from specific known and anticipated sources, and will provide for significant investments into developing domestic digital twins or applying digital-twin innovations to the real world; and
(4) Whether the total financial support from non-Federal sources promotes a stable and sustainable business model for the Institute without the need for long-term Federal funding.

5.3.3 Overall Scientific and Technical Merit

This criterion addresses the quality, innovativeness, and feasibility of the proposed Institute Narrative and the potential for meeting the mission and objectives of the CHIPS Manufacturing USA Program, as expressed in 1.1.3.2. Specifically, the proposal must be clear and concise and identify the technical Institute-level targets, a detailed plan and rational approach to achieving those targets, and major technical hurdles, risks, and mitigations. Reviewers will therefore evaluate the extent to which:

(1) The proposed Institute Investment Strategy, including the draft Phase-Specific Project Plan, are well-reasoned, well-organized, presented in sufficient technical detail, and likely to achieve CHIPS Manufacturing USA Program goals;
(2) The proposed activities are innovative, original, or potentially transformative;
(3) The proposal demonstrates knowledge of the current state of the art in relevant fields and the feasibility of the proposed Institute-level targets to be achieved, considering gaps, constraints, and significant challenges that must be addressed; and
(4) The proposal incorporates effective mechanisms to assess success, including meaningful milestones and effective technology demonstrations.

5.3.4 Transition and Impact Strategy

This criterion addresses the project's potential for supporting the commercialization and domestic production of funded innovations, as well as beneficial impacts to the broader domestic research, development, and innovation ecosystem. Reviewers will consider the extent to which the proposal:

(1) Includes a Market Transformation Plan that demonstrates an understanding of relevant competing commercial and emerging technologies and how the proposed Institute would provide a significant, marketable improvement over these competing technologies, as applicable;
(2) Provides a reasonable approach for transitioning Institute-supported technologies to commercial deployment;
(3) Includes a Broader Impacts Statement that demonstrates a credible commitment to future investment, support for other R&D programs, creating inclusive opportunities, environmental responsibility, and community impact and support; and
(4) Describes the potential for the proposed work to contribute to establishing sustainable domestic semiconductor manufacturing capability, such as contributions to the development of new or existing regional semiconductor industry clusters.

The evaluation may also consider the applicant's history of transitioning (or plans to transition) technologies to foreign governments or to companies that are foreign owned, controlled, or influenced.

5.3.5 Education and Workforce Development

Full applications will be evaluated for the quality, completeness, rationality, and feasibility of the proposed Institute's EWD models and plans. Reviewers will therefore evaluate the extent to which the proposal's Education and Workforce Development plan:

(1) Includes rational and feasible targets, milestones, and metrics (e.g., students trained, graduated, hired, and retained), appropriate to developing a diverse and skilled workforce;
(2) Provides evidence of alignment with U.S. industry needs, such as demonstrated linkages between the skills to be developed and in-demand high-quality jobs or to industry-recognized curriculum, credentials, or certifications; and
(3) Encourages participation by underserved communities, including the education, training, of veterans and individuals with disabilities.

5.4 SELECTION FACTORS

The selection factors for this competition are:

(1) Merit Review. Results of the merit reviewers' evaluations, including technical comments, and the evaluation panel's evaluations and adjectival rankings.

(2) Relevance to Program and Mission. Alignment with the objectives and priorities of the CHIPS Manufacturing USA Program and the mission, goals, and priorities of CHIPS R&D.

(3) Funding. The availability of funding and the reasonableness and reliability of cost share or co-investment from specific, known, and anticipated non-Federal sources.

(4) Non-Duplication. The degree to which the proposed program duplicates other projects funded by NIST or other Federal sources.

(5) Diversity of Projects and Participants. The degree to which the proposed team and project provides for a diversity of proposed project topics, regional diversity, and institutional diversity in the overall CHIPS R&D Manufacturing USA portfolio.

(6) Broader Impacts and Workforce Development. The potential for the proposed Institute to contribute to broader U.S. research, development, innovation, manufacturing, education, workforce development, and regional economic development goals — including plans for broader impact consistent with Sections 1.6.5 and Section 1.7 of this NOFO.

5.5 REVIEW AND SELECTION PROCESS

Proposals, reports, documents, and other information related to applications submitted to CHIPS R&D and/or relating to awards issued by CHIPS R&D will be reviewed and considered by Federal employees, or non-Federal personnel who have entered into conflict of interest and confidentiality agreements covering such information, when applicable.

5.5.1 Initial Review of Applications

Concept papers and full applications received by the respective deadlines will be reviewed to determine eligibility, completeness, and responsiveness to this NOFO and stated program objectives. Concept papers and full applications determined to be ineligible, incomplete, and/or nonresponsive will be eliminated from further review. However, CHIPS R&D, in its sole discretion, may continue the review process for any concept paper or full application that is missing non-substantive information, the absence of which may easily be rectified during the review process.

Applicants are reminded that it is a crime to knowingly make false statements to a Federal agency. Misrepresentation of material facts may be the basis for denial of an application. Penalties upon conviction may include fine and imprisonment. For details, please refer to 18 U.S.C. § 1001.

5.5.2 Review of Concept Papers

Concept papers that are determined to be eligible, complete, and responsive will proceed for full reviews in accordance with the review and selection process below.

5.5.2.1 Merit Review

At least three (3) independent, objective reviewers, who may be Federal employees or non-Federal personnel, with appropriate professional and technical expertise relating to the topics covered in this NOFO, will each provide a written evaluation and adjectival rating (see Section 5.5.2.3) for each eligible, complete, and responsive concept paper based on the evaluation criteria (see Section 5.1). While every

concept paper will have at least three (3) reviewers, concept papers may have more than three (3) reviewers if specialized expertise is needed. During the review process, the reviewers may discuss concept papers with each other, but evaluations will be determined on an individual basis, not a consensus.

5.5.2.2 Evaluation Panel

Following the merit review, an evaluation panel consisting of CHIPS R&D staff and/or other Federal employees with the appropriate technical expertise will conduct a panel review of the concept papers. The evaluation panel may contact applicants via e-mail to clarify the contents of a concept paper.

5.5.2.3 Adjectival Rating

The evaluation panel will provide a final adjectival rating and written evaluation of each concept paper to the Selecting Official for further deliberation, considering:

- All concept paper materials.
- Results of the merit reviewers' evaluations, including written assessments.
- Any relevant publicly available information.
- Any clarifying information obtained from the applicants.

The adjectival ratings that will be assigned are:

- Outstanding
- Very Good
- Average
- Deficient

For decision-making purposes, concept papers receiving the same adjectival rating will be considered to have an equivalent ranking.

5.5.2.4 Selection of Successful Concept Papers and Invitations to Submit Full Applications

The NIST Director or designee will serve as the Selecting Official and will make final determinations regarding which concept papers to invite to submit full applications. The Selecting Official shall generally select the most meritorious concept papers for invitation based upon the adjectival ratings and one or more of the Selection Factors. The Selecting Official retains the discretion to select concept papers from a lower adjectival category based on one or more of the Selection Factors. The decisions of the Selecting Official regarding the selection of concept papers are final and may not be appealed. CHIPS R&D may publicly release successful concept paper applicant names to facilitate re-teaming.

5.5.3 Review of Full Applications

Full applications that are determined to be eligible, complete, and responsive will proceed for full reviews in accordance with the review and selection process below.

5.5.3.1 Merit Review

At least three (3) independent, objective reviewers, who may be Federal employees or non-Federal personnel, with appropriate professional and technical expertise relating to the topics covered in this NOFO, will each provide a written evaluation and adjectival rating (see Section 5.5.3.4) for each eligible, complete, and responsive application based on the evaluation criteria (see Section 5.3). While every application will have at least three (3) reviewers, applications may have more than three (3) reviewers if specialized expertise is needed to evaluate an application. During the review process, the reviewers may discuss the applications with each other, but evaluations will be determined on an individual basis, not a consensus.

5.5.3.2 Evaluation Panel

Following the merit review, an evaluation panel consisting of CHIPS R&D staff and/or other Federal employees with the appropriate technical expertise will conduct a panel review of the ranked applications. The evaluation panel may contact applicants via e-mail to clarify contents of an application.

5.5.3.3 Pre-selection Interviews and Site Visits

At CHIPS R&D's discretion, applicants may be requested to participate in Pre-Selection Interviews and/or Site Visits during the evaluation panel phase, either at CHIPS R&D, the applicant's site, a mutually agreed upon location, or via conference call or webinar. The interviews and site visits are intended to allow the applicant to provide clarifications on the contents of the application and provide CHIPS R&D an opportunity to ask questions and collect relevant information. Information provided during the interview and/or site visit will contribute to CHIPS R&D's evaluation of the applications.

5.5.3.4 Adjectival Rating

The evaluation panel will provide a final adjectival rating and written evaluation of the applications to the Selecting Official for further deliberation, considering:

- All application materials.
- Results of the merit reviewers' evaluations, including written assessments.
- Any relevant publicly available information.
- Any clarifying information obtained from the applicants.

The adjectival ratings that will be assigned are:

- Outstanding

- Very Good
- Average
- Deficient

For decision-making purposes, applications receiving the same adjectival rating will be considered to have an equivalent ranking.

5.5.3.5 Selection

The Selecting Official, the NIST Director or designee, will make final award recommendations to the NIST Agreements Officer. The Selecting Official shall generally select and recommend the most meritorious application for an award based upon the adjectival ratings and one or more of the Selection Factors. The Selecting Official retains the discretion to select and recommend an application from a lower adjectival category based on one or more of the Selection Factors.

CHIPS R&D reserves the right to negotiate the budget costs with any applicant selected to receive an award, which may include requesting that the applicant removes certain costs. Additionally, CHIPS R&D may request that successful applicants modify objectives, work plans, or team composition, and provide supplemental information required by the agency prior to award.

CHIPS R&D also reserves the right to reject an application where information is uncovered that raises a reasonable doubt as to the responsibility of the applicant. CHIPS R&D may select some, all, or none of the applications, or part(s) of any application. The final approval of selected applications and issuance of awards will be by the NIST Agreements Officer. The award decisions of the NIST Agreements Officer are final and may not be appealed.

5.5.3.6 Federal Awarding Agency Review of Risk Posed by Applicants

To inform the review by the Selecting Official, NIST will also conduct the research security review described in Section 2.8.6 and the results will be provided to the Selecting Official. Applicants with proposals that have been assessed as having high risk may be given an opportunity to mitigate the risk, as described in Section 2.8.8.

After applications are proposed for funding by the Selecting Official, the NIST Grants Management Division (GMD) performs pre-award risk assessments, which may include a review of the financial stability of an applicant, the quality of the applicant's management systems, the history of performance, and/or the applicant's ability to effectively implement statutory, regulatory, or other requirements imposed on award recipients.

In addition, prior to making an award where the total Federal share is expected to exceed the simplified acquisition threshold (currently $250,000), NIST GMD will review and consider the publicly available Responsibility/Qualification records about that applicant in SAM.gov (formerly available via the Federal Awardee Performance and Integrity Information System (FAPIIS)). An applicant may, at its discretion, review and comment on information about itself previously entered into SAM.gov by a Federal awarding agency. As part of its review of risk posed by applicants, NIST GMD will consider any comments made by the applicant in SAM.gov in making its determination about the applicant's integrity, business ethics, and record of performance under Federal awards. Upon completion of the pre-award risk assessment, the

NIST Agreements Officer will make a responsibility determination concerning whether the applicant is qualified to receive the subject award and, if so, whether appropriate specific conditions that correspond to the degree of risk posed by the applicant should be applied to an award.

5.6 ADDITIONAL INFORMATION

5.6.1 Safety

Safety is a top priority at NIST. Employees and affiliates of award recipients who conduct project work at NIST will be expected to be safety-conscious, to attend NIST safety training, and to comply with all NIST safety policies and procedures, and with all applicable terms of their guest research agreement.

Further, activities funded under this NOFO must be conducted, regardless of location, in compliance with the requirements of the Occupational Safety and Health Act.

5.6.2 Changes in Applicant and Reteaming

An entity invited to submit a full application may change the lead entity to another eligible entity prior to submission of a full application. An applicant may also revise the requested budget amount within its concept paper prior to submission of the full application or reteam by adding new participants or collaborators. The entity that submitted the concept paper must provide written notice of its intent to change the proposed lead entity or revise its requested budget amount in advance of the full application due date to the agency contact listed in Section 7. After submission of a full application and merit review, further revisions may be requested by NIST during award negotiation.

5.6.3 Notification to Unsuccessful Applicants

Unsuccessful applicants at the concept paper stage will be notified by e-mail and may be encouraged to attempt to re-team with those offerors who have been invited to submit a full proposal, as described in Section 5.6.2.

Unsuccessful applicants will have the opportunity to receive a debriefing after the opportunity is officially closed. Applicants must request within 10 business days of the email notification to receive a debrief from CHIPS R&D. CHIPS R&D will then work with the unsuccessful applicant in arranging a date and time of the debrief.

5.6.4 Retention of Unsuccessful Applications

Unsuccessful applications will be retained in accordance with the General Record Schedule 1.2/021.

6 Federal Award Administration Information

6.1 FEDERAL AWARD NOTICES

Successful applicants will receive an award package from the NIST Agreements Officer.

6.2 ADMINISTRATIVE AND NATIONAL POLICY REQUIREMENTS

6.2.1 Terms and Conditions

The complete terms and conditions of each award will be contained in the award package signed by the NIST Agreements Officer.

6.2.1.1 NIST/CHIPS R&D Discretion

Awards in this program require significant ongoing involvement from CHIPS R&D staff and provide NIST the flexibility to alter the course of the project in real-time to meet the overarching goals. This will generally include collaboration with the recipient organization in developing and implementing the approved scope of work.

6.2.1.2 Management Systems and Procedures

Recipient organizations are expected to have systems, policies, and procedures in place by which they manage funds and activities. Recipients may use their existing systems to manage Federal award funds and activities as long as they are consistently applied regardless of the source of funds and across their business functions. To ensure that an organization is committed to compliance, recipient organizations are expected to have in use clearly delineated roles and responsibilities for their organization's staff, both programmatic and administrative; written policies and procedures; training; management controls and other internal controls; performance assessment; administrative simplifications; and information sharing.

6.2.1.3 Financial Management System Standards

Recipients must have in place accounting and internal control systems that provide for appropriate monitoring of other transaction accounts to ensure that obligations and expenditures are congruent with programmatic needs and are reasonable, allocable, and allowable. In addition, the systems must be able to identify unobligated balances, accelerated expenditures, inappropriate cost transfers, and other inappropriate obligation and expenditure of funds, and recipients must notify CHIPS R&D when problems are identified. A recipient's failure to establish adequate control systems constitutes a material violation of the terms of the award.

6.2.2 Funding Availability and Limitation of Liability

Funding for the program listed in this NOFO is contingent upon the availability of appropriations. NIST or the Department of Commerce will not be responsible for application preparation costs, including but not limited to if this program fails to receive funding or is cancelled because of agency priorities. Publication of this NOFO does not oblige NIST or the Department of Commerce to award any specific project or to obligate any available funds.

6.2.3 Collaborations with CHIPS R&D and Other Federal Agencies

CHIPS R&D employees may not participate in the preparation of any application in response to this NOFO. After award, the team is expected to interact with CHIPS R&D and with Federal government organizations and FFRDCs, as appropriate and consistent with their respective missions, objectives, and operational structures.

The award recipient is encouraged to collaborate with Federal entities to support the program goals and to ensure that the Federal investment in this team can be leveraged to the extent appropriate for national priorities.

6.2.4 Post-Award Involvement of Foreign Entities

Once an award has been issued, on a case-by-case basis and subject to a determination by CHIPS R&D, majority foreign-owned or foreign-controlled entities may be allowed as subrecipients or contractors, based on the unique and specific needs of the team. CHIPS R&D's determination of whether a specific foreign-owned or foreign-controlled entity will be allowed to participate as a subrecipient or contractor will be based on information provided by the team and by other Federal agencies. CHIPS R&D will consider whether the foreign entity's participation is in the best interest of the team and the United States, including the domestic economy generally, U.S. industry, and U.S. manufacturing competitiveness. CHIPS R&D will also consider whether the team has sufficiently demonstrated that, among other items, adequate intellectual property and data protection protocols exist between the proposed entity and its foreign parent organization(s).

6.2.5 Use of Federal Government-Owned Intellectual Property

If the applicant anticipates using any Federal government-owned intellectual property, in the custody of NIST or another Federal agency, to carry out the work proposed, the applicant should clearly identify such intellectual property in the proposal. This information will be used to ensure that no Federal employee involved in the development of the intellectual property will participate in the review process for that competition. In addition, if the applicant intends to use the Federal government-owned intellectual property, the applicant must comply with all statutes and regulations governing the licensing of Federal government patents and inventions, described in 35 U.S.C. § 200-212, 37 C.F.R. § 401, 2 C.F.R. § 200.315. Questions about these requirements may be directed to the Chief Counsel for NIST, (301) 975-2803, nistcounsel@nist.gov.

Any use of Federal government-owned intellectual property by a recipient of an award under this announcement is at the sole discretion of the Federal government and will need to be negotiated on a case-by-case basis by the recipient and the Federal agency having custody of the intellectual property if a project is deemed meritorious. The applicant should indicate within the statement of work whether it already has a license to use such intellectual property or whether it intends to seek a license from the applicable Federal agency.

If any inventions made in whole or in part by a NIST employee arise in the course of an award made pursuant to this NOFO, the United States Government may retain its ownership rights in any such invention.

Licensing or other disposition of the Federal government's rights in such inventions will be determined solely by the Federal government, through NIST as custodian of such inventions and include the possibility of the Federal government putting the intellectual property into the public domain.

6.2.6 Export Controls

Some activities may require access to export-controlled items and therefore be subject to export control laws and regulations. If an applicant is selected for award, the applicant and all subrecipients agree to comply with United States export laws and regulations, including, but not limited to, the International Traffic in Arms Regulations and the Export Administration Regulations. Under no circumstances may foreign entities (organizations, companies, or persons) obtain access to export-controlled items unless proper procedures have been satisfied and such access is authorized pursuant to law or regulation. If involvement of foreign entities is approved by CHIPS R&D under Section 6.2.4, recipients must develop measures to properly protect export-controlled information, as appropriate.
Such approval by CHIPS R&D does not constitute authorization for any export licensing requirements which may apply.

Recipients are further responsible for, regarding any Institute-funded innovation (which may include software), complying with applicable laws, regulations, and policies governing intellectual property rights, licensing, and export control.

6.3 REPORTING

6.3.1 Reporting Requirements

The following reporting requirements apply to awards in this program.

6.3.1.1 Financial Reports

Each award recipient will be required to submit an SF-425, Federal Financial Report on a quarterly basis for the periods ending March 31, June 30, September 30, and December 31 of each year. Reports will be due within 30 days after the end of the reporting period. A final financial report is due within 120 days after the end of the project period.

6.3.1.2 Research Performance Monitoring and Reporting

Award recipients will be required to submit quarterly research progress reports within 30 days of the close of the reporting period. CHIPS R&D expects the recipient to include similar content to that requested in the Research Performance Progress Report (*see* 2 C.F.R. § 200.329). However, CHIPS R&D may approve the use of a different format at the request of the recipient.

A final consolidated report shall be submitted within 120 days after the expiration date of the award. The recipient is required to submit publication citation information, links to publicly available data, and other public outputs as soon as they become available.

In addition to the formal quarterly progress reports, the award recipient will be expected to meet quarterly with the Federal Program Officer to discuss operational, technical, and strategic plans. It is expected that the recipient will additionally establish regular and ongoing cadence of informal communication with the Federal program team to ensure timely awareness of issues and achievements.

The recipient is also expected to report progress against specific NIST-issued activity metrics at the end of each phase period, and to contribute data for the Manufacturing USA annual report on a Federal fiscal year basis. NIST will work with the recipient in the start-up phase of the award to implement activity metrics.

6.3.1.3 Patent and Property Reports

In accordance with the terms and conditions governing the award, the recipient may need to submit property and patent reports. The award recipient is required to notify CHIPS R&D of any patents and other intellectual property issuing from work funded by this award. CHIPS R&D requires periodic reporting on the utilization or efforts at obtaining utilization that are being made by the recipient or its licensees or assignees, provided that any such information as well as any information on utilization or efforts at obtaining utilization shall be treated by the Federal agency as commercial and financial information obtained from a person and privileged and confidential and not subject to disclosure.

6.3.1.4 Recipient Integrity and Performance Matters

In accordance with section 872 of Public Law 110-417 (as amended; see 41 U.S.C. § 2313), if the total value of a recipient's currently active grants, cooperative agreements, and procurement contracts from all Federal awarding agencies exceeds $10,000,000 for any period of time during the period of performance of an award made under this NOFO, then the recipient shall be subject to maintaining the currency of information reported to SAM that is made available in FAPIIS about certain civil, criminal, or administrative proceedings involving the recipient.

6.3.2 Audit Requirements

Any recipient that expends Federal awards of $750,000 or more in the recipient's fiscal year must conduct a single or program specific audit similar to the requirements set out in the 2 C.F.R. § 200 Subpart F. Additionally, unless otherwise specified in the terms and conditions of the award, entities that are not subject to Subpart F of 2 C.F.R. § 200 (e.g., for-profit commercial entities) that expend $750,000 or more in DOC funds during their fiscal year must submit to the assigned NIST Agreements Officer either: (i) a financial related audit of each DOC award or subaward in accordance with Generally Accepted Government Auditing Standards; or (ii) a project specific audit for each award or subaward with similar content to that requested in 2 C.F.R. § 200.507. Applicants are reminded that CHIPS R&D, the Department of Commerce Office of Inspector General, the Government Accountability Office, or another authorized Federal agency may conduct an audit of an award at any time.

6.3.3 Federal Funding and Accountability Transparency Act of 2006

In accordance with 2 C.F.R. § 170, all recipients of a Federal award made on or after October 1, 2010, are required to comply with reporting requirements under the Federal Funding Accountability and Transparency Act of 2006 (Public Law No. 109-282). In general, all recipients are responsible for reporting sub-awards of $25,000 or more. In addition, recipients that meet certain criteria are responsible for reporting executive compensation. Applicants must ensure they have the necessary processes and systems in place to comply with the reporting requirements should they receive funding. Also see the Federal register notice published September 14, 2010, at 75 FR 55663.[34]

[34] See http://www.gpo.gov/fdsys/pkg/FR-2010-09-14/pdf/FR-2010-09-14.pdf

7 AGENCY CONTACTS

Questions should be directed to the following:

Subject Area	Point of Contact
Programmatic and Technical Questions	E-mail: askchips@chips.gov with "2024-NIST-CHIPS-MFGUSA-01 Questions" in subject line
Technical Assistance with Grants.gov Submissions	www.grants.gov Phone: 800-518-4726 E-mail: support@grants.gov
Award Management Inquiries	Lisa Ko E-mail: Lisa.Ko@nist.gov with "2024-NIST-CHIPS-MFGUSA-01 Questions" in subject line

8 OTHER INFORMATION

8.1 PERSONAL AND BUSINESS INFORMATION

The applicant acknowledges and understands that information and data contained in applications for other transactions, as well as information and data contained in financial, performance and other reports submitted by applicants, may be used by CHIPS R&D in conducting reviews and evaluations of its financial assistance programs. For this purpose, applicant information and data may be accessed, reviewed, and evaluated by Department of Commerce employees, other Federal employees, Federal agents and contractors, and/or by non-Federal personnel, all of whom enter into appropriate conflict of interest and confidentiality agreements covering the use of such information. As may be provided in the terms and conditions of a specific award, applicants are expected to support program reviews and evaluations by submitting required financial and performance information and data in an accurate and timely manner, and by cooperating with Department of Commerce and external program evaluators. Applicants are reminded that they must take reasonable measures to safeguard protected personally identifiable information and other confidential or sensitive personal or business information created or obtained in connection with a Department of Commerce financial assistance award.

In addition, Department of Commerce regulations implementing the Freedom of Information Act (FOIA), 5 U.S.C. Sec. 552, are found at 15 C.F.R. § 4, Public Information. These regulations set forth rules for the Department regarding making requested materials, information, and records publicly available under the FOIA. Applications submitted in response to this NOFO may be subject to requests for release under the Act. If an application contains information or data that the applicant deems to be confidential commercial information that should be exempt from disclosure under FOIA, that information should be identified, bracketed, and marked as Privileged, Confidential, Commercial, or Financial Information. In accordance with 15 C.F.R. § 4.9, CHIPS R&D and the Department of Commerce will protect from disclosure confidential business information contained in other transaction applications and other documentation provided by applicants to the extent permitted by law.

8.2 PUBLIC WEBSITE

CHIPS R&D has a public website that provides a "Frequently Asked Questions" page and other information pertaining to this NOFO. Any amendments to this NOFO will be announced through Grants.gov.

Applicants must submit all questions pertaining to this NOFO in writing to askchips@chips.gov with "2024-NIST-CHIPS-MFGUSA-01 Questions" in the subject line.