Interactions Between Two Independently Contacted and Rotationally Aligned Graphene Layers

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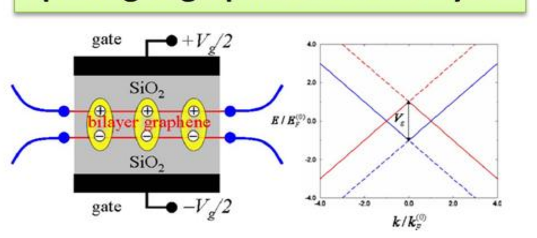
I. Motivation

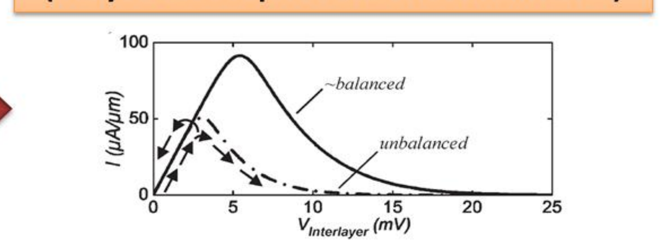
- Graphene double layers may enable novel low-power, low-voltage logic devices.
- Graphene 2D-2D tunneling field-effect transistors: rotational alignment key for momentum conserving tunneling , and negative differential resistance.

Room-temperature electron-hole pairing in graphene double layer



H. Min *et al.*, Physical Review B **78**, 121401 (2008).

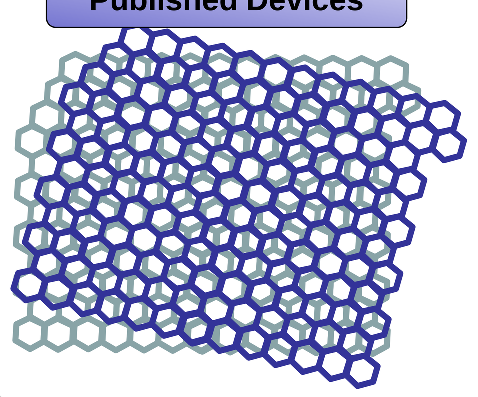
Graphene-based logic device, BiSFET (Bilayer PsedoSpin Field-Effect Transistor)



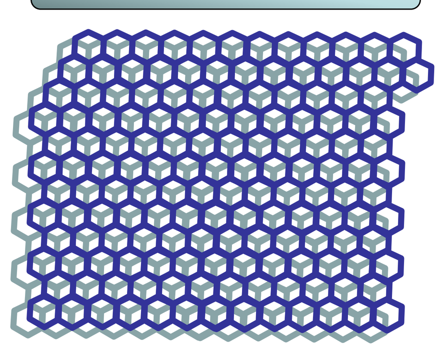
S. K. Banerjee *et al.*, Electron Device Letters, IEEE **30**, 158 (2009).

Bose Einstein condensation of electron-hole pairs → Enhanced interlayer tunneling near zero interlayer bias → Negative differential resistance when rotationally aligned

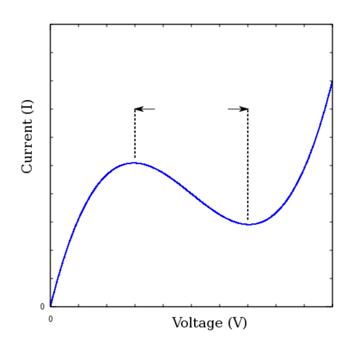
Published Devices



UT Austin New Devices

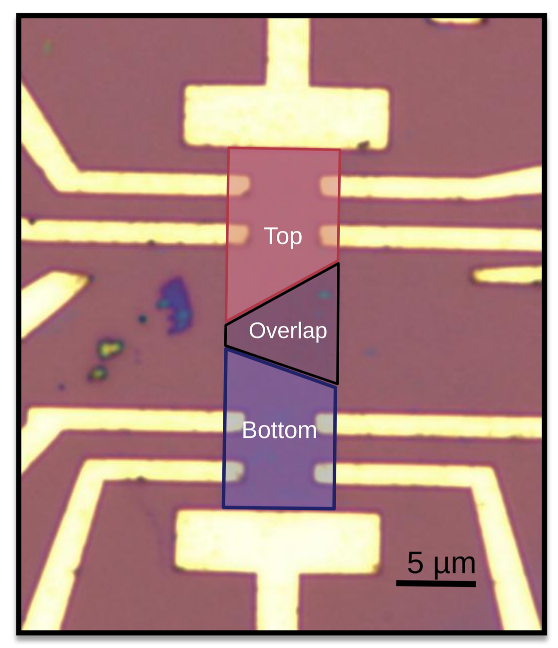


NDR Expected



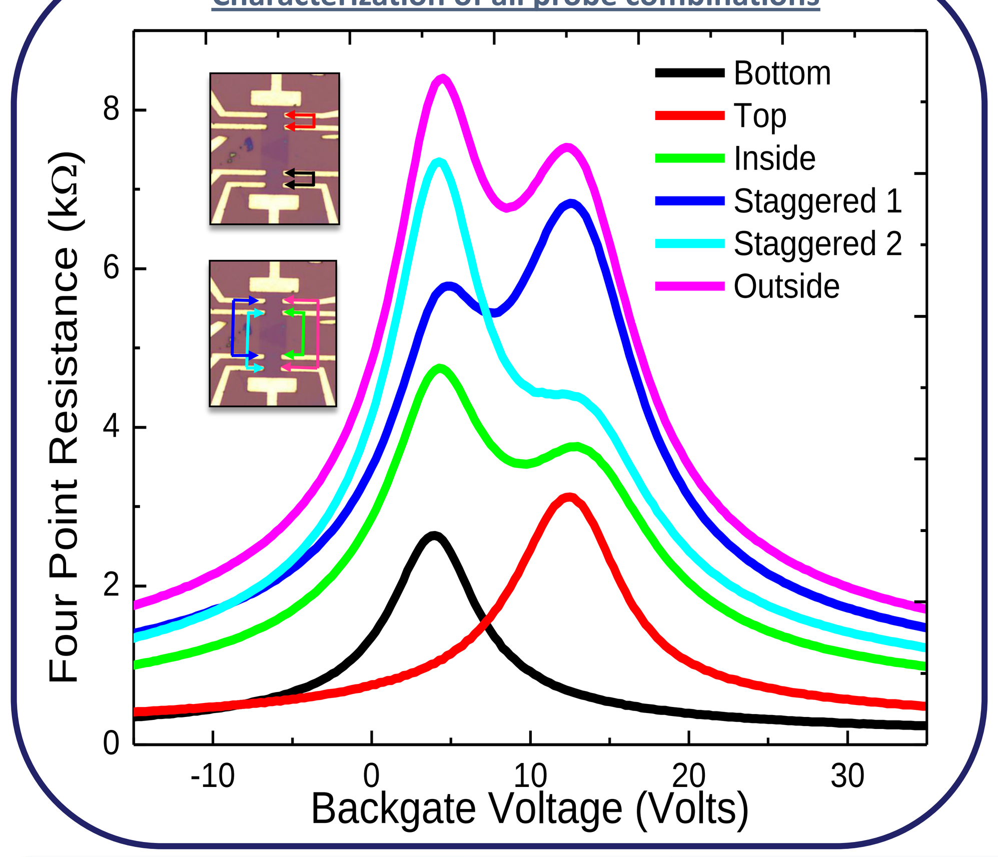
II. Devices Without Rotational Alignment

Device Schematic



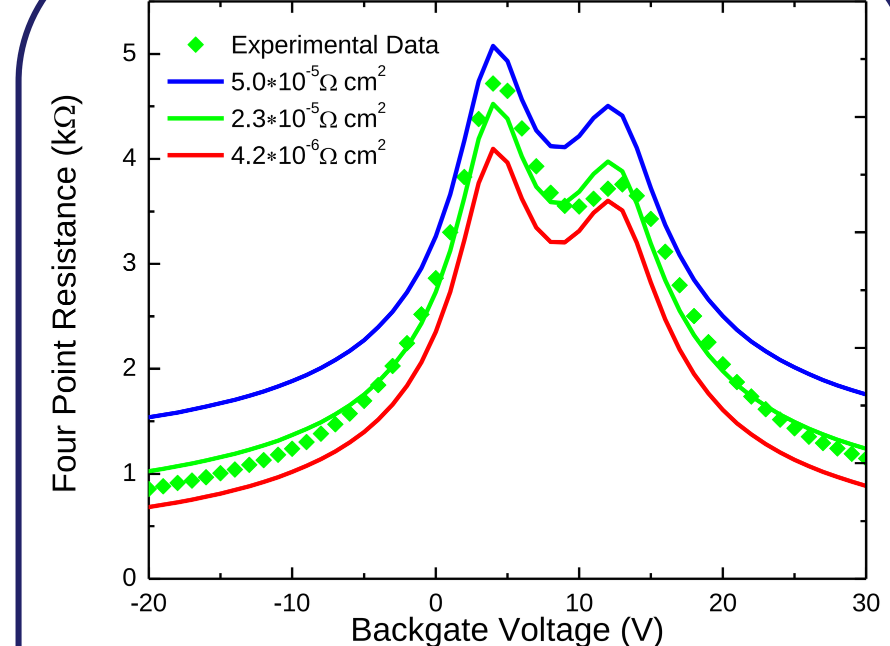
- Independent Hall-bar geometry on top and bottom flakes
- Channel width of 6µm
- Device length of 19 µm
- Total overlap area of 35 µm²
- Overlap areas are device dependent

Characterization of all probe combinations



- ➢Both the bottom and the top flake have high mobilities with low impurity carrier concentrations
- ➢Resistance profiles reflect Dirac point and probe combinations

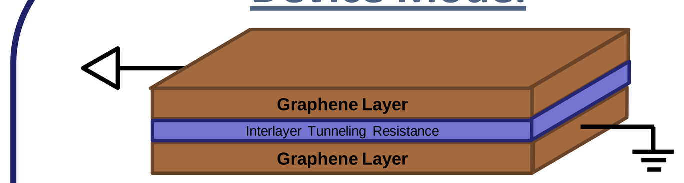
III. Calculating Specific Interlayer Resistance



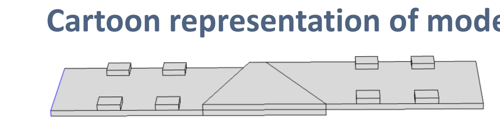
Resistance:

- Calculated using extracted parameters from top and bottom flakes
- Several devices ranging from $2.5 - 7.8 \cdot 10^{-5}$ Ω·cm²
- Several orders of magnitude higher than out of plane graphite

Device Model



Cartoon representation of model



Model of device shown in panel II

Specifics:

- COMSOL Multiphysics 4.0 – FEM Software
- Set layer characteristics and boundary conditions
- Insert / extract interlayer resistance

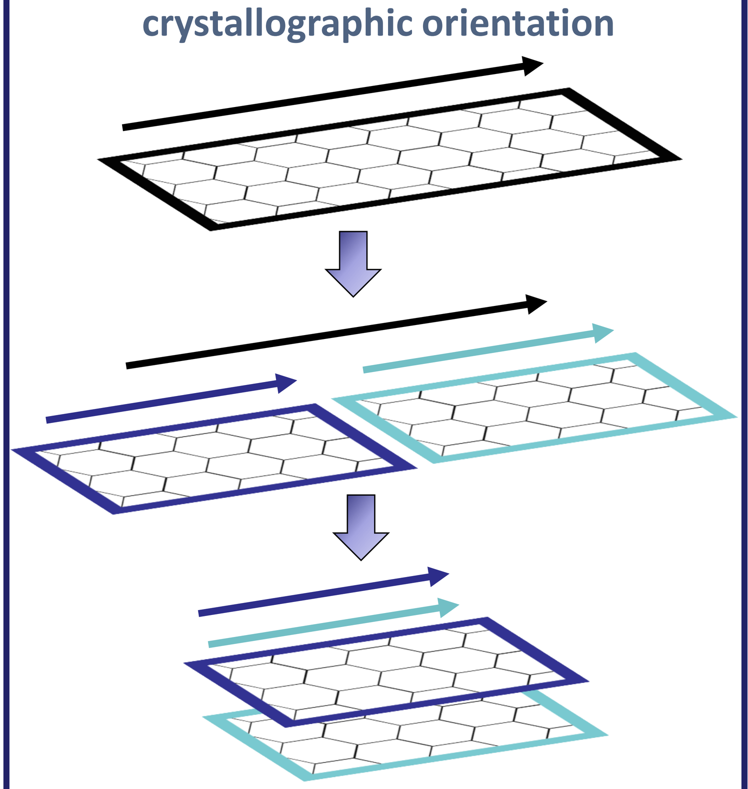
The graphene to graphene contact resistance is

$2.5 \cdot 10^{-5}$Ω·cm²

IV. Exfoliated Graphene Pathway to Rotational Alignment

The Approach

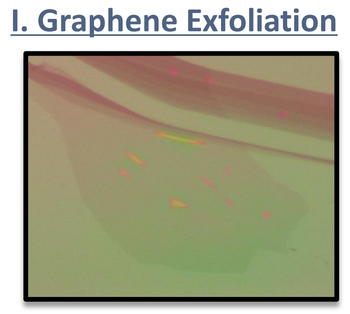
- Exfoliated graphene monolayers are single crystal
- Every monolayer has a single crystallographic orientation



- Isolate a very large exfoliated graphene
- Split the crystal in two sections!
- Keep track of orientation!
- Stack the two sections!

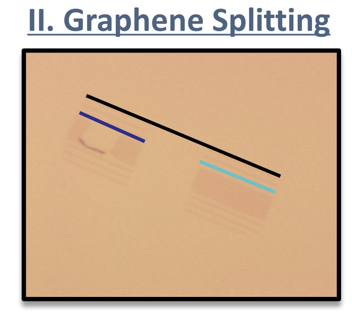
Process Flow

I. Graphene Exfoliation



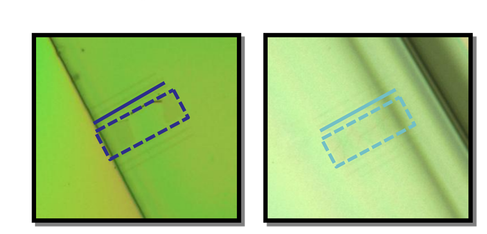
- Micromechanical exfoliation
- Single extremely large flake is required, > 1000 µm²
- EBL and O_2 plasma etching can be used to isolate flakes

II. Graphene Splitting



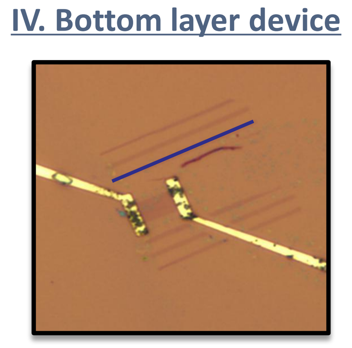
- EBL and O_2 plasma etching used to create active areas
- 'Alignment markers' made of the graphene flake are built in
- Assumption of single crystal

III. Split film and transfer to separate substrates



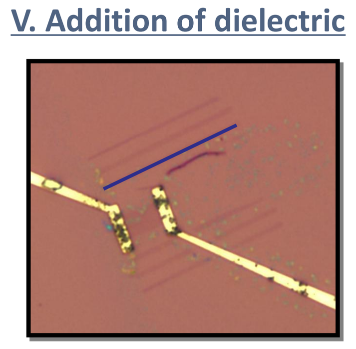
- Split the graphene into separate films and move to individual substrates
- Extend the sacrificial film to center the graphene flakes

IV. Bottom layer device



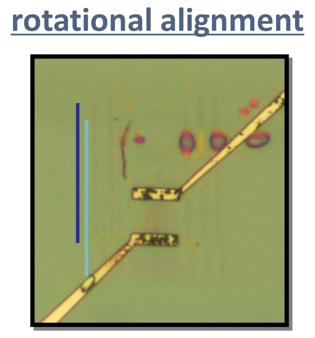
- O_2 plasma to define active area
- 50nm evaporated nickel contacts

V. Addition of dielectric



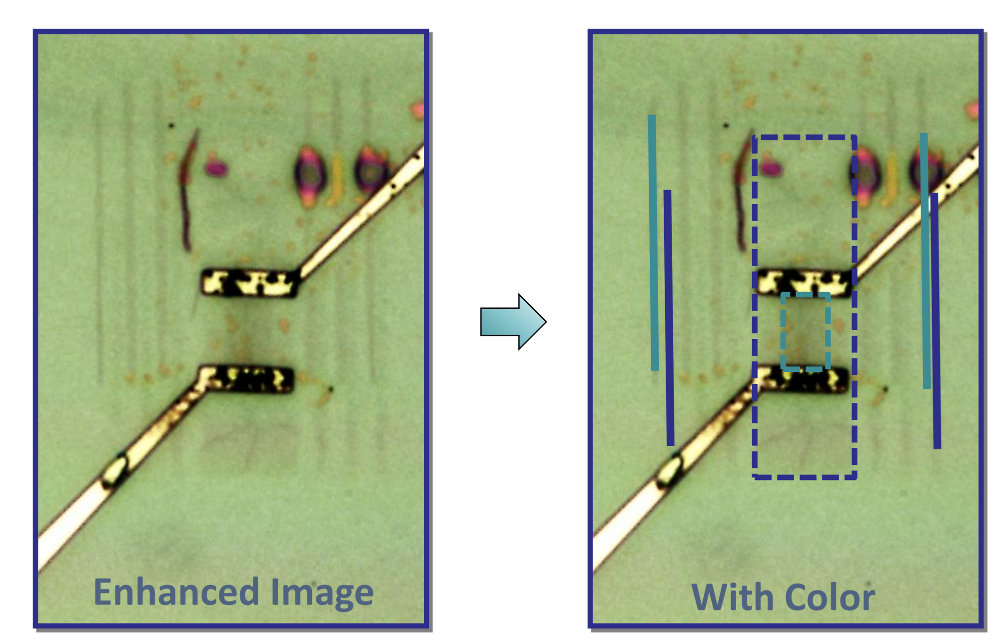
- 8 Angstrom evaporated titanium seed layer
- 2.7 nm alumina atomic layer deposition

VI. Transfer - preserving the rotational alignment



- Transfer secondary film on top of current device
- Preserve rotational alignment via alignment markers

VI. Guaranteed Rotational Alignment



- **Fully overlapped, rotational alignment to less than 1 degree**
- Several devices made
- Various dielectric possibilities, including ultrathin HBN
- Process being improved to avoid polymer residues

VII. Summary

- Theory predicts rotational alignment will be key in achieving negative differential resistance
- Non-rotationally aligned devices fabricated as a baseline
- Model created to extract the specific interlayer contact resistance of the graphene to graphene interface
- The graphene to graphene contact resistance is $2.5 \cdot 10^{-5}$Ω ·cm²
- **Single large grain graphene has been split and overlapped with a rotational alignment of less than one degree**
- Several large grain overlap devices made, reproducible results
- Current issues in device cleanliness, specifically residues from the transfer process.

VII. Acknowledgments

- This work is supported by NRI-SWAN, and DARPA.

SWAN Southwest Academy of Nanoelectronics