FinFET Sidewall Roughness Measurement And Correlation To Device Performance

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INTRODUCTION

o CMOS device performance is directly affected by carrier mobility, which is strongly modulated by surface roughness.

o The high field carrier mobility depends on surface scattering and hence surface roughness.

o In this paper we measure the sidewall roughness using AFM and the LER using CD-SEM of Fin array structures that have gone through a variety of anneal processing.

o A theory is developed on how to correlate this roughness to device transport electrical performance.

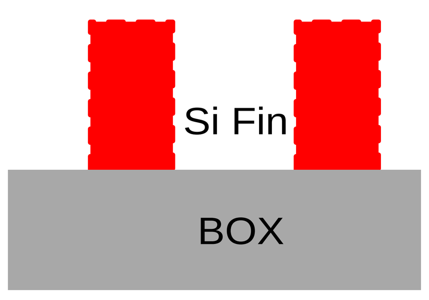

Figure 1. (a) Representation of SOI (silicon on insulator) fin structure cross section with sidewall roughness. The arguments for this paper apply just as well to bulk fins.

Experiment

Sample Preparation

o Hydrogen annealing improves the electrical performance of FinFET devices [1 - 4] through the smoothing of sidewall.

o Ten different hydrogen annealing conditions studied.

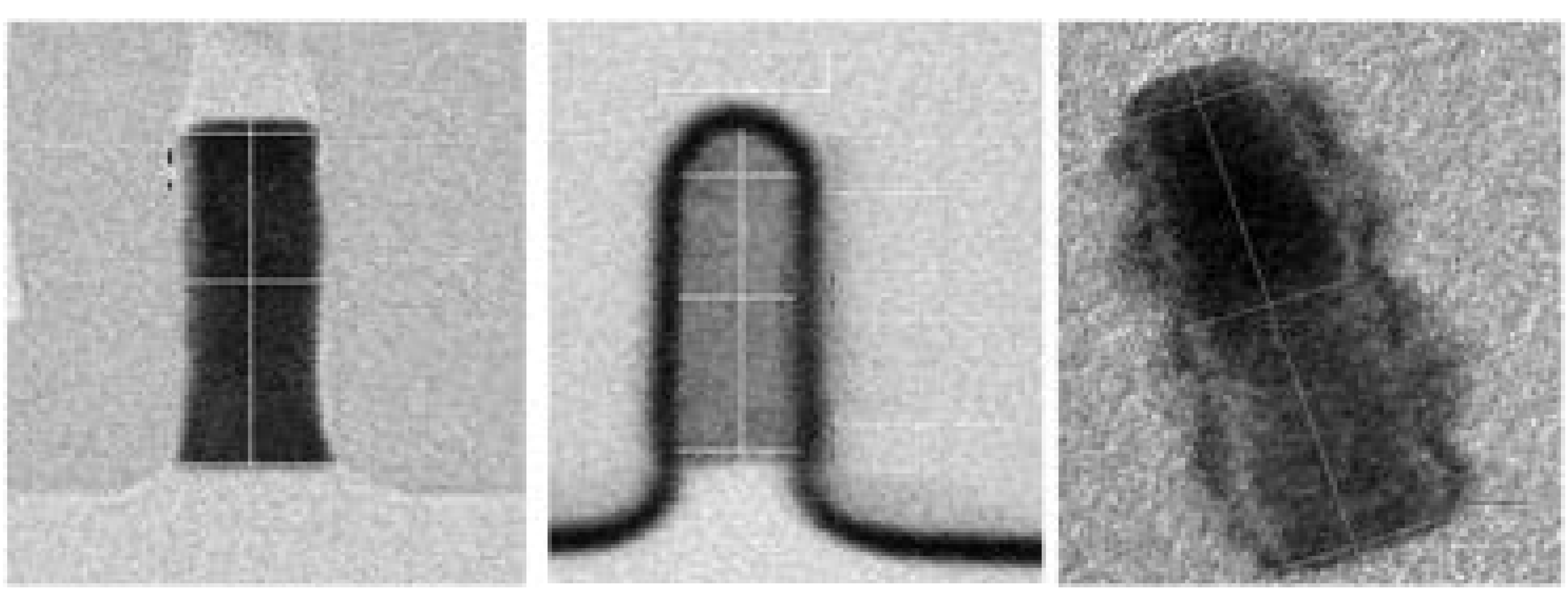

Figure 2. Representative TEM cross section of Fin structures that have been hydrogen annealed with various conditions. The shape and sidewall roughness are highly dependent on the conditions.

CD-SEM and AFM

o Fin were measured by CD-SEM and AFM

- For the AFM, the critical dimension (CD) measurement mode was used – the instrument will dynamically change from dithering vertically on flat surfaces to dithering horizontally on sidewalls.

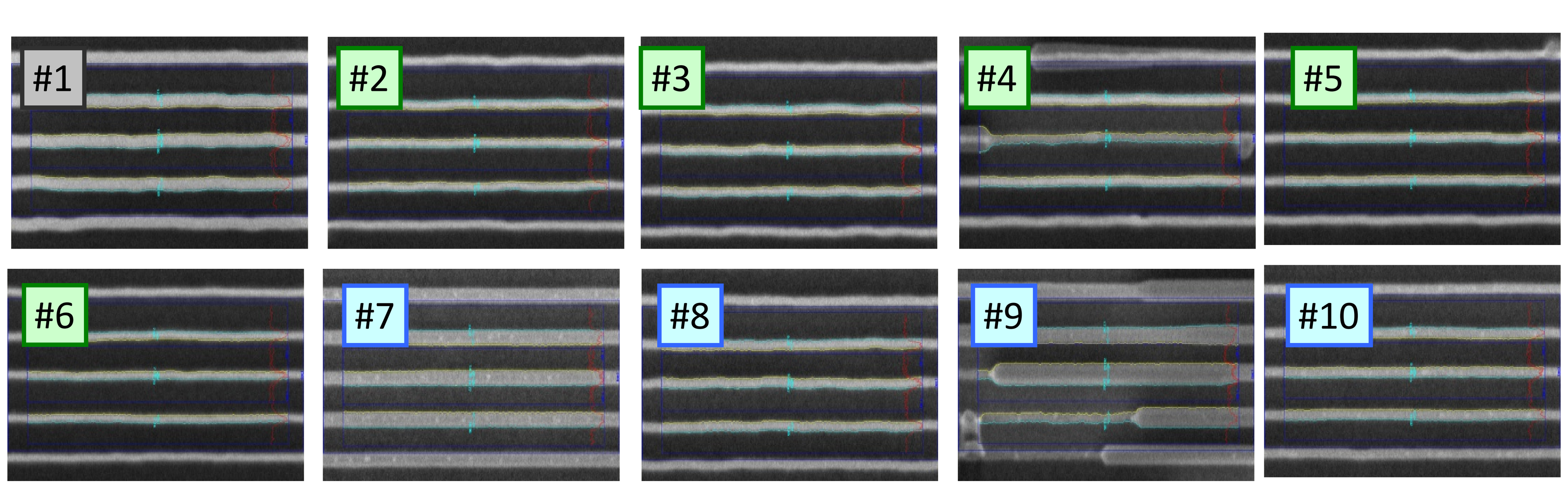

Figure 3. Top-down CD-SEM images on Fins of ten different annealing conditions. From these images the line edge roughness is calculated.

RESULTS

o Fig. 3 shows CD-SEM images from the various process conditions. The figure labeled 1 is the unannealed sample.

- Roughness and line width differences is visually evident.
- LER is obtained by the RMS of the fitted line edge

o Fig. 4 shows a typical 2-fin AFM measurement.

- Sidewall roughness is different from CD-SEM LER in that the sidewall is fitted to a plane, with the residual defining the RMS.

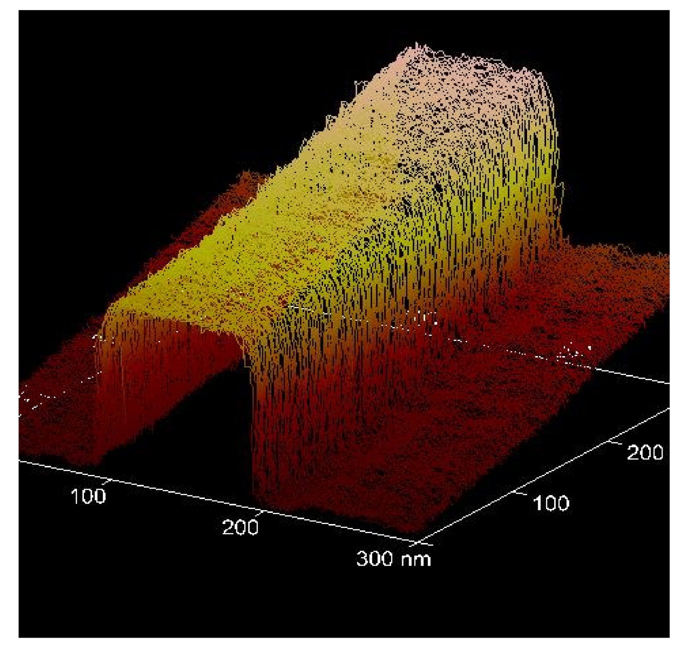

Figure 4. AFM of the 2-fin structure. The tip is too wide to measure between fins, so only the outside sidewall data was used for the roughness calculation.

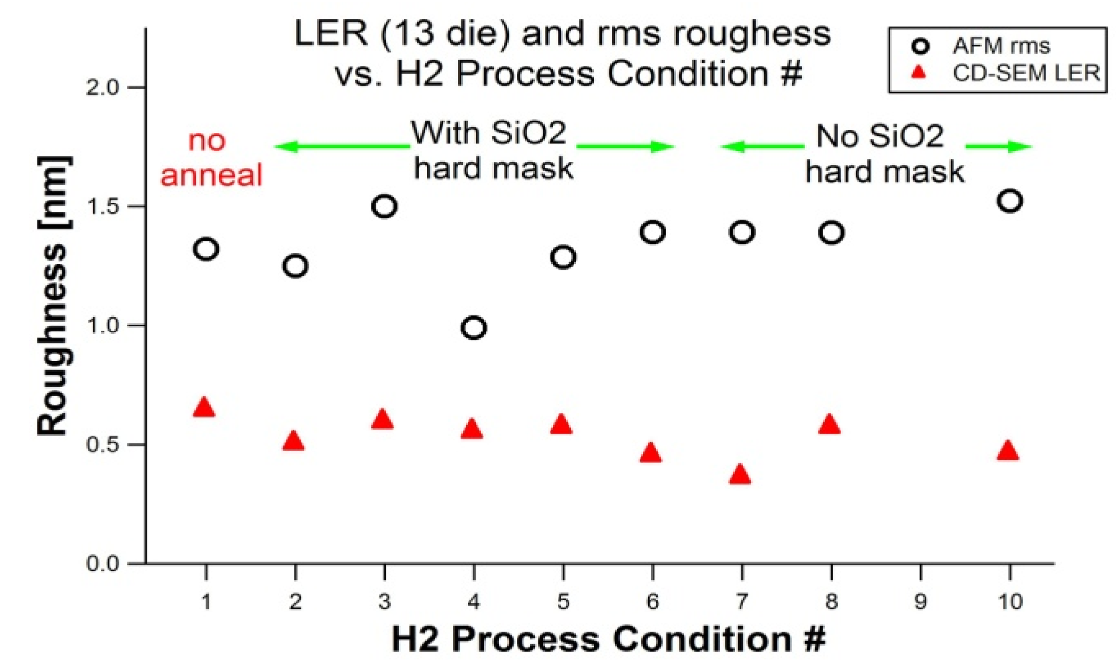

Figure 5. The AFM RMS and CD-SEM LER are not directly comparable, although are expected to provide the same trends.

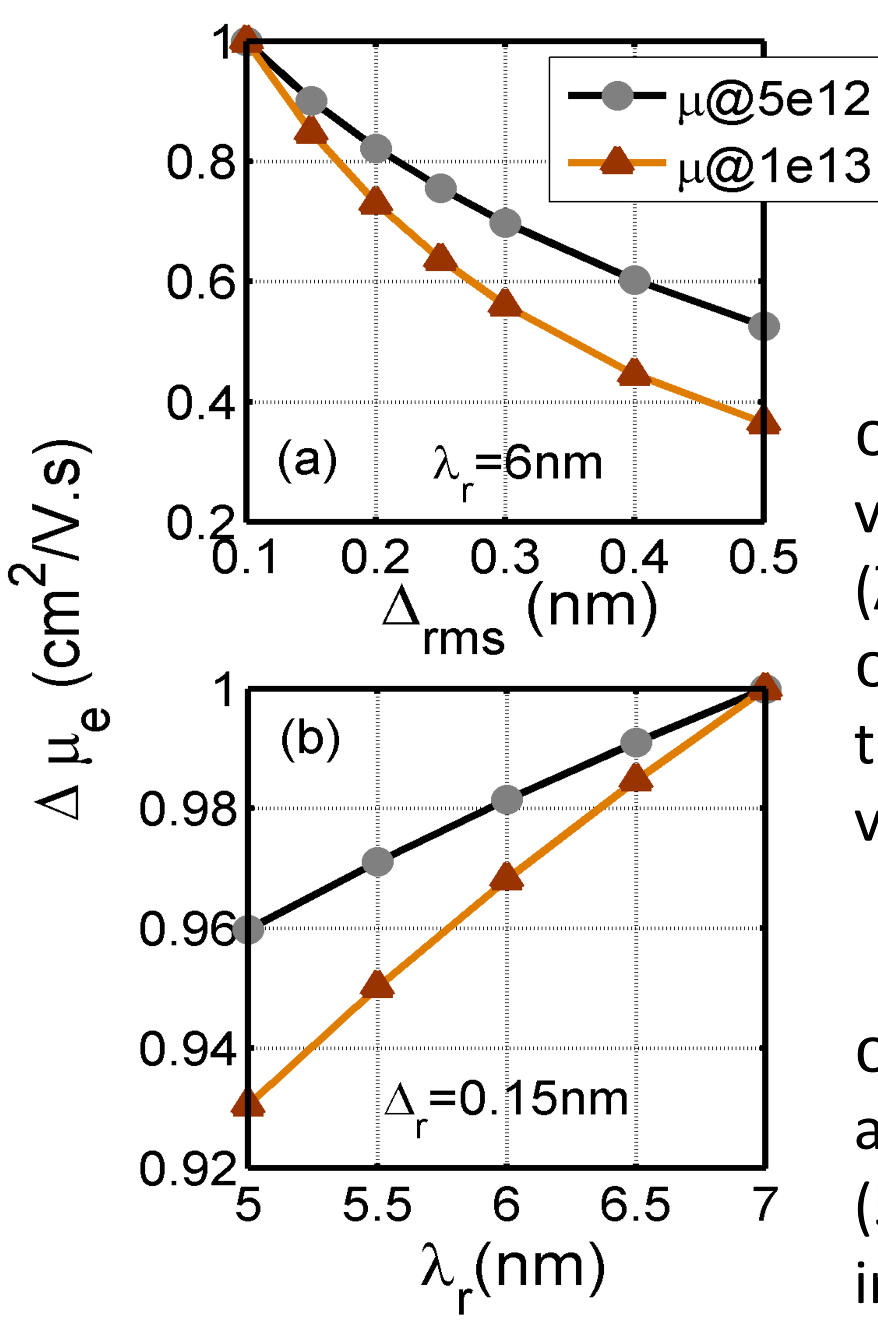

Figure 6. Mobility calculations. (a) Relative electron mobility reduction with increasing Δ_{RMS} for low (5e12/cm2) and high (1e13/cm2) vertical electric field. (b) Relative electron mobility change with increasing λ_r .

o Roughness is described by RMS value (Δ_{RMS}), and correlation length (λ_r) [5].

o The sidewall roughness degrades the carrier mobility(μ) under high vertical electric field.

- Carriers feel the potential fluctuation due to the roughness.

o Figure 6 shows the impact of Δ_{RMS} and λ_r on the electron mobility at low (5e12/cm2) and high (1e13/cm2) inversion charge density.

o **An increase of 0.1 nm in Δ_{RMS} degrades mobility by ~20%.**

o **A reduction in λ_r by 2 nm degrades the mobility by only ~4-6%.**

o **Improvement in surface roughness is essential for improving the electrical transport in next generation finFETs.**

CONCLUSIONS AND SUMMARY

o We report the roughness measurements of fin sidewalls using AFM and the line edge using CD-SEM, and show its effect on mobility

- H2 anneal conditions were used to vary the roughness

o The mobility of finFET devices was calculated with roughness parameters of RMS and correlation length as inputs

- Small variations in roughness, especially RMS, have a large effect on the high field electrical mobility

o The ability to measure variations of 0.05 nm in RMS roughness or LER is critical if it because a requirement to track for process control.

REFERENCES

1. J.-S. Lee, Y.-K. Choi, et al., *IEEE Elec. Dev. Lett.* **24(3)**, 186 (2003).
2. T. Tezuka, N. Hirashita, et al. , *Appl. Phys. Letters* **92**, 191903 (2004).
3. W. Xiong, G. Gebara, et al., *IEEE Elec. Dev. Lett.* **25(8),** 541 (2004).
4. Y-K Choi, et al., EDM 2002, p259 (2002).
5. Goodnick, S. M., Ferry, D. K. et al., Phys. Rev B. 32 (12) 8171-8186, 1985.

ACKNOWLEDGEMENTS

- Adam Ge and Ofer Adan of Applied Materials were influential in analyzing the CD-SEM data. This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.