# Joseph J. Kopanski

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***Positions Held:***

*Currently* – Project Leader, Nanowire Devices, Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD. Lead a group of researchers developing synthesis, fabrication, and metrology techniques for silicon nanowire devices. Recruit, train, and mentor Post-Docs, undergraduate student researchers, contractors, and Foreign Guest Researchers. Prepare written quarterly management reports, annual project reviews and lab tours, and advocate project's research to internal funding sources. Conduct research into the applications of various scanning probe microscopes to nanostructures and microelectronic devices.

2004-2005 Program Analyst, Director's Program Office, National Institute of Standards and Technology, Gaithersburg, MD Facilitated communications between the NIST director's office and NIST laboratory management and the nanotechnology strategic working group.

2003-2004 Project Leader, Electronic Materials Characterization, Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD.

*1995 to 2003* – Project Leader, Scanning Probe Microscope Metrology, Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD

*1985 to 1995* – Member of the Technical Staff, Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD

***Example Project Management Experience:***

*Scanning Probe Microscope Metrology Project* (1995-2002) – Proposed and obtained internal funding to develop practical metrology techniques for using the scanning capacitance microscope to meet the International Technology Roadmap's goal for two-dimensional dopant profiling of the source/drain regions of MOSFETs. Demonstrated 2D dopant profiles of silicon MOSFETs with 10 nm spatial resolution. Led effort to model the SCM using a finite element solution of Poisson's equation and transfer the technology to extract dopant profiles to industrial collaborations by means of a Visual Basic program (FASTC2D). My work on 2D dopant profiling using the SCM has been

presented in invited talks in Japan, Germany, and the USA. Invented and developed intermittent contact mode of SCM (1998). Working with a Post-Doc, we developed my ideas for optical pumping of SCM for lifetime and diffusion length measurements (2003). I wrote the chapter on SCM for the Wiley Encyclopedia of Imaging Science and Technology (2002).

*Resistivity Mapping of Semiconductor Uniformity* (1990-1995) – Developed techniques and software to map semiconductor resistivity with 40 micrometer spatial resolution using an automated probe station and a fabricated array of metal-semiconductor contacts. Developed a new method to automatically measure metal-semiconductor contact resistivity as a function of dopant concentration. Applied the technique to silicon and HgCdTe. As part of an externally funded program, I reviewed test structure applications to II-VI semiconductors, which was later published as an invited paper.

*Oxidation of Silicon Carbide* (1985-1990) – As part of my thesis work, I applied the Deal and Grove linear-parabolic oxidation formalism developed for silicon to cubic silicon carbide and extracted the rate constants. Conducted some of the earliest measurements of interface trap densities, current tunneling, and current-voltage stress to grown and deposited insulators on cubic SiC. I obtained funding from NASA Lewis to continue this work at NIST for two years. I wrote the chapter on Oxidation of Silicon Carbide for the EMIS Datareview of SiC published in 1992. My interest in wide band gap semiconductors continues to today, recently beginning an effort with a Post-Doc to apply scanning probe microscopes to wide bandgap semiconductor characterization and work function measurements.

### ***Recent Leadership Activities and Awards:***

Organized and chaired the 7th International Workshop on the Fabrication, Characterization and Modeling of Ultra Shallow Doping Profiles in Semiconductors (Ultra-Shallow Junctions 2003), Santa Cruz, Ca, April 27-May 1, 2003.

Recruited Post-Docs and student researchers through my representation of NIST at the SEMATECH student relations TAB and through the NIST SURF (summer undergraduate research fellowship) program.

2002 Bronze Metal Award for superior federal service: For outstanding contributions in improving teamwork, communications, and cooperation within the EEEL Semiconductor Electronics Division.

2000 Bronze Metal Award for superior federal service: For accelerating development of scanning capacitance microscopy to become the practical instrument of choice for semiconductor 2-D dopant profiling.

## *Education and Skills*

Masters of Science in Electrical Engineering and Applied Physics, Case Western Reserve University, Cleveland, OH May 1985. Thesis: "Development of fabrication technologies for Silicon Carbide MOSFETs"

Bachelor of Science in Applied Physics, Case Western Reserve University, Cleveland, OH, May 1982. Senior Project: "Design and fabrication of a gate array for digital and analog applications"

Proficient with Windows-based personal computers, including Microsoft Office, and Visual Basic, RoboHelp, and Install Shield applications.

Electrical Characterization of Semiconductors: C-V and I-V characterization of MOS capacitors and transistors, Interface trap density measurement techniques, Spreading resistance, four-point probe, metal-semiconductor contact resistance and work function measurements, DLTS. Ten years experience using scanning probe microscopes (AFM, SCM, and EFM) to characterize semiconductors.

Semiconductor Processing: Practical experience with complete CMOS fabrication process steps; including photolithography, diffusion, oxidation, ion implantation, thermal and e-beam evaporation, rf sputtering, and RIE. Develop fabrication processes for unique test chips for model verification. Designed and setup Semiconductor Electronic Division's mechanical cross-section sample preparation laboratory.