MATERIAL ISSUES AND IMPACT ON RELIABILITY OF Cu/LOW k INTERCONNECTS

Paul S. Ho
Microelectronics Research Center
The University of Texas at Austin

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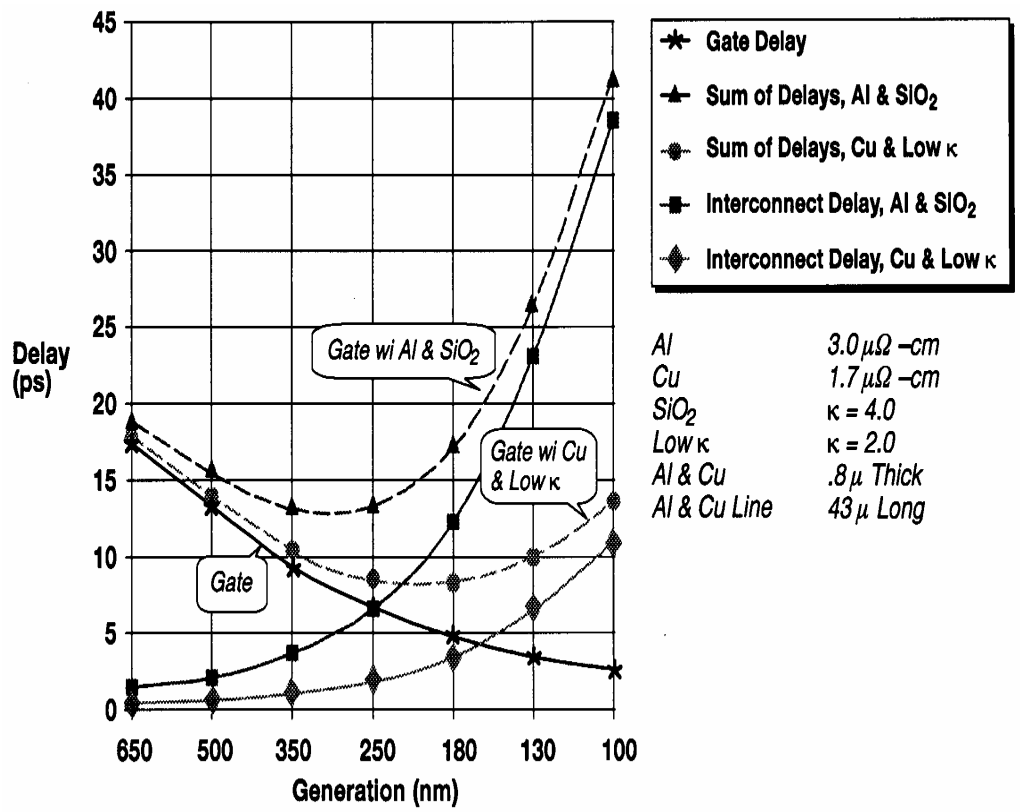
- Technology challenges for low k dielectrics
- Chemical bond and polarizability
- Impact of low k dielectrics on reliability of Cu interconnects
    - Dielectric confinement effects
    - Electromigration characteristics
- Summary

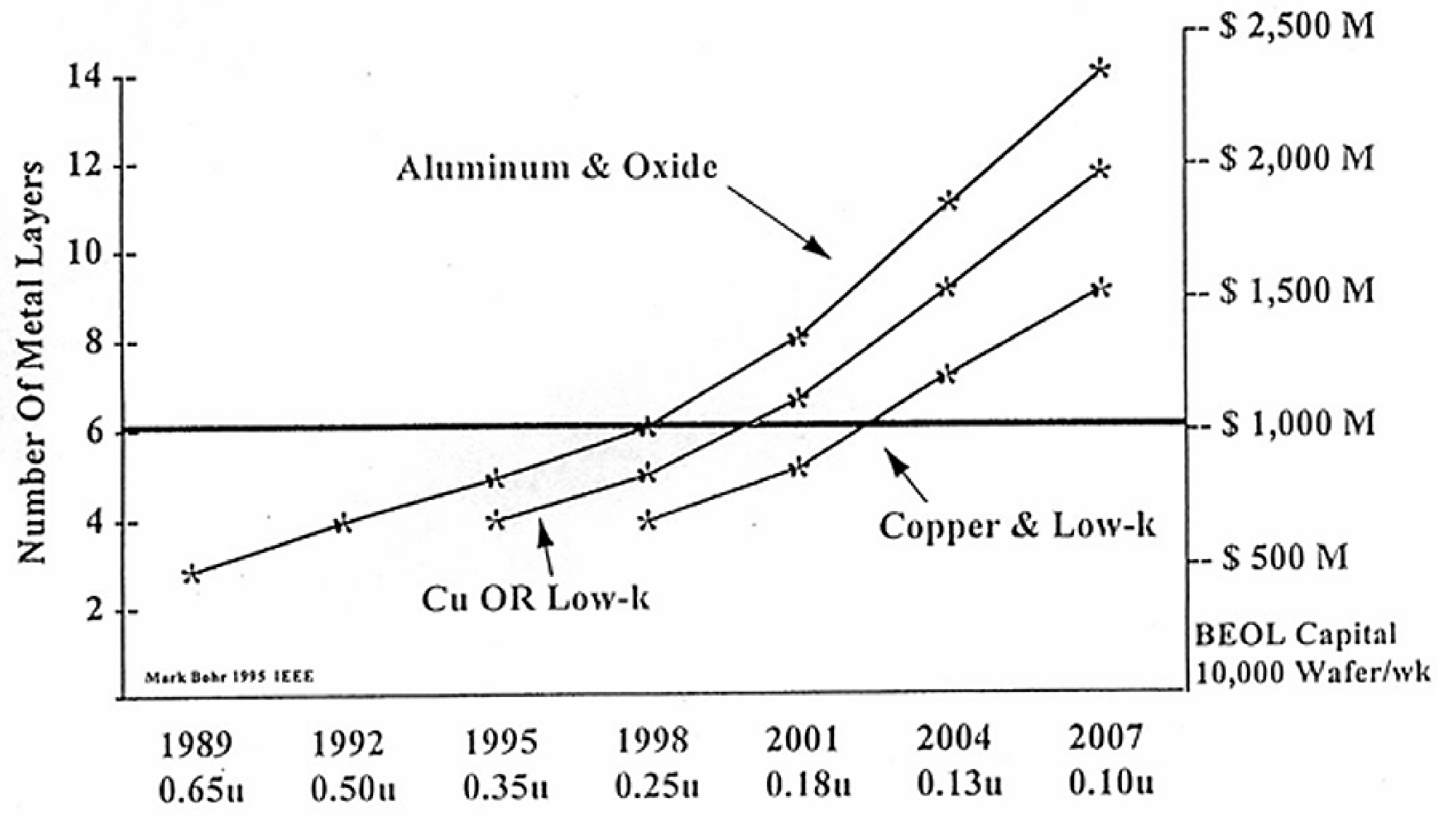
Effect of Scaling on Gate and Interconnect Delays

- Interconnect delay dominates IC speed
- Implementation of low k dielectrics reduces
  - RC delay
  - Power dissipation
  - Crosstalk noise
  - Number of metal level



Mark Bohr, IEEE IEDM Proc. 1995

Cost and Manufacturability Issue



Sematech 1998

The University of Texas at Austin

Table 1: Technology Trends and the Need for Low-Dielectric Constant Materials

Year	1995	1998	2001	2004	2007
Feature Size (μm)	0.35	0.25	0.18	0.13	0.10
Metal Levels	4 - 5	5	5 - 6	6 - 7	7 - 8
Device Frequency (MHz)	200	350	500	750	1,000
Interconnect Length (m/chip)	380	840	2,100	4,100	6,300
Capacitance (fF/mm)	0.17	0.19	0.21	0.24	0.27
Resistance (metal1)(ohm/μm)	0.15	0.19	0.29	0.82	1.34
Dielectric Constant (*k*)	4.0	2.9	2.3	<2	2 - 1

- Based on the National Technology Roadmap for Semiconductors, 1994

Interconnect Technology Requirements for MPU

Year of introduction “Technology Node”	1999 180nm	2000	2001	2002 130nm	2003	2004	2005 100nm
MPU ½ pitch	230	210	180	160	145	130	115
Minimum metal effective resistivity (μΩ-cm) Al wiring*	3.3	3.3	3.3	3.3	3.3		
Minimum metal effective resistivity (μΩ-cm) Cu wiring*	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (conformal) (nm)	17	16	14	13	12	**11**	**10**
Interlevel metal insulator- effective dielectric constant (κ)	3.5-4.0	3.5-4.0	2.7-3.5	**2.7-3.5**	**2.2-2.7**	**2.2-2.7**	**1.6-2.2**

Solutions Exist ☐
Solutions Being Pursued 🟩
No Known Solutions 🟥

International Technology Roadmap for Semiconductors, 1999

Interconnects Technology Requirements for MPU

Year of introduction “Technology Node”	2001 130nm	2002	2003	2004 130nm	2005	2006	2007 65nm
MPU ½ pitch	150	130	107	90	80	70	65
Minimum metal effective resistivity (μΩ-cm) Al wiring*	3.3	3.3					
Minimum metal effective resistivity (μΩ-cm) Cu wiring*	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (conformal) (nm)	16	14	12	🟩	🟩	🟩	🟥
Interlevel metal insulator- effective dielectric constant (κ)	3.0-3.6	3.0-3.6	3.0-3.6	🟩	🟩	🟩	🟥

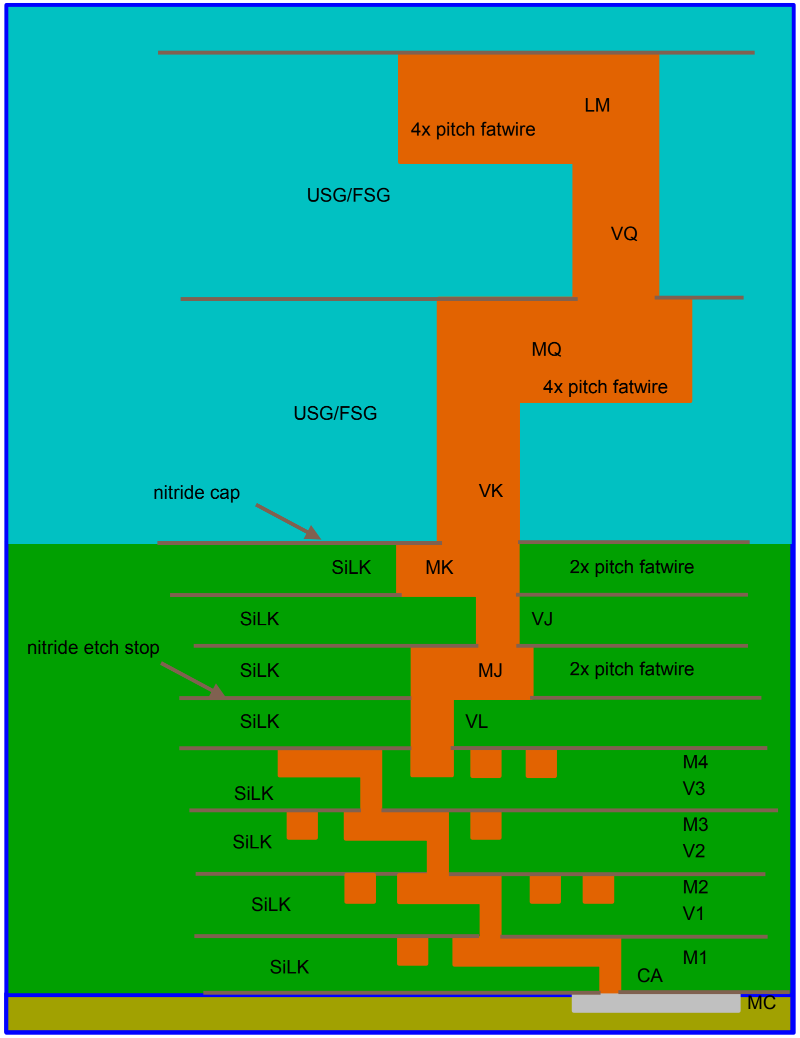
Solutions Exist ⬜
Manufacturing Solutions known 🟩
No Known Solutions 🟥

International Technology Roadmap for Semiconductors, 2001

IBM CMOS9S0 Technology

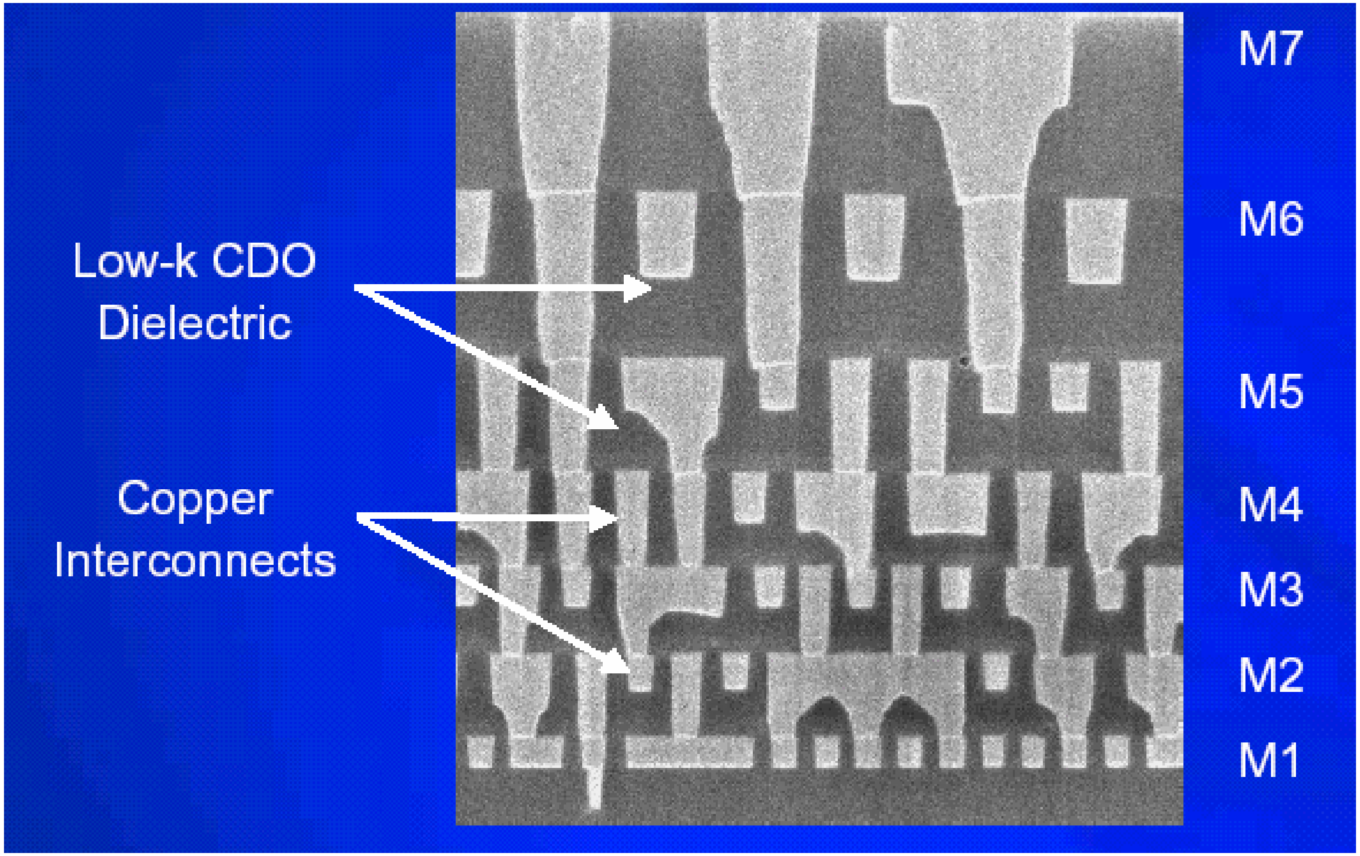
9S BEOL Stack
8 Level Metal
(4@1x, 2@2x, 2@4x)

	0.13 µm	**0.18 µm**
MDR shrink	0.25x	0.35x
Supply Voltage	1.2V	1.5V
Gate Length (drawn)	0.125 µm	0.175 µm
M1 pitch	0.35 µm	0.49 µm
M2 pitch	0.40 µm	0.63 µm
Mx pitch	0.45 µm	0.63 µm
2x pitch FW	0.90 µm	1.26 µm
4x pitch FW	1.80 µm	NA
Metal Levels	8	7
ILD	SiLK	USG/FSG
K_{eff}	3.0	4.0



R. Goldblatt et al., IITC 2000

Intel 90nm Interconnect Technology



7 metal levels on 300mm wafer
Low k CDO, Capacitance improved by 18%
M. Bohr, Intel Developer Forum 9/2002

Contributions to Dielectric Constant

$$\varepsilon = 1 + 4\pi \mathbf{P/E}$$

- Electronic polarizability

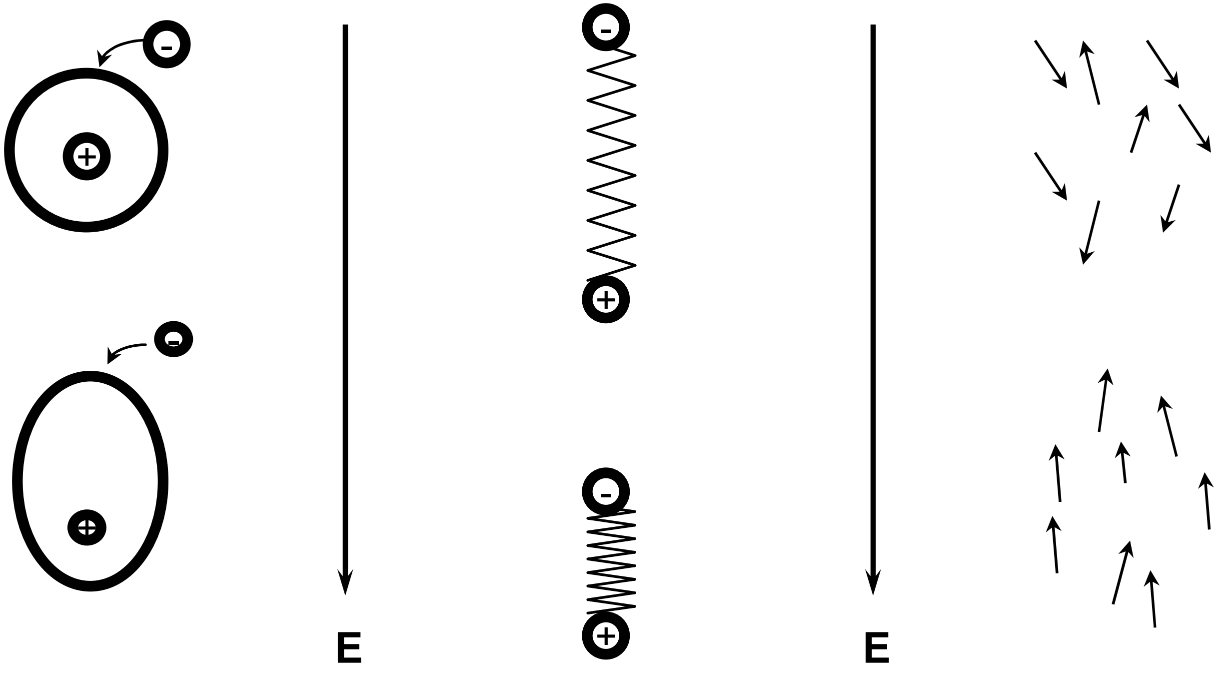
  optical frequency ($10^{14\text{-}15}$ S^{-1})
- Vibrational (atomic)

  IR ($10^{12\text{-}13}$ S^{-1})
- Rotational (orientation of permanent dipoles)

  microwave (10^{9} S^{-1})

Microscopic Origins of Polarization

3 Sources of Polarization



Electronic
(Induced)
Visible -UV

Atomic
(Induced)
Infrared

Orientational
(Permanent)
μw - infrared

K. Taylor, IRPS Tutorial 2000

Basic Approaches to Reduce Dielectric Constant

- Optimization of molecular structure
  - Minimize configurational and dipole polarizability, e.g. use of C-C and C-F bonds
- Reduce density and incorporation of porosity
  - Add uniform and microscopic pores with k of 1
- Limitation: both approaches degrade the thermomechanical properties
  - Proper tradeoff of dielectric constant and thermomechanical properties important

Electronic Polarizability vs. Strength of Chemical Bonds

Bond	*Polarizability* (angstrom^3)*	*Ave. Bond Energy# (Kcal/mole)*
C-C	0.531	83
C-F	0.555	116
C-O	0.584	84
C-H	0.652	99
O-H	0.706	102
C=O	1.020	176
C=C	1.643	146
C≡C	2.036	200
C≡N	2.239	213

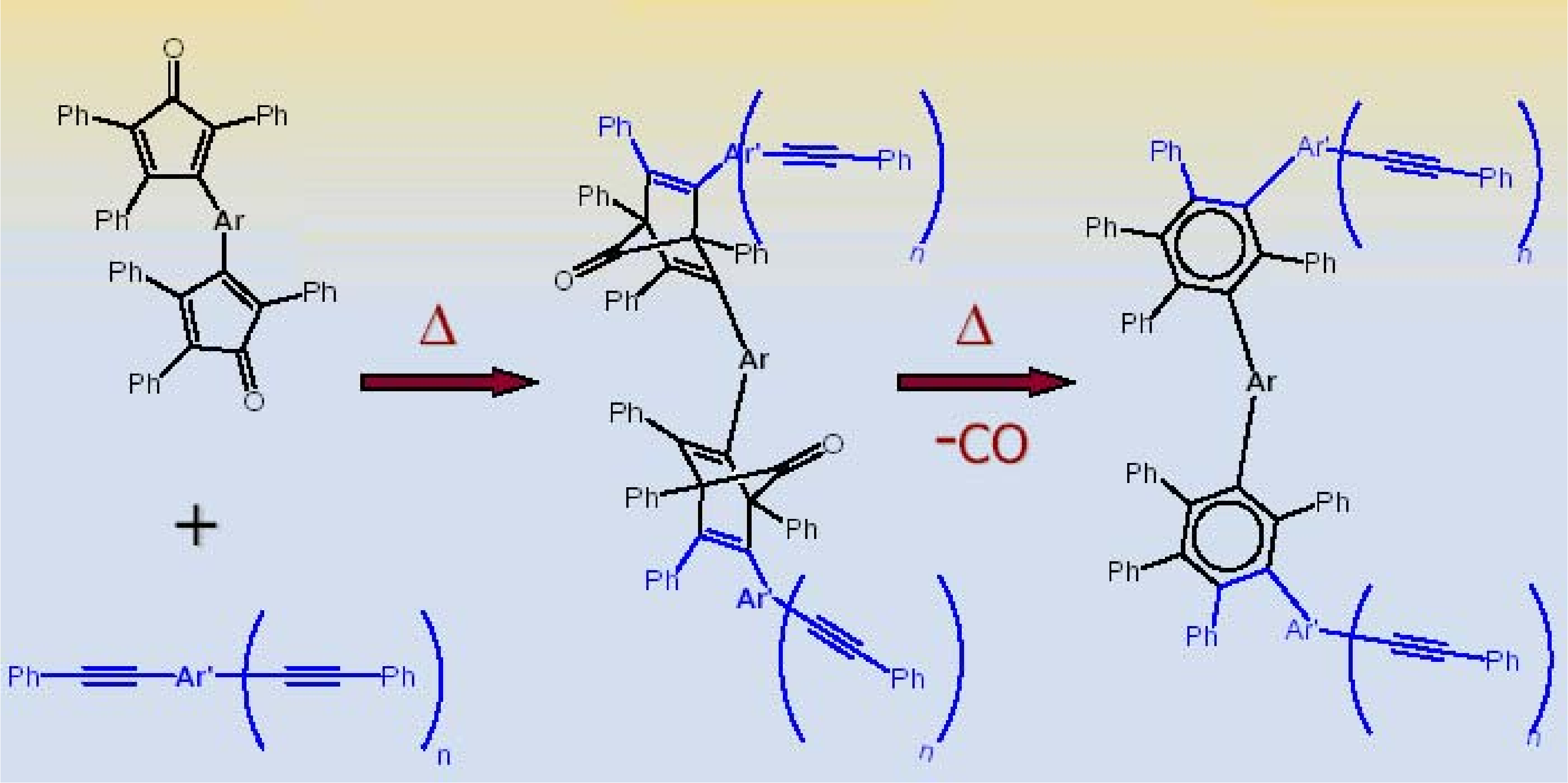
* J. Am. Chem. Soc. 1990, 112, p.8533.
# S. Pine, Organic Chemistry 5th ed.(1987).

Recent Low k Dielectric Materials

Material	Type	Manufact.	k
SiLk	Organic themoset	Dow Chemical	2.65
FLARE 2.0	Poly aryl ether	Allied Signal	2.8-2.9
Black Diam. Corel	MSQ type CVD	Applied Mat. Novellus	2.7
P SiLK Orion LKD 5109 XPX	Porous spin on material	Dow Trikon JSR Asahi	2.0-2.3

Molecular Structure of SiLK

(S.J. Martin et al. Adv. Mat. 12, 1769, 2000)



Formation of polyphenylene polymer structure

H. C. Silvis, Am. Chem. Soc., Boston, 2002

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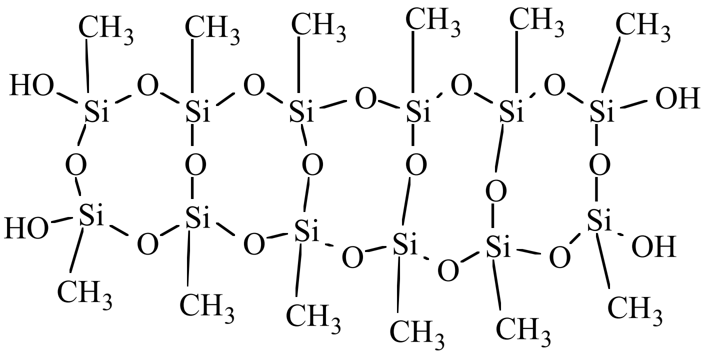
Crosslinked Silica-Based Materials

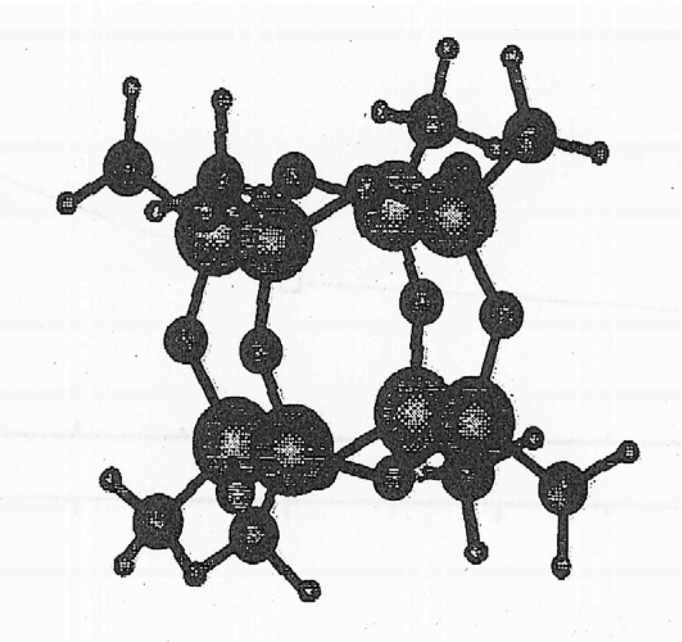
- Si-O network provides rigidity
- Organic groups lower k to 2.5-3.3

silsesquioxane $RSiO_{1.5}$

HSQ
k = 2.9-3.0

MSQ
k = 2.7-2.8





Dielectric and Thermomechanical Properties of Low k Films

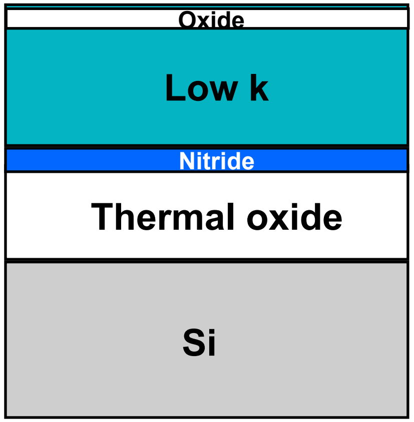
Material	k	Young's Modulus (GPa)	Lateral TEC 25-225 °C (ppm/°C)	Tg (°C)	TGA % weight loss (425 °C, 8 hrs.)
PTFE	1.92	0.5	135	250	0.6
BPDA-PDA	3.12	8.3	3.8	360	0.4
crosslinked PAE	2.8-3.0	2.7	52	350	2.5
Fluorinated PAE	2.64	1.9	52	>400	x
BCB	2.65	2.2	62	-	30
SiLK	2.65	2.3	54	-	2.1
Parylene-N	2.58	2.9	55-100+	425 (melt)	30
Parylene-F	2.18	4.9	33	-	0.8
HSQ	2.8-3.0	7.1*	20.5	-	x

* Biaxial modulus
x Not measured
\- None observed

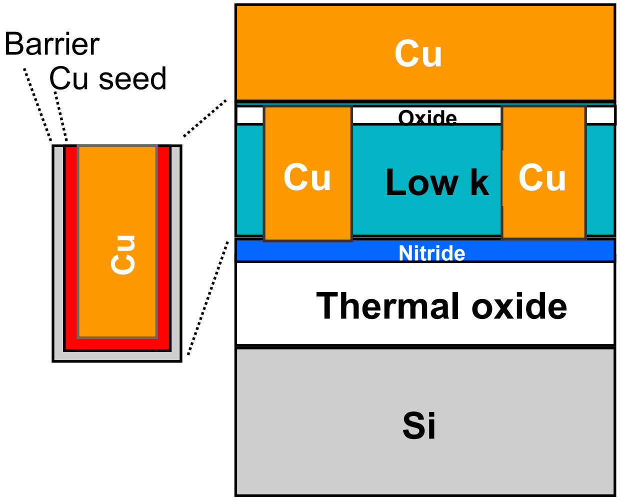
M. Kiene et al., Handbook of Si Semicond. Metrology, Marcel Dekker Inc. 2001

Integration of Cu Damascene Structure

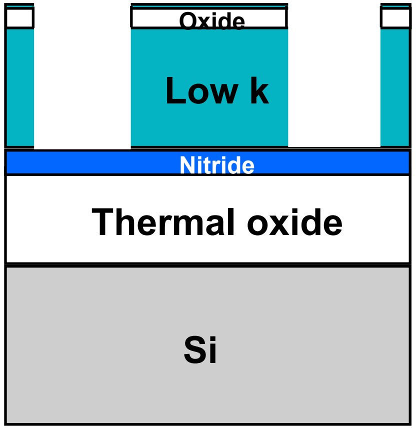
1. **Deposit Low κ**
2. **Deposit Cap (350 - 400°C)**



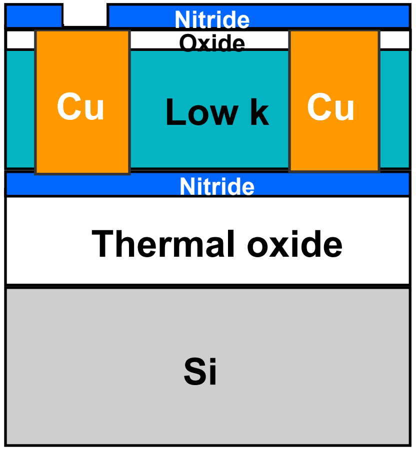
4. **Deposit barrier (< 200°C)**
5. **Deposit Cu seed (< 200°C)**
6. **Electroplated Cu fills trench**
7. **Cu anneal (250 - 350°C)**



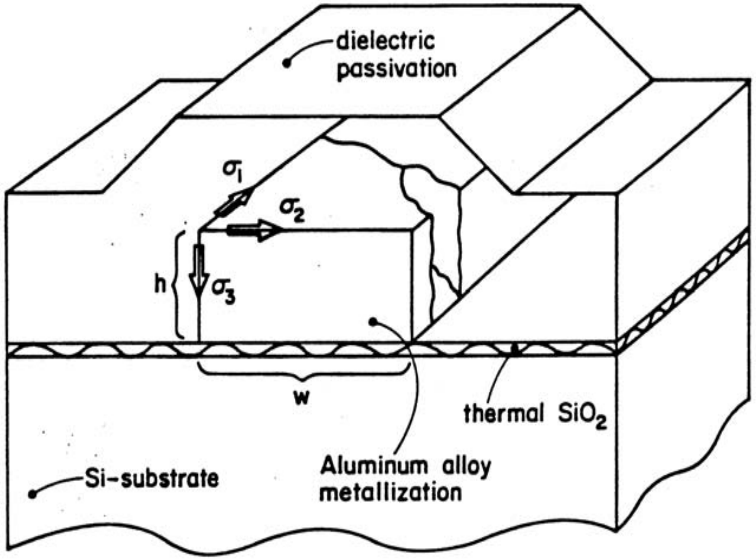
3. **Pattern and etch Low κ**



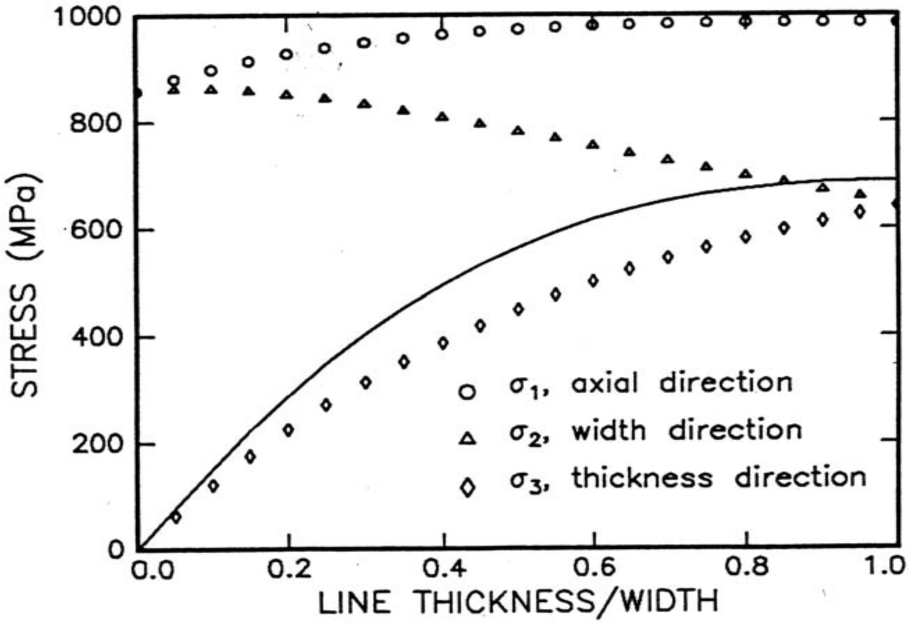
8. **CMP Cu**
9. **Deposit cap (350 - 400°C)**



EFFECT OF QUARTZ CONFINEMENT ON THERMAL STRESS OF AL LINE STRUCTURES

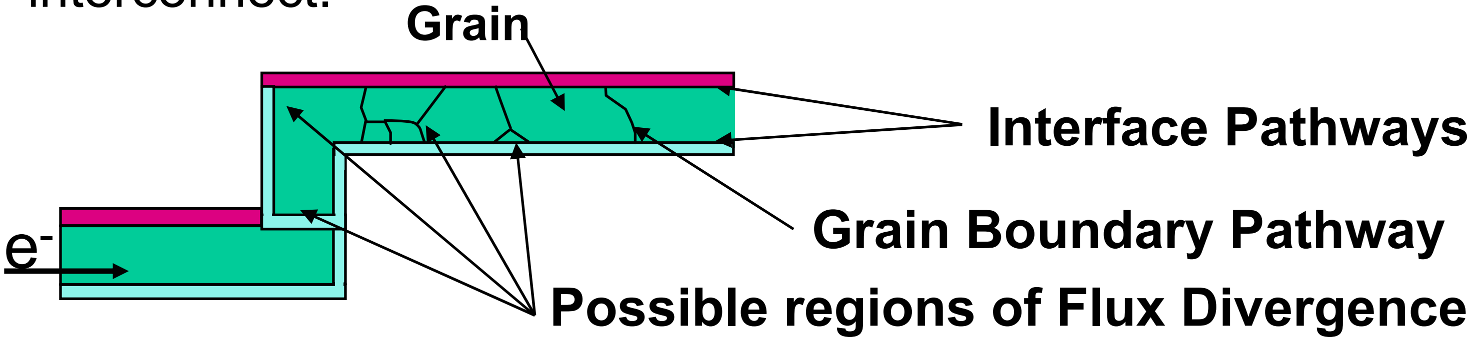


ESHELBY'S MODEL OF ELASTIC INCLUSIONS
M. Korhonen et al., MRS Bulletin, 1992)



EM Damage Formation in Damascene Structure

Damage formation due to flux divergence in dual-damascene interconnect.

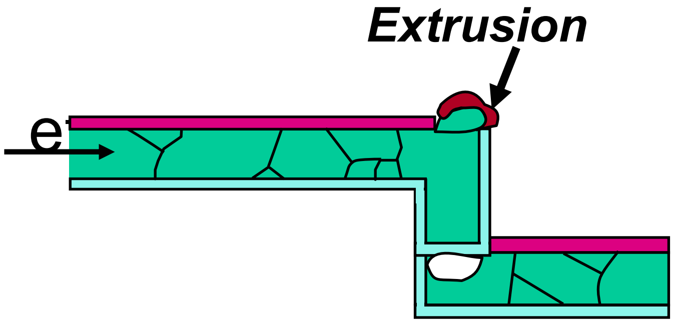


Grain

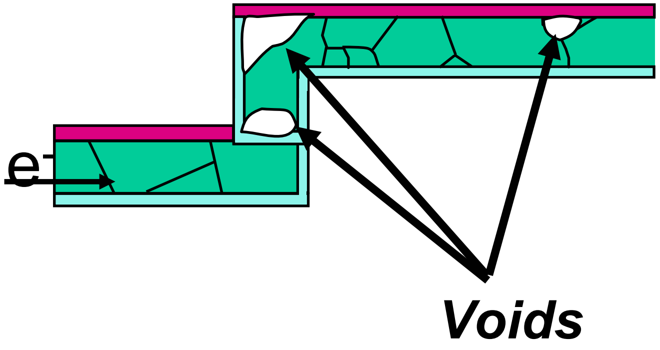
Interface Pathways

Grain Boundary Pathway

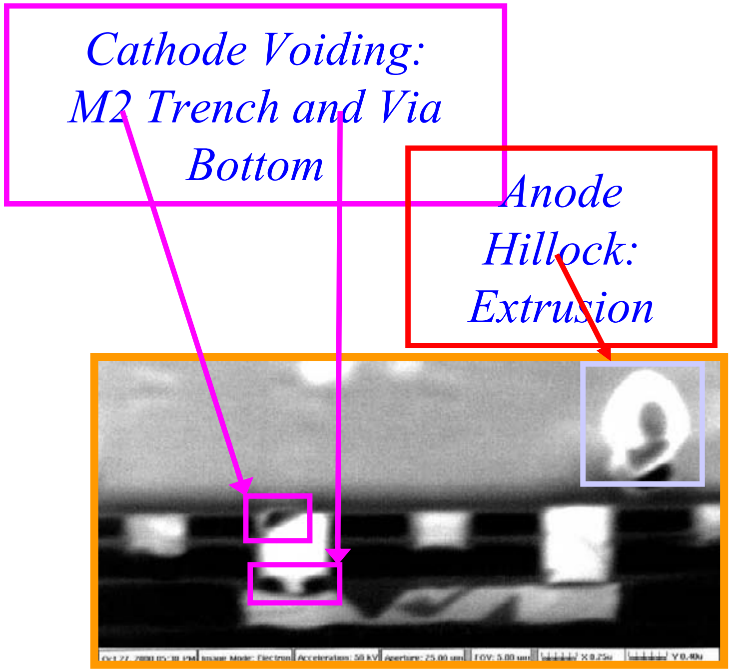
Possible regions of Flux Divergence



Extrusion



Voids



Cathode Voiding: M2 Trench and Via Bottom

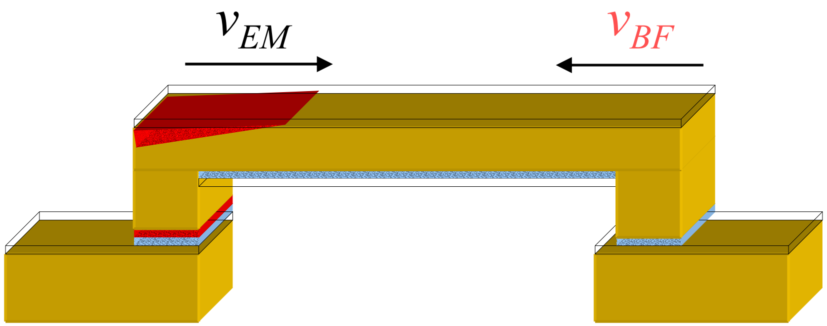
Anode Hillock: Extrusion

E. T. Ogawa et al., *2001 IEEE Int. Reliability Physics Symposium Proc.* 2001, pp. 341-349.

Blech effect and jL_c threshold product

The average drift of metal ions under EM is balanced by a back flow stress as:

$$v_d = v_{EM} + v_{BF} = \mu\,(Z^* e\rho j - \Omega\Delta\sigma/L)$$

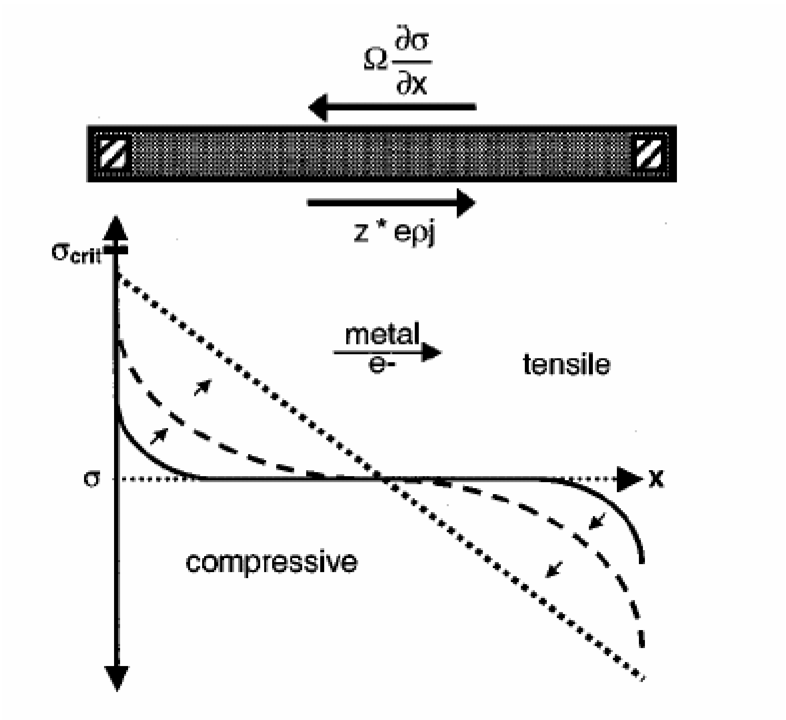


There is a threshold or critical product jL_c, when $v_d = 0$,

$$jL_c = \Omega\Delta\sigma/ Z^* e\rho \propto \Delta\sigma$$

$\Delta\sigma$ changes the net drift rate, hence the EM lifetime. It depends on the dielectric confinement and $(jL)_c$ provides a measure for $\Delta\sigma$

Stress evolution in confined metal lines under EM



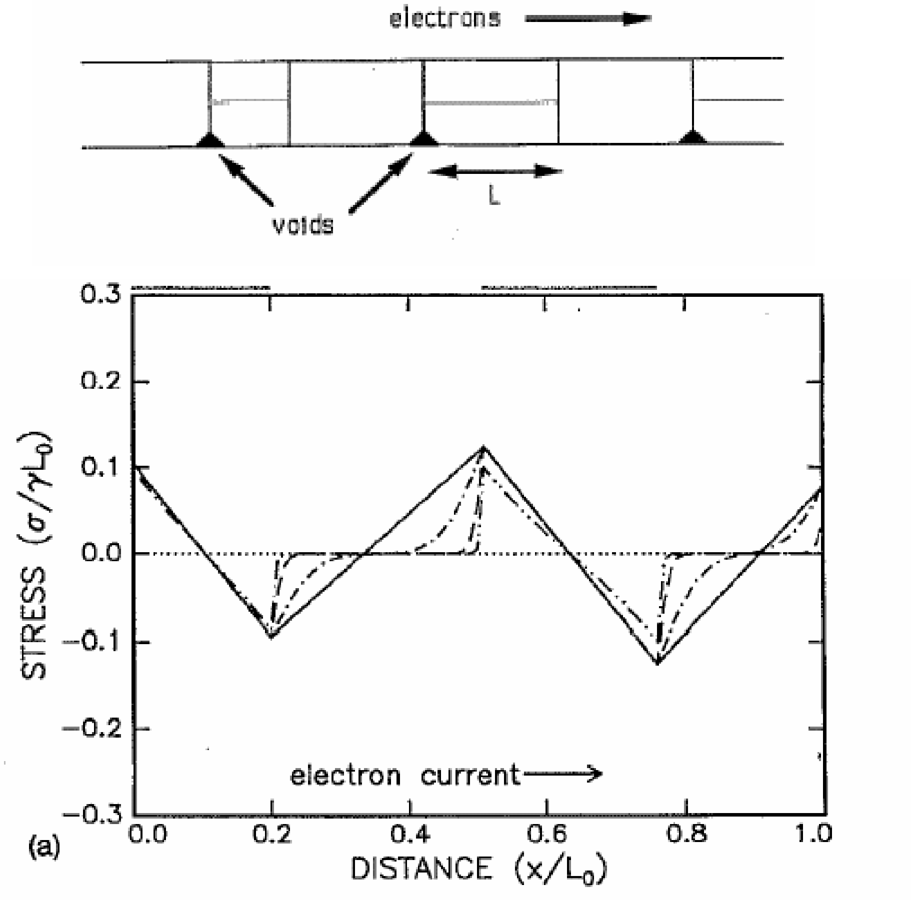
No void formation

No metal extrusion

Applicable to AlCu

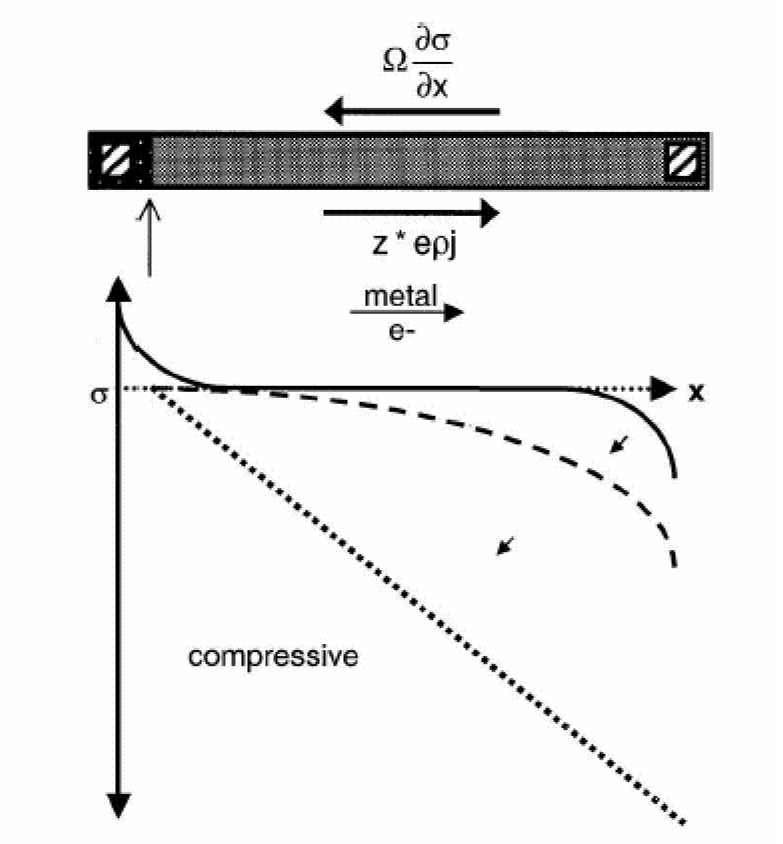
M.A. Korhonen et al., JAP **73,** 3790, 1993

S. Hau-Riege JAP **91**, 2014, 2002



Stress generation in lines with clusters of blocking grains

Stress evolution in confined metal lines under EM



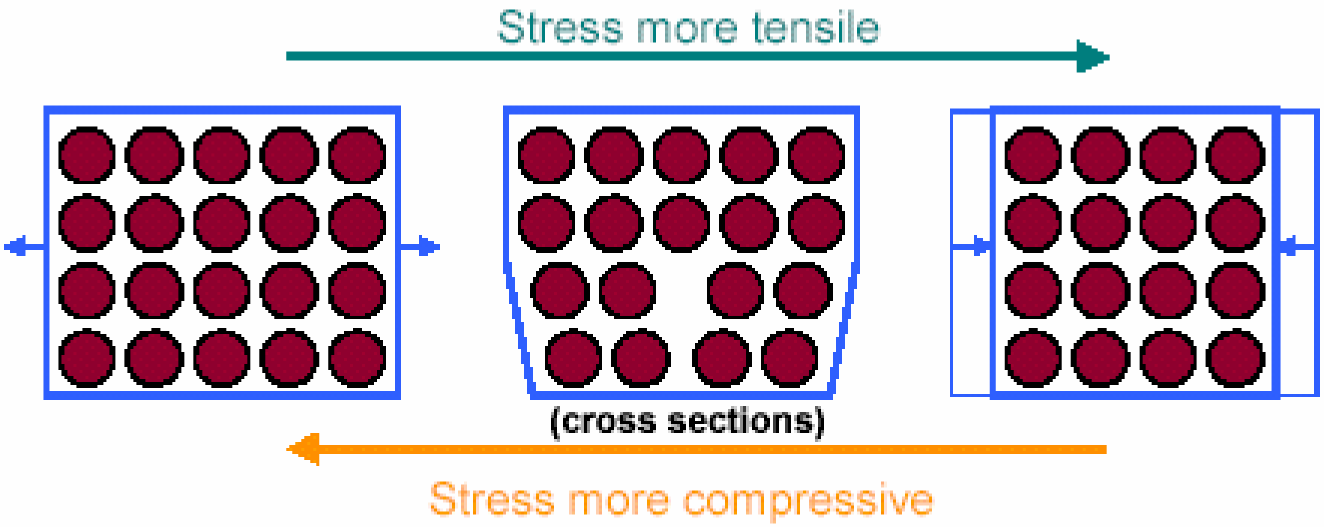
With void formation, local stress relaxation leads to a compressive stress state.

Voids can form under a low tensile stress, the case is applicable to Cu.

With mass transport dominated by interfacial diffusion, microstructure effect is reduced but σ_{max} depends on interfacial adhesion

M.A. Korhonen et al., JAP **73,** 3790, 1993
S. Hau-Riege JAP **91**, 2014, 2002

Effective Modulus for Interconnects under EM



Stress more tensile

(cross sections)

Stress more compressive

- **Restoring force from surrounding dielectric determines hydrostatic stress**

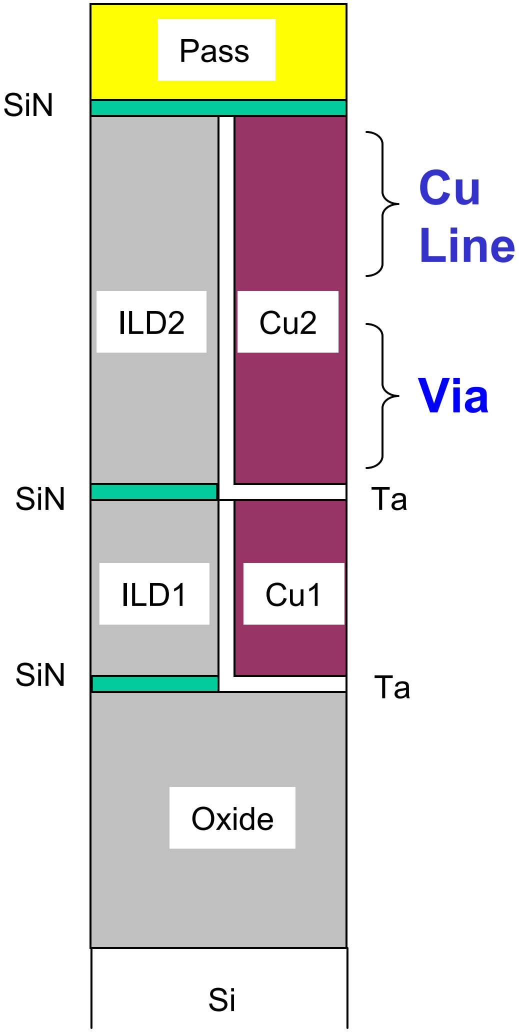
$$\boxed{\frac{dC}{C} = -\frac{d\sigma}{B}}$$

(Korhonen 93)

B is a function of dielectric, geometry, and metallization.

M.A. Korhonen et al., JAP **73,** 3790, 1993; S. Hau-Riege, UC Berkeley Short Course 2002

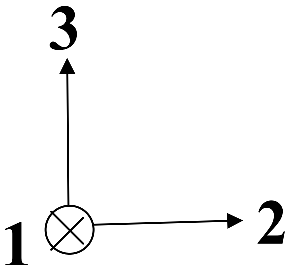
Finite element analysis of effective modulus B



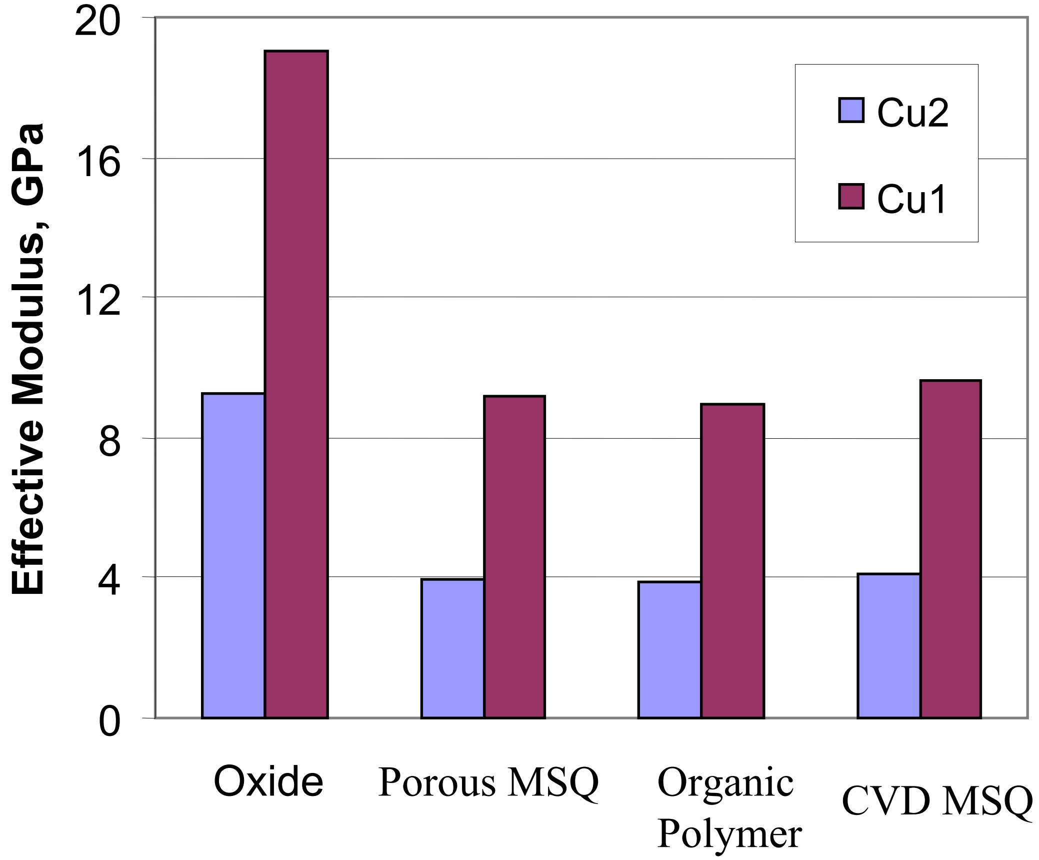
For Cu interconnects, $\varepsilon_1 = \varepsilon_2 = 0$ but $\varepsilon_3 \neq 0$ to account for mass transport via interfacial diffusion

Modeling :

- 3 Dimensional
- **1 MA/cm^2**
- Test at 325°C
- ILD
  - SiO$_2$
  - Organic Polymer
  - CVD MSQ
  - Porous MSQ



Effective Modulus of Cu Dual Damascene Interconnects



Reduced Effective Modulus on M2

B: $\varepsilon_1 = \varepsilon_2 = 0$, only $\varepsilon_3 \neq 0$

Void formation in Cu interconnect

Void can be nucleated at interface with a relatively low stress[1]

Maximum void volume at steady state [2]

$$V_{\max} = \frac{\sigma^T L}{B} + \frac{J\rho e Z^* L^2}{2\Omega B}$$

$$V_{\max} \propto 1/B$$

Void volume depends not only on j but also on σ^T, thermal stress.

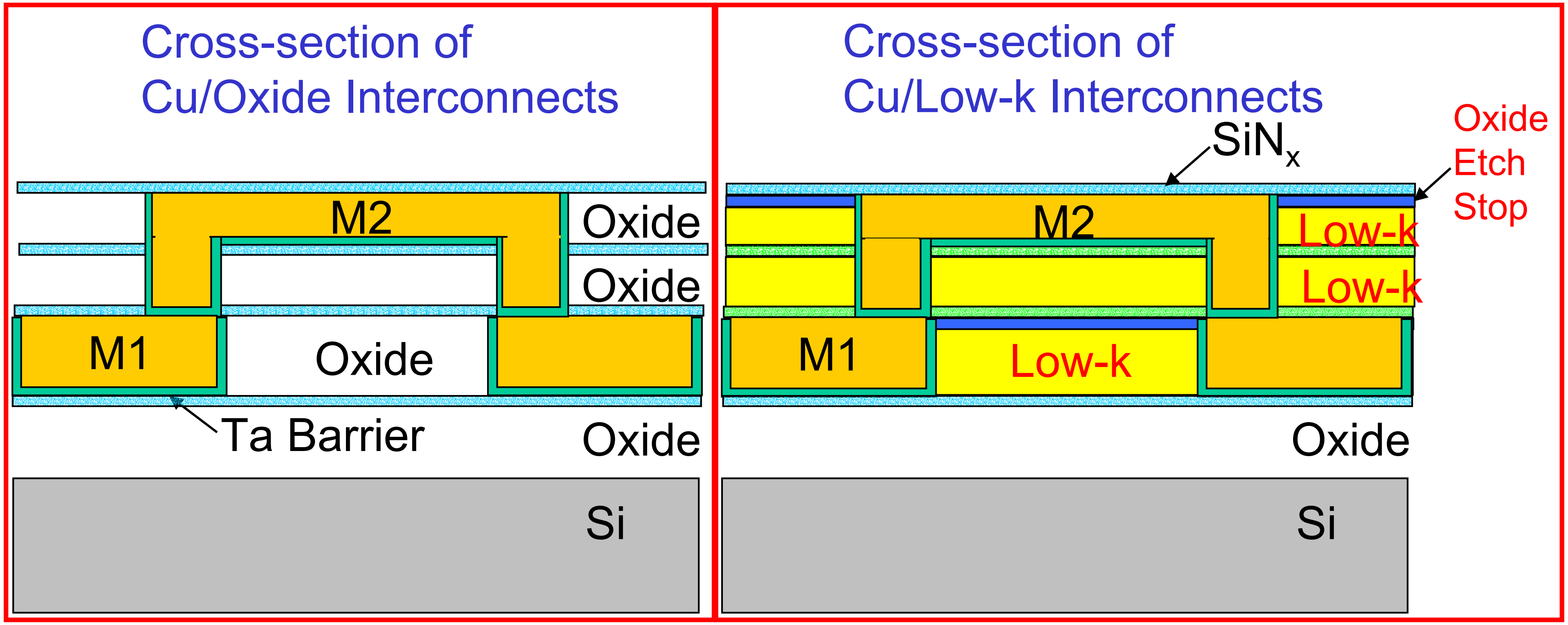
If line failure by the same void volume, EM lifetime will be proportional to B under similar test conditions.

But lifetime will be reduced if interfacial delaminates before reaching the steady state $V_{\max}$.

1. S. Hau-Riege JAP **91**, 2014, 2002.
2. M.A. Korhonen et al., JAP **73,** 3790, 1993

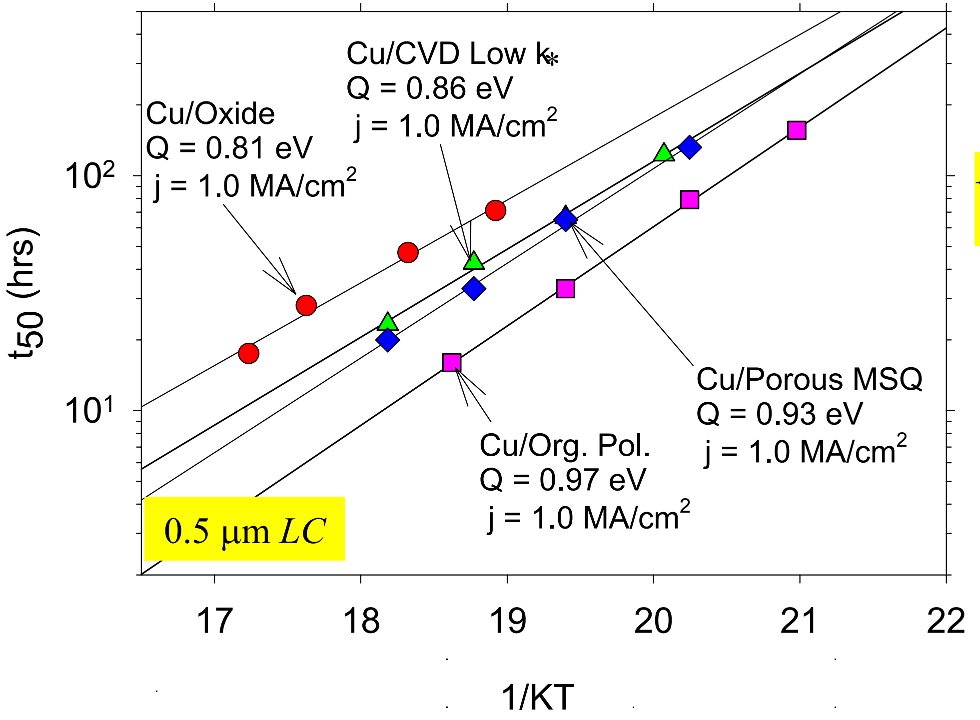
EM Cu/low k test structure

- Low-k dielectric materials are implemented in all levels
- Oxide etch stop layer is deposited on low-k material.
- The low k ILD and CMP etch stop layer introduce new interfaces in Cu/low k interconnects.



EM Lifetime Characteristics

The EM lifetime of Cu/low k interconnects is shorter than Cu/oxide. This can be attributed to the thermomechanical properties of low k ILDs.



Drift velocity for a confined structure:

$$v_d = v_{EM} + v_{BF} = \mu\,(Z^* e\rho j - \Omega\Delta\sigma/L)\ ^{**}$$

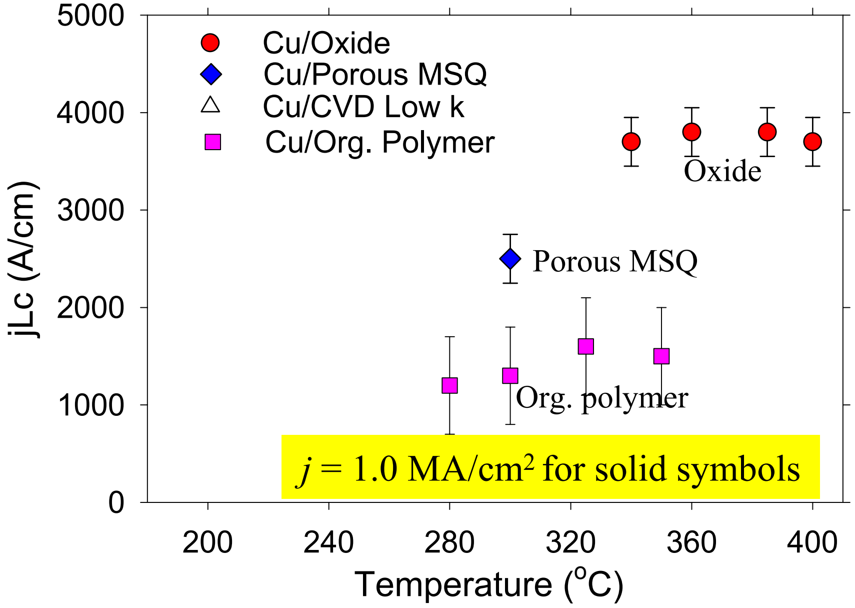
Decrease in $\Delta\sigma/L$ due to less confinement increases v_d and reduces EM lifetime.

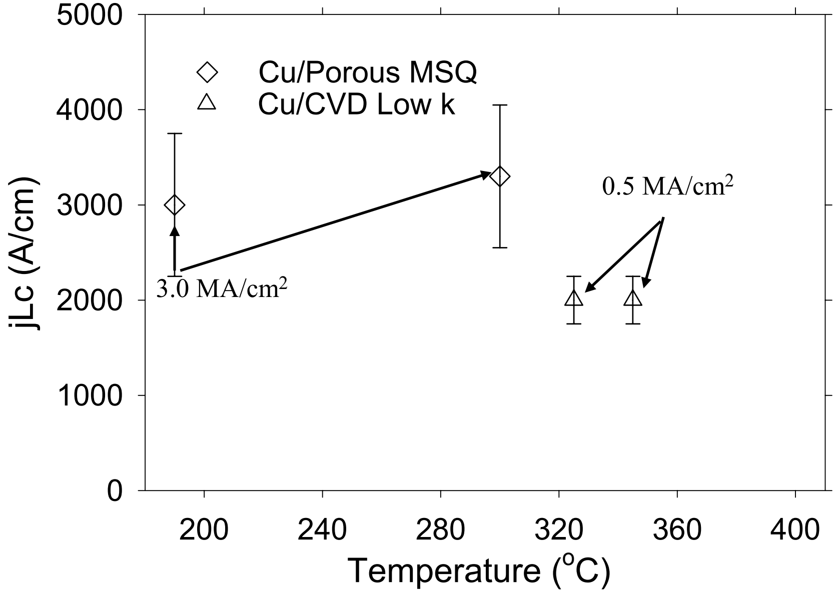
** *I. A. Blech, JAP **47**, 1203 (1976)*

	Org. Pol.	Por. MSQ	CVD Low k	Oxide
Modulus (GPa)	2.5	3.6	6	71.4
B (GPa)	7.2	7.3	7.6	13.7

$t_{50} \propto B$

jL_c for Cu Interconnects





	Org. Pol.	Por. MSQ	CVD Low k	Oxide
Modulus (GPa)	2.5	3.6	6	71.4
B (GPa)	7.2	7.3	7.6	13.7

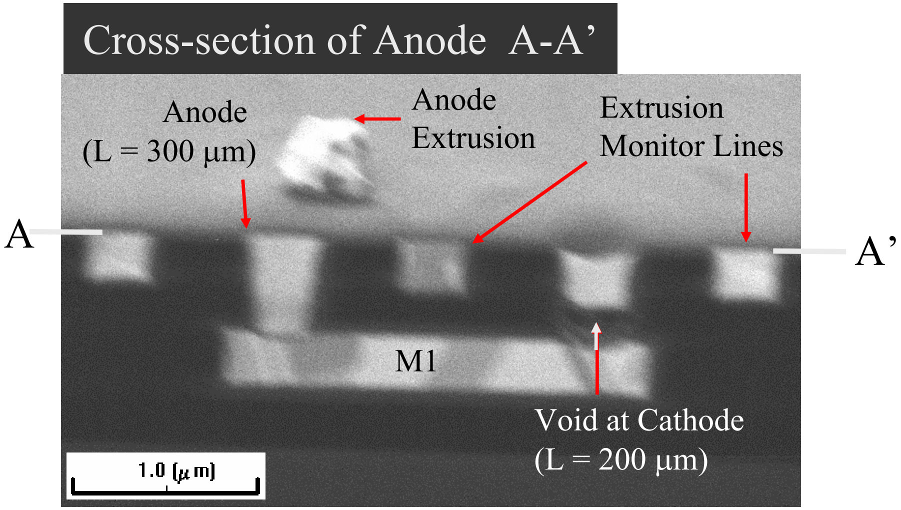
$$jL_c \propto \Delta\sigma \propto B$$

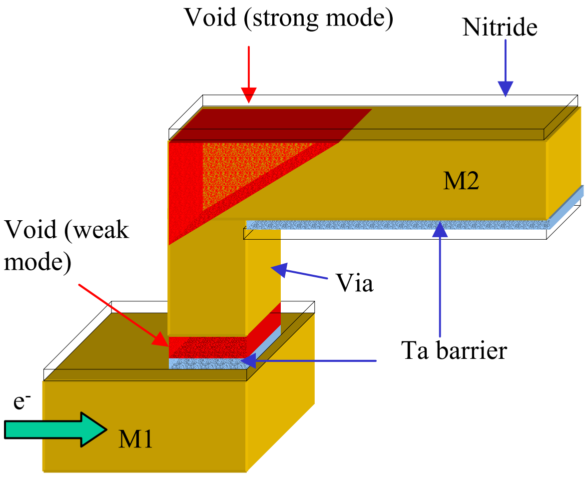
Temperature dependence of jL_c was not observed.

jL_c values of organic polymer are below that estimated from B due to interfacial delamination.

EM Failure Analysis in Cu/Oxide Structure

- At the anode end, extrusion occurs through the SiNx cap layer due to EM induced Cu mass transport . (Anode Extrusion)
- After extrusion, back stress in the line will decrease to enhance void formation at the cathode.



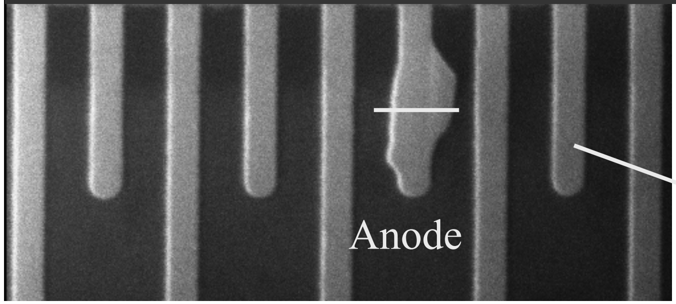


Cathode

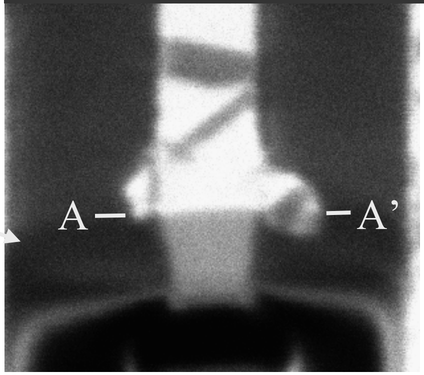
EM Failure in Cu/Low k Interconnect

- A hydrostatic compressive stress at anode breaks the interface of organic polymer and cap layer.
- Cu extrudes through interface between organic polymer and cap layer; failure due to interfacial delamination.

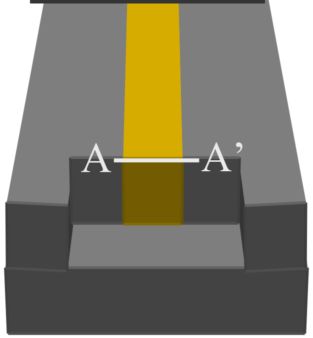
Top down view of Anode extrusion

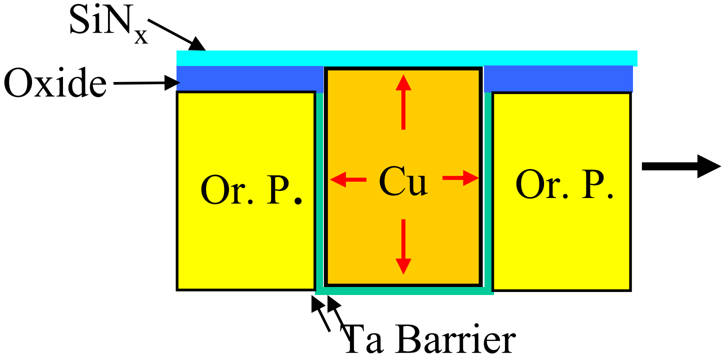


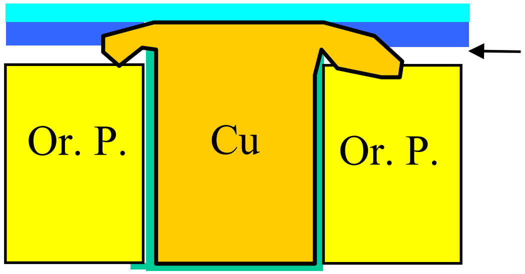
Cross-section of Anode



FIB cutting





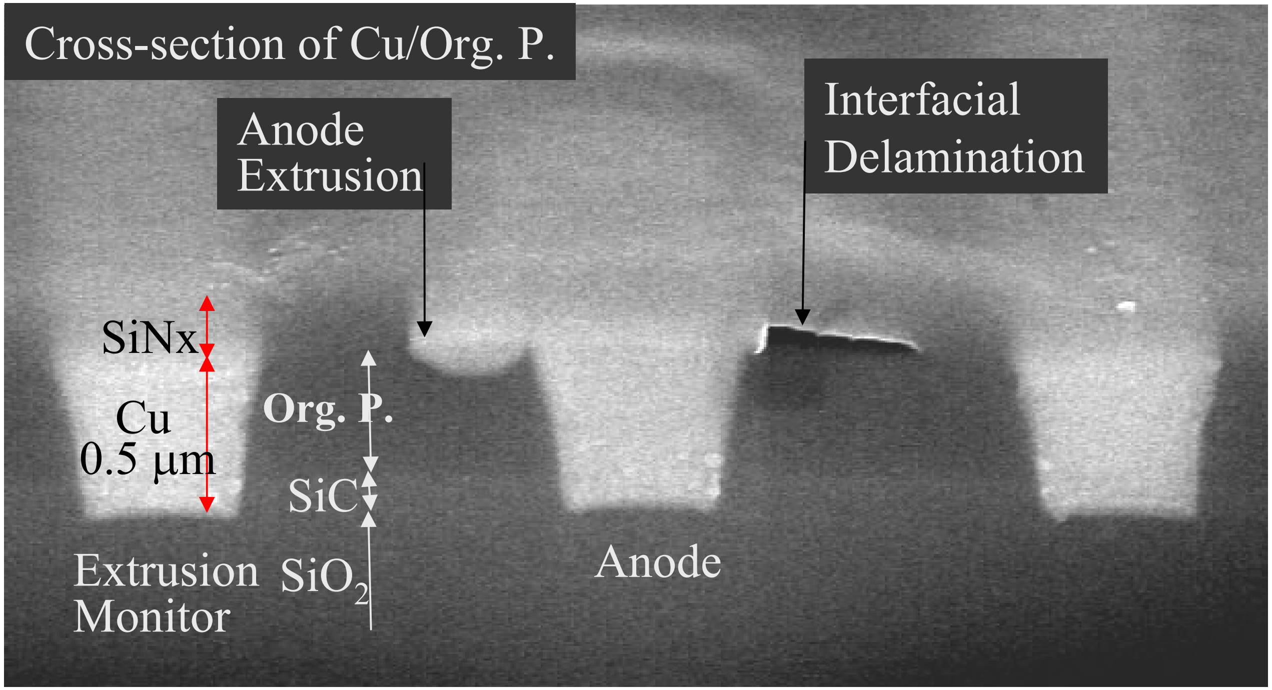


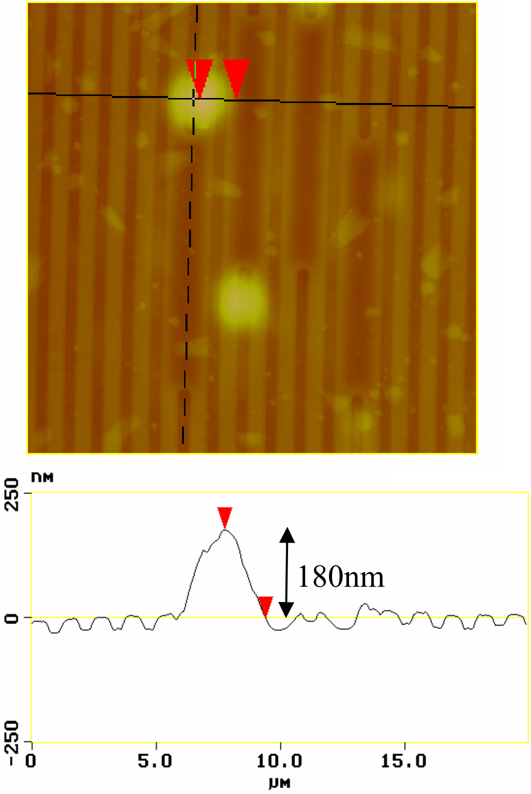
Interfacial adhesion can be an EM reliability issue

(K.D. Lee, UT Austin, 2001)

Failure Analysis - Cu/Organic polymer

- A high compressive stress at anode caused interfacial delamination as well as anode extrusion.





Summary

- Low k dielectrics are required for development of Cu interconnects for 130 nm technology node and beyond.
- Thermal stress behavior indicates that barrier and cap layers are important in sustaining structural integrity of low k interconnects. Local stress concentration can lead to delamination and failure of structure.
- EM results show mechanical properties can significantly affect lifetime and distinct failure modes are observed due to interfacial delamination in low k structures.
- Implementation of surface coating to reduce the interfacial mass transport and enhance adhesion is important for reliability improvement for Cu/low k interconnects

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Summary

- Low k dielectrics are required for development of Cu interconnects for 130 nm technology node and beyond.
- Dielectric confinement is important in controlling EM reliability of Cu interconnects. The effect depends on material properties, interconnect geometry and structures.
- The activation energies of Cu/oxide and Cu/low k interconnects are in the range from 0.81 to 0.93 eV, indicating that interfacial diffusion dominates mass transport for Cu interconnects.
- There is a good correlation between the effective elastic modulus B and EM characteristics of Cu/lowk structures. Results is affected by damage formation due to interfacial delamination or metal extrusion.