



Direct Observation of Alloyed Contact Formation in Nanowire Cross-section

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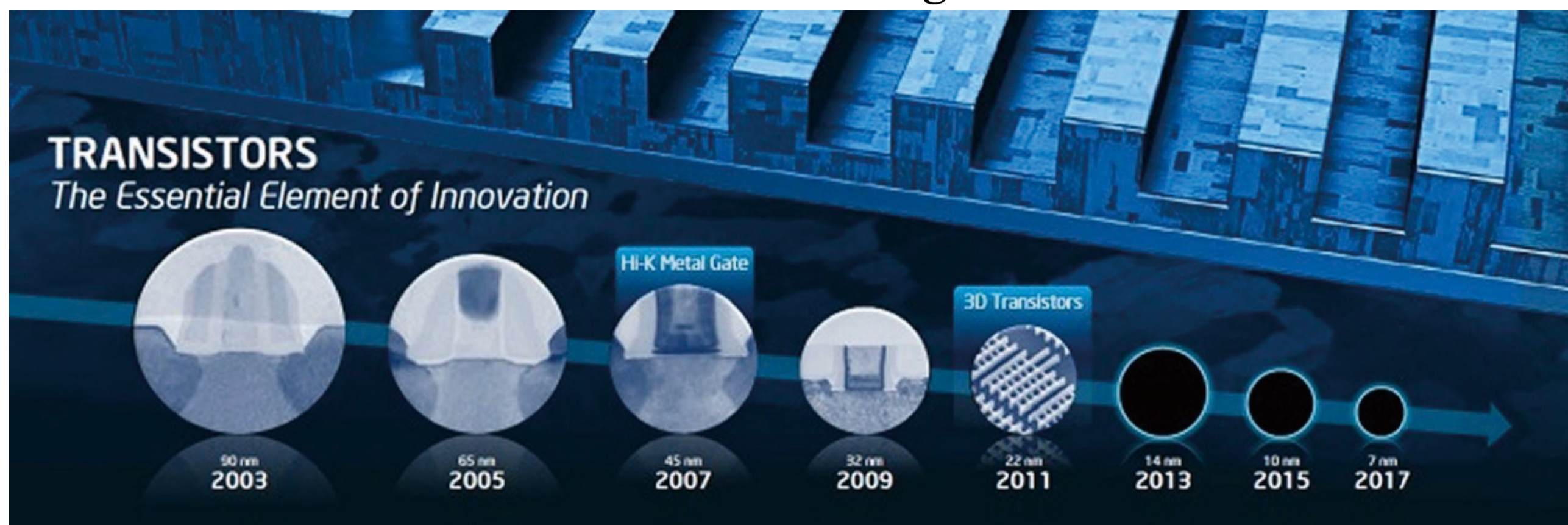
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Motivation

CMOS Scaling

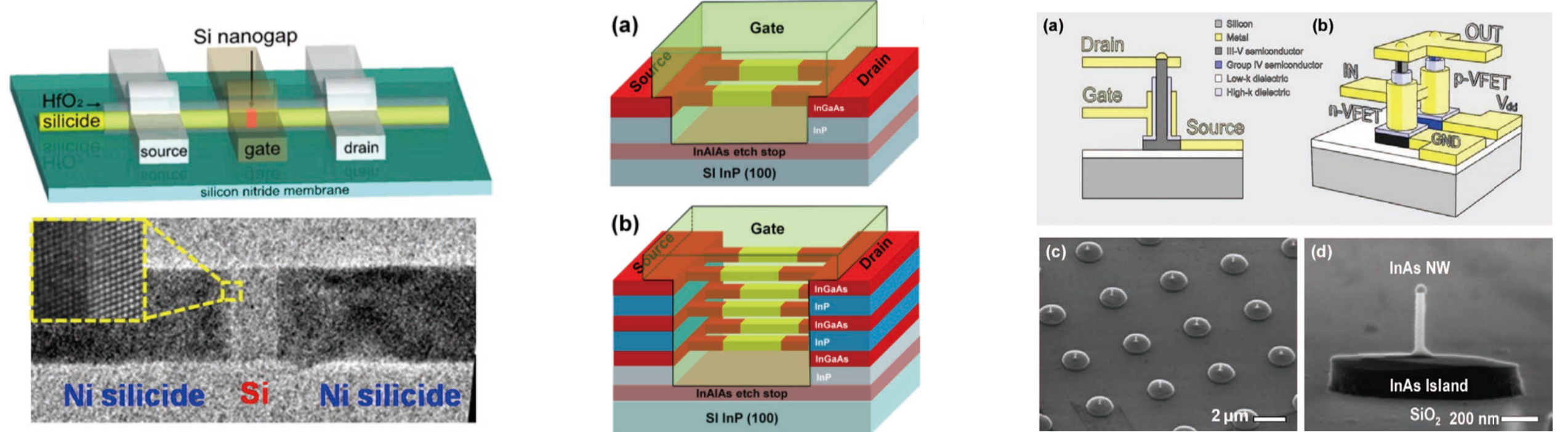


Intel Manufacturing Roadmap 2003-2017

The metal-semiconductor contact in ultra-scaled devices is one of the most critical factors limiting device performance.

Opportunities and Challenges

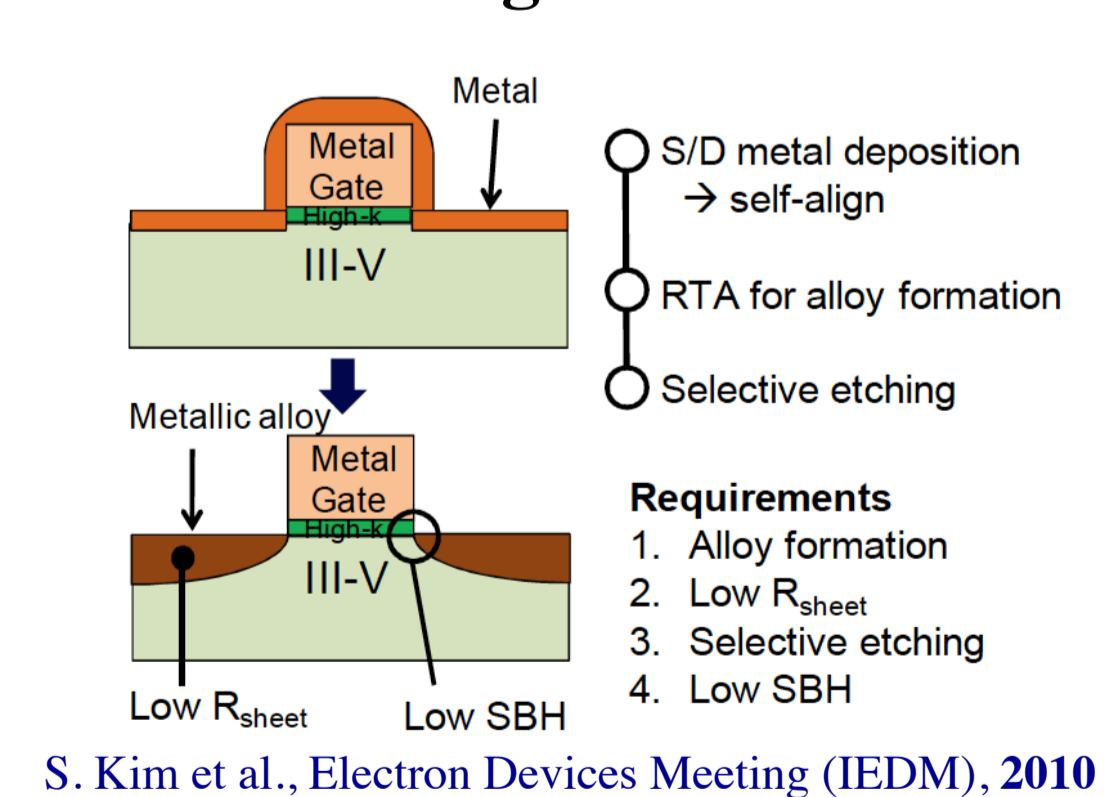
Nanowire Transistors



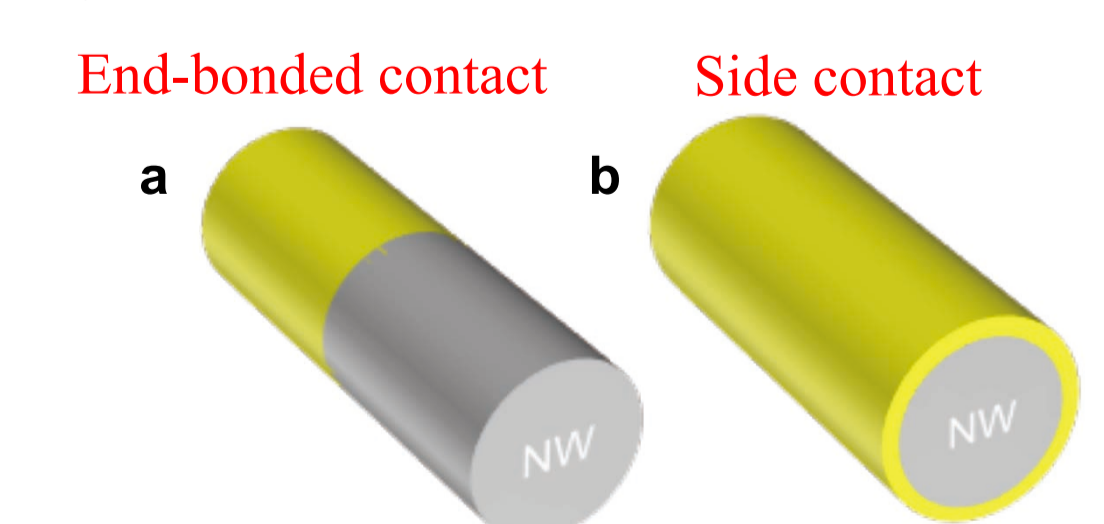
Tang and et al. *Nano Letters*, 12, 3979, 2012; Gu and et al., Electron Devices Meeting (IEDM), 2012; Dayeh and et al. *Nano Today*, 4.4, 347, 2009

- Nanowires are promising building blocks for future nanoscale electric devices.
- High electron-mobility III-V nanowires hold great potential in sub-7 nm MISFETs.
- Metal-semiconductor alloyed contact has not been evaluated in nanowire cross-sections, which will be critical for a self-aligned gate-first process.

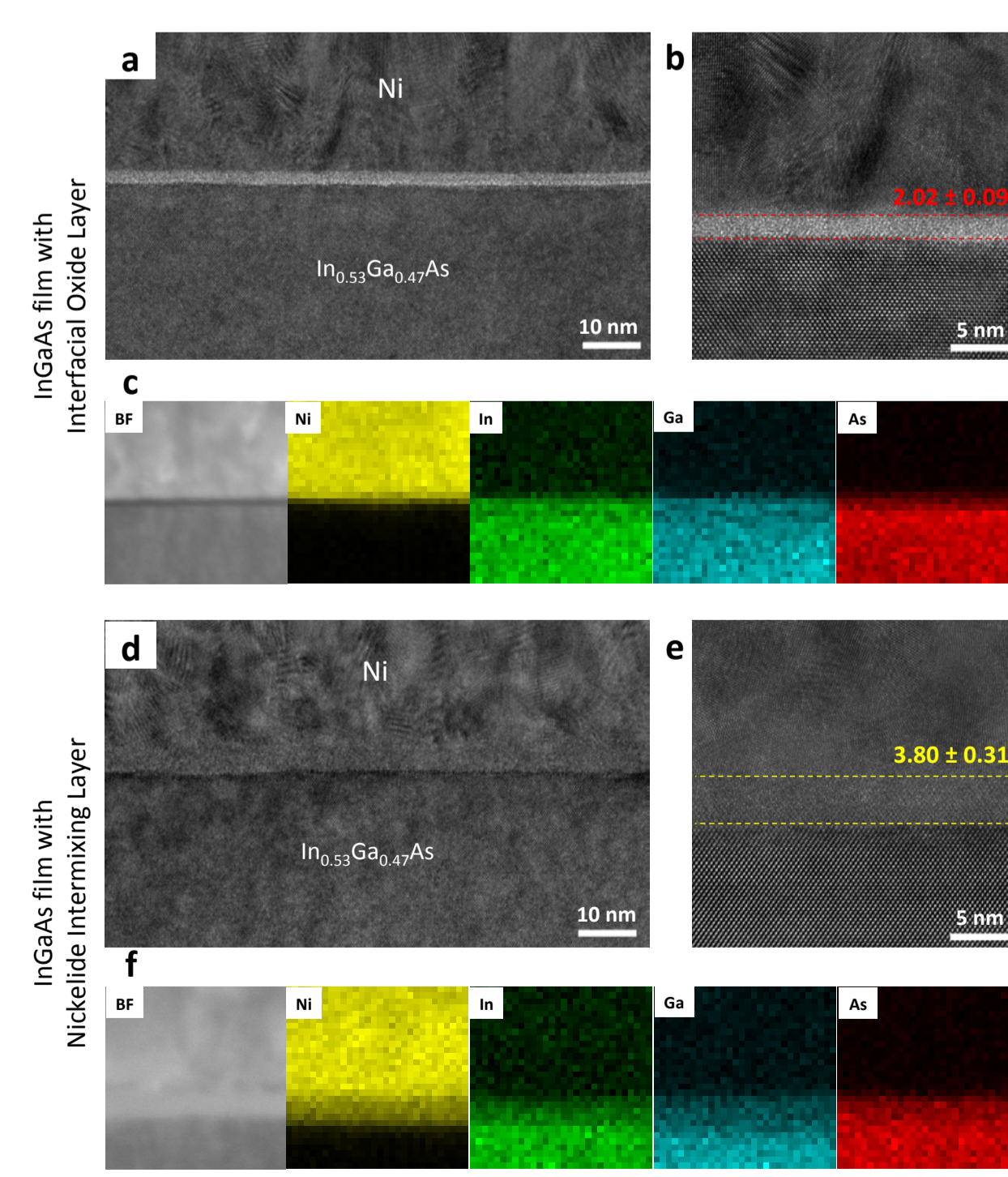
Self-aligned Contact



Contacts in Nanowire Geometry

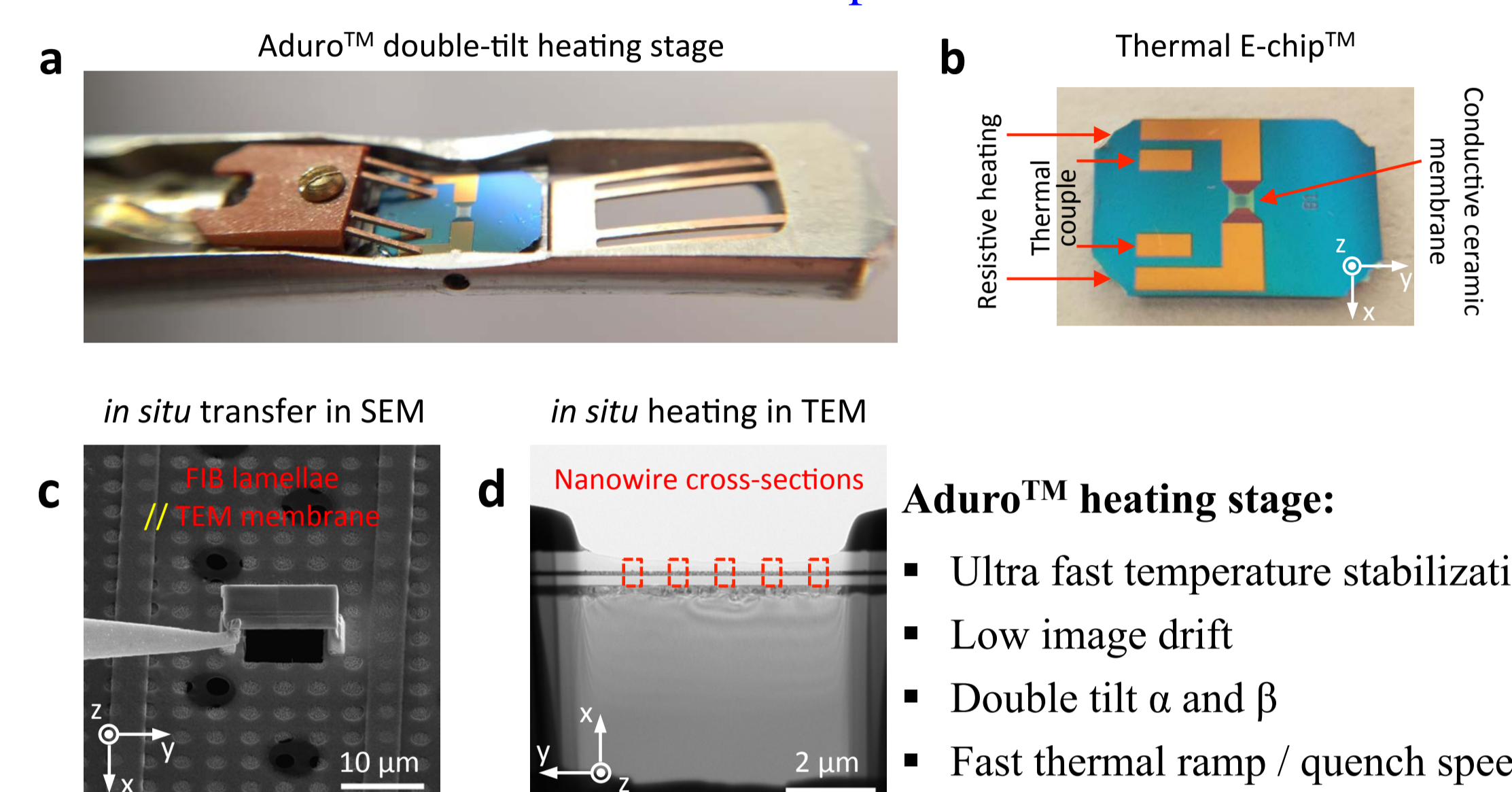


Metal-semiconductor Interfaces

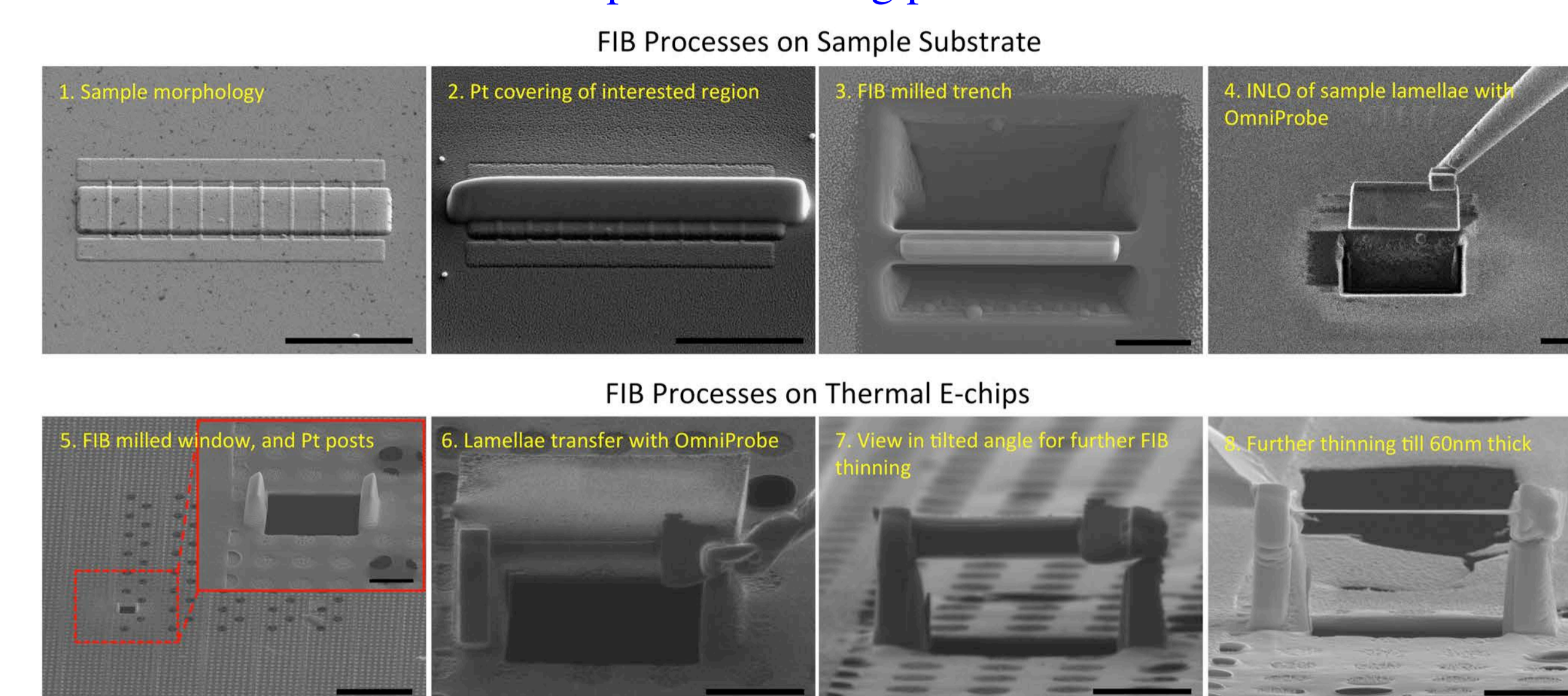


Integration of FIB Lamellae on *in situ* Heating TEM Platform

in situ TEM platform



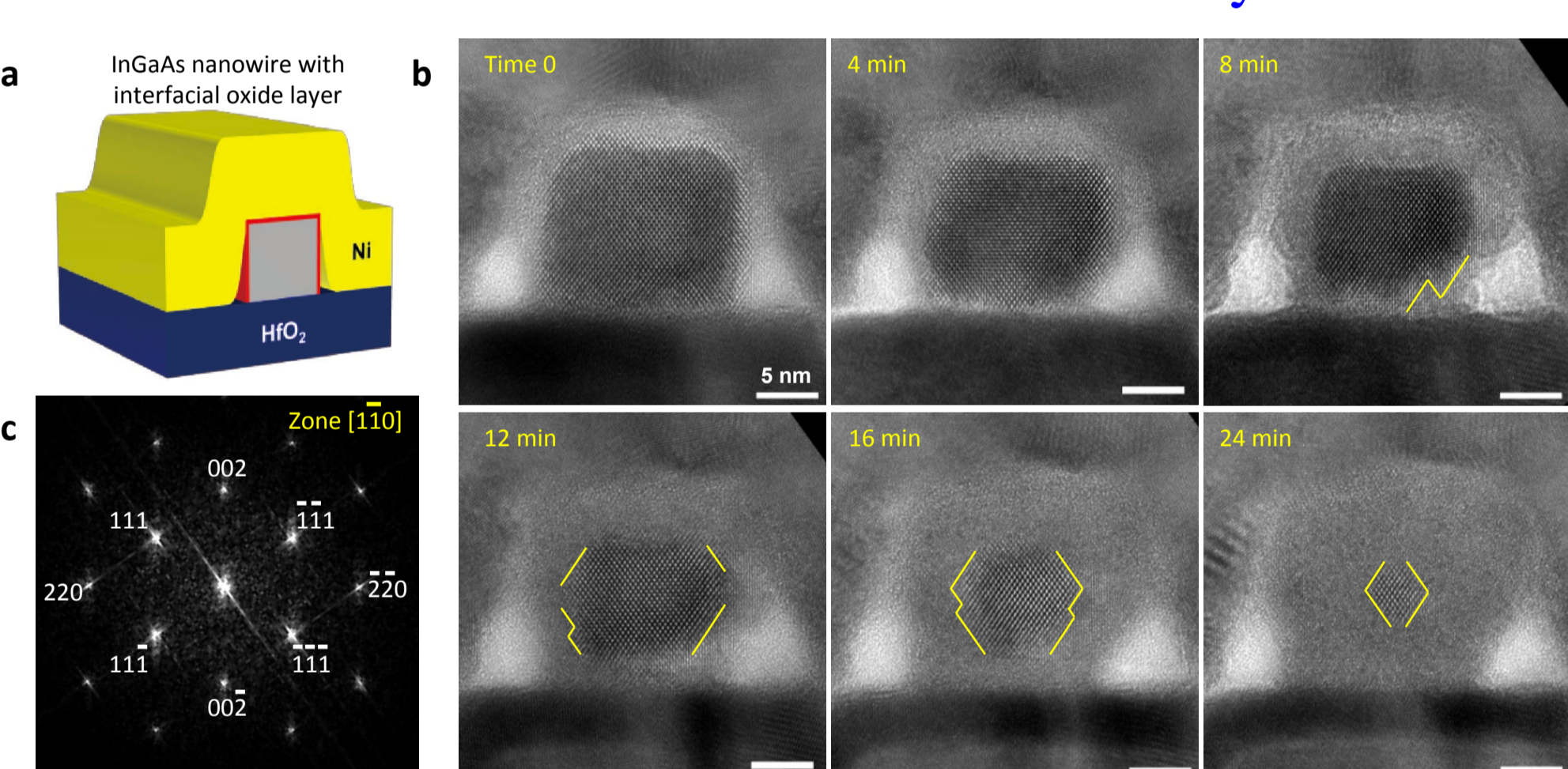
Sample transferring procedures



- Aduro™ heating stage:**
- Ultra fast temperature stabilization
 - Low image drift
 - Double tilt α and β
 - Fast thermal ramp / quench speed

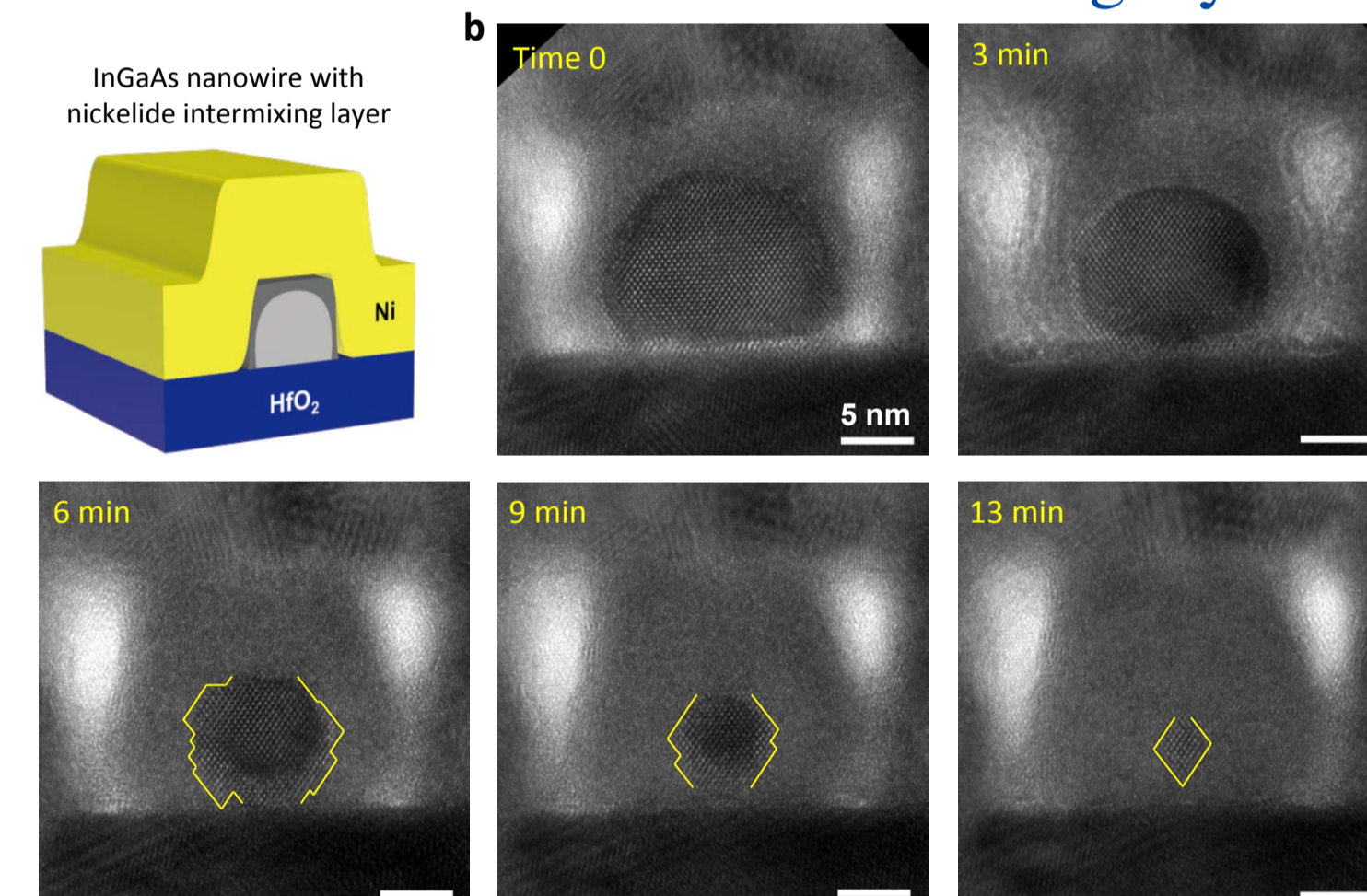
Interface-determined Reaction Kinetics

Influence of InGaAs surface oxide layer

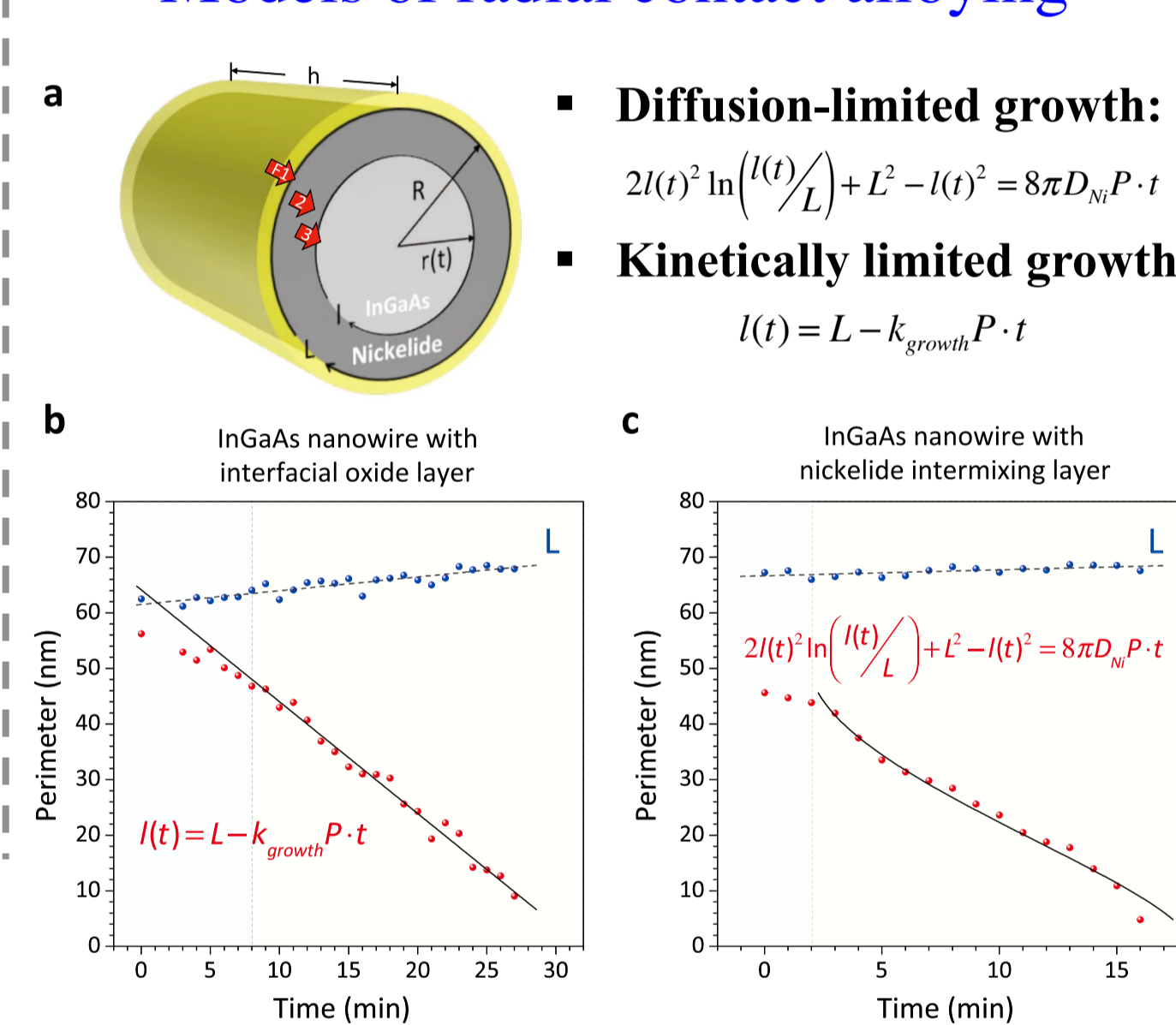


- At temperatures above 180°C, the nanowire cross-section experiences a solid-state reaction and forms amorphous $Ni_xIn_{0.53}Ga_{0.47}As$ ($x < 2$).
- The reaction is kinetically limited when there exists an interfacial oxide layer, otherwise, it changes to a diffusion-limited growth with the presence of an intermixing layer during metal deposition.

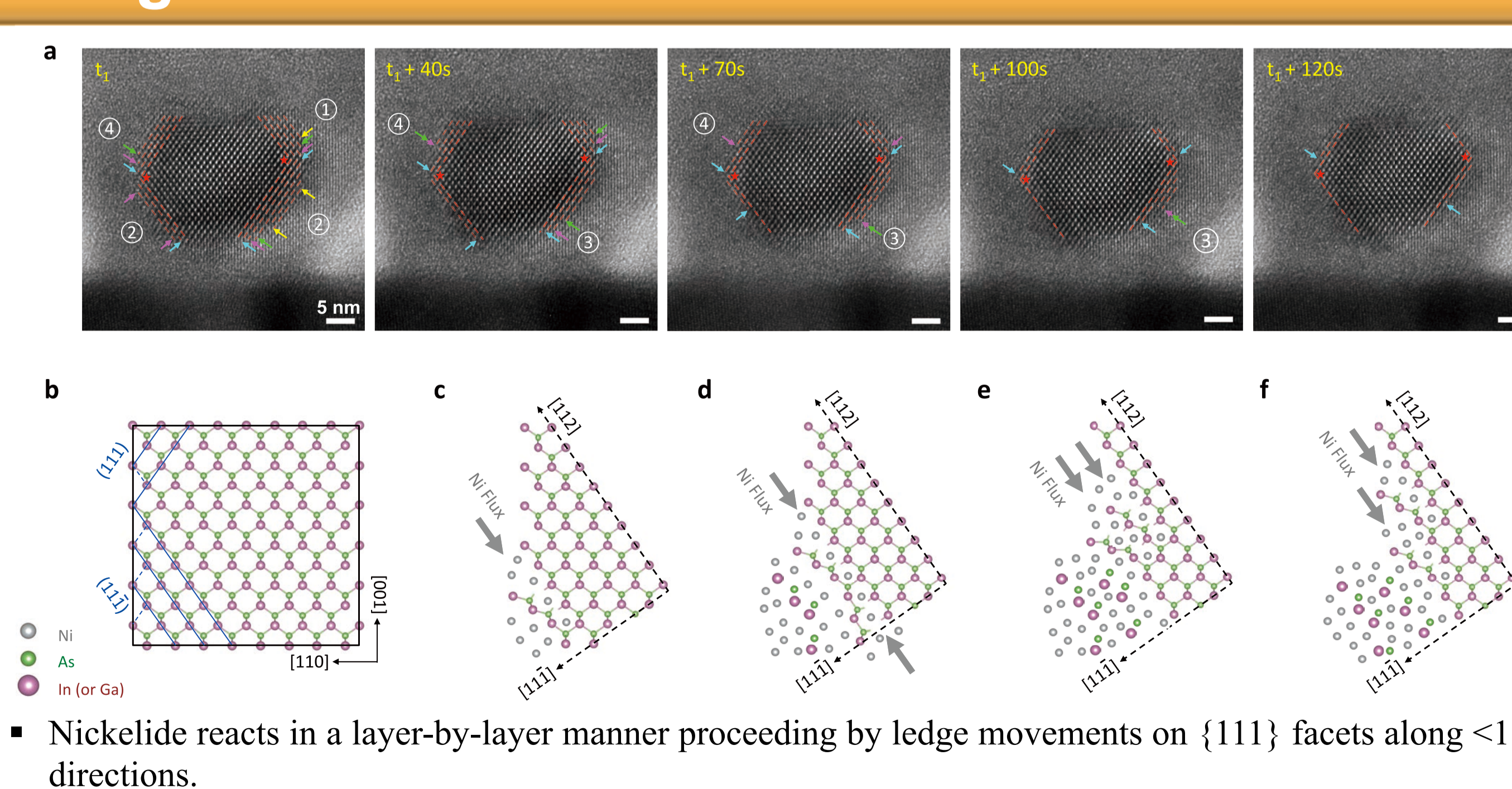
Influence of Ni-InGaAs intermixing layer



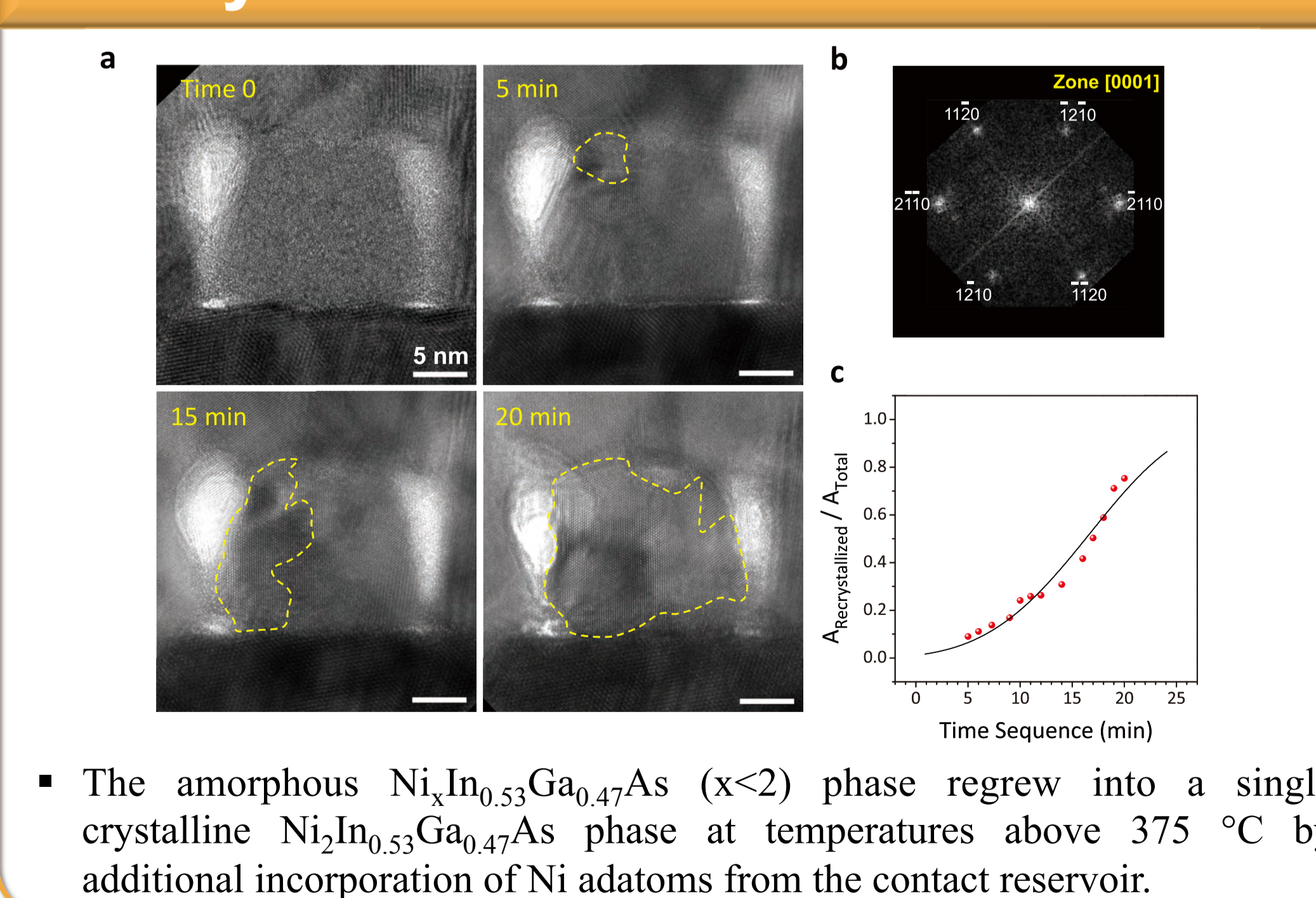
Models of radial contact alloying



Ledge Formation and Movement



Recrystallization



Renjie Chen, Katherine L. Jungjohann, William M. Mook, John Nogan, and Shadi A. Dayeh "Atomic Scale Dynamics of Contact Formation in the Cross-section of InGaAs Fin/Nanowire Channels" *Nano Letters*, accepted, 2017