

Electrical Property Characterization of Vacuum-Channel Nanoelectronics via Scanning Capacitance Microscopy

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Introduction & Sample

Efforts to harden components and systems have become a major engineering operation for space exploration agencies [1] and other organizations that seek to safeguard their electronic components and systems. Unfortunately, such processes are not only time-consuming but expensive; hardening electronics against radiation and heat lead to solutions that are both costlier and older than what is available to other types of consumers [2].

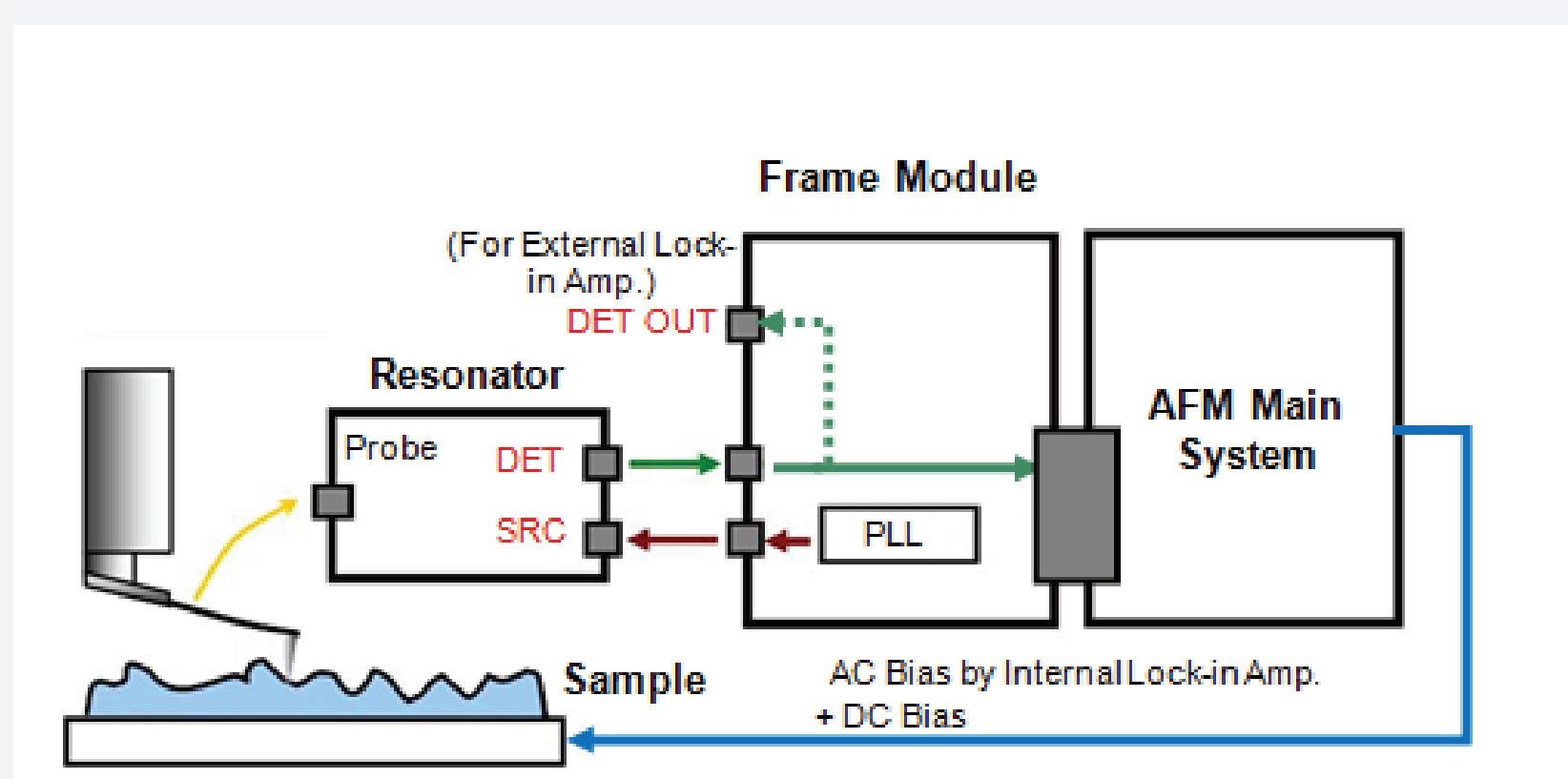


Solid-state electronics used in space-flight equipment are vulnerable to radiation and heat effects experienced in outer space. Vacuum-channel based alternatives are being developed to have more robust performance in extreme environments.

In order to address these drawbacks and produce a transistor technology that can achieve higher speeds and frequencies than any semiconductor device, research has begun focusing on reviving vacuum tube technology and applying its principles at nanoscale whilst still leveraging a silicon-based fabrication method. The result is a vacuum-channel transistor device which could potentially be manufactured at an industrial scale using already existing silicon fabs for solid-state transistor devices [2]. This investigation uses Scanning Capacitance Microscopy (SCM) to investigate the nanoscale electrical properties of a newly developed vacuum-channel device to both ascertain its viability as a transistor as well as to observe if the method used to fabricate its gate insulators can be controlled.

Methods

In SCM, a metal probe tip and a highly sensitive capacitance sensor augment standard Atomic Force Microscopy (AFM) hardware. A voltage is then applied between the probe tip and the sample surface creating a pair of capacitors in series (in Metal-Oxide-Semiconductor devices) from (1) the insulating oxide layer on the device surface and (2) the active depletion layer at the interfacial area between the oxide layer and doped silicon. Total capacitance is then determined by the thicknesses of the oxide layer as well as the depletion layer which is influenced by the both how doped the silicon substrate is well as the amount of DC voltage being applied between the tip and device surface.



Above left, a silicon SCM probe is lowered by its cantilever onto a sample surface (blue). The system diagrams to the right describe the resonator, frame module, and AFM system hardware processes for data acquisition.

The principle of how capacitance is measured in vacuum-channel devices via SCM is similar. Again, a thin layer of oxide is used as insulation on the device [4], this time insulating the gate from the source-drain interface on the device surface. A DC voltage is applied between the probe tip and the sample surface as the tip scans across various device features. The data of the detected changes in capacitance are also supplemented by AFM data generated by recording the deflections of the probe's cantilever as the tip engages the device surface [5]. As the sample scan is being completed, a laser beam is reflected off the probe cantilever and onto a position-sensitive photodiode. The deviations of the laser's position are then processed with software to create a rendering of the device's surface topography.

Data and Results

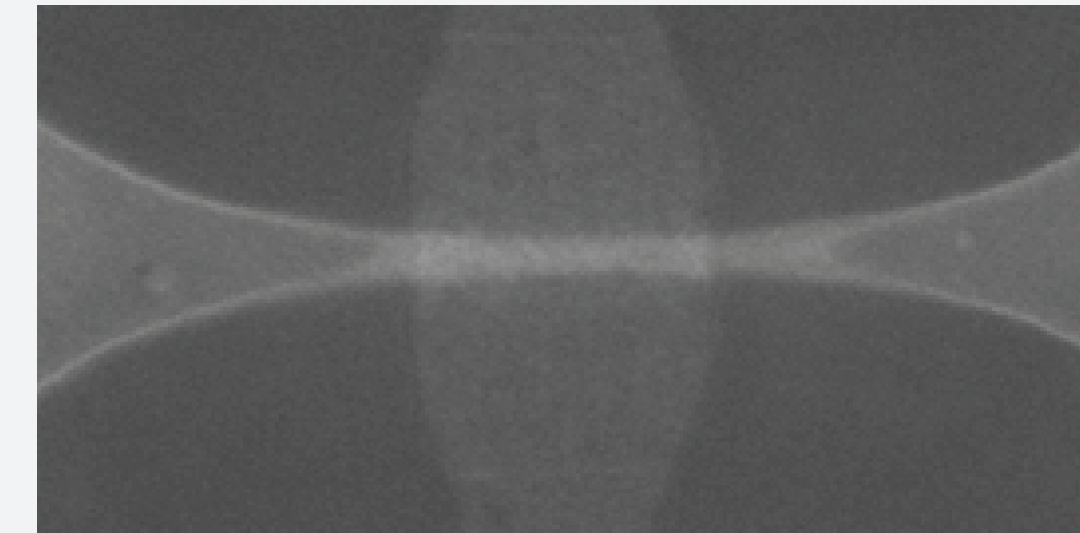


Figure 1 - SEM survey image of the vacuum-channel device for visual reference.

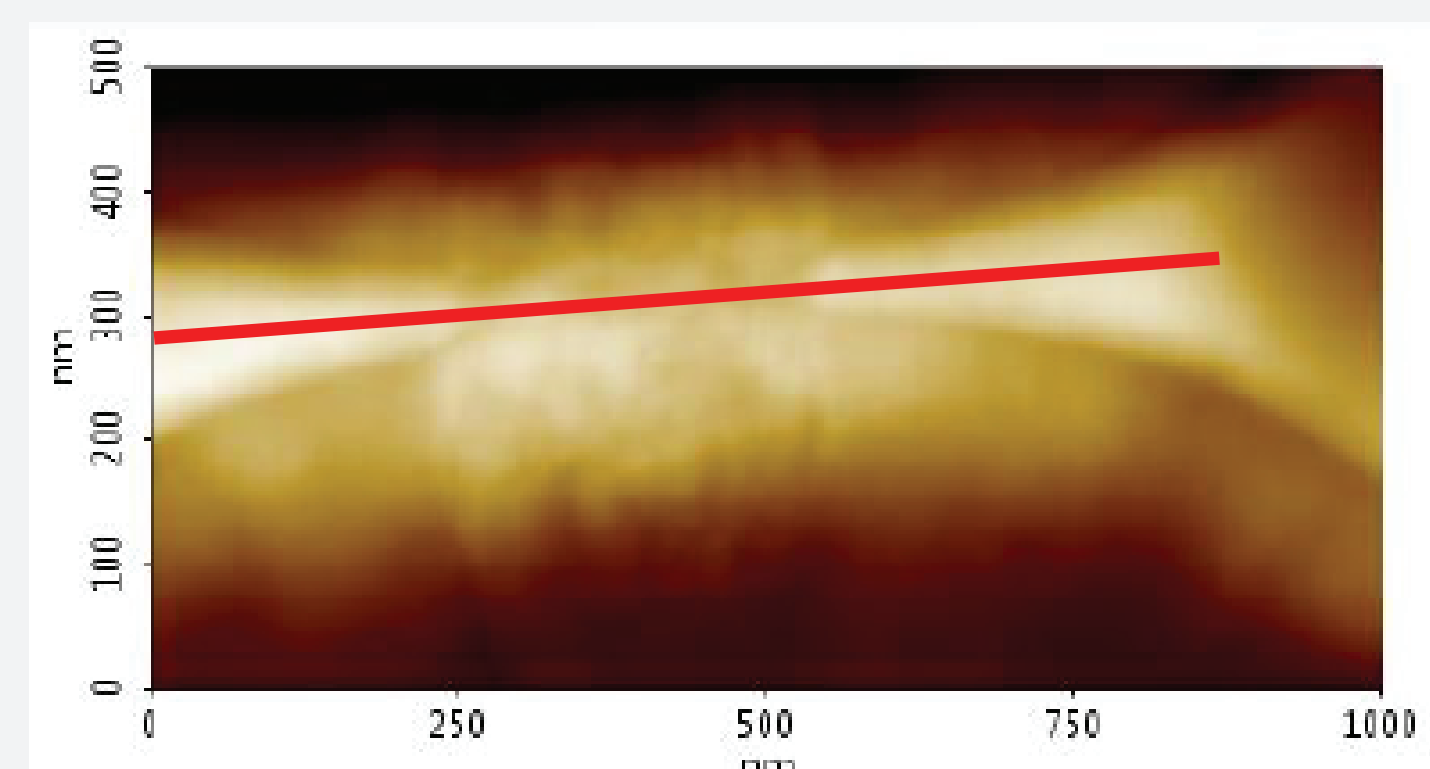


Figure 2 - Contact mode AFM topography image of the vacuum-channel device's source-drain interface. The overlaid red line corresponds to the topography line profile displayed in Figure 4. Scan size: 500 x 1000 nm.

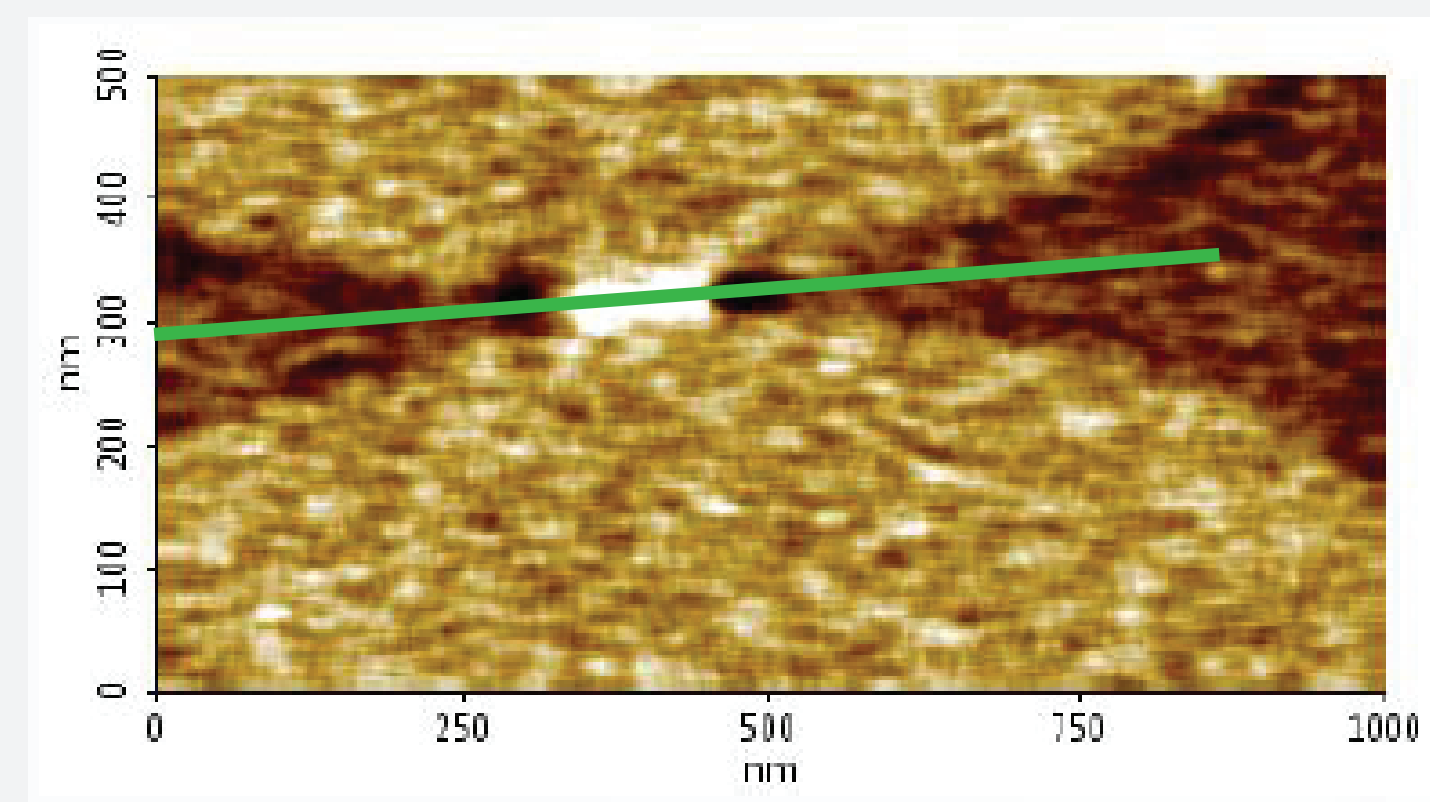


Figure 3 - An SCM capacitance image of the region containing the device's source-drain interface. Brighter colors correspond to relatively more positively charged areas on the device whereas darker colors correspond to relatively more negatively charged areas. The overlaid green line corresponds to the capacitance line profile displayed in Figure 4. Scan size: 500 x 1000 nm.

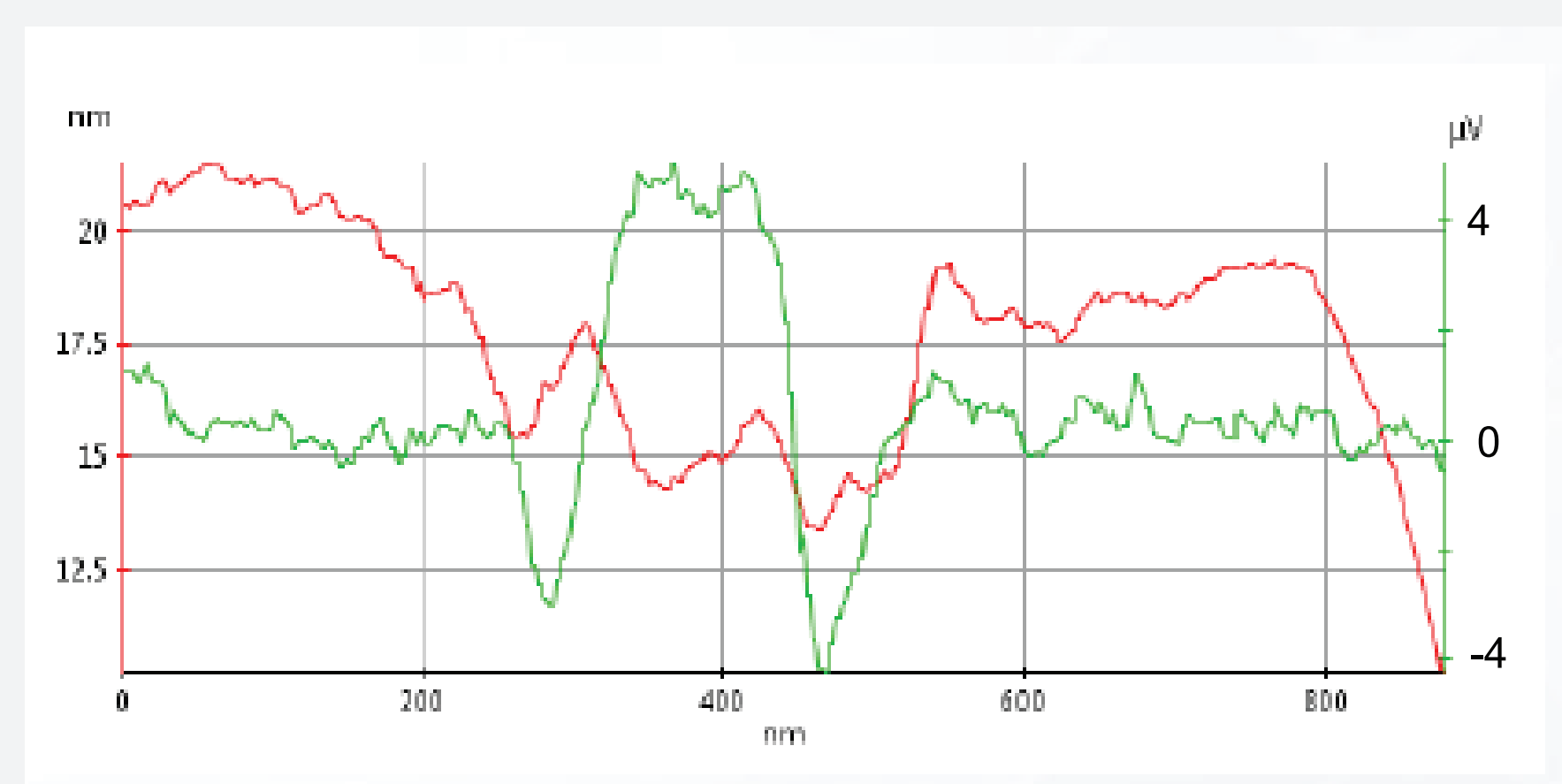


Figure 4 - Line profiles of the AFM topography (red, left y-axis in nm) and the capacitance data (green, right y-axis in μV) of the device area scanned in Figures 2 and 3.

Conclusions

SCM together with AFM successfully characterized both the spatial variations in capacitance as well as the topography of a newly developed vacuum-channel nanodevice. By examining the line profiles of the topography and capacitance data acquired down an identical path on the device's source-drain interface, additional insight was gained into the relationship of key physical structures with changes in capacitance. The device's topography at its source-drain interface was imaged and revealed a vacuum-channel spanning 250 nm in length with peaks and valleys separated by a distance of approximately 5 nm. The electrical functionality of the device was assessed through the acquisition of a capacitance map. This map revealed a relatively negatively charged (0.4 to 0.8 μV) source-drain terminal and adjacent quantum dot followed by a relatively positively charged vacuum-channel (5 μV) and another dot-terminal structure (0.4 to 0.8 μV) on the other end of the source-drain interface. This alternating series of capacitance changes at these key structures suggest the device is capable of effective functionality as a transistor.

References

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