Atom Probe: Opportunities for CMOS Characterization

Poster 018

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INTRODUCTION

The functional properties of complementary metal oxide semiconductor field-effect transistors (CMOSFETs) depend on structure, elemental distribution, and interface roughness among other factors, at the nanometer or even the sub-nanometer scale. The distribution of just a few individual atoms, near the gate in a fin-shaped FET (finFET) or adjacent to a strained layer, often determines the performance of individual devices. As such, optimal metrology methods are needed to routinely measure these features in 3D near, or even at, the atomic scale [1]. This poster discusses the opportunities for atom probe tomography (APT) to contribute to understanding the construction of these technologies by looking at both test structures and real devices. We find that when the tungsten in the high-κ metal gate (HKMG) structure and some of the SiO_x insulating regions are removed, significantly higher analysis yield and less distortion in the reconstruction can result.

APT SPECIMEN PREPARATION

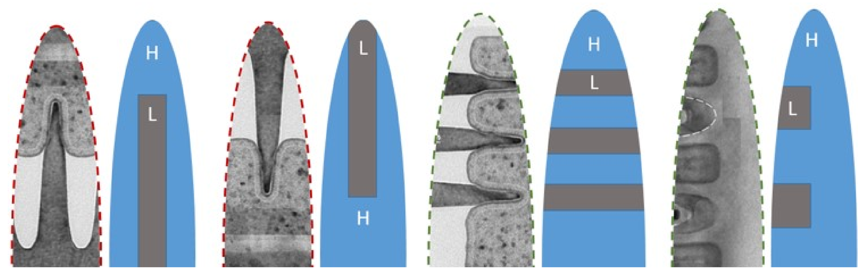


FIGURE 1. FinFET analysis options alongside the resulting simplified, evaporation field variation expected for, from left to right, top-down, backside, parallel to the gate, and parallel to the fin.

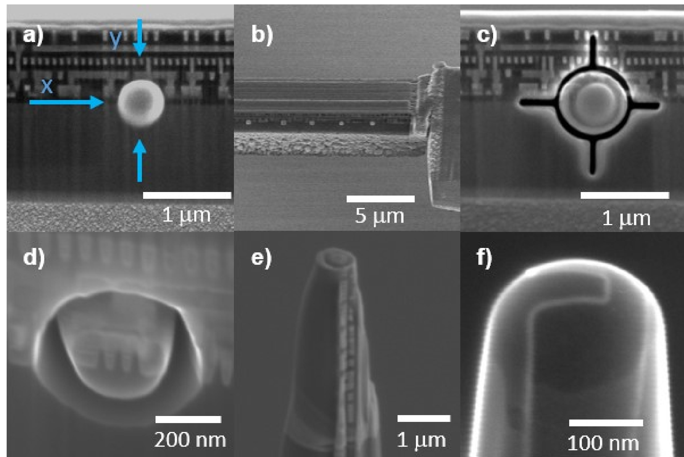
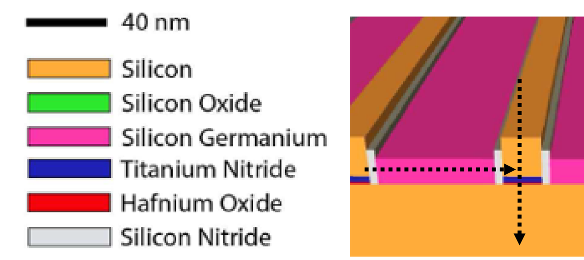
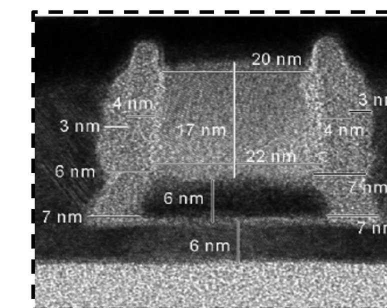


FIGURE 2. Illustration of the targeted cross-section lift-out method. a) A fin located and marked. b) Multiple fins are similarly marked and protected. c) Ion-beam creates additional markers. d) The wedge is aligned and the Pt is removed. e) Annular milling proceeds f) View of a final specimen after field evaporation.

- Modern APT analysis can require sophisticated approaches for sample preparation.
- Focused-ion-beam (FIB) methods are used to manufacture APT specimens in the required nano-needle geometry [2].
- The standard lift-out process can be as simple as one, two, three: 1) extract wedge of material, 2) propagate material to multiple posts, and 3) sharpen.
- Successful analysis of CMOS devices, additional strategies to de-process, cap, isolate, encapsulate, fill, and/or reorient regions-of-interest (ROIs) become important to achieve successful analysis [3].
- Overall goals are always the same:
  1. capture the ROI centered in the near-apex of a sharp tip,
  2. remove or avoid regions that are unimportant and might reduce analysis quality or yield,
  3. use capping or encapsulation to protect the ROI and control the field-of-view,
  4. orient the ROI to maximize the opportunity to achieve desired analysis goals.

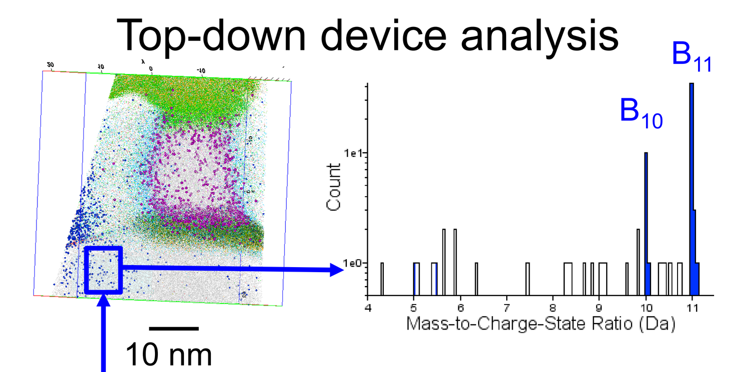
TEST STRUCTURES





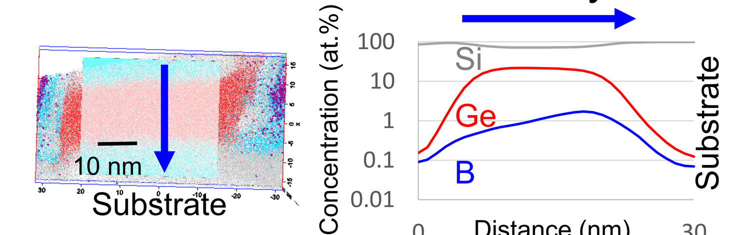
- Complete Structure Yield:
  - 4/8 top-down direction preparation
  - 2/5 cross-section preparation
- Two analysis directions and analysis repeats provide higher analysis confidence

Top-down device analysis



- ROI selected below source/drain
- 0.12 at.% B measured

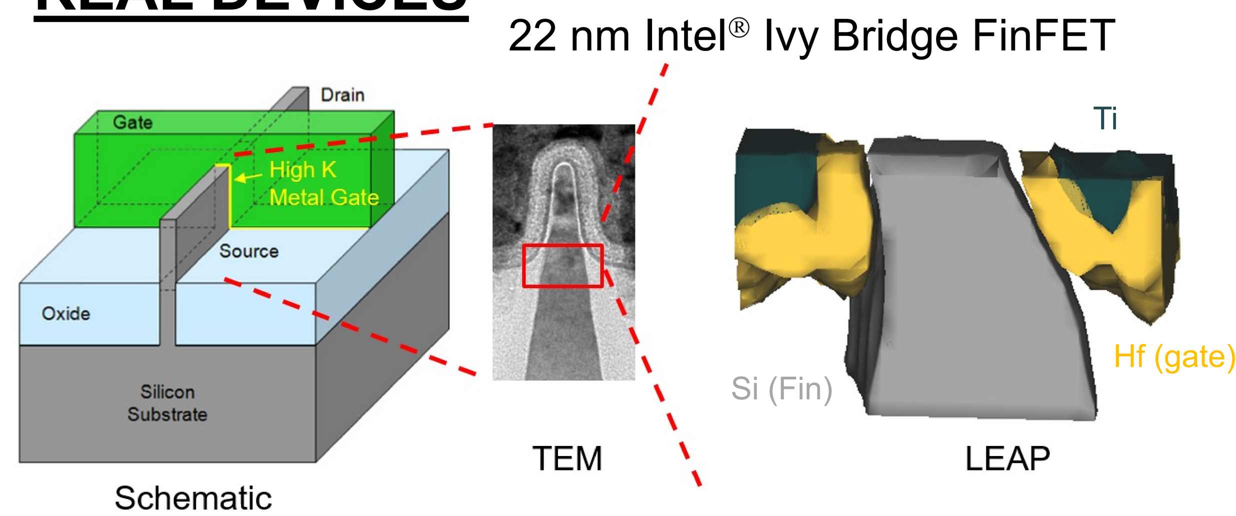
Cross-section device analysis



- Cross-section captures full SiGe region between devices
- Concentration profile shows B increases to 1.8 at.% approaching the Si substrate

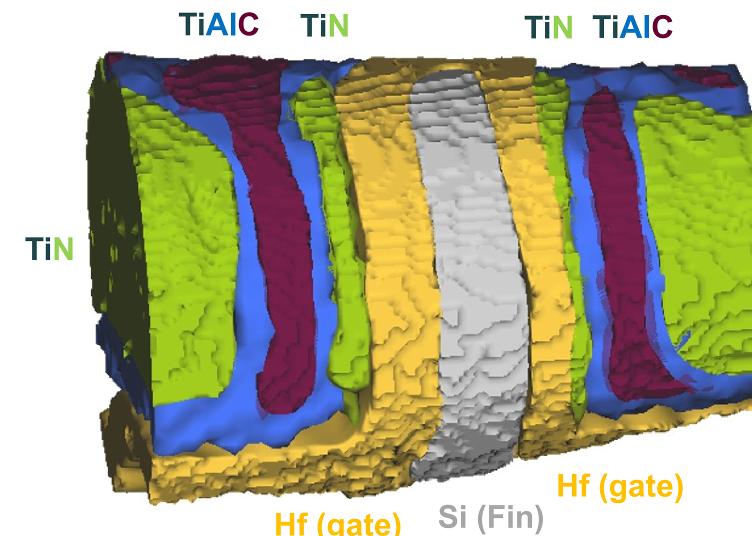
REAL DEVICES

22 nm Intel® Ivy Bridge FinFET



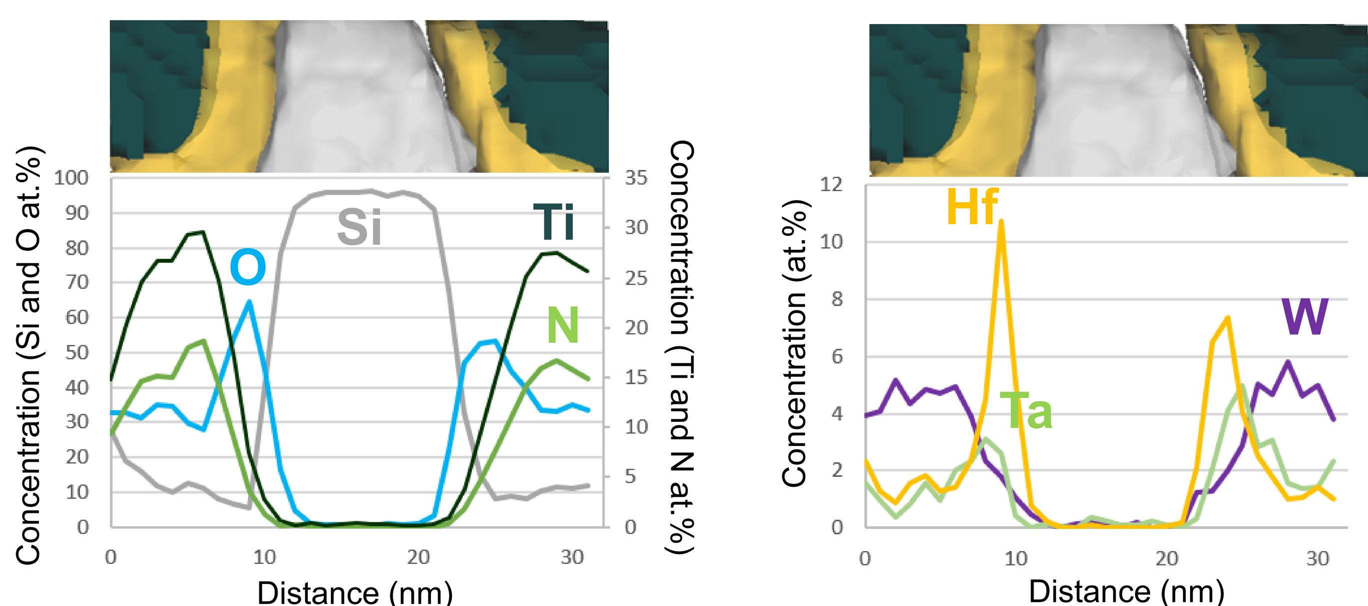
- Yield
  - 2 cross-section analyses with fin and metal gate visible,15 other partial analyses
  - 0 successful top-down analyses (even those which yielded data presented reconstruction challenges)
- Cross-section preparation leads to some success, but unsatisfactory yield
- Alternatives strategies to be considered

14 nm FinFET Technology

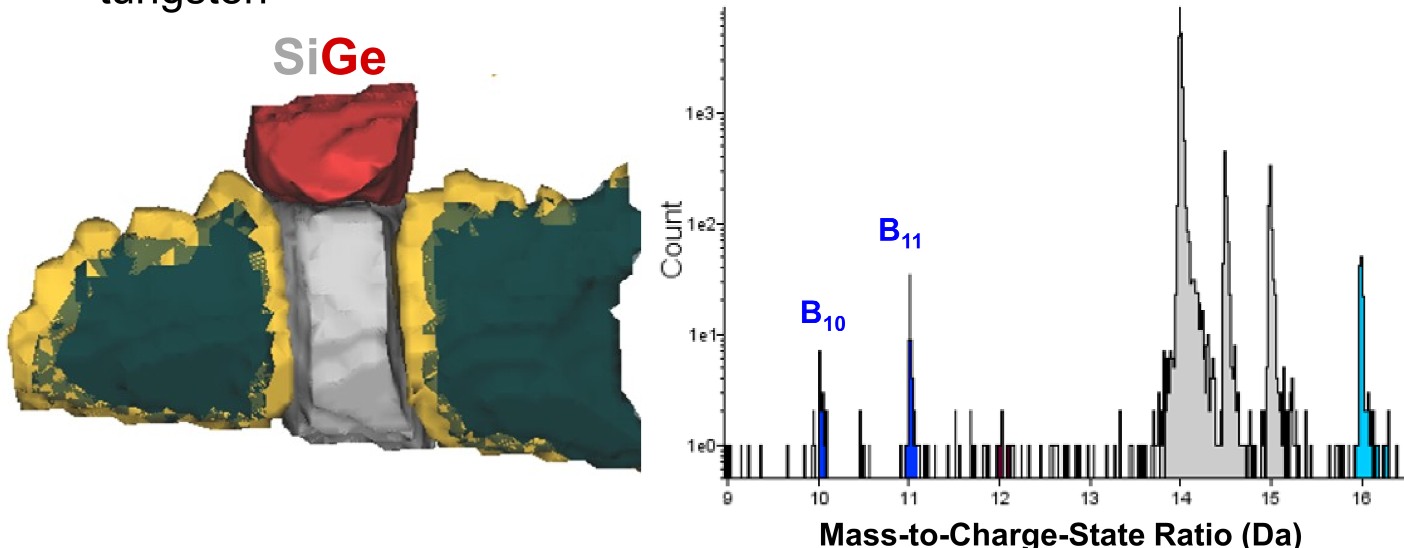


- A de-processing procedure was performed to remove tungsten (believed to lead to low analysis yield)
- Initial attempts yielded successful analysis (higher yield?)
- Various HKMG structures are clearly define in cross-section analysis along the gate direction.

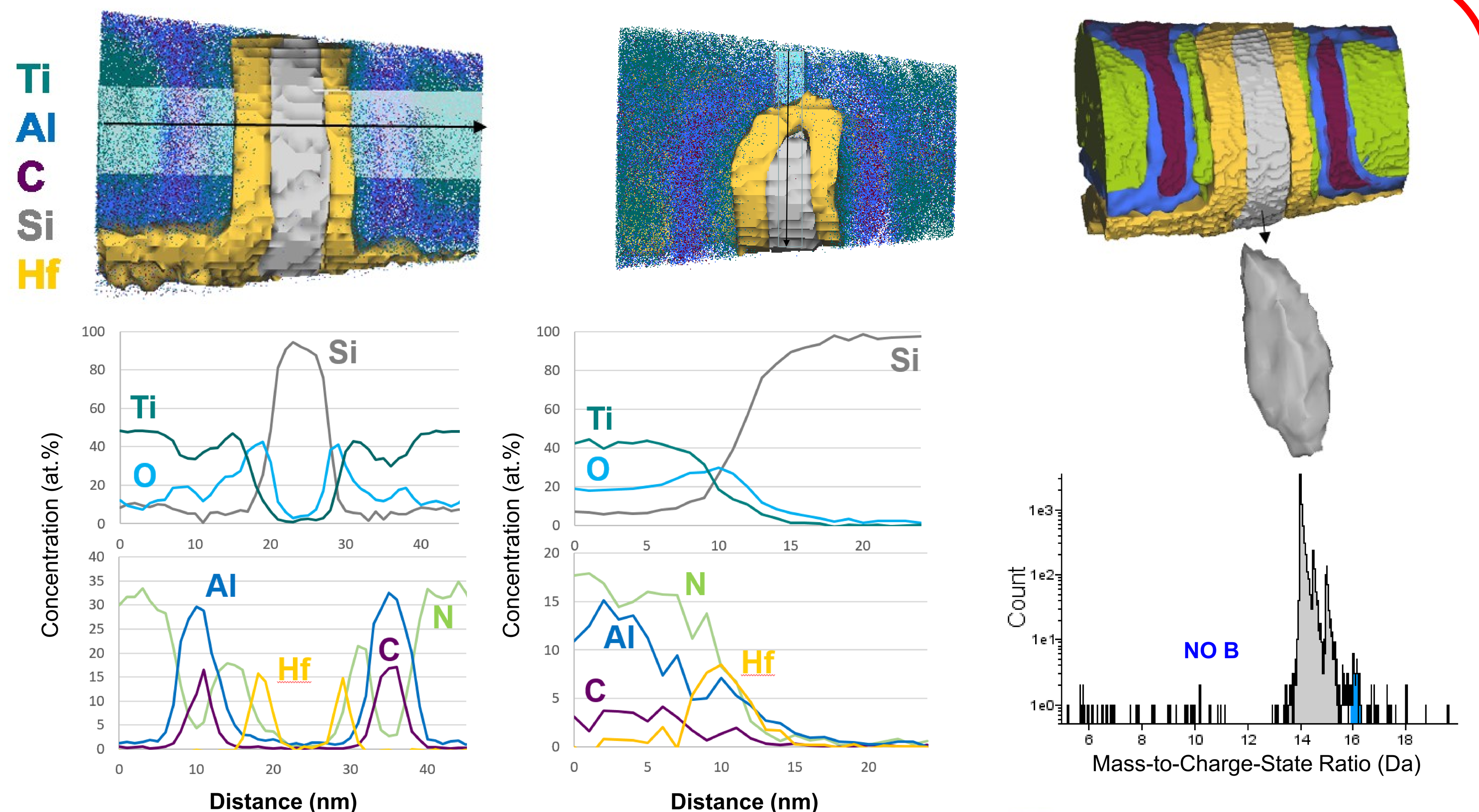
FULL DEVICE CHARACTERIZATION



- 1D composition profiles extracted normal to the fin (along the HKMG) reveal the silicon fin surrounded by HfO, Ta, TiN, as well as tungsten



- The advantage of full 3D APT data is that any individual sub-volume can be isolated for further analysis
- Here, a high-concentration-Ge sub-volume was isolated and its mass spectrum extracted for further chemical analysis
- Arsenic was not detected inside the SiGe region, but 0.2 at.% of B was found



- 1D composition profiles extracted normal to the fin (along the HKMG) reveal the silicon fin surrounded by HfO, TiN, and an TiAlC layers
- Good fin symmetry is observed in this reconstruction
- A silicon fin sub-volume from within the HKMG does not show any detectable boron
- Various views of the HfO layer wrapped around the silicon fin are shown to the right. This analysis appears to have captured a fin that terminates within the HKMG as it surrounds the fin on 3 sides

REFERENCES

[1] M. Mayberry, *Pushing Beyond the Frontiers of Technology*, in FCMN, E.M. Secula, D.G. Seiler, Eds., 2013, p. 21.

[2] D.J. Larson *et al.*, *Local Electrode Atom Probe Tomography*, New York: Springer, 2013.

[3] T.J. Prosa and D.J. Larson, *Microsc. Microanal.*, accepted (2017).

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CONCLUSIONS

The presence of many disparate material layers within real device structures is challenging APT because the evaporation field and adhesion differences can lead to limitation in both analysis yield and reconstruction accuracy. Test structures (structures with fewer layers) have been shown to provide higher yield and while still providing useful information for developers. For real devices, removal of regions with limited analysis value (like tungsten contacts) might provide a path to improved analysis yield. Properly extracting the real region of interest and removing unnecessary or less interesting surrounding structures may provide predictable yield to make APT a more standard CMOS characterization tool.