micro and nanoelectronics
microsystems
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# Characterization of Integrated Nano Materials

**Amal CHABLI**

leti

cea

# From Europe - France

**Micro and nano technologies**

- ✓ 300mm facility
- ✓ 200mm MEMS facility
- ✓ **Nanocharacterization**

ESRF

http://www.minatec.com

# Characterization International Acknowledgment

*IBM press release – April 9, 2009*

**CEA/Leti and IBM to Collaborate on Future Nanoelectronics Technology**

***CEA/Leti Becomes a Research Associate of IBM and IBM's Semiconductor Joint Development Alliance Ecosystem Centered in Albany***

**« GRENOBLE, France - 09 Apr 2009:** CEA/Leti (the Electronics and Information Technology Laboratory of the CEA, based in Grenoble), and IBM today announced that they will collaborate on research in semiconductor and nanoelectronics technology.

…

**Co**

Th

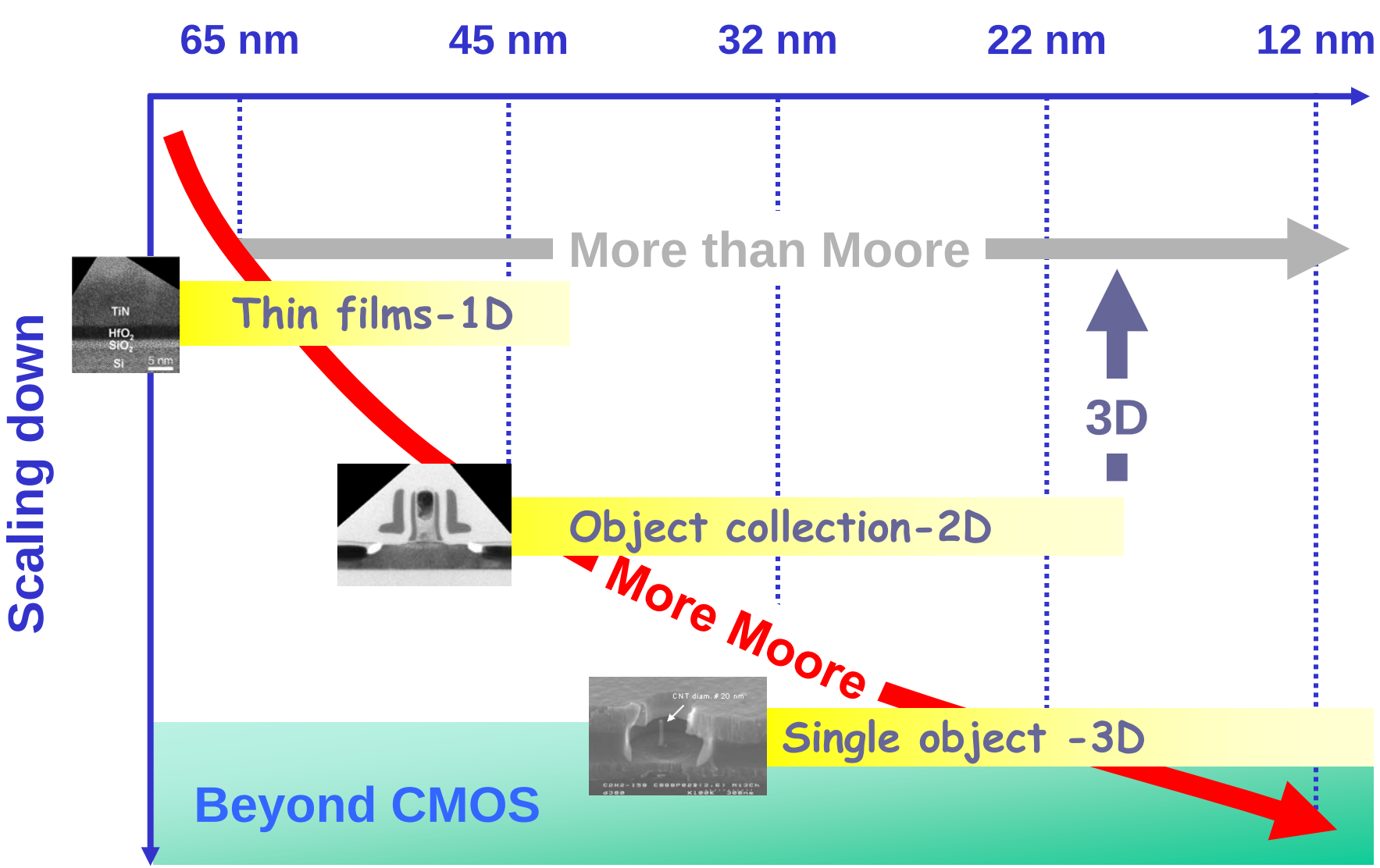
**innovative nanoscale characterization techniques**

• CMOS technologies and low-power devices for 22nm chip technology and beyond

• Technology enablement, including innovative nanoscale characterization techniques for research and for the monitoring of manufacturing protocols … »

*http://www-03.ibm.com/press/us/en/pressrelease/27187.wss*

# Driving forces for nanoscale characterization

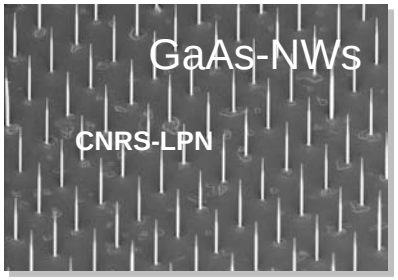


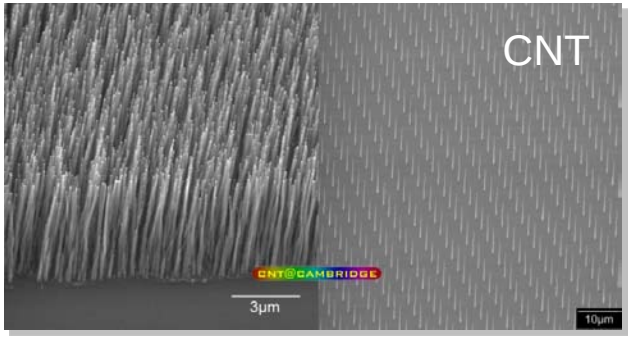
# Outline

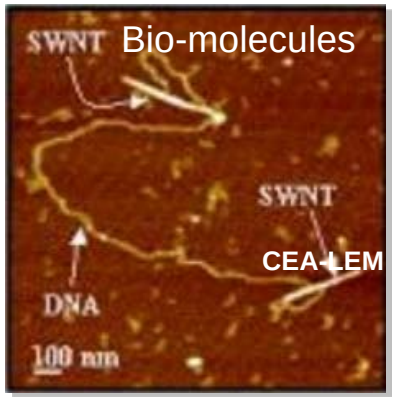
- A new nanomaterial context
- Down to 45 nm CMOS technology
- Below the 45 nm CMOS technology
- Integration of nanomaterials
- Conclusion

From the point of view of characterization

# Beyond CMOS and Extreme CMOS objects



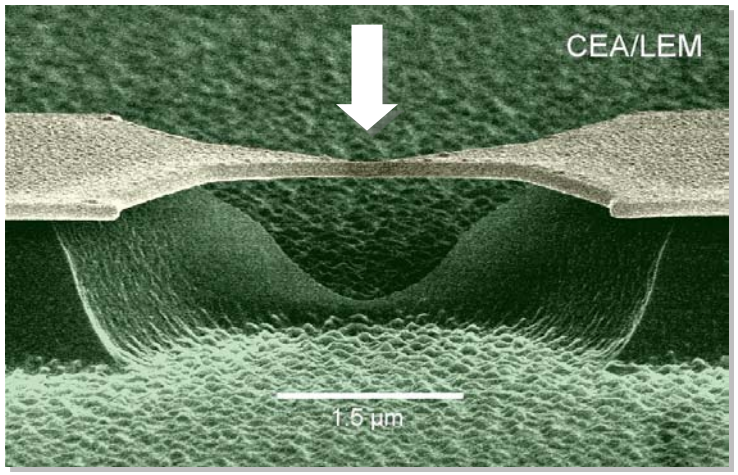




**Nanotechnology devices**

- Material science
  - Nanosize effect characterization
  - Huge instrumental effort
  - Powerful simulation
  - Elaborated data interpretation

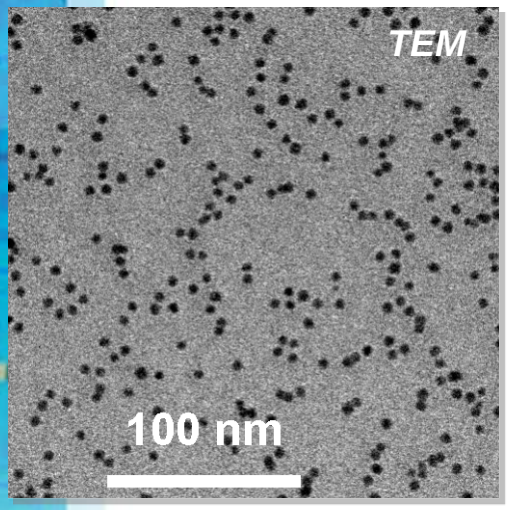
**Nano-bridge for contacting a single Np**

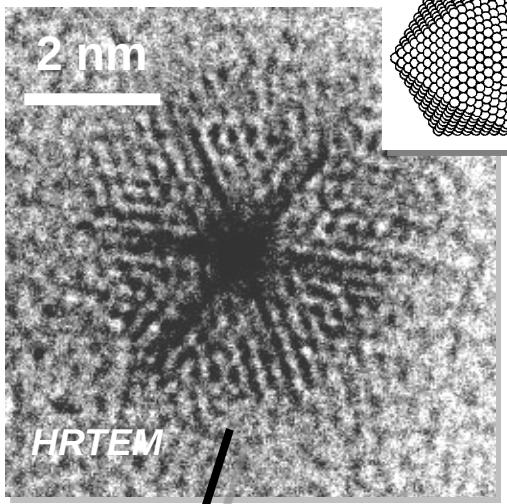



**Challenges for integrated NMs ?**

# Integrated materials characterization challenges

- Co multi-twinned nanocrystal on **TEM C membrane**

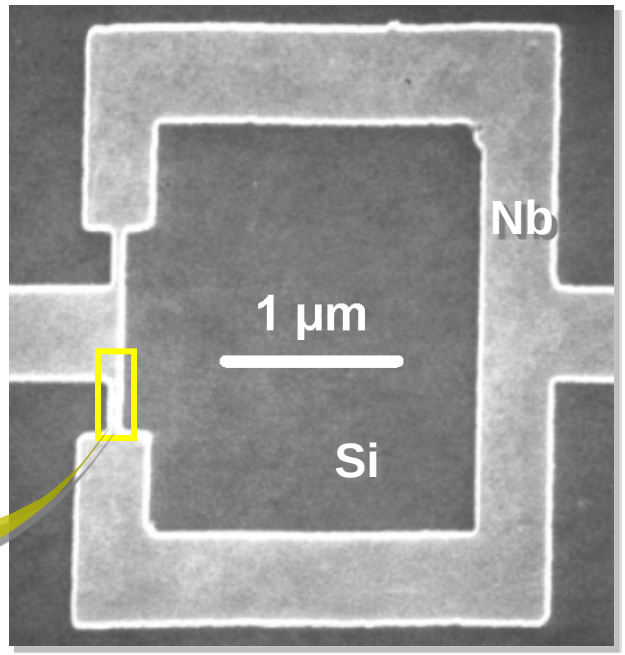





**Structural characterization wo preparation**

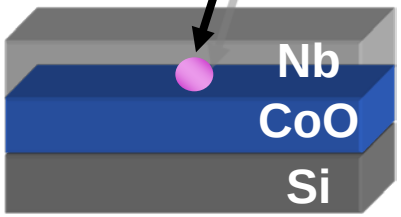
**µSQUID device single cluster magnetism**




*M. Jamet et al., Phys. Rev. lett. 86, 4676 (2001)*

*R. Morel et al., Eur. Phys. J. D24, 287 (2003)*

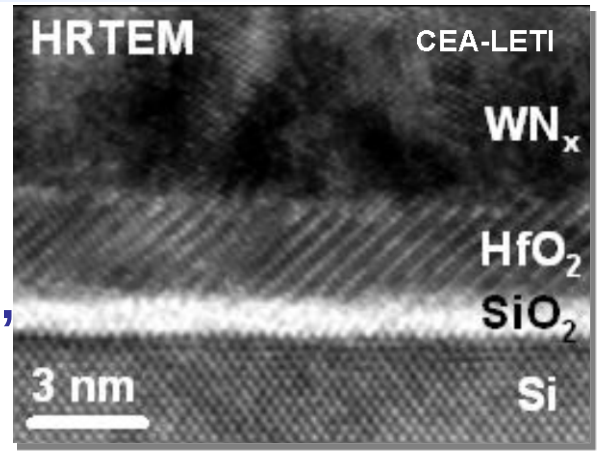
**Characterization using a TEM lamella**




- **Process induced changes**
- **Crystallographic orientation *vs* TEM**
- **Where are we, today ?**

# Down to 45 nm node CMOS technology

- New materials **HiK,**
  - *Metal gate stacks, Cu interconnects*
- Advanced processes **ALD,**
- Layer thickness down to the nm




*Courtesy A.-M. Papon*

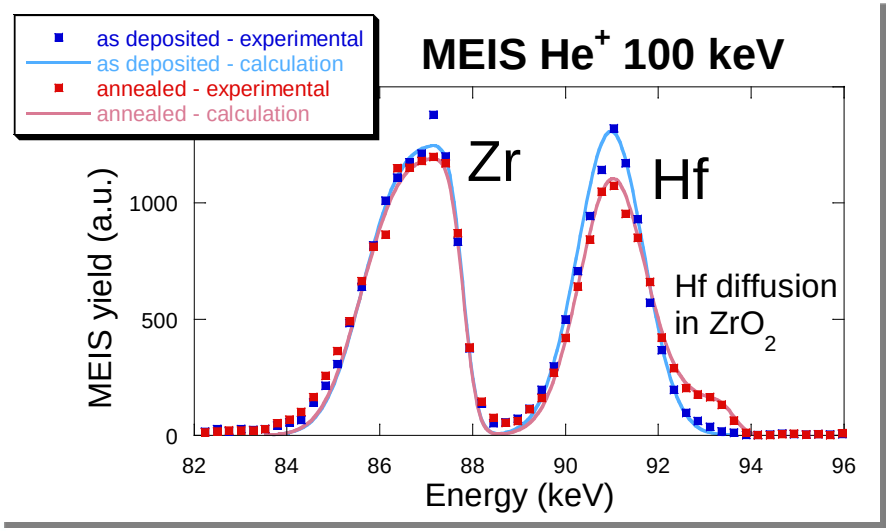
- Process improvement and control require mainly **1D information**
- Representative **full wafer layers and stacks** of the integrated materials are available
- Sub **nanometer depth resolution** mandatory

**Integration**

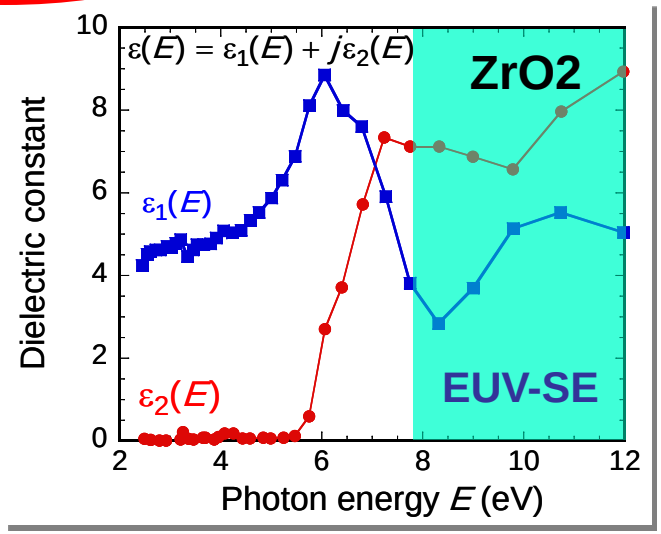
- **Material properties within thin layers**
- **Interface stability**

# 1D information from full wafer layer stacks

## Complementarities



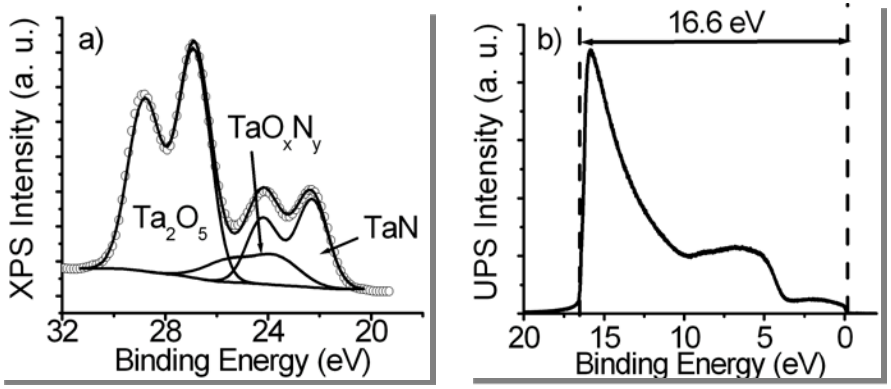

S. Lhostis et al., proc. of 213th ECS Conf. (2008)




Courtesy F. Ferrieu

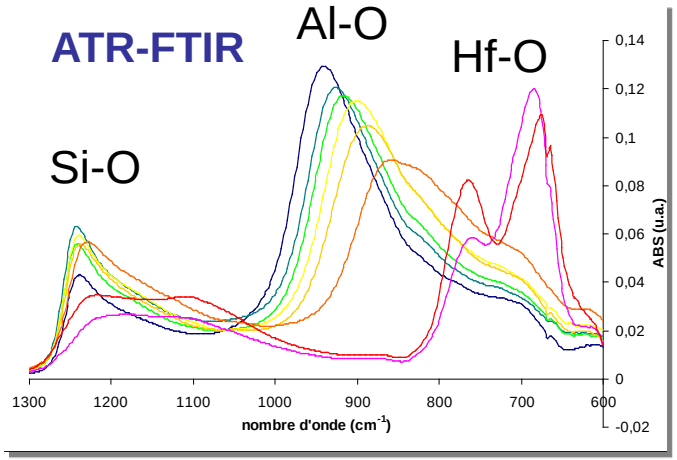
## Cutting edge capabilities

### XPS-UPS




A. Martinez et al., JAP, 104, 073708 (2008)

### ATR-FTIR




N. Rochat et al., FCMN (2007)

# Below 45 nm node CMOS technology

- Size effect on material properties **Cu lines**
- Local growth (SiGe S/D) **Selective epitaxy**
  - Process improvement and control require more and more **2D information**
  - Representative **features** of integrated materials **with only conservative 3rd dimension** are available
  - Imaging with **nanometer spatial resolution** required

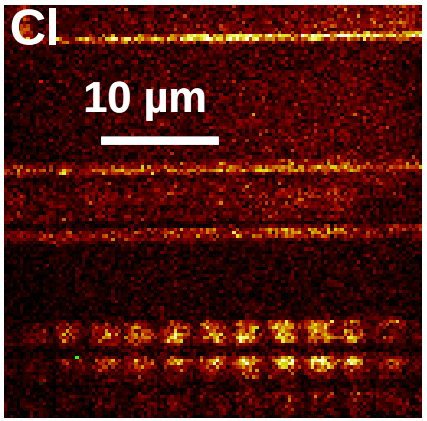
**Integration**

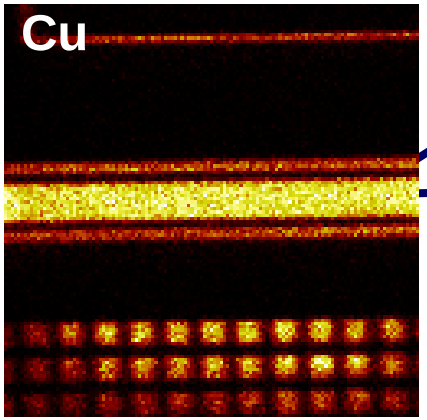
- **Size dependent properties**
- **Induced new phenomena and properties**

# 2D information for specific features

## Cu interco.

**TOF-SIMS**




0.4 µm Cu line

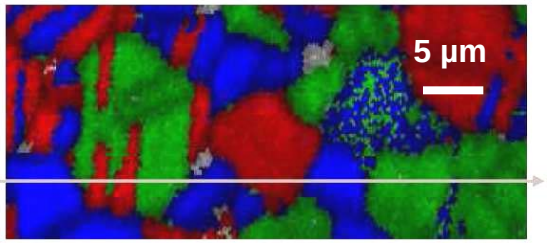
3 µm Cu line

*J.-P. Barnes et al.*
*SIMS XVI Int. Workshop (2007)*

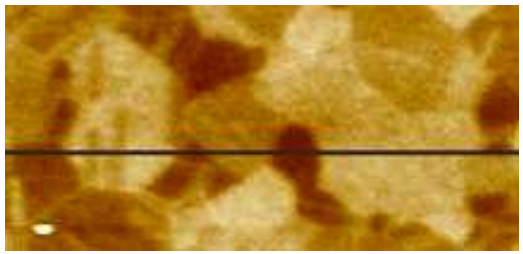
## Metal gate

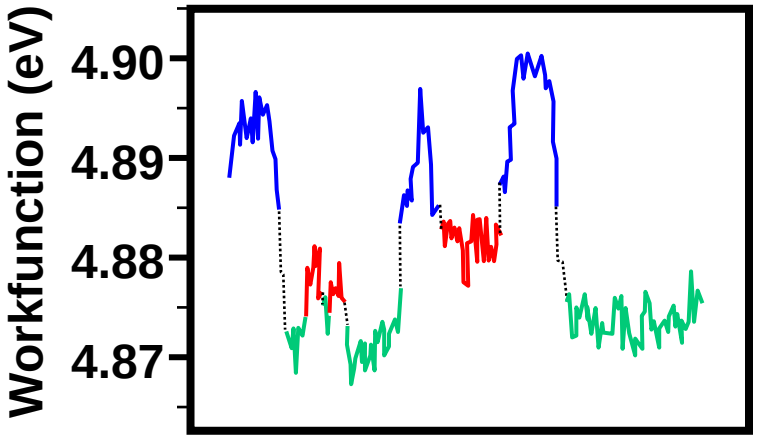
**EBSD**

<111>
<100>
<110>




**KFM**






*N. Gaillard et al., Microelec. Eng.* ***83*** *(2006)*

K. Kaja et al.
Poster TU-011

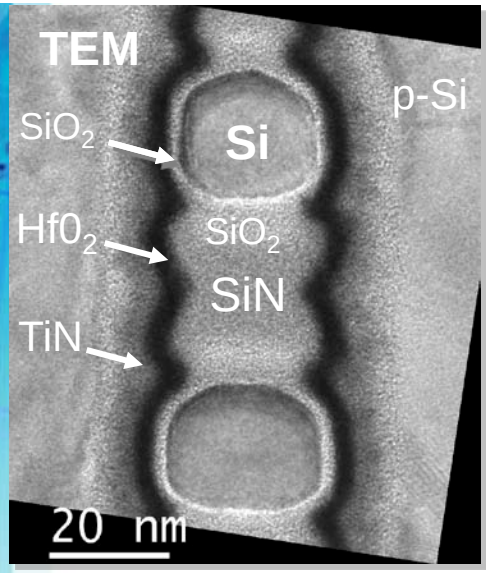
N. Barrett et al.
Poster WE-025

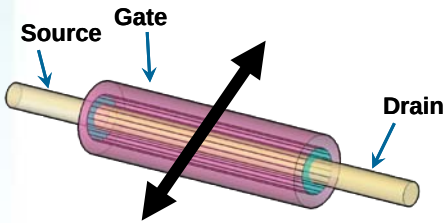
## Surface topography

# 2D information from electron microscopy

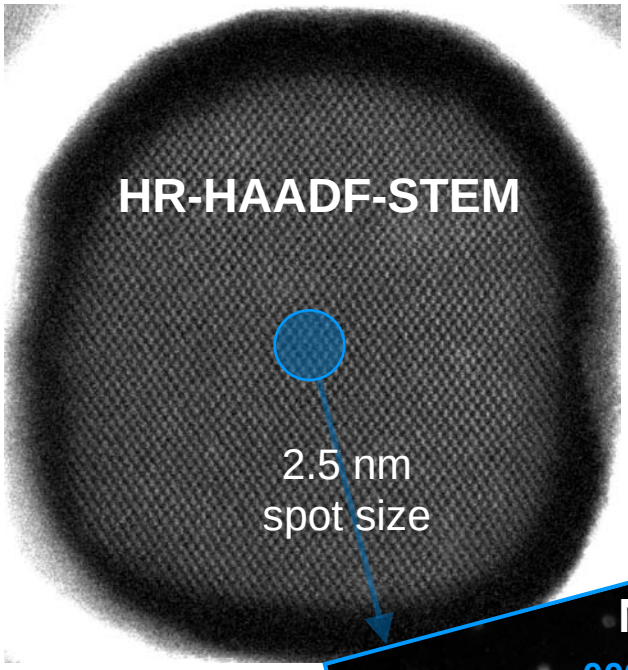
- **ϕ-FET structure** *C. Duprey et al., IEDM (2008)*

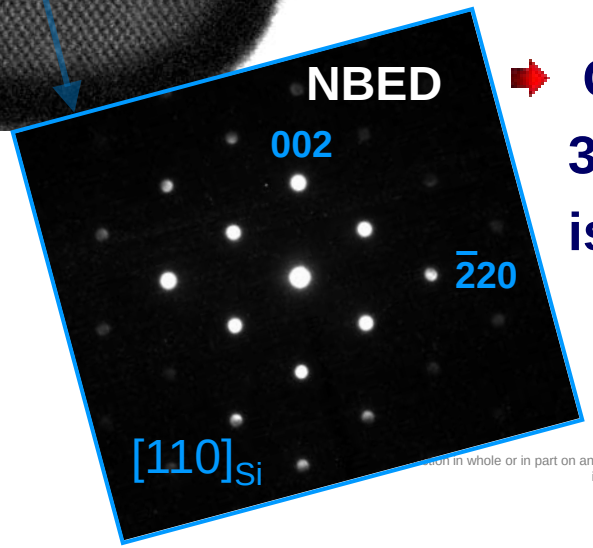
*Th. Ernst, this conf., invited*



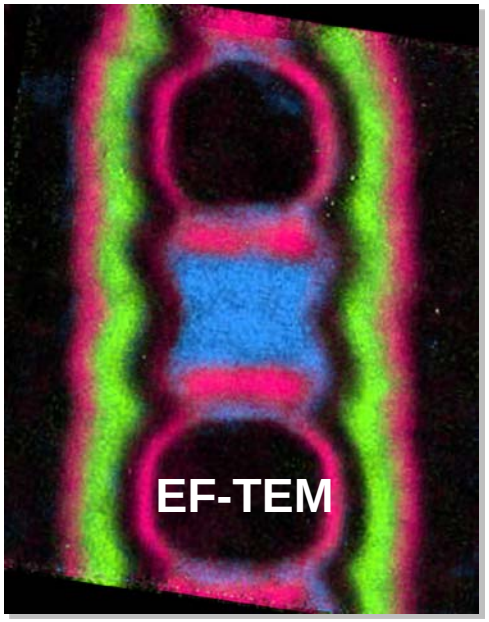

**Uppermost spatial resolution**




- **Orientation**
- **Strain**
- **Chemistry**

Ti O N

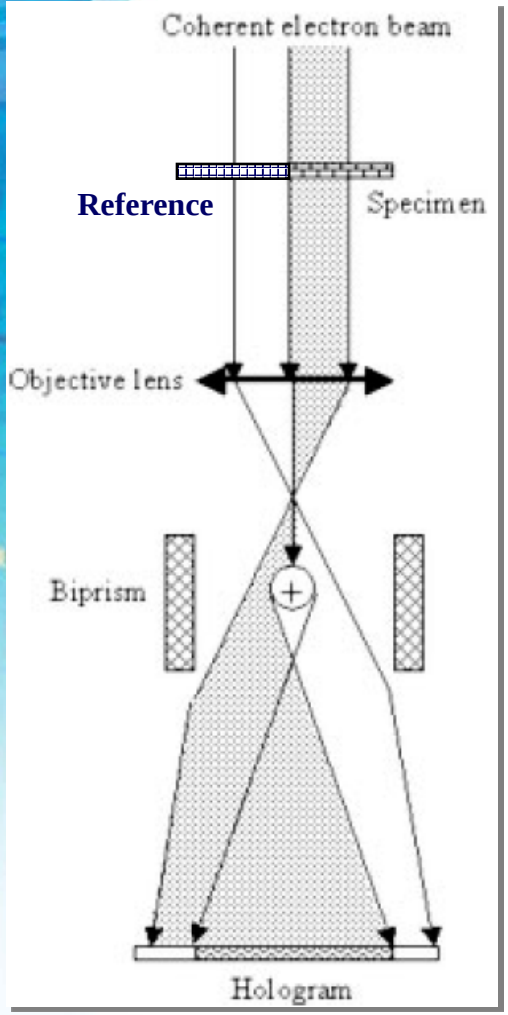



*Courtesy M. Jublot*

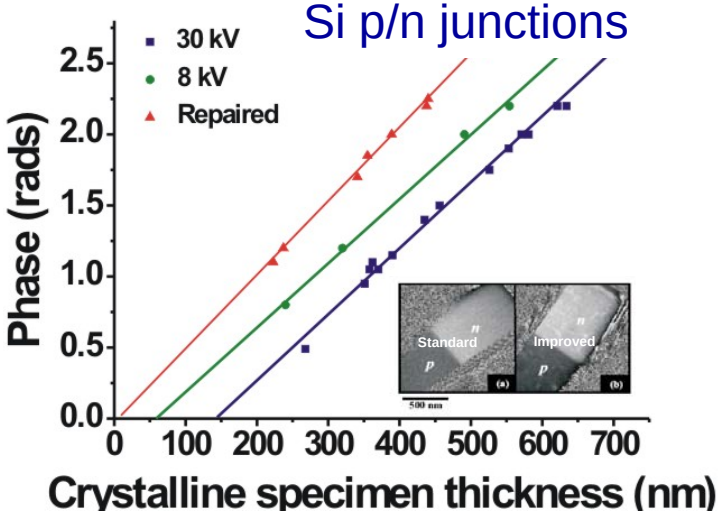
- **Conservative 3rd dimension is required**

# 2D information from electron microscopy

## Electron holography

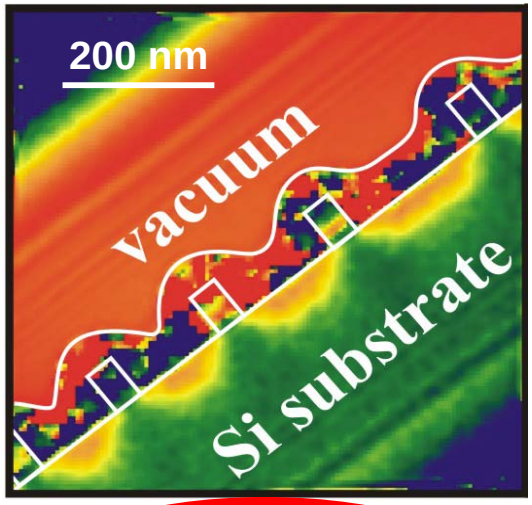



Si p/n junctions



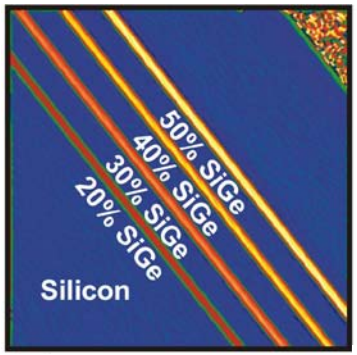

*D. Cooper et al., APL **93,** 183509 (2008)*

45 nm CMOS

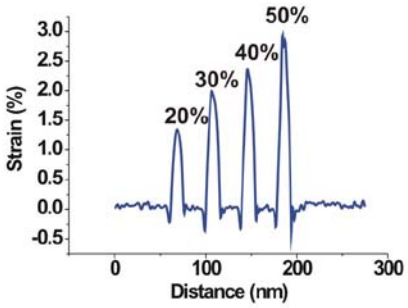



D. Cooper et al.
Poster TH-014

## Dark field holography




*Courtesy D. Cooper*

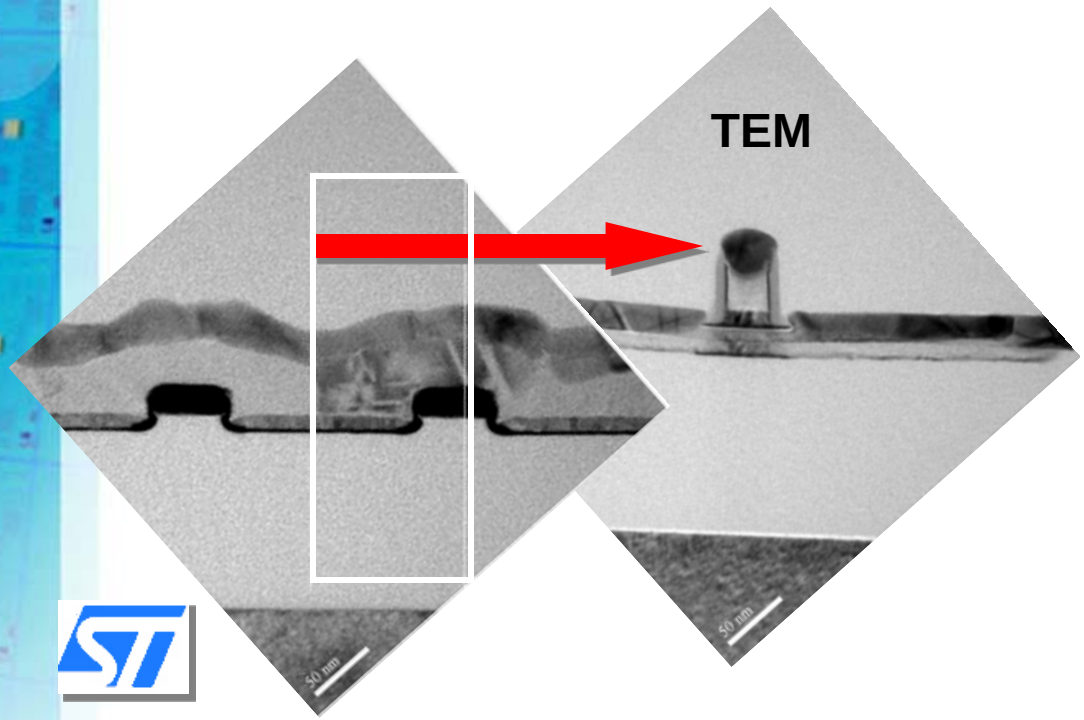


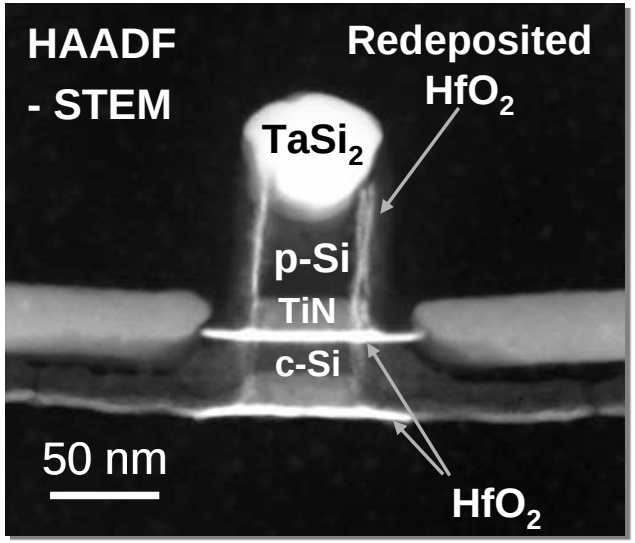

- **Conservative 3rd dimension is required**

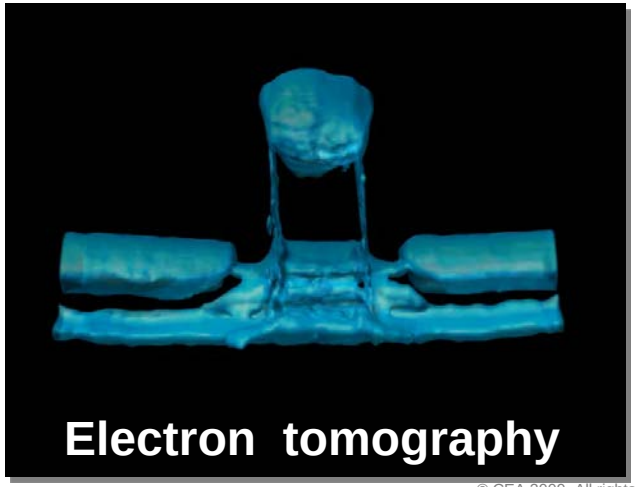
*More about dark field holo.: M. Hitch, this conf., invited*

# Non-conservative 3rd dimension case

- 50nm gate SOI device



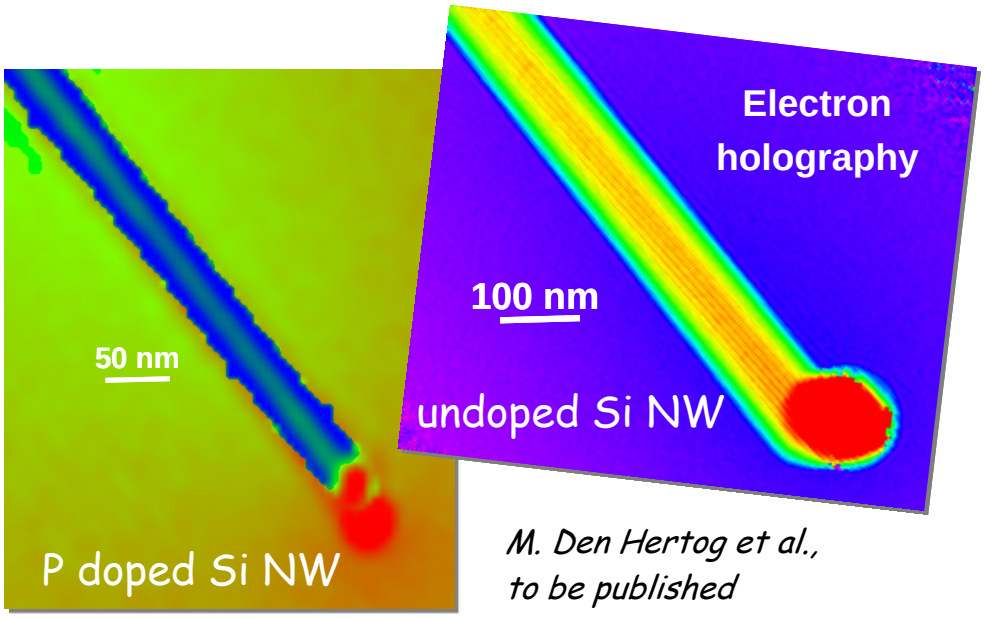



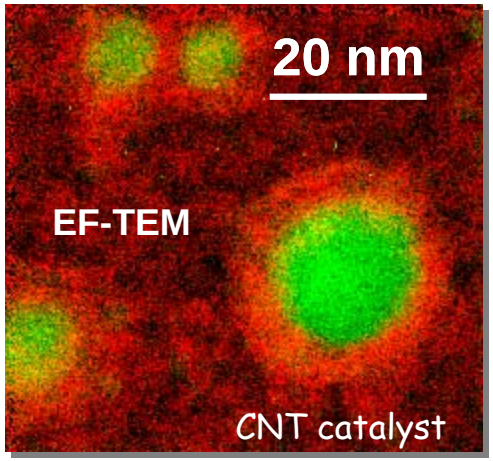

- **Full structure not identified by a unique view**
- **3D information required**

# Integration of nanomaterials

- Features of nanometer size **Wires, Dots, CNT,…**
- Bottom up approach **Self organization, catalysis,…**
  - Process improvement and control require **3D information**
  - Only **features** with no conservative dimension
  - **Needs down to atomic resolution**

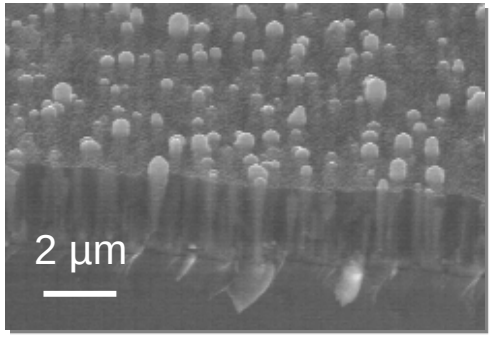



*M. Den Hertog et al., to be published*

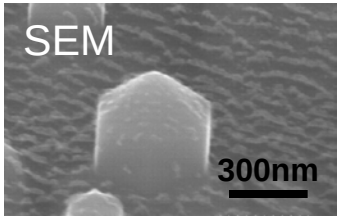


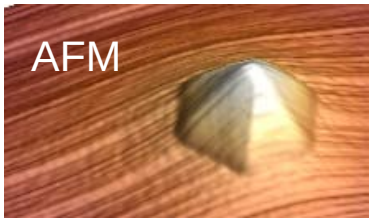

**Promising on isolated objects but still mainly qualitative**

# Beyond CMOS nanomaterial integration

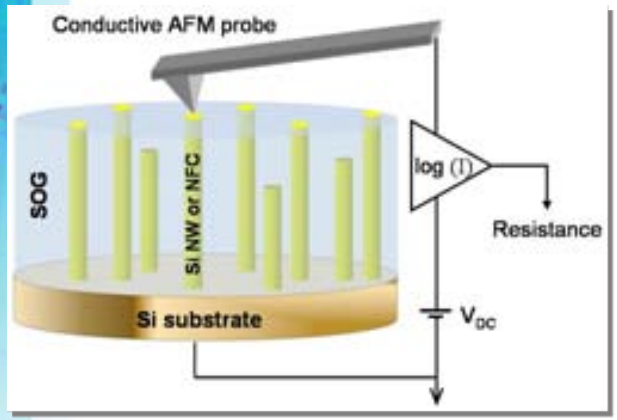



- Vertical ZnO NWs embedded in polymer

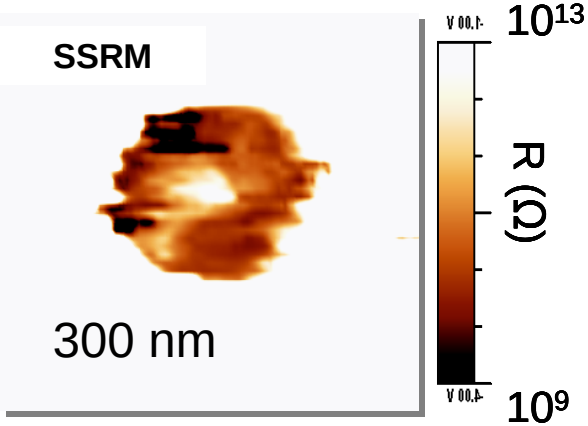


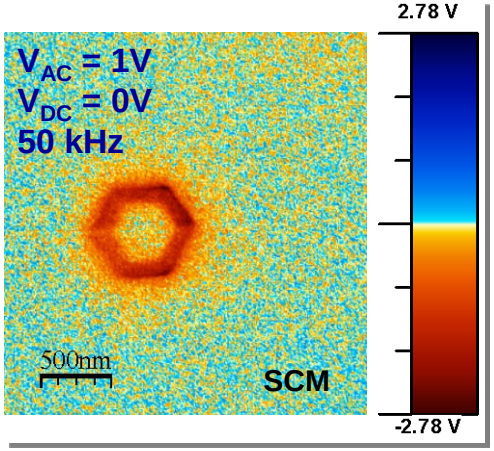




## Electrical Scanning Probe Microscopy




N. Chevalier et al.
Poster TH-020



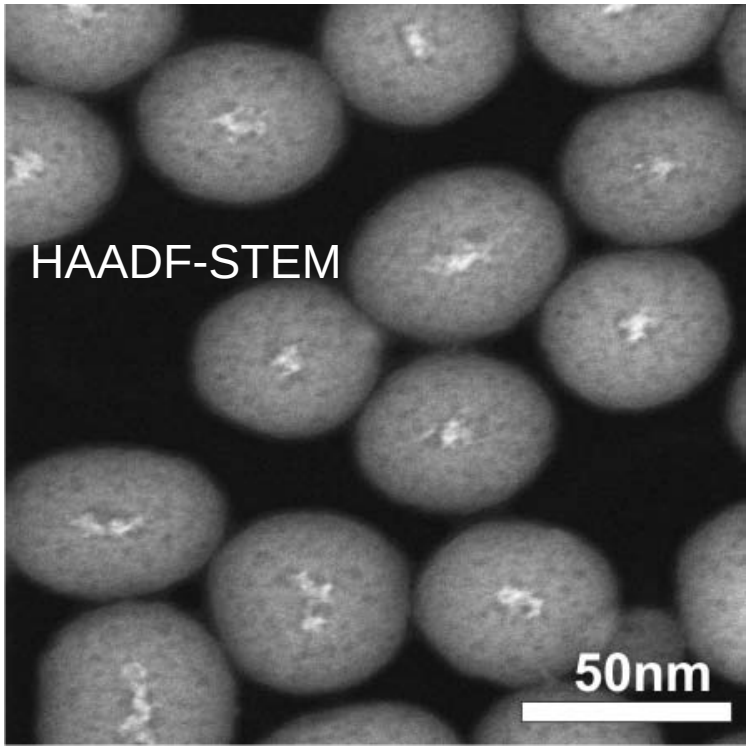




*E. Latu-Romain & al., EMRS (2008)*

➧ **Properties modification**

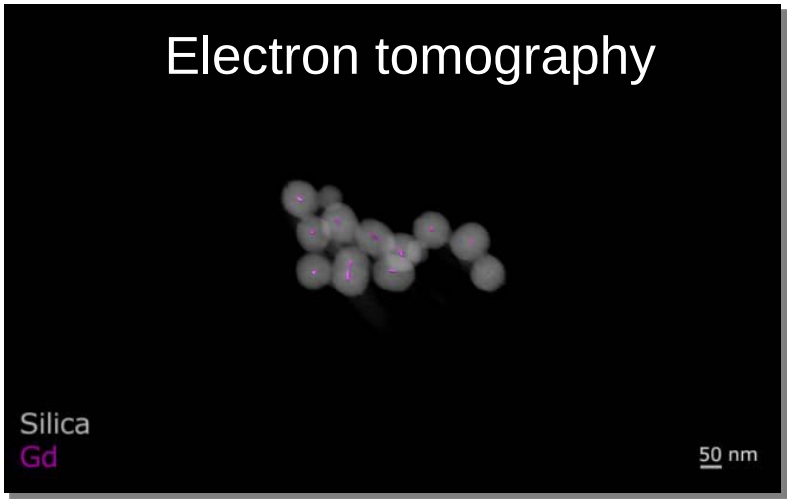
# Beyond CMOS nanomaterial integration

- **Gd inclusion in silica nanospheres**




**Where is the Gd cluster ?**

**Back projection of HAADF tilt series**

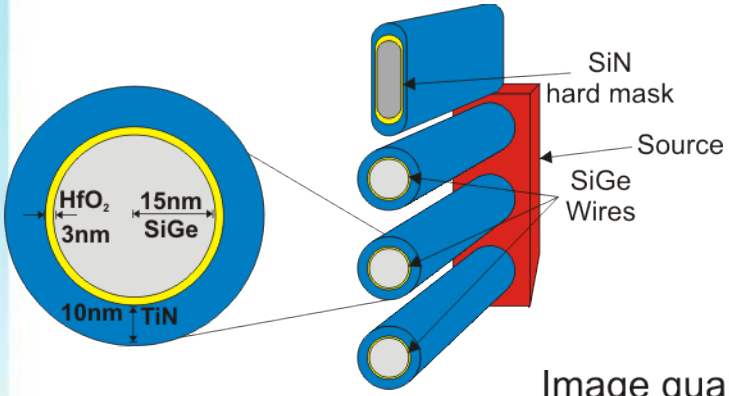



**3D observation mandatory even if isolated nanospheres**

# 3D for top down approach extreme CMOS

- **Gate-all-around (GAA) transistors**

Th. Ernst, this conf., invited




**Conventional preparation**

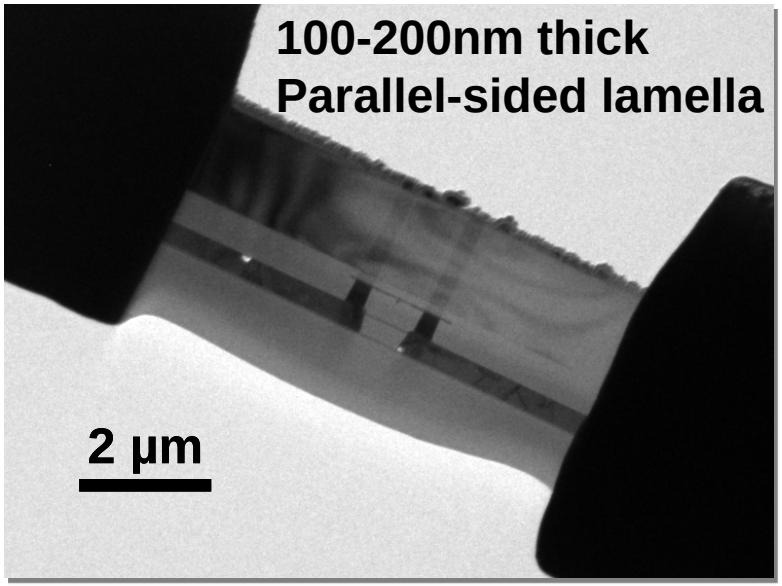
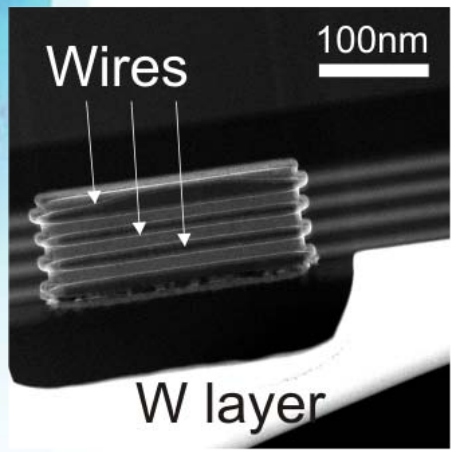
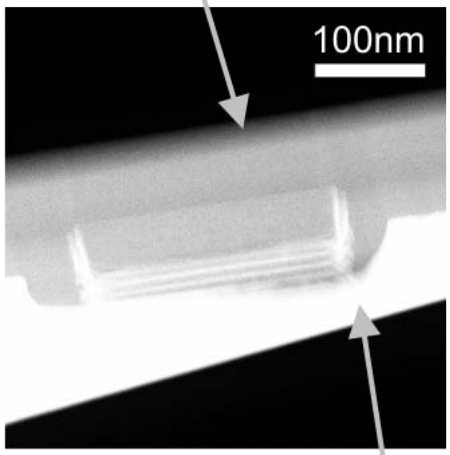



Image quality degradation



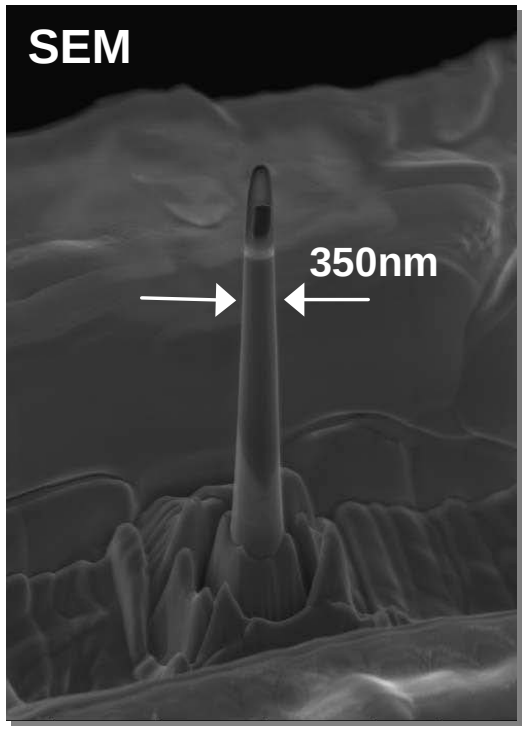

0° 60° Shadowing

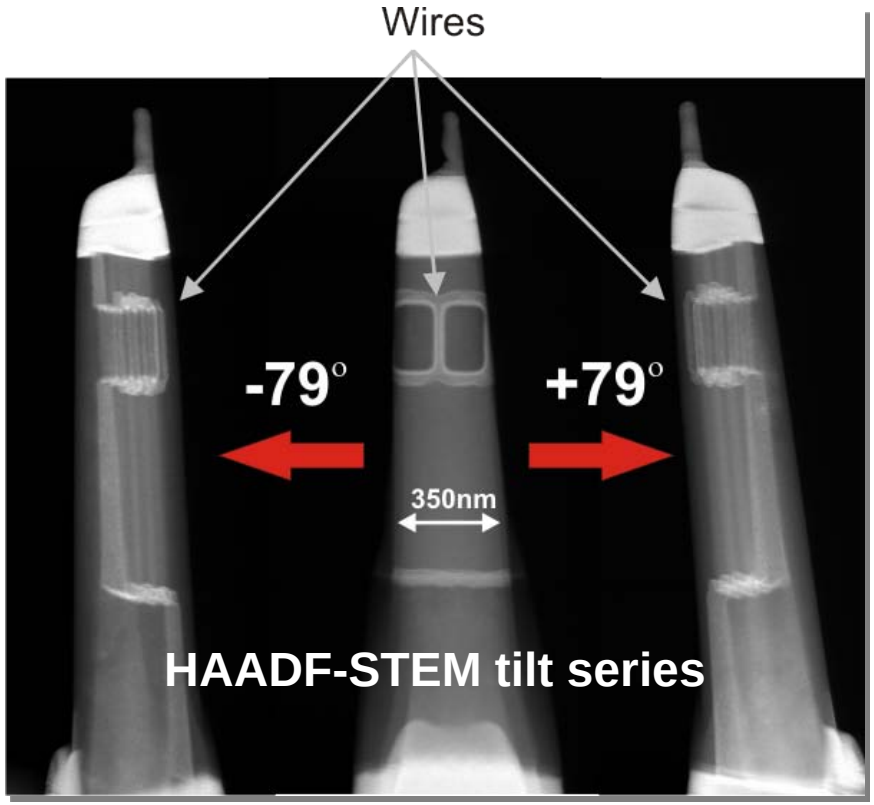
- **Thickness changes with tilt**
- **Shadowing at high angle**

# Specialized sample preparation for 3D

P. Cherns et al.
Poster TH-021

- Needle by FIB annular milling

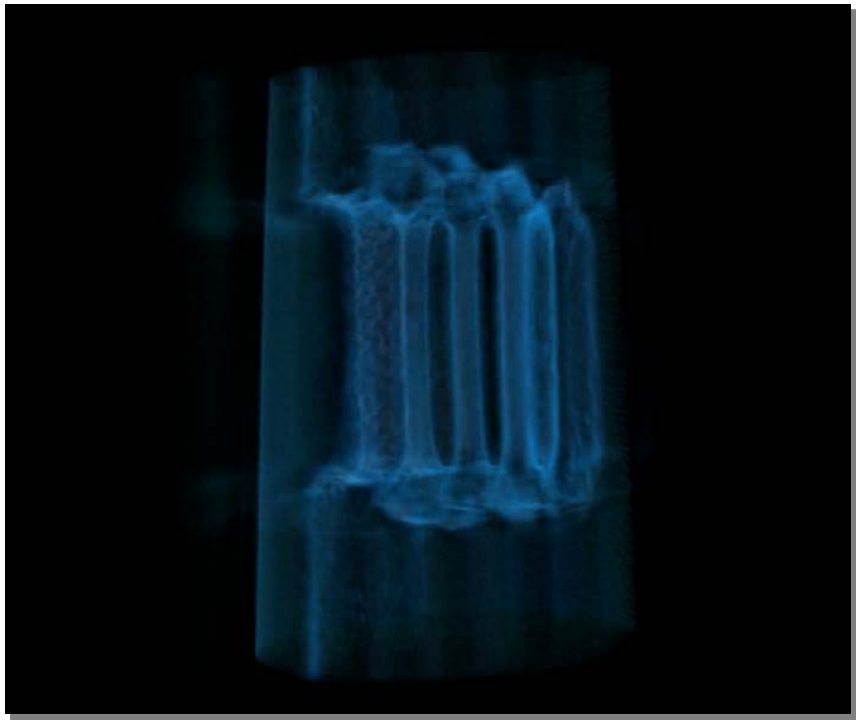


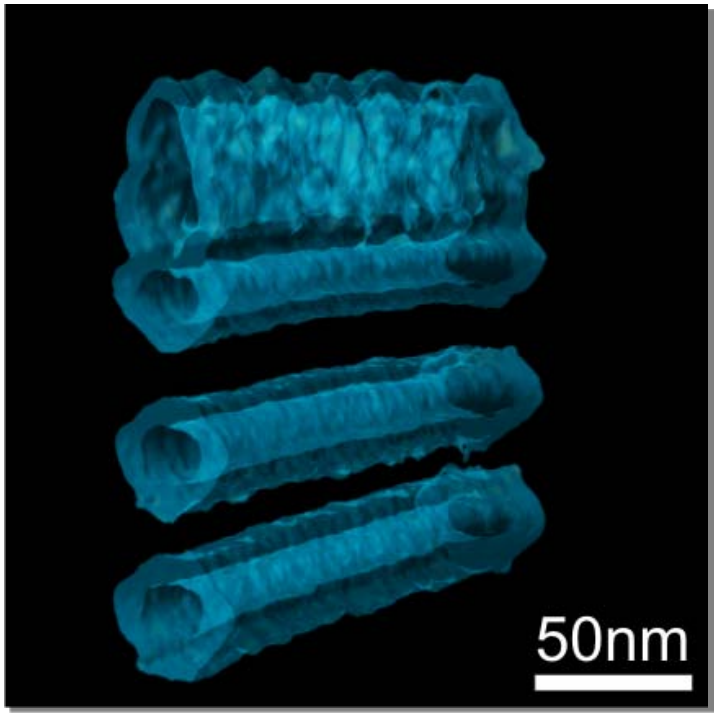




- **No thickness changes with tilt**
- **No shadowing over the full tilt range**

# 3D reliable information for GAA devices

- **Needle tomogram reconstruction by Weighted Back Projection**






**Boundaries of TiN layers**

- **Still some artifacts**
- **Quantification…**

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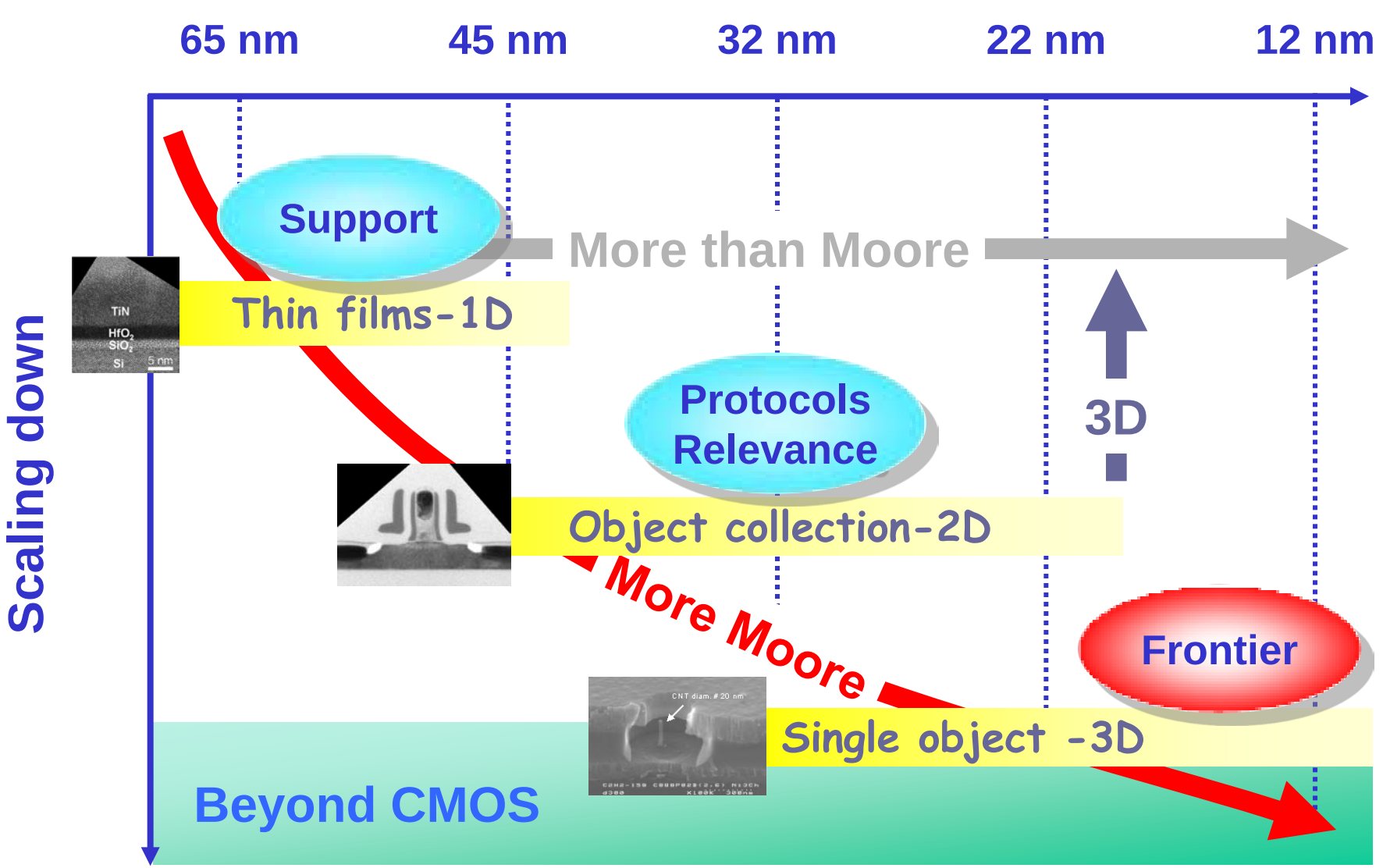
Poster TH-021

# Challenges in nanoscale characterization



# Aknowledgments


- A. Bailly
- J.-P. Barnes
- N. Barrett
- F. Bertin
- N. Bernier
- N. Bicaïs
- P. Bleuet
- A. Brenac
- P. Cherns
- N. Chevalier
- D. Cooper
- H. Dansas
- Th. Ernst
- F. Ferrieu
- F. Fillot
- P. Gergaud
- J.-M. Hartmann
- M. Jublot
- K. Kaja
- D. Lafond
- E. Latu-Romain
- W. Li Ling
- M. Lavayssière
- Ch. Licitra
- D. Mariolle
- E. Martinez
- A.-M. Papon
- F. Pierre
- O. Renault
- N. Rochat
- J.-L. Rouvière
- R. Truche
- ...

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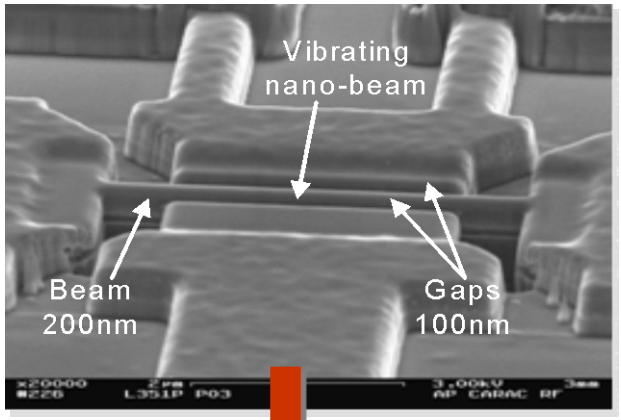
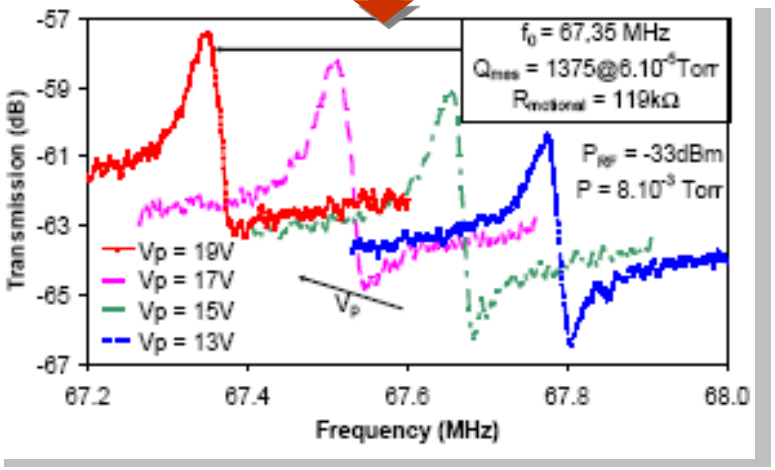
# What about NEMS ?

- **Dynamic properties**

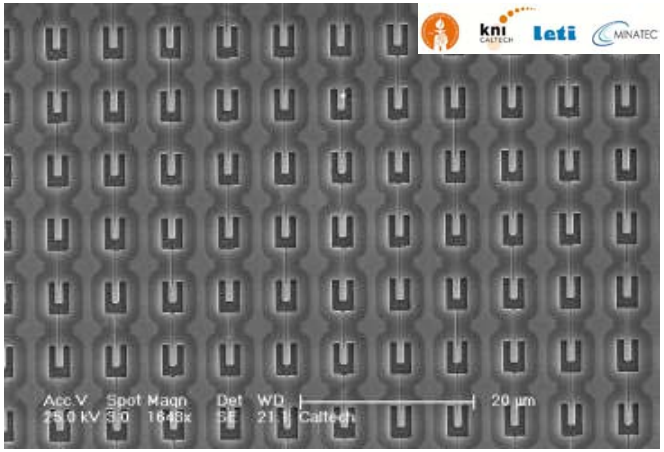



**Frequency vs. DC voltage**

- **After complete process**

- **NEMS VLSI**




- **Optical detection for MEMS**
- **Electron detection in a SEM for NEMS**

*S. Petitgrand and A. Bosseboeuf, J. of Micromech. and Microengin.**14**, S97-101 (2003)*

*M. Zalalutdinov et al., Appl. Phys. Lett. **77**, 3287 (2000)*