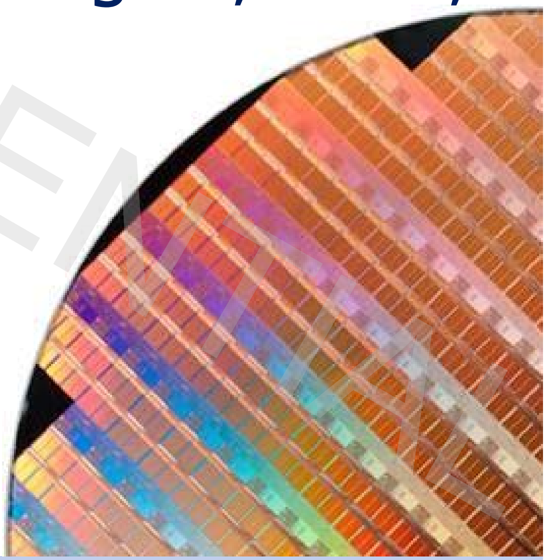
Characterization and Metrology Challenges for Emerging Memory Technology Landscape

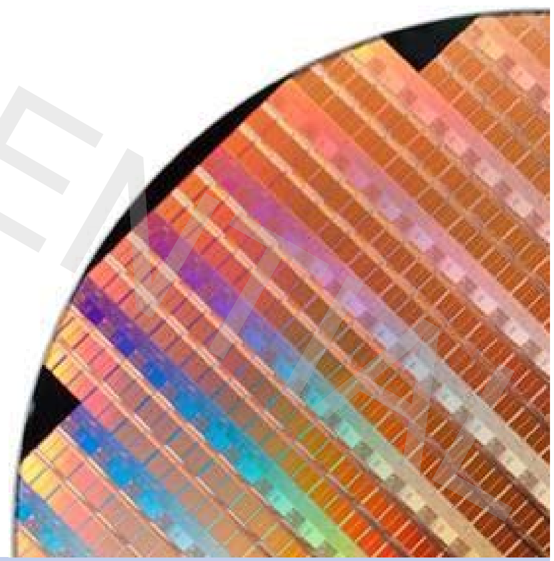
Naga Chandrasekaran, Steve Hues, Shifeng Lu, Du Li, and Chris Bishop

Process R&D
Micron Technology

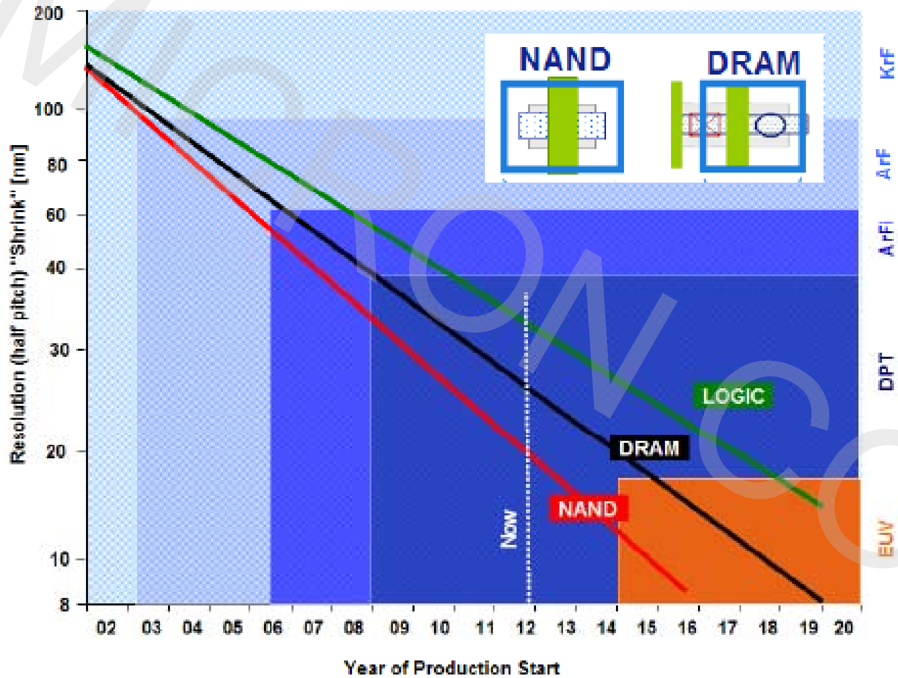


Presentation Outline

- Conventional Memory Scaling Trends
- Emerging Memory Technology Landscape
- Metrology and Characterization Challenges
- Opportunities
- Closing Remarks

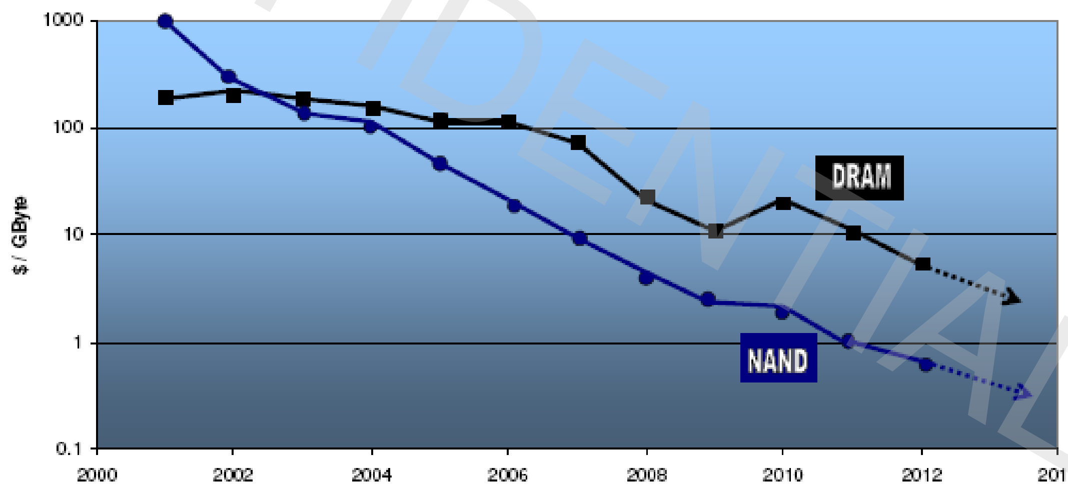


Memory Scaling Trends



- NAND followed by DRAM continue to drive minimum feature dimensions
- Increased density needs driven by applications

- NAND and DRAM market continue to be driven by race to reduce $/GB



Source: Yoon & Tressler, 2012 Flash Summit

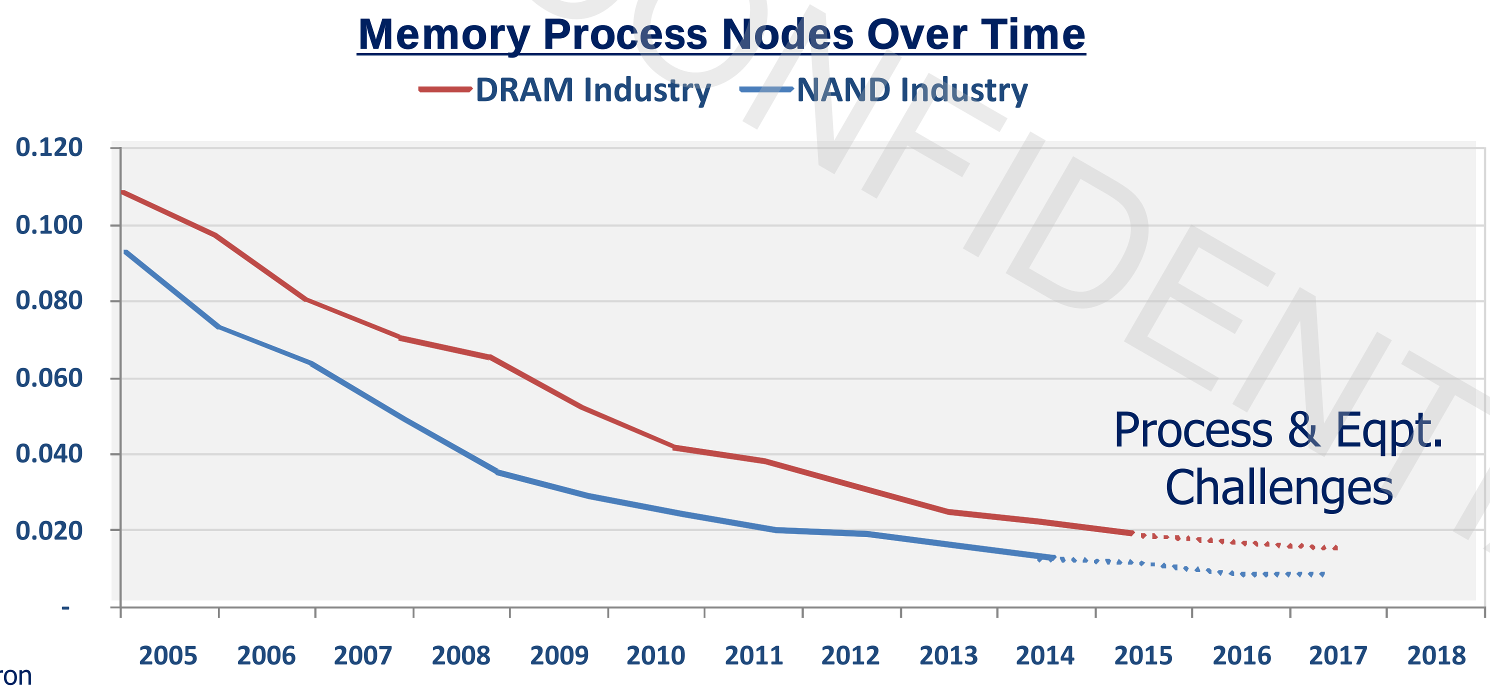
Major Challenges to the Longevity of DRAM and NAND Scaling

Endurance
- Cycling capabilities

Shrink
- Physical limitations

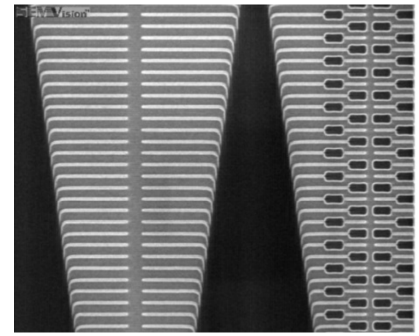
Equipment capability
- Increasing equipment complexity

Cost
- Path of diminishing returns

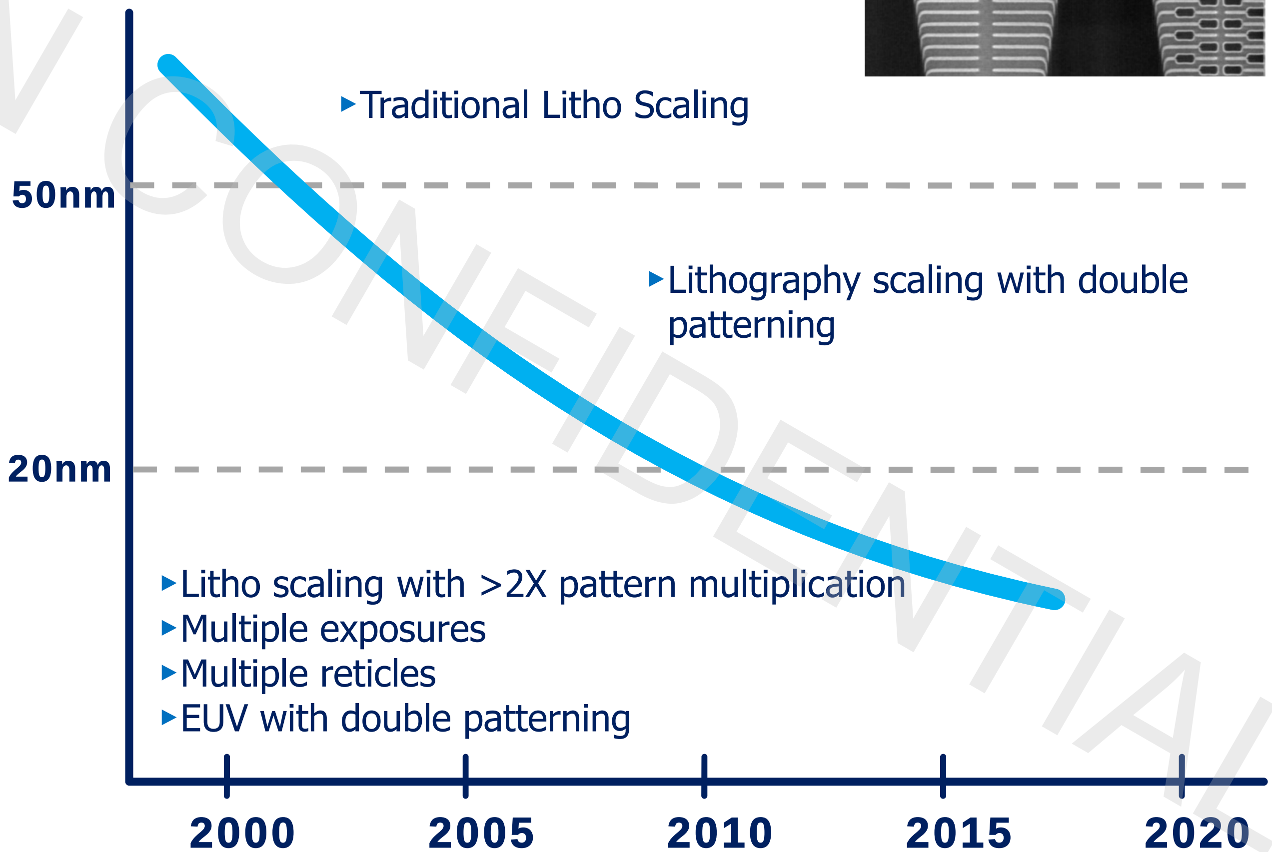


Source: Micron

Resolution is not "the" primary gating item limiting scaling

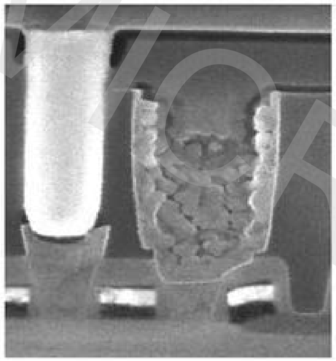


- Sub 20nm Lithography Enabled by Fab and Photomask complexity
- Cost structure more a question than pure capability
- **Challenges:**
  - Process margins – overlay, CDU, LWR
  - Materials challenges
  - Metrology challenges

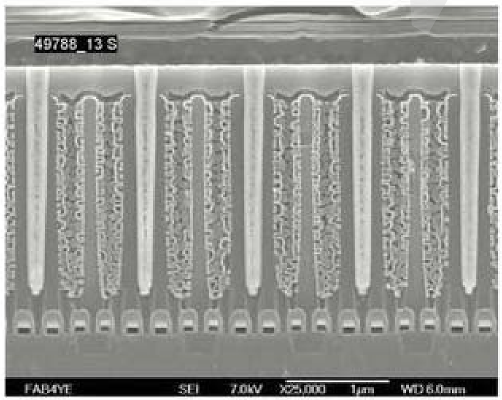


Source: Micron

DRAM Scaling Challenges



Simple structures and materials



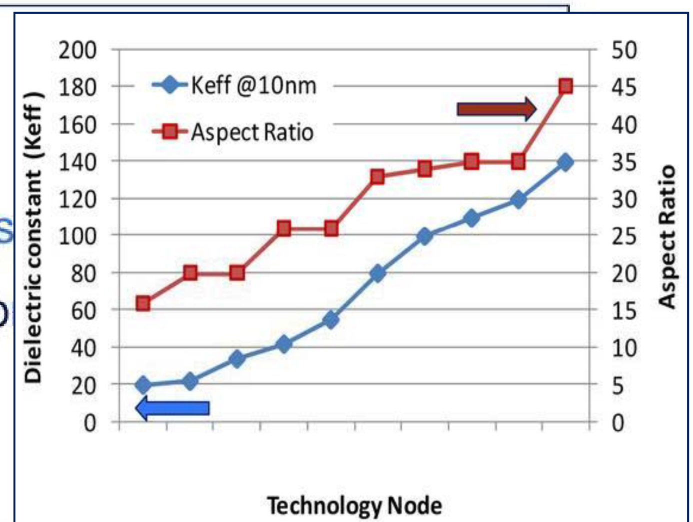
Structures getting complex but manageable AR and materials development

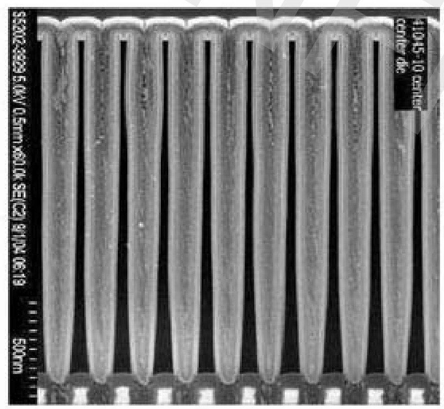
Structural Integrity

- 3D Integration
- Huge Aspect Ratios

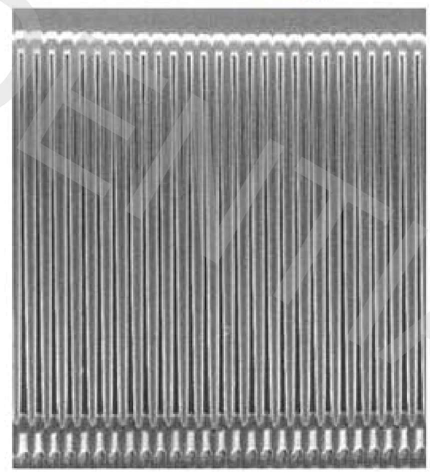
New Materials Develop

- Electrodes
- Dielectrics





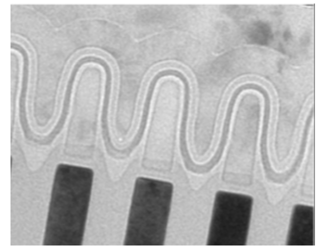
Advanced Materials & Processing

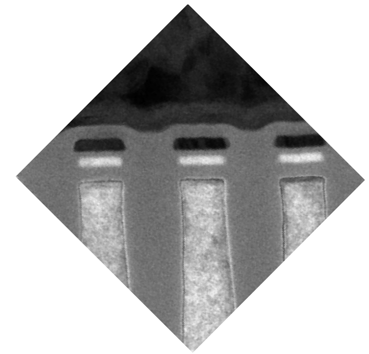


DRAM scaling will be limited by capacitor challenges. Capacitor technology will demand new materials.

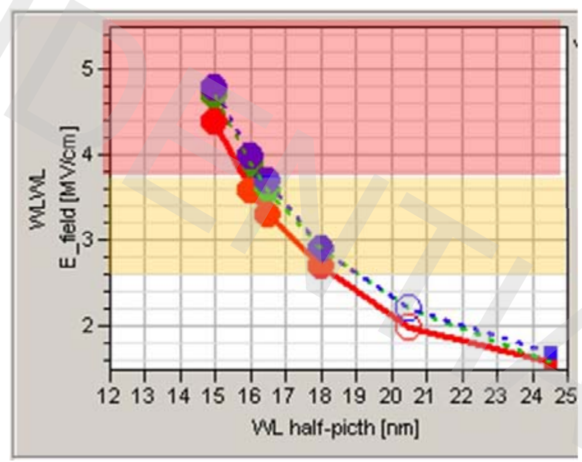
NAND Scaling Challenges

Floating Gate (wrap around or planar), continues to face scaling challenges with unanswered questions about sub-1X scaling





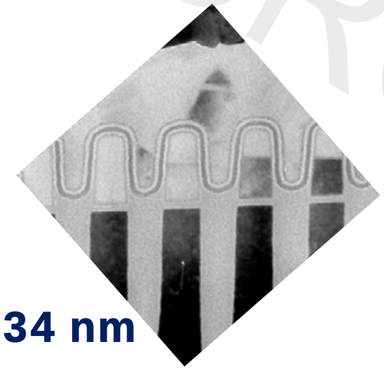
Even if physical limitations are resolved, reliability of such devices is a challenge 1xnm NAND technology node is challenged by >50% interference, E-fields at breakdown limits, & disturb issues



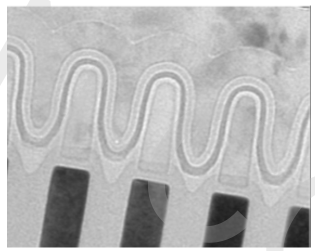
Vertical Scaling – Path to NAND Scaling

Planar NAND – Continued Leadership Position

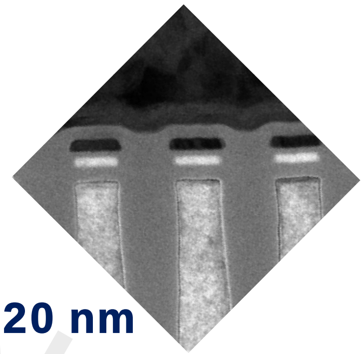
Transition from floating gate to charge trap based technology



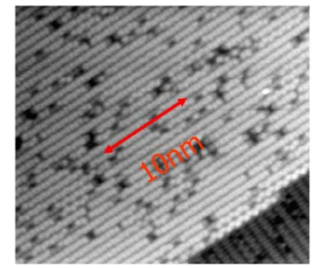
34 nm



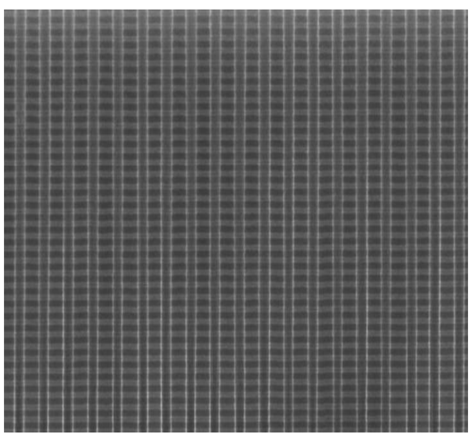
25 nm



20 nm



1X nm

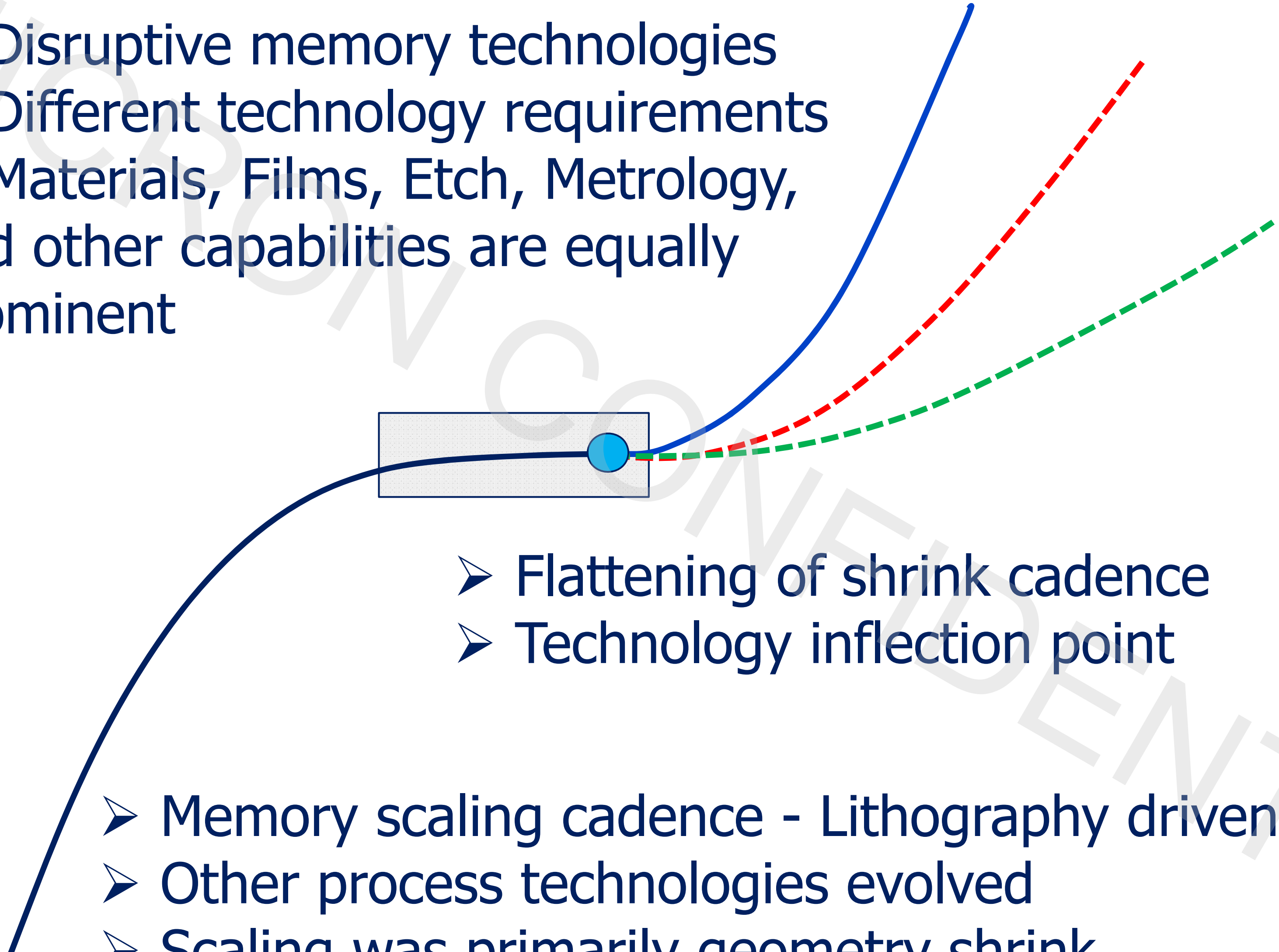


<u>Vertical NAND:</u>

- **Not limited by lithography**
- **Complex etch and deposition**
- **Complex metrology requirements**
  - **IR range**
  - **Registration challenges**
  - **Defect detection**
  - **Hidden features measurement**

Technology Inflection Point

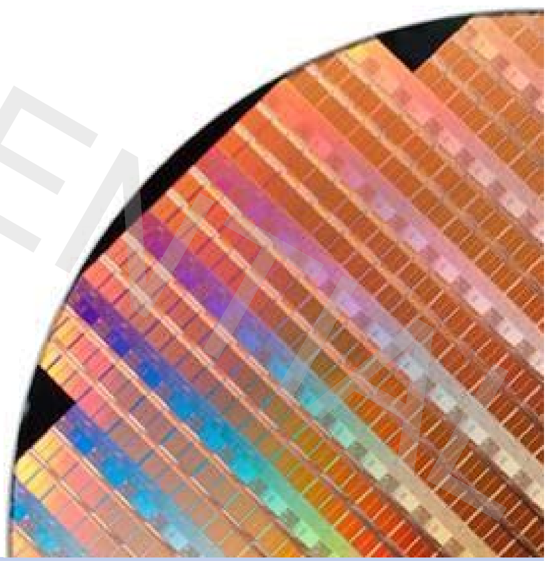
- Disruptive memory technologies
- Different technology requirements
- Materials, Films, Etch, Metrology, and other capabilities are equally prominent



- Flattening of shrink cadence
- Technology inflection point

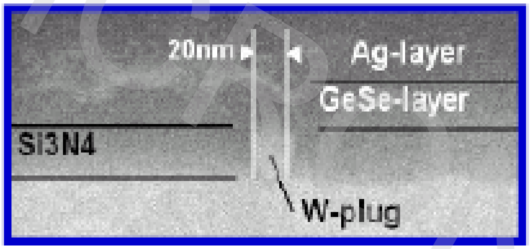
- Memory scaling cadence - Lithography driven
- Other process technologies evolved
- Scaling was primarily geometry shrink

Emerging Memory Trends



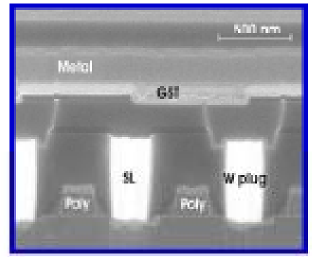
Alternate Memory Concepts

CBRAM

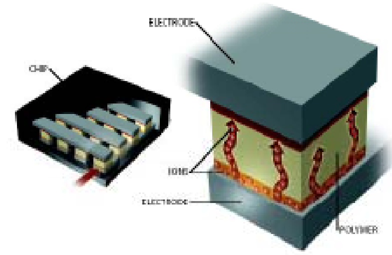


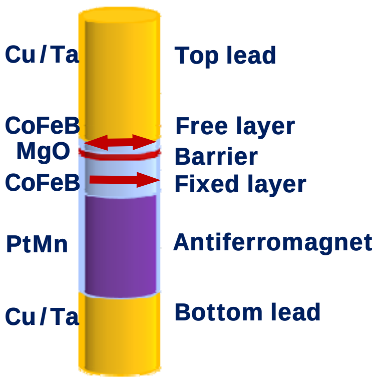
FERAM

PCM

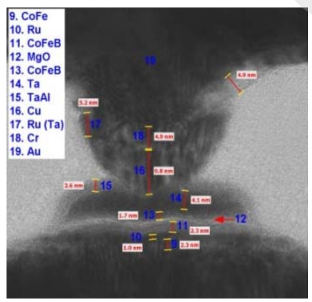


Polymer RRAM

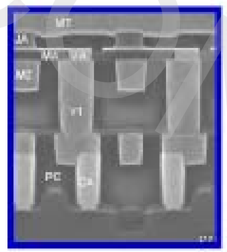




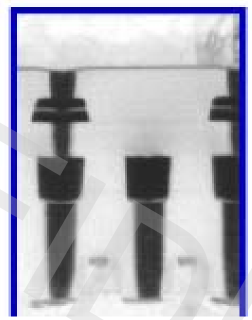
STT-MRAM



MRAM

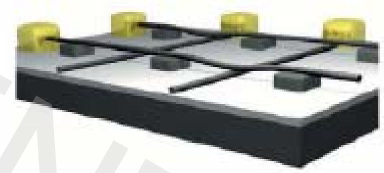


MOx-RRAM



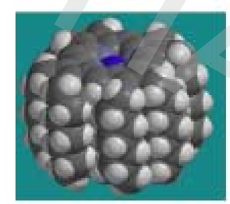
Polymer FeRAM

CNT



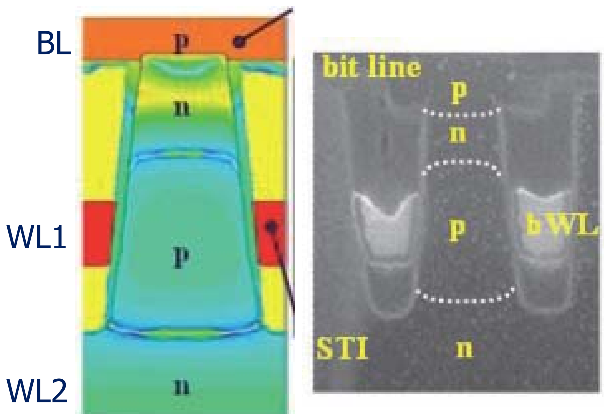
Explosion of new memory concepts with new materials, storage concepts, and materials technology

Molecular



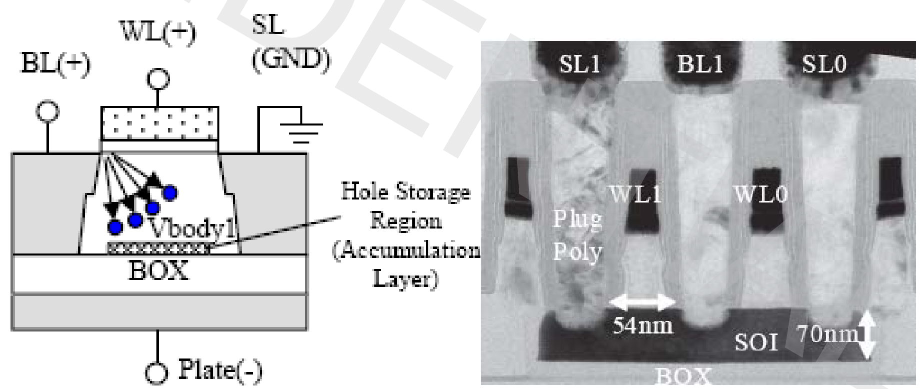
Capacitorless DRAM Structures:

- Capacitor-coupled Thyristor
- P+ cathode (BL); n+ anode (WL)
- Three junctions – two critical
- Capacitor: “p-base” – Gate
- No exotic materials
- Vertical structure of interest



Qimonda, VLSI Tech 2009

- Floating body (FB) MOS Transistor
- FB = Storage Node
- No exotic materials
- Vertical structure of interest



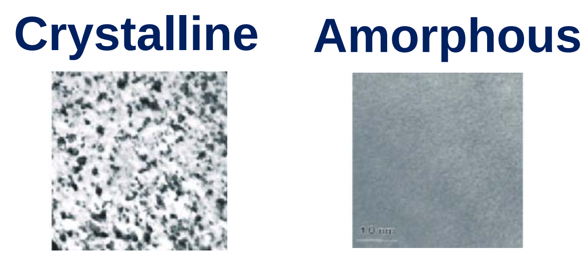
Hynix, VLSI Tech 2009

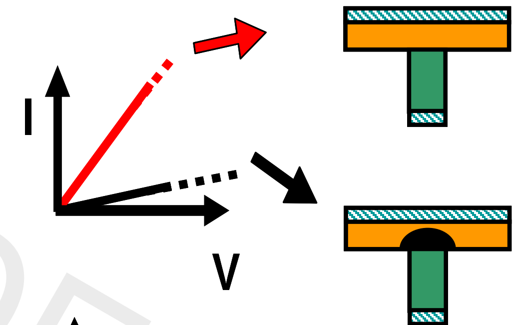
Phase Change Memory Operation

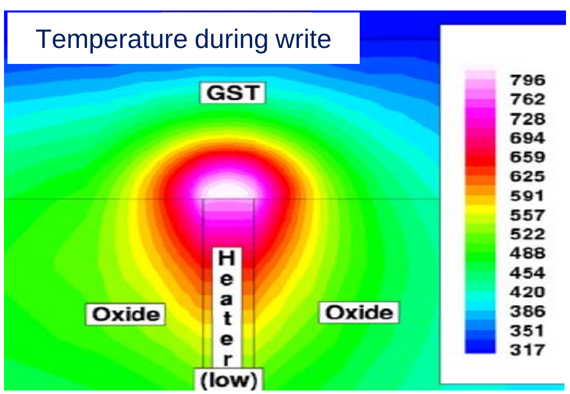
Storage
- GST: Germanium-Antimony-Tellurium Chalcogenide glass
- Cell states varying from amorphous (high resistance) to crystalline (low resistance) states

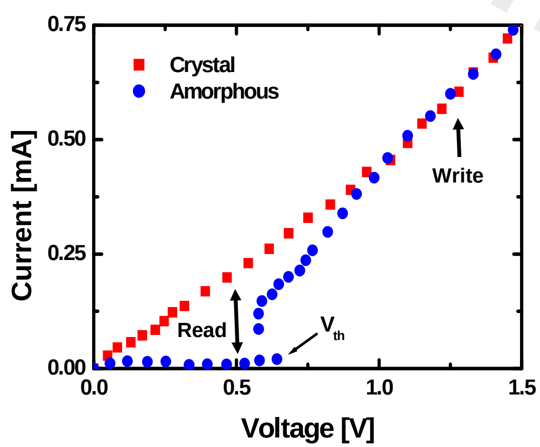
Read Operation
- Measure resistance of the GST

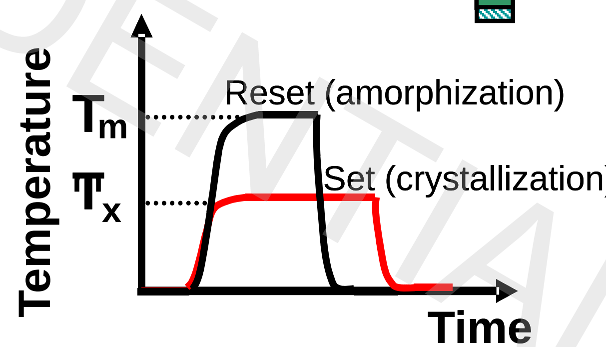
Write Operation
- Heat GST via current flow (Joule effect)
- Time at temperature determines cell state





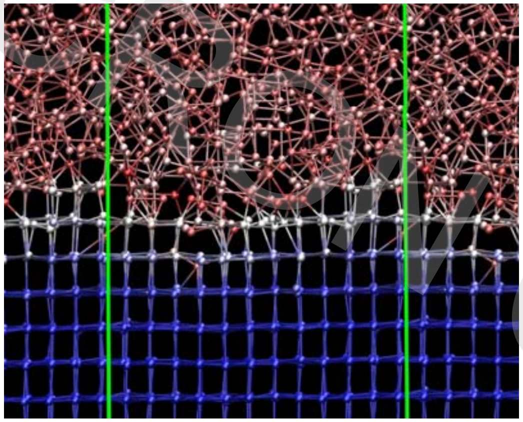




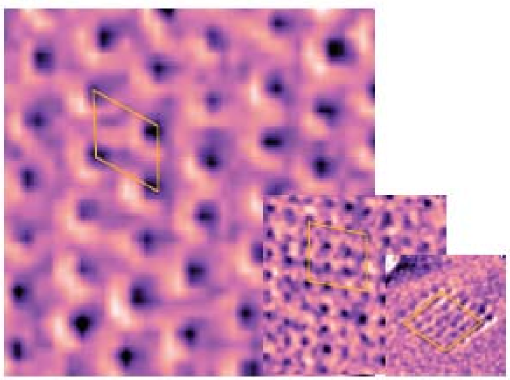


Phase Change Memories Do That !

Amorphous/crystal interface: GeTe



Courtesy of M.Bernasconi,
University of Milan - Bicocca



Crystalline Bits in Amorphous Matrix.

C. Lam, SRC NVM Forum 2004

1750 atoms

GeTe(001) surface

Interface energy

σ = 0.10 J/m^2 (001)

σ = 0.20 J/m^2 (111)

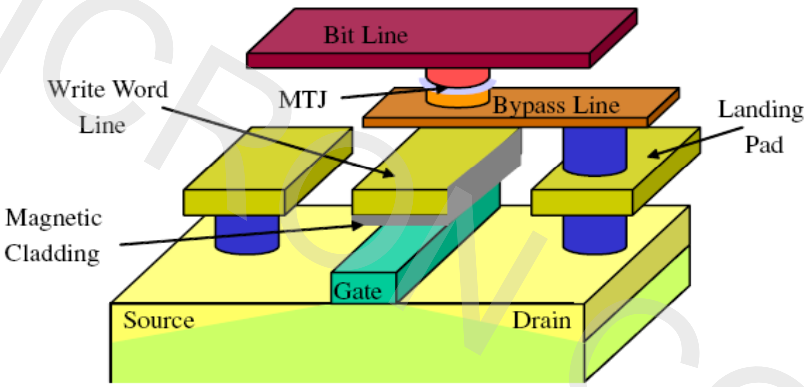
Amorphous vs crystal energy

$\Delta E_{\alpha\text{-}c}$= 110 meV/atom

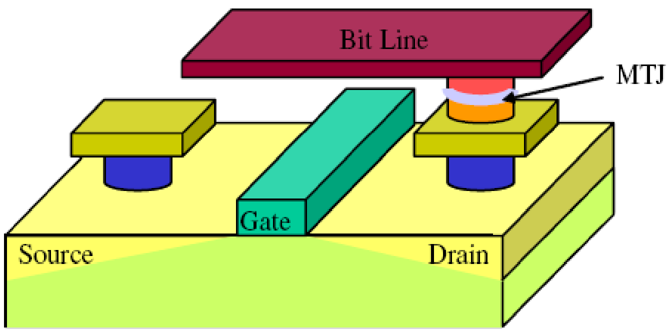
Phase change mechanism appears scalable to at least ~5nm

Need to characterize the amorphous - crystalline interface and phase transitions with accuracy

MRAM vs. STTRAM



MRAM

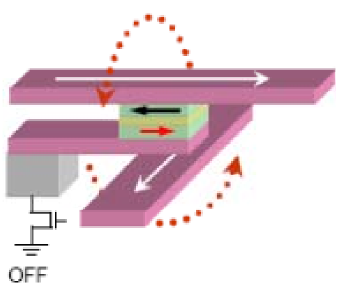


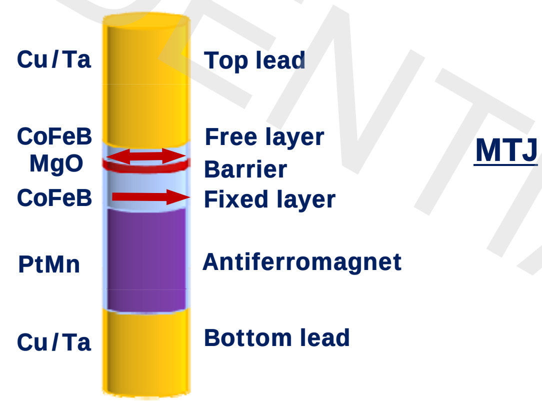
STTRAM

<u>Scaling issues:</u>

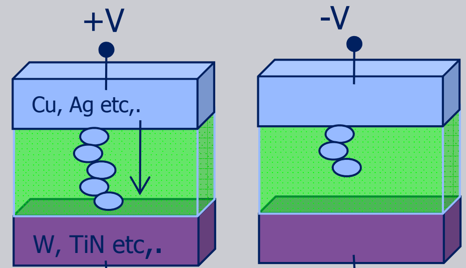
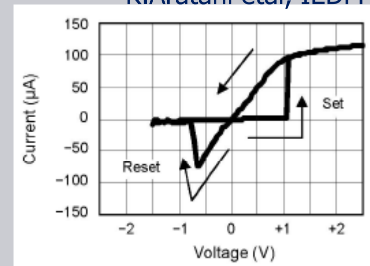
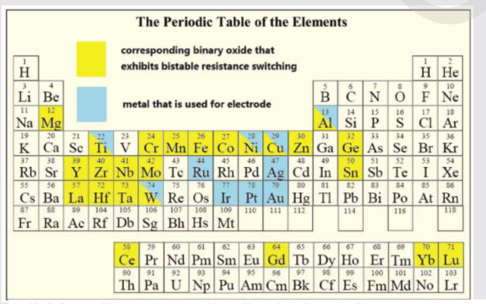
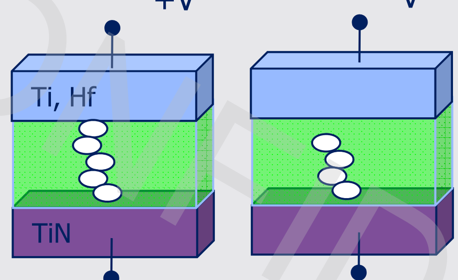
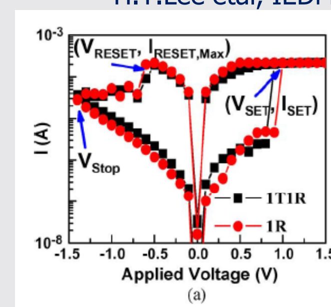
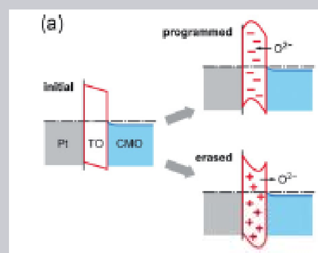
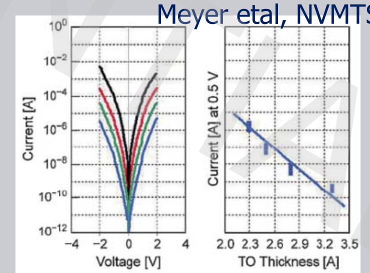
- Exponential increase in write current to achieve same magnetic field
- Read and write disturb

Current pulses of opposite polarity switch the magnetic tunnel junction between high and low resistance states





RRAM Options

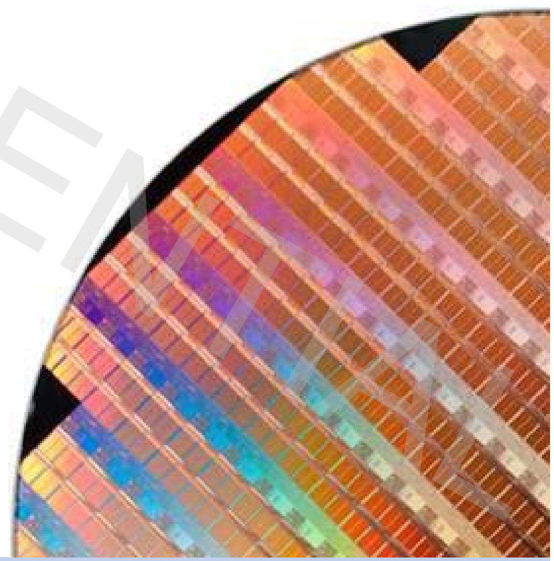
RRAM	Material Systems	Switching mechanism	Comments
RRAM-M	Cu/GdO_x Ag/SiO_2 Ag/GeS	 Metal Filament in Electrolyte	K.Aratani etal, IEDM 2008  Ion/Ioff ~ 1000
Bipolar RRAM-Ox	Ti/HfOx, Ti/ZrOx  By H.-S. Philip Wong, Fellow IEEE, Heng-Yuan Lee, Student Member IEEE, Shimeng Yu, Student Member IEEE, Yu-Sheng Chen, Yi Wu, Pang-Shiu Chen, Byoungil Lee, Frederick T. Chen, and Ming-Jinn Tsai	 Oxygen vacancy filament in dielectric TiOx, ZrOx, TaOx etc,.	H.Y.Lee etal, IEDM 2008  Ion/Ioff ~ 10
RRAM-MVO	Mixed Valence Oxides SrTiOx, PCMO etc,.	 Uniform oxygen movement	Meyer etal, NVMTS 2008  Ion/ Ioff ~10

Emerging Memory Landscape

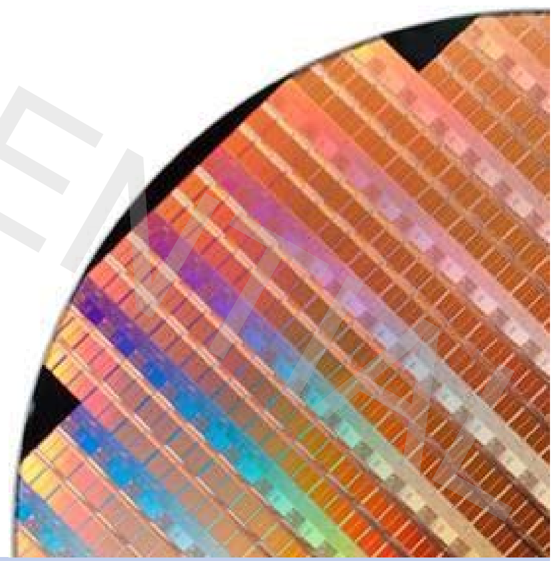
- *Several new emerging memory technologies under development*

- *Innovators Dilemma: Identify niche market segment needs that cannot be met by conventional memory alone*

- *Emerging Memory operating mechanisms are highly dependent on*
  - *Materials engineering*
  - *Precise control of stoichiometry*
  - *Complex materials stack*
  - *Controlling material states*



Characterization Challenges



Characterization Challenges

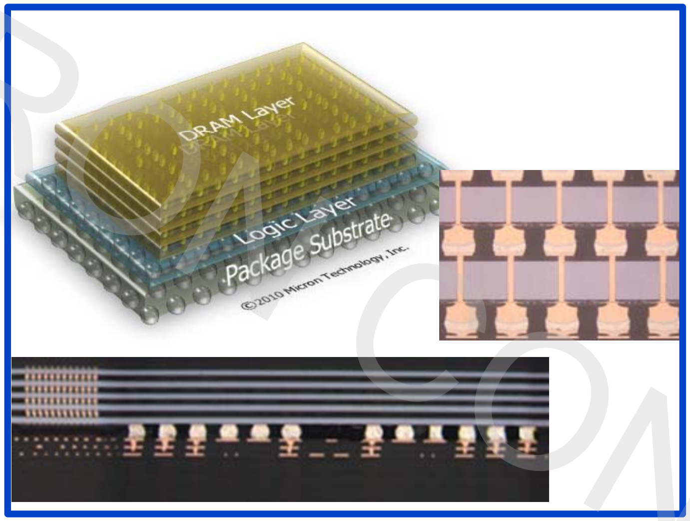
- **Characterization (Metrology) in Emerging Memory landscape can be broadly classified into three buckets**
  - Structural characterization challenges
  - Material characterization challenges
  - Defect inspection challenges

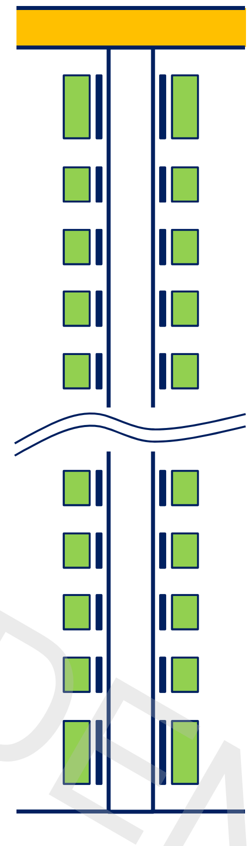
- **As device dimensions decrease, the volume (number of atoms) available for analysis are reduced to the point where the intensity from each atom becomes critical**

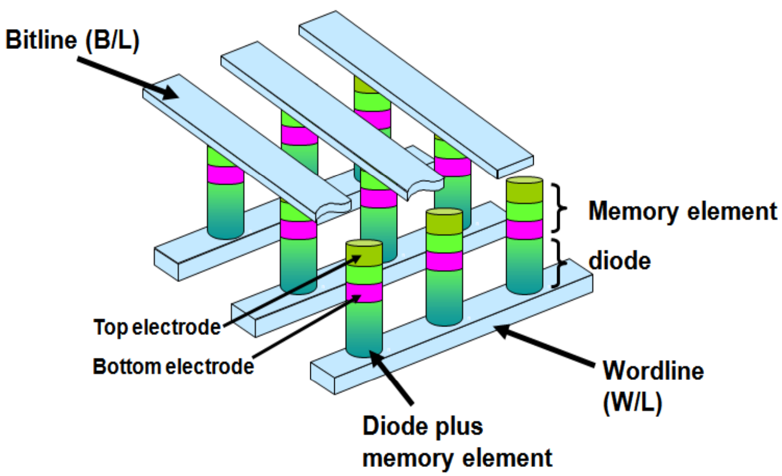
- **New memory operating mechanisms (state change in materials) present constraints on techniques that can be used to characterize such materials**

Memory Transitions to 3-D

TSV and 3DI

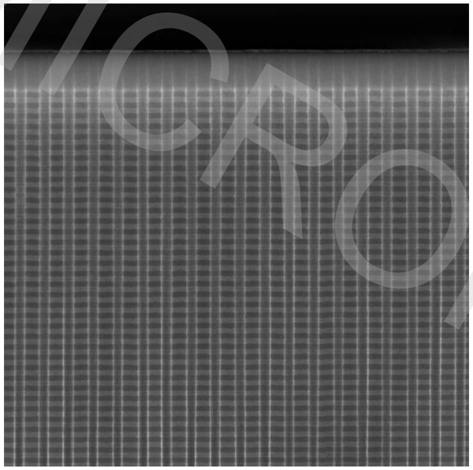




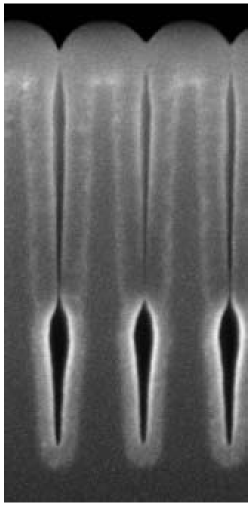


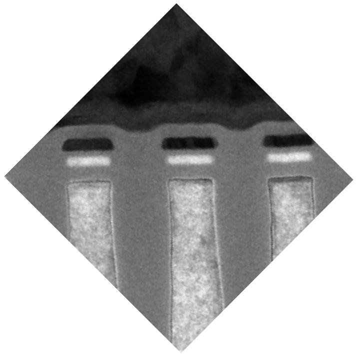
Unique Metrology and Inspection Challenges…

Complex Structural Challenges



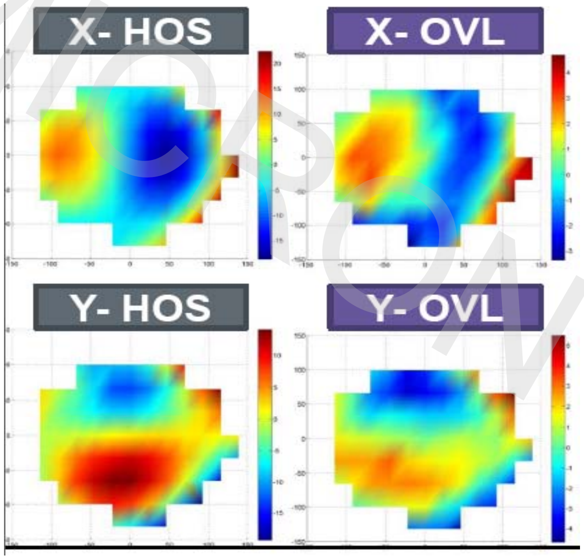
- ➢ Recess measurements
- ➢ Top, Bottom CD, Profile
- ➢ Defect visibility and sensitivity
- ➢ Thick layers: Transition to IR
- ➢ Registration concerns



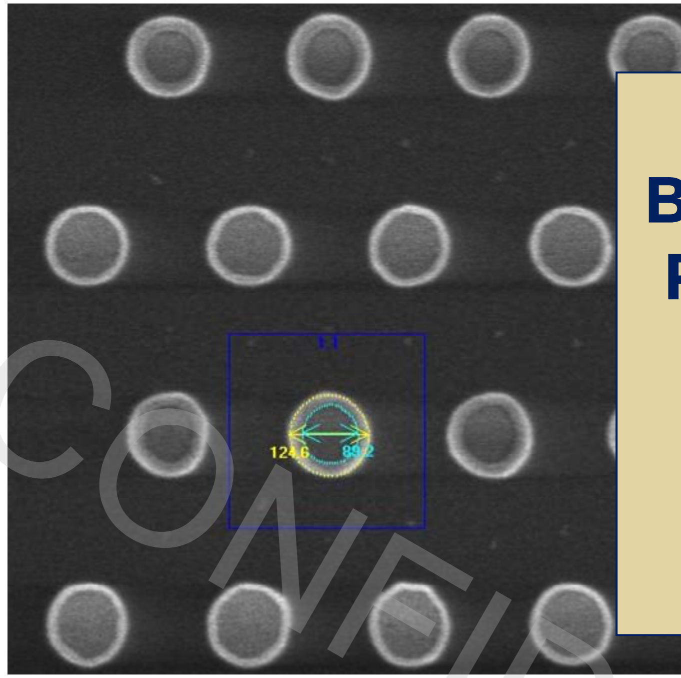


- ➢ Hidden (or) buried structures
- ➢ Multi layer stack - Optical gap
- ➢ High Aspect Ratio measurement
  - ➢ CD and Profile
- ➢ Optical CD – Time to Solution

Complex Structural Challenges

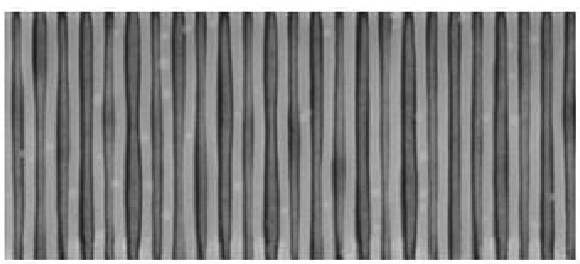


Wafer shape engineering



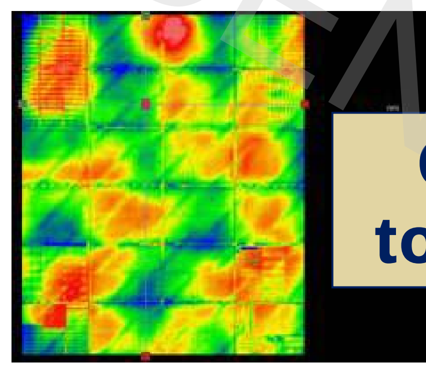
Top CD + Bottom CD and Profile in HAR Structures

Time to OCD Solutions



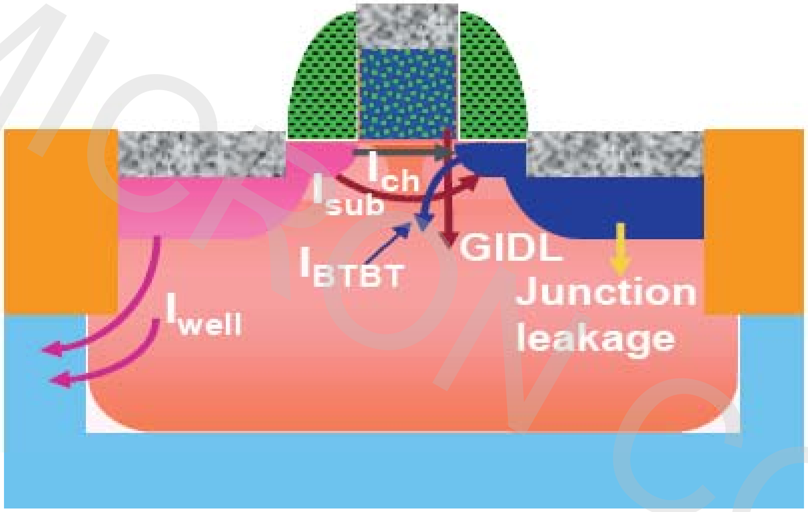
Structure bending

Film Stress Engineering

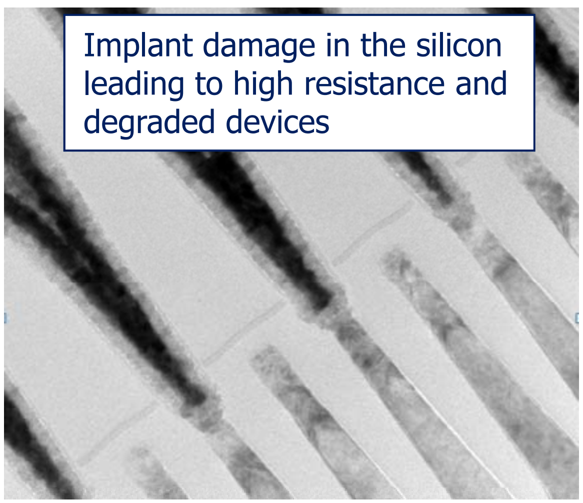


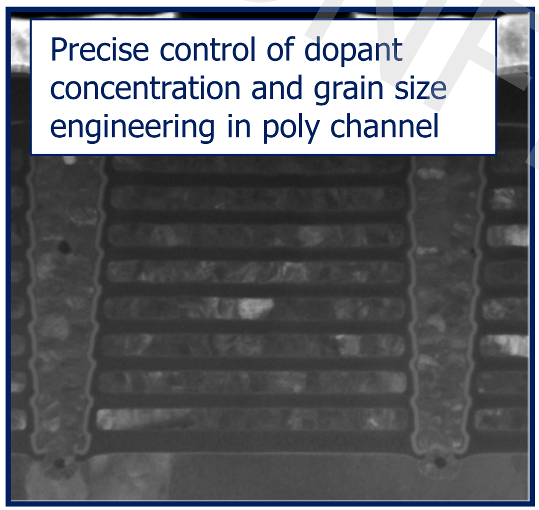
Complex topography

Device Technology Scaling



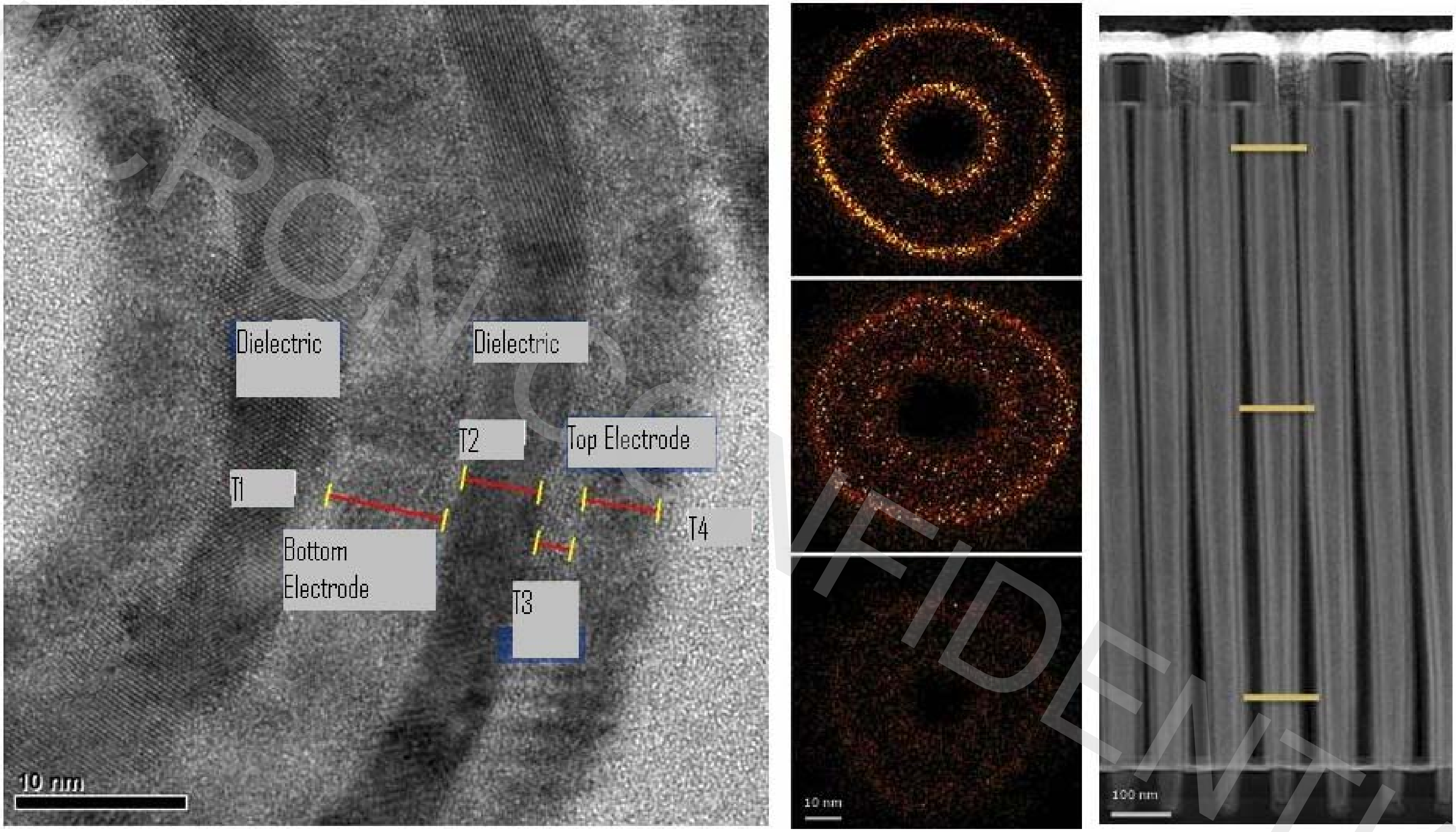
- Implant damage
- Contact resistance
- Dopant Profile Control
  - As implanted profile
  - Post thermal treatment





Requirements drive advanced SIMS technology to enable precise dopant engineering

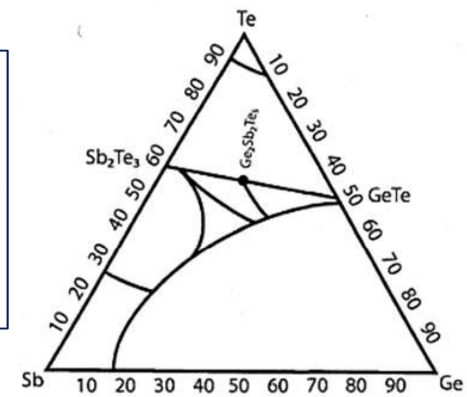
Transmission Electron Microscopy



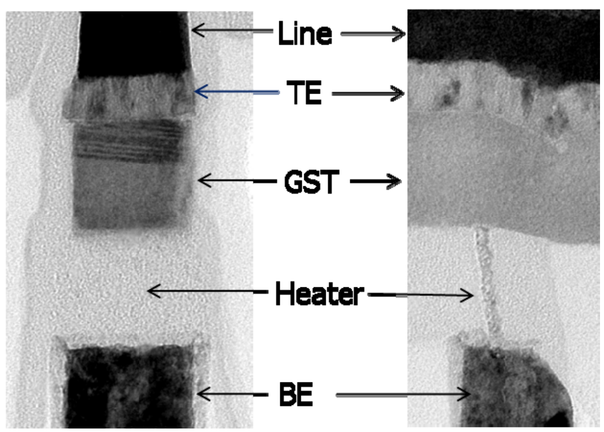
Atomic resolution TEM imaging (left) and elemental distribution mapping at three different heights (center) of a capacitor structure (right)

Phase Change Memory

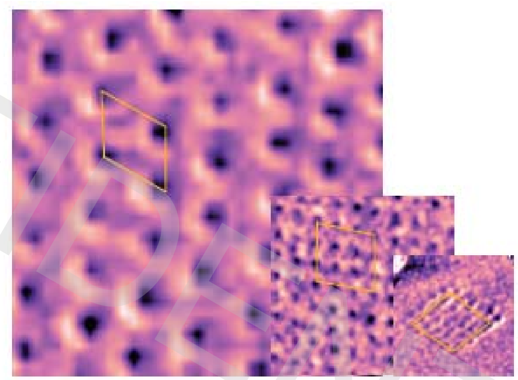
The ternary compounds prevalent in Phase Change Memory technologies (e.g., GST) have a much more complex phase and compositional space than traditional semiconductor materials



GST Phase Diagram. From: "A Layered Chalcogenide Phase Memory Device, Aaron Gibby, Doctoral Dissertation , Stanford University, 2008



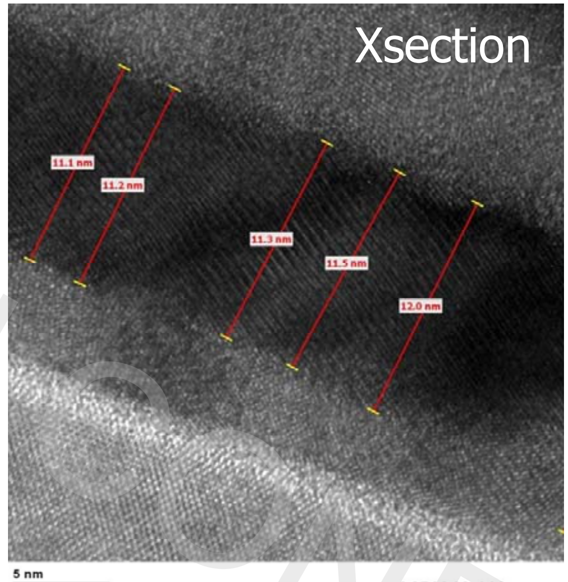
Phase Change Memory Stacks requiring good characterization of heater resistivity and phase change material characterization

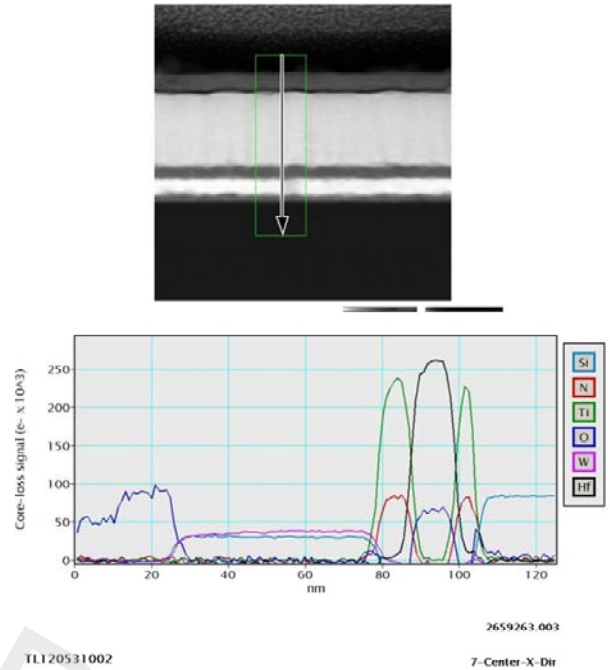


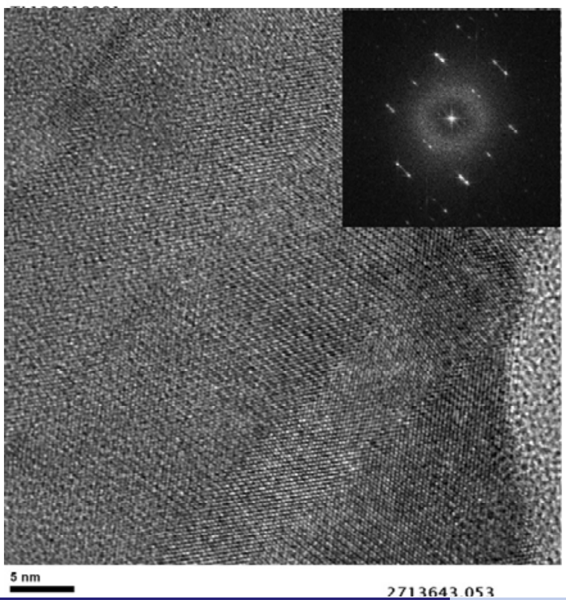
Crystalline Bits in Amorphous Matrix.

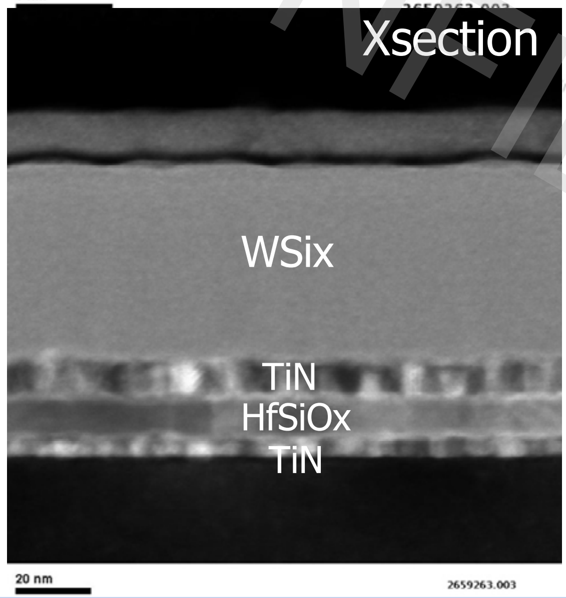
Characterizing material ability to switch between amorphous and crystalline states and using it as a control methodology

$HfSiO_x$(2), TEM structure of FE HfSiOx



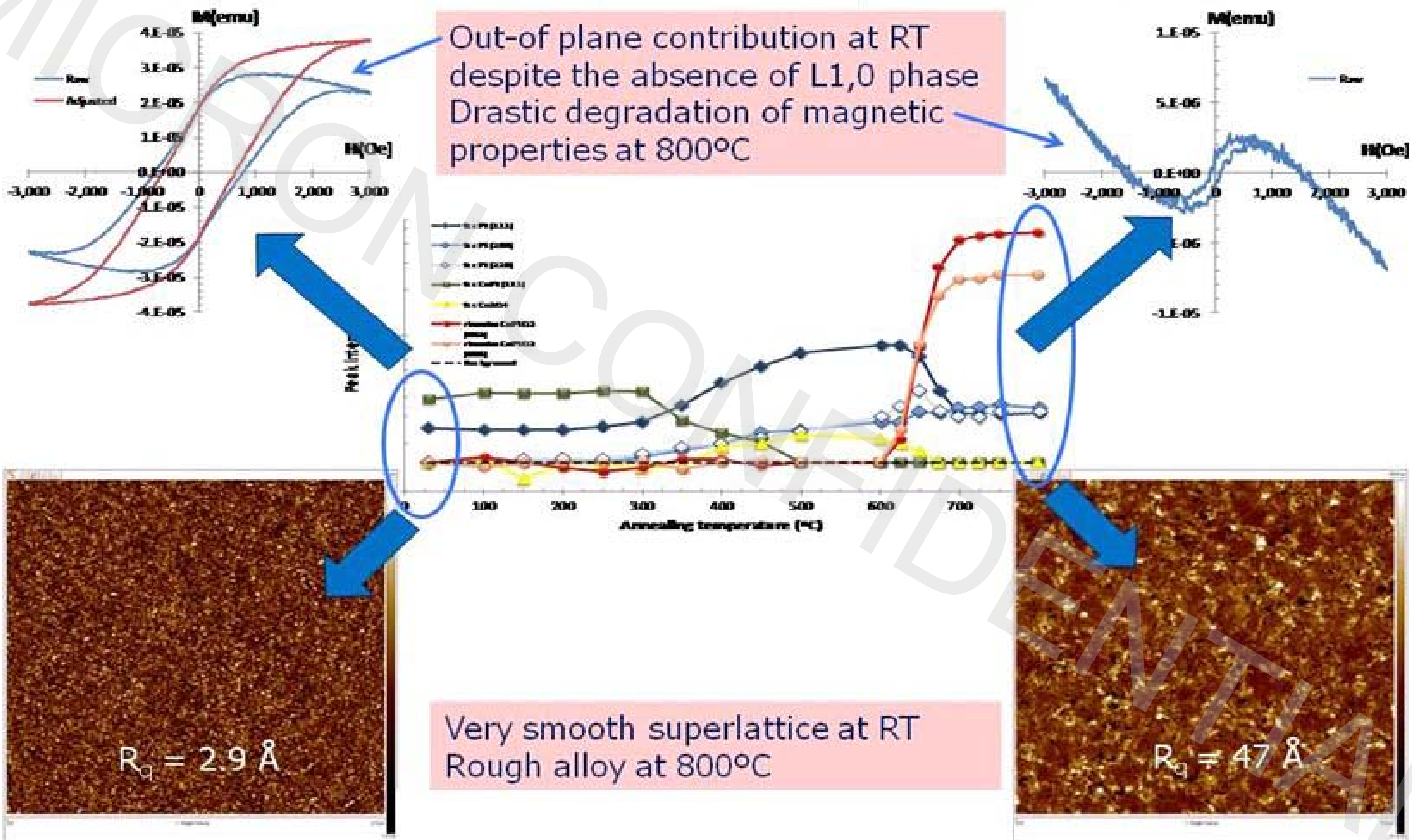






- Fully crystallized HfSiOx material with clear twin structures observed by TEM
- Grain size is large (hundred of nm to um level) but twin period is small (~10nm)
- Strong [110] fiber texture

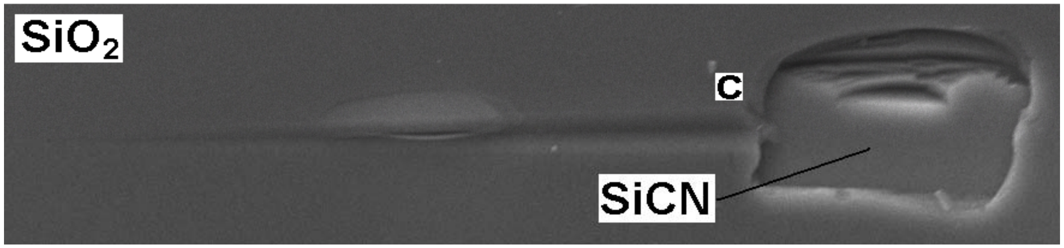
Correlation of XRD-Measured Phase Transitions with Magnetic Properties and Roughness by AFM for STTRAM

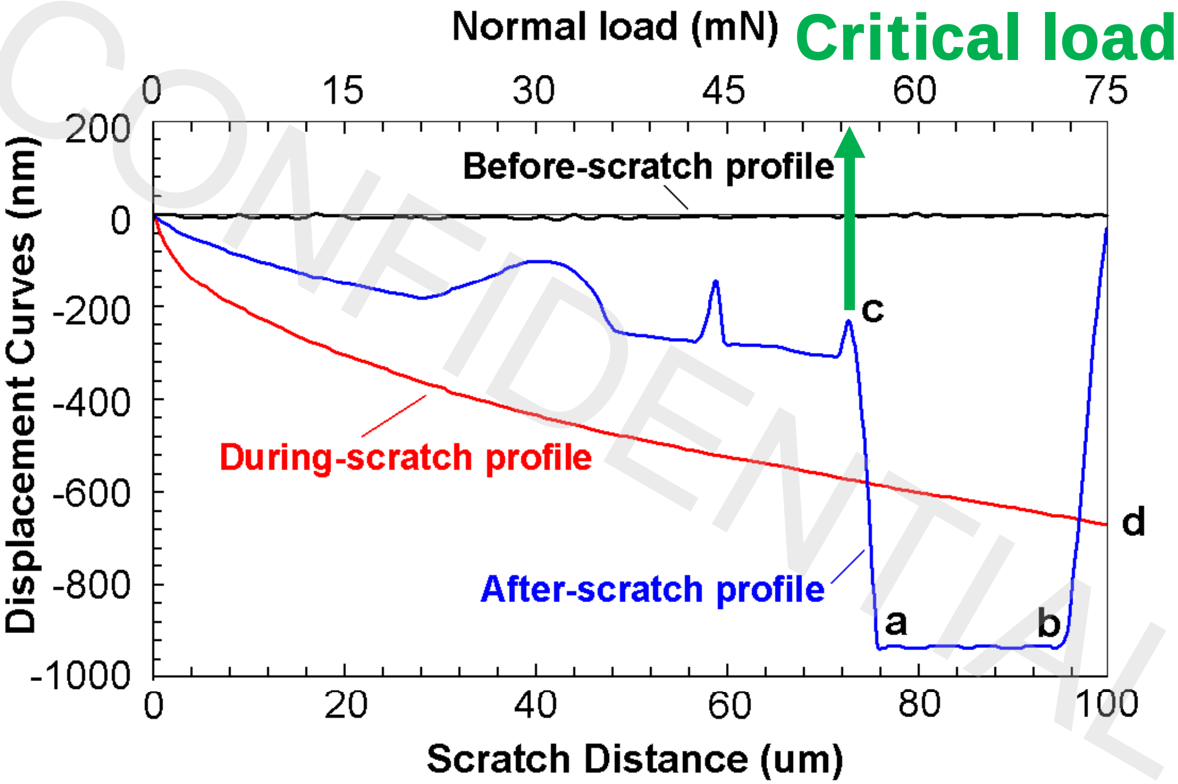


Adhesion of SiCN/SiO_2 by Nanoscratch

- **Point d:** maximum *in situ* depth < SiO_2 thickness → scratch tip did not penetrate into the SiCN/SiO_2 interface during the entire nanoscratch test
- **Point a to b:** residual scratch depth close to SiO_2 thickness → SiO_2 delaminated
- **Point c:** critical position → delamination initiated

Scratch direction →





Atom Probe Tomography

The sample is formed, using a focused ion beam, into a small sharp tip.

The tip is then field and thermally evaporated producing pulses of ions from single atomic layers that are subsequently mass separated using a time-of-flight approach.

The 3-D image is then reconstructed from the individual atomic layers.

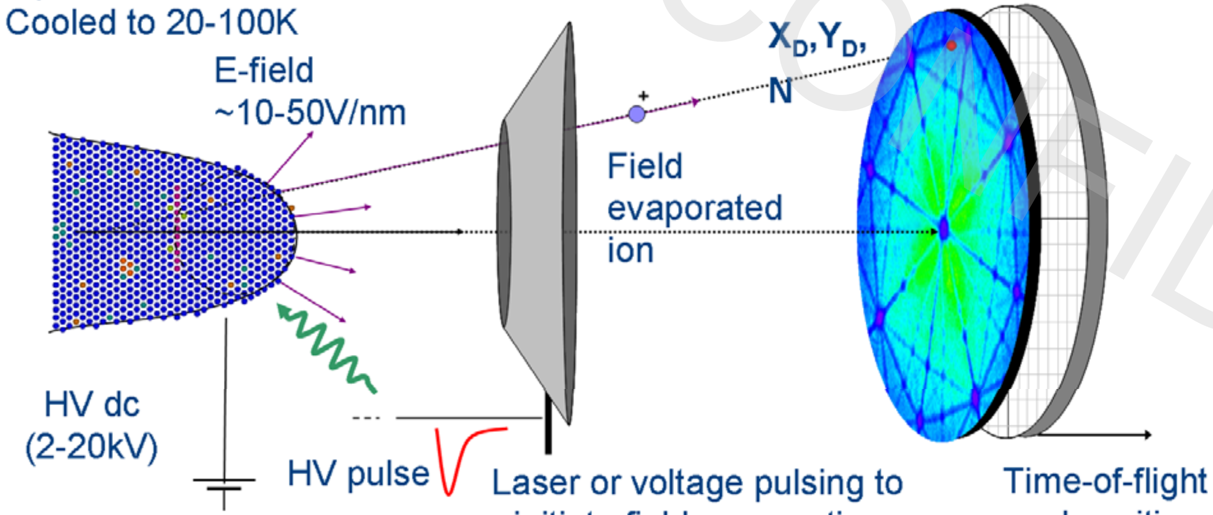
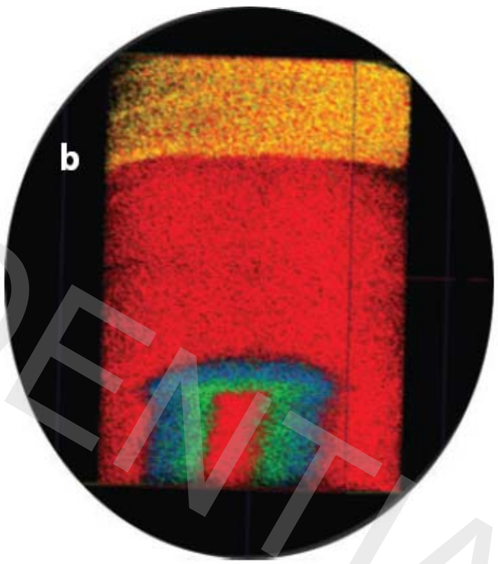


Image from: FIM Group – University of Oxford

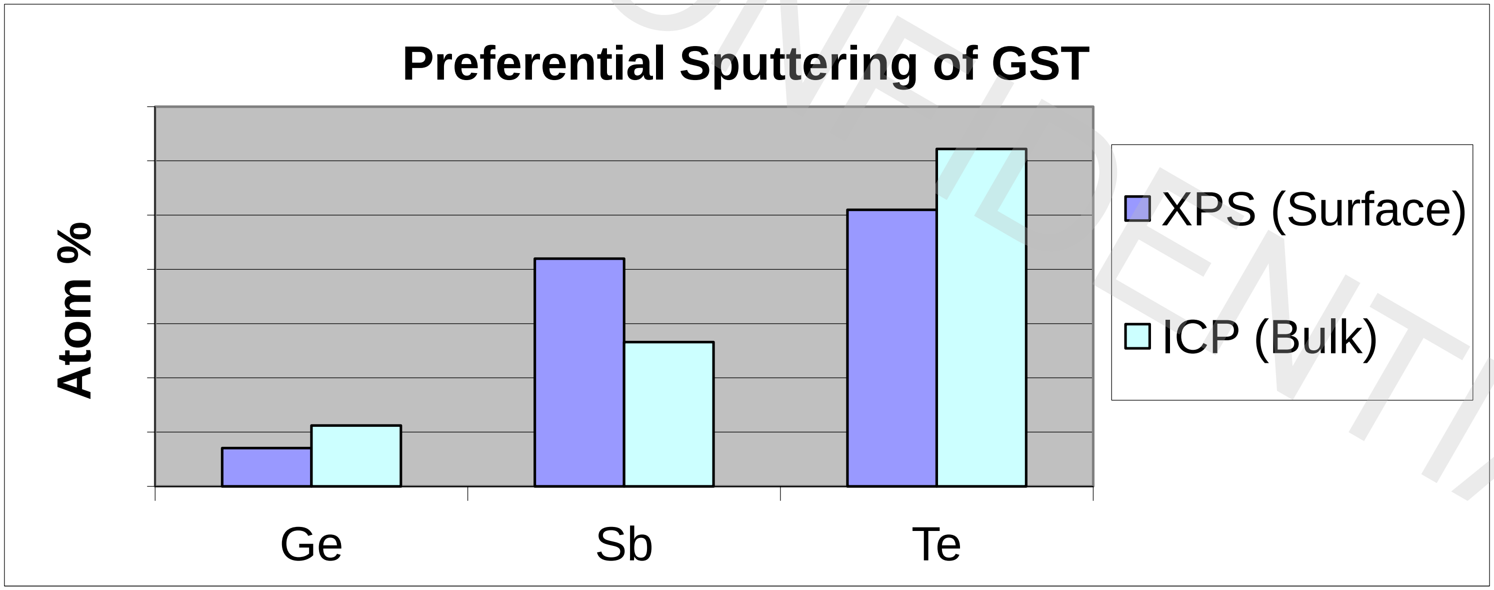


Atom Probe Tomography of high-k metal gate FINFET structure. From: T.F. Kelly and D.J. Larson, Annu. Rev. Mater. Res. (2012), 42:1-31

Challenges of Alternate Memory Technologies

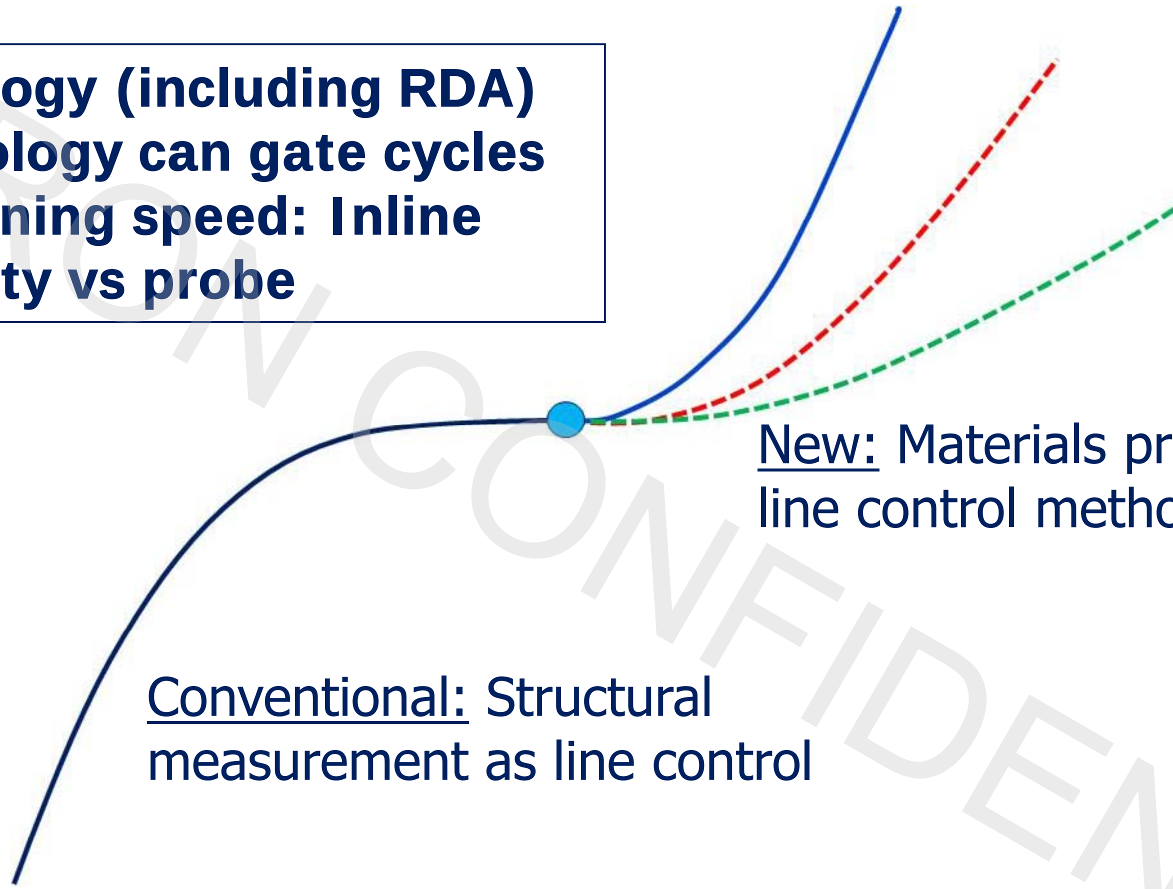
The very act of measuring many of the emerging memory materials can change them

GST films oxidize as a function of aging. Accurately measuring the film chemical composition with a surface sensitive technique, such as x-ray photoelectron spectroscopy (XPS) requires removing the oxidized layer with ion sputtering. Preferential sputtering alters the surface layer affecting the accuracy of the measurement.



Inflection Point in Characterization

Metrology (including RDA) technology can gate cycles of learning speed: Inline visibility vs probe

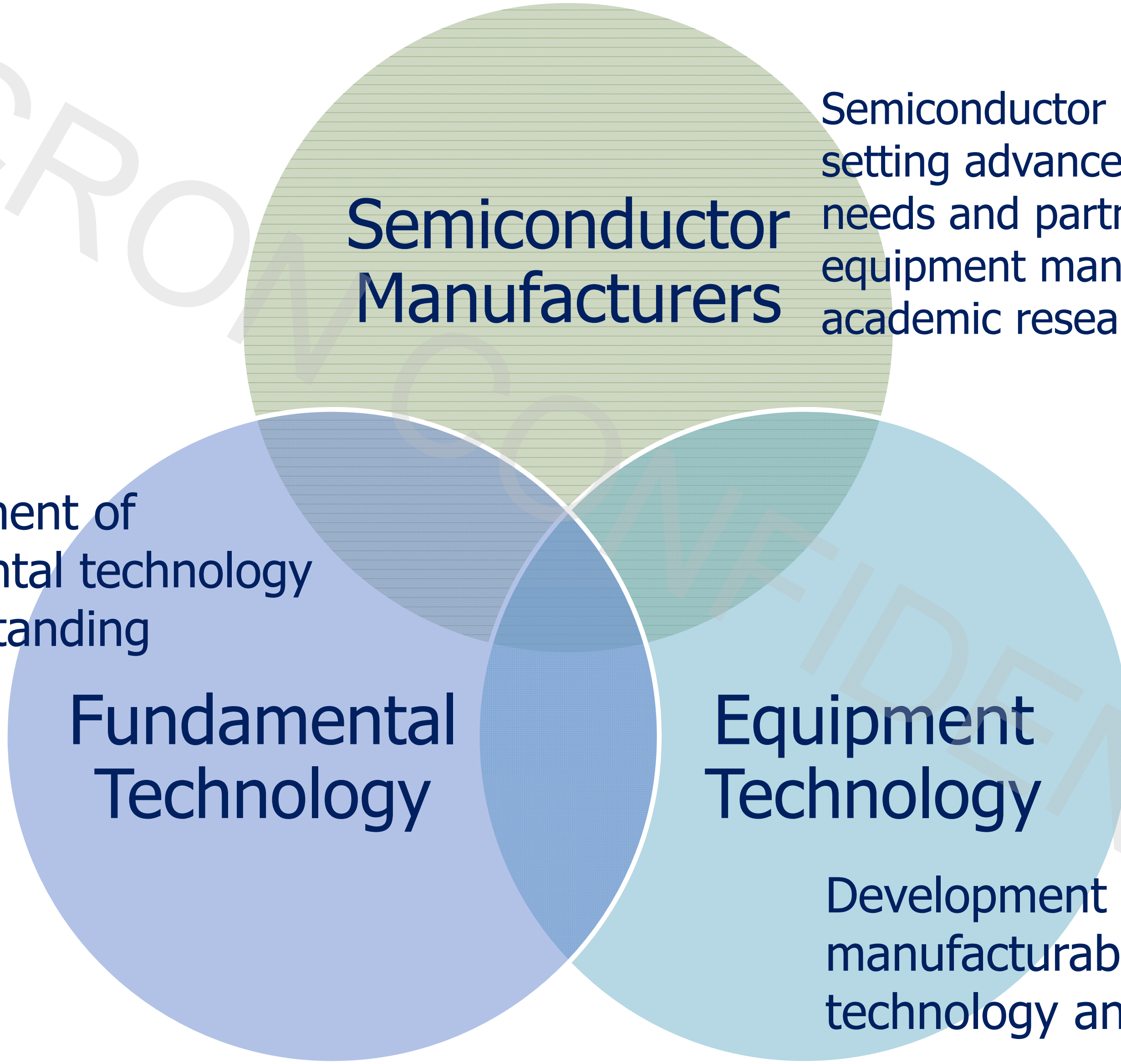


New: Materials properties as a line control methodology

Conventional: Structural measurement as line control

- X-ray based technology: Elemental bandwidth, sensitivity, and CoO
- Advanced material characterization systems: Sensitivity and CoO
- Techniques that can measure with high SNR and low impact to structures

Partnership



Summary

- *Emerging memory technologies present significant challenges in the area of materials and structural characterization*

- *Acceptance of existing characterization techniques in high volume manufacturing will require them to be production worthy*

- *Current techniques for materials characterization involve elaborate sample preparation time*

- *Most of the materials characterization techniques involve considerable perturbation of the samples introducing potential artifacts and ambiguity in data interpretation*

- *It is possible we are entering a decade where cadence of technology development and fundamental understanding will be gated by our ability to characterize, measure, control, and improve unique materials and structures rather than lithography capability*

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