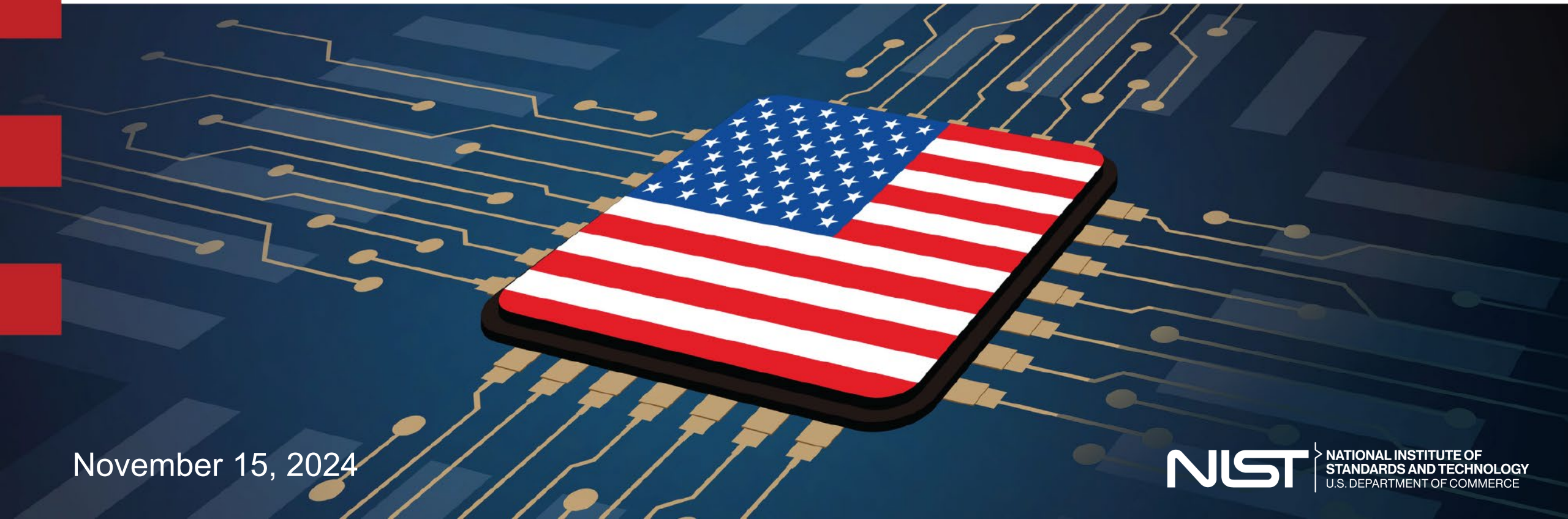
CHIPS for America
CARISSMA Program Proposers' Day



November 15, 2024

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Disclaimer

- Statements and responses to questions about advanced packaging research and development programs in this presentation:
  - Are informational, pre-decisional, and preliminary in nature.
  - Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
  - Are subject in their entirety to any final action by NIST or the Department of Commerce.
- Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or Notices of Funding Opportunity.

Agenda

Time	Session	Speaker
7:30AM – 8:30AM	Check-in	
8:30AM – 8:50AM	Welcome Remarks	**Don Graves** Deputy Secretary of Commerce **Laurie Locascio** Director of NIST and the Under Secretary of Commerce for Standards and Technology
8:50AM – 9:00 AM	Proposer's Day Expectations	**Sarah Georgin** Special Project Manager, CHIPS R&D
9:00AM – 9:30AM	CARISSMA Program Overview	**James Warren** CARISSMA Interim Program Manager, CHIPS R&D
9:30AM – 9:40 AM	Co-optimization Targets	
9:40AM – 9:50AM	Programmatic Targets	
9:50AM – 10:20AM	Networking Break	
10:20AM – 10:35AM	CHIPS Manufacturing USA Program Overview	**Eric Forsythe** Director, CHIPS Manufacturing USA Program
10:35AM – 10:50 AM	NSTC Overview	**Scott Shepard** Technical Program Manager, CHIPS NSTC Program
10:50AM – 11:20AM	Teaming and Poster Session Instructions	**Carol Handwerker** Head of Technology Strategy, CHIPS CPO
11:20AM – 11:35AM	Panel Q&A	James Warren, Eric Forsythe, Scott Shepard, Carol Handwerker

Agenda (Continued)

Time	Session	Speaker
11:35AM – 12:20PM	Poster Session 1:Non-Academic Stakeholders (Industry, Non-profit organizations, State, Local, Territorial, and Tribal Governments, FFRDCs, Federal Entities, etc) and ERIs	
12:20PM – 1:50PM	***Lunch (On Your Own)***	
1:50PM – 2:35PM	Poster Session 2: Institutions of Higher Education (Except ERIs)	
2:35PM – 2:40PM	Transition to Auditorium	
2:40PM – 2:55PM	CHIPS R&D Policy Overview	**Richard-Duane Chambers** Director, Policy and Integration CHIPS R&D Office
2:55PM – 3:10PM	Research Security	**Anita Balachandra** Senior Policy Advisor, CHIPS R&D
3:10PM – 3:25PM	Application Preparation and Submission	**Shanell Williams** Other Transaction Agreements Officer
3:25PM– 4:10PM	Panel Q&A	James Warren, Richard-Duane Chambers, Anita Balachandra, and Shanell Williams
4:10PM – 4:15PM	What's Next?	**James Warren** Interim Program Manager, CHIPS R&D
4:15PM – 5:00PM	No Host Networking in Lobby	
5:00PM	Adjourn	

Proposers' Day Expectations

Sarah Georgin

Proposers' Day Expectations

Agenda

- CARISSMA Program Overview
- Co-optimization and Programmatic Overview
- CHIPS R&D Policy Overview
- Application Process
- Answers to Questions
- Teaming Overviews and Poster Session
- Next Steps

By the end, attendees should better understand

- Outcomes of the CARISSMA Program
- Requirements and Stages/Phases of the CARISSMA Program
- How to apply to the CARISSMA NOFO
- The importance of teamwork!

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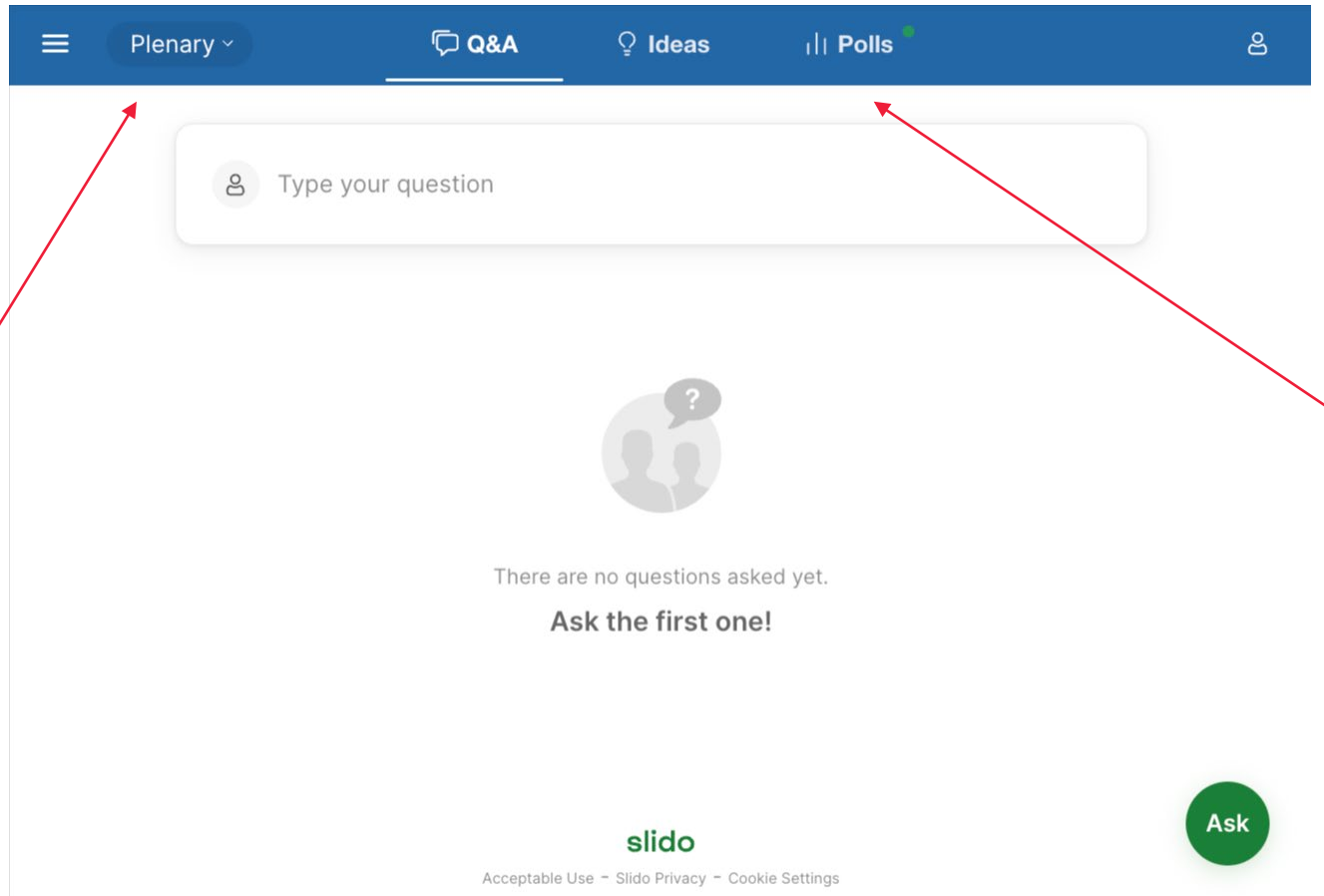


You can change rooms any time using this dropdown menu

Toggle between functions, as needed

Scan the QR code or go to slido.com and enter code #CHIPSCARISSMA

CHIPS AI/AE for Rapid, Industry-informed Sustainable Semiconductor Materials and Processes (CARISSMA)

James Warren

Director, Materials Genome Program, NIST

Interim Program Manager, CARISSMA

CHIPS for America

$39 billion for incentives

Invest in U.S. production of strategically important semiconductor chips, and assure a sufficient, sustainable, and secure supply of older and current generation chips for national security purposes and for critical manufacturing industries.

$11 billion for R&D

Strengthen U.S. semiconductor research and development (R&D) leadership to catalyze and capture the next set of critical technologies, applications, and industries.

$2 billion for DoD Microelectronics Commons

A national network that will create direct pathways to commercialization for US microelectronics researchers and designers from “lab to fab.

2030 Goals

Vision

A vibrant and self-sustaining U.S. domestic semiconductor ecosystem that revitalizes American manufacturing, grows a skilled and diverse workforce, and leads the world in semiconductor research and innovation.

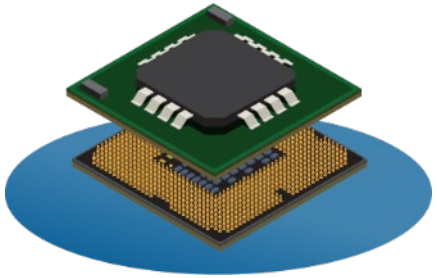
Mission

Accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic tools, resources, workers, and facilities.

2030 Goals

- **U.S. Technology Leadership:** The United States improves its capacity to invent, develop, prototype, and deploy the foundational semiconductor technologies of the future.
- **Accelerated Ideas to Market:** The best ideas achieve commercial scale as quickly and cost effectively as possible.
- **Robust Semiconductor Workforce:** Inventors, designers, researchers, developers, engineers, technicians, and staff meet evolving domestic government and commercial sector needs.

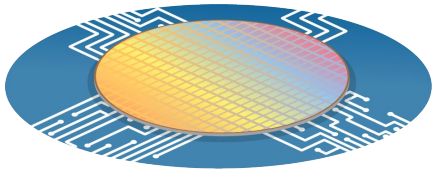
CHIPS R&D Programs



CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast

Natcast is a purpose-built nonprofit organization and operator of the NSTC consortium



CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

Manufacturing USA

CHIPS Manufacturing USA Program

CHIPS Metrology Program

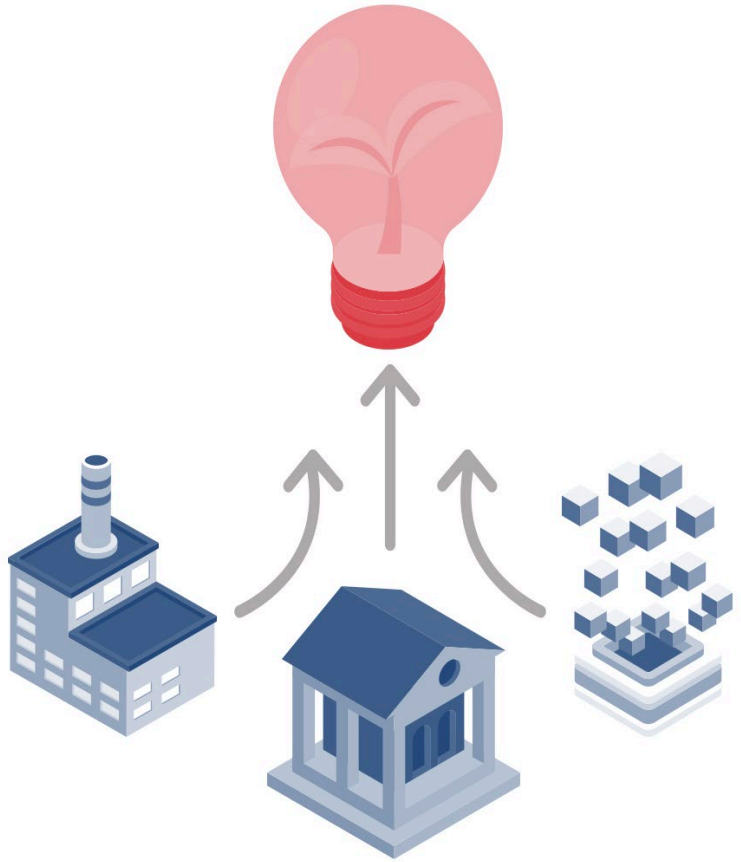
Workforce Initiatives

CARISSMA NOFO Background

Sustainable Semiconductor Manufacturing

Key Industry Sustainability Drivers
- Not addressing them creates ECONOMIC RISK

- Manufacturing Processes
  - **Chip fabs use immense amounts of water and energy.**
  - Building and operating fabs is **expensive**
- Regulatory/Litigation Pressure
  - **Emissions:** 5 million metric tons of CO_2-equivalents emissions from F-GHGs in 2022.[1]
  - **Supply chain risk:** Suppliers of PFAS chemicals are exiting the market.[2]
- Products (Customer Driven)
  - **It is estimated that data centers consume 2% of all U.S. electricity**.[3]
  - Consumers want more efficient products!



[1] Environmental Protection Agency, "Fluorinated Greenhouse Gas Emissions and Supplies Reported to the GHGRP"
[2] 3M, "3M to Exit PFAS Manufacturing by the End of 2025"
[3] Semiconductor Research Corporation, "MAPT Microelectronics and Advanced Packaging Technologies Roadmap"

F-GHGs - Fluorinated-Greenhouse Gases PFAS - Perfluoroalkyl and polyfluoroalkyl substances.

Materials Discovery is Key to Semiconductor Innovation

To continue to drive innovation and achieve the desired functionality required by today's [semiconductor] market, the demand for new and innovative materials and chemistries is increasing. At the same time, there is also a need to develop more efficient, more effective, and safer materials and chemistries.

SRC Industry Roadmap for Microelectronics and Advanced Packaging Technologies, 2023 (page 47)

AI-enabled autonomous experimentation (AI/AE) is an R&D Priority for Industry

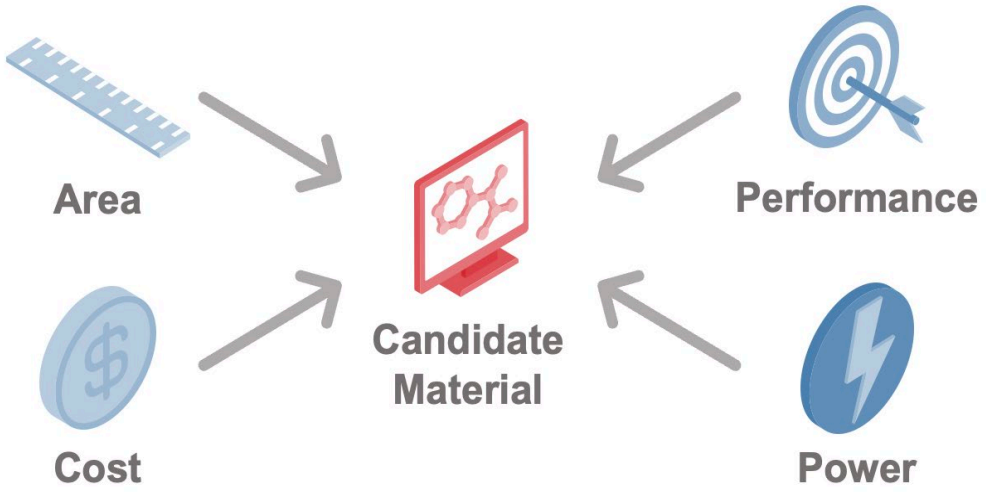
*New integrated software tools are needed to **bring together leading-edge computational tools** (e.g., modeling and simulation from atomistic to mesoscale) **and high-throughput experimental tools** (e.g., physical chemical characterization and synthesis), while simultaneously allowing for predictions and/or optimization against key performance metrics.*

*Such [AI/AE] tools are essential to help optimize for both key performance metrics and environmental, health, and safety metrics. **Tools encompassing co-optimization of performance metrics and environmental, health, and safety metrics** will help accelerate the discovery of more sustainable materials and chemicals without compromising the performance of the product.*

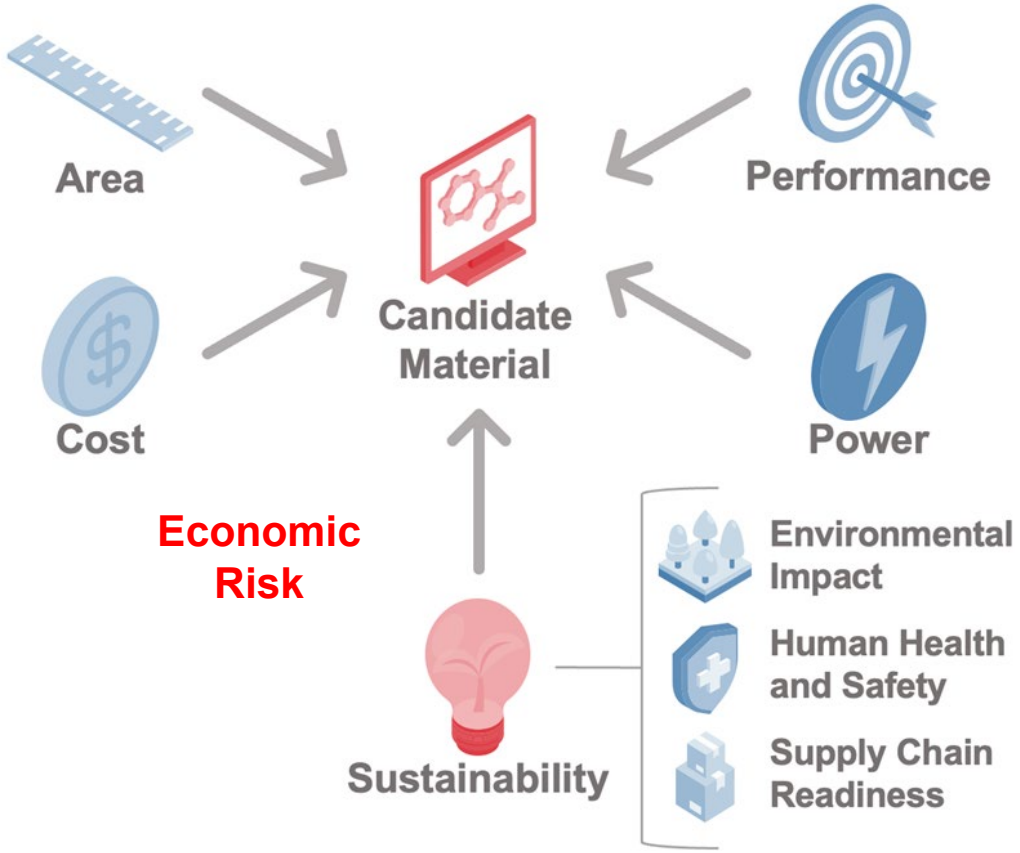
SRC Industry Roadmap for Microelectronics and Advanced Packaging Technologies, 2023 (page 48)

Materials Design Challenge: Multi-Parameter Co-optimization

Traditional Materials/Device Design: PPAC



The Future of Materials Design: PPAC + Sustainability



Optimization Complexity

- Optimizing for PPAC is difficult enough – additional sustainability constraints compound the problem's complexity.
- ***How will we address the very high optimization complexity to make meaningful materials discoveries in a reasonable timeframe?***

Imagine doing this better!

- Instead of taking 10-25 years[1] to design and deploy a new material, we deliver new materials/processes to industry in < 5 years
- We can achieve better performance, smaller footprints, lower power, and lower costs
- We can co-optimize for *sustainability* at the same time

[1] Semiconductor Industry Association PFAS Consortium, "The Impact of a Potential PFAS Restriction on the Semiconductor Sector", April 13, 2023.

Opportunity: AI/AE AI Powered Autonomous Experimentation, a.k.a. Self-Driving Labs

Background on AI/AE Systems

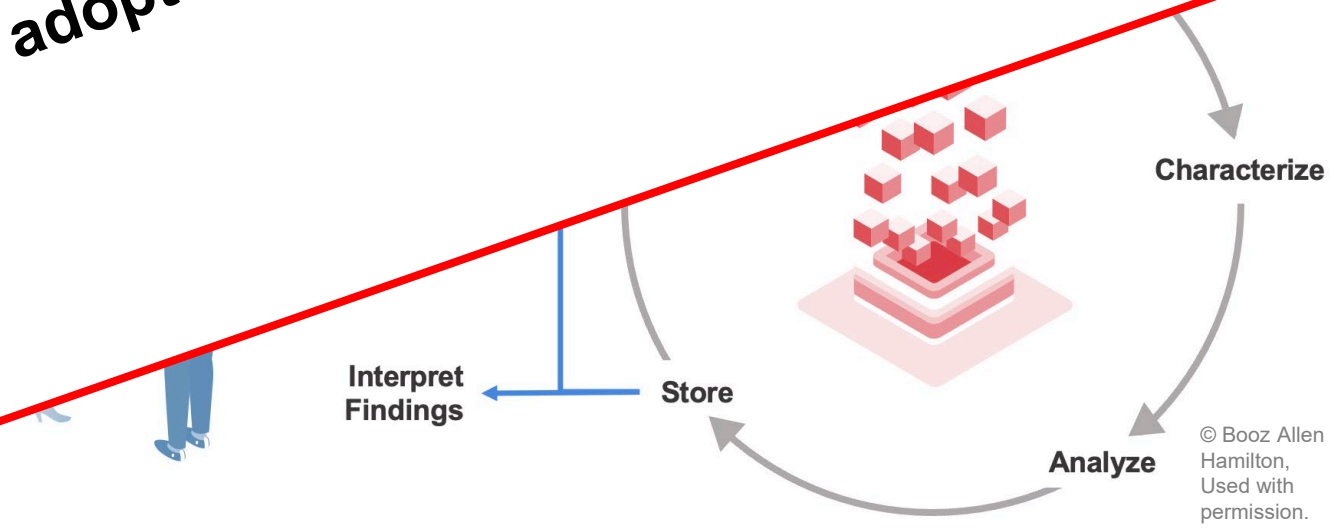
- ***AI/AE: What is it?***
  1. Automated (robotic) laboratory equipment
  2. Rapid/automatic characterization enabled b… AI-trained pattern recognition
  3. Automated data storage
  4. Decision algorit… next re…

- …
  - …r the researcher, …y reducing biases and errors
  - …ous multi-dimensional or multi-parameter optimization

Goal: Demonstrate that new sustainable semiconductor materials, meeting industry needs, can be designed and adopted by industry for testing within five years

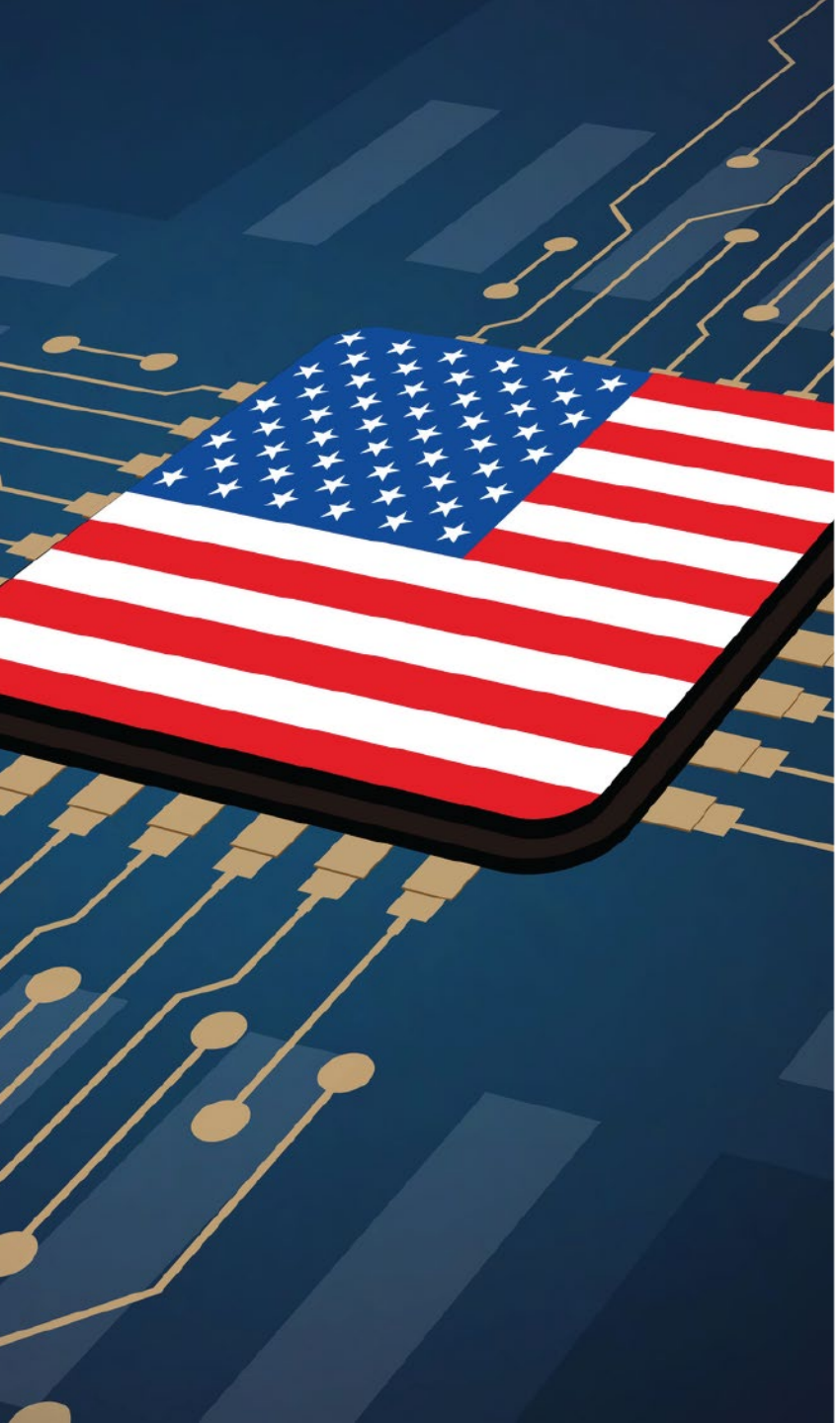
- What can be done?
- How?
- By whom?

AI/AE System C…



Humans initialize the closed-loop cycle, assess performance, and come to conclusions based on the reported results. The AI/AE system iteratively plans, experiments, and analyzes the data autonomously.

CARISSMA NOFO Overview



CARISSMA NOFO Objectives

1) Accelerate research into and delivery of targeted, industry-relevant, sustainable semiconductor materials and processes through the application of AI/AE;
2) Propagate models for incorporating sustainability metrics into semiconductor industry materials design and discovery, in addition to continued advancement in power, performance, area, cost, or other relevant technology metrics;
3) Expand the capabilities of emerging research institutions and other emerging R&D participants through cohesive, innovative teams of universities, industry, government labs, and other stakeholders; and
4) Build an exceptional workforce of university graduates and faculty with AI/AE R&D expertise.

If successful, CHIPS R&D investments under this NOFO should demonstrate that new sustainable semiconductor materials and processes, meeting industry needs, can be designed and adopted for industry testing within five years. Further, the investment should accelerate a step-change in the number of universities, researchers, and graduates participating in the U.S. semiconductor R&D ecosystem.

Eligibility

Eligible Applicants

- Domestic accredited institutions of higher education and domestic non-profit or for-profit organizations that manage consortia of accredited institutions of higher education.
- A domestic entity is one incorporated within the United States (including U.S. territories) with its principal place of business in the United States (including U.S. territories).

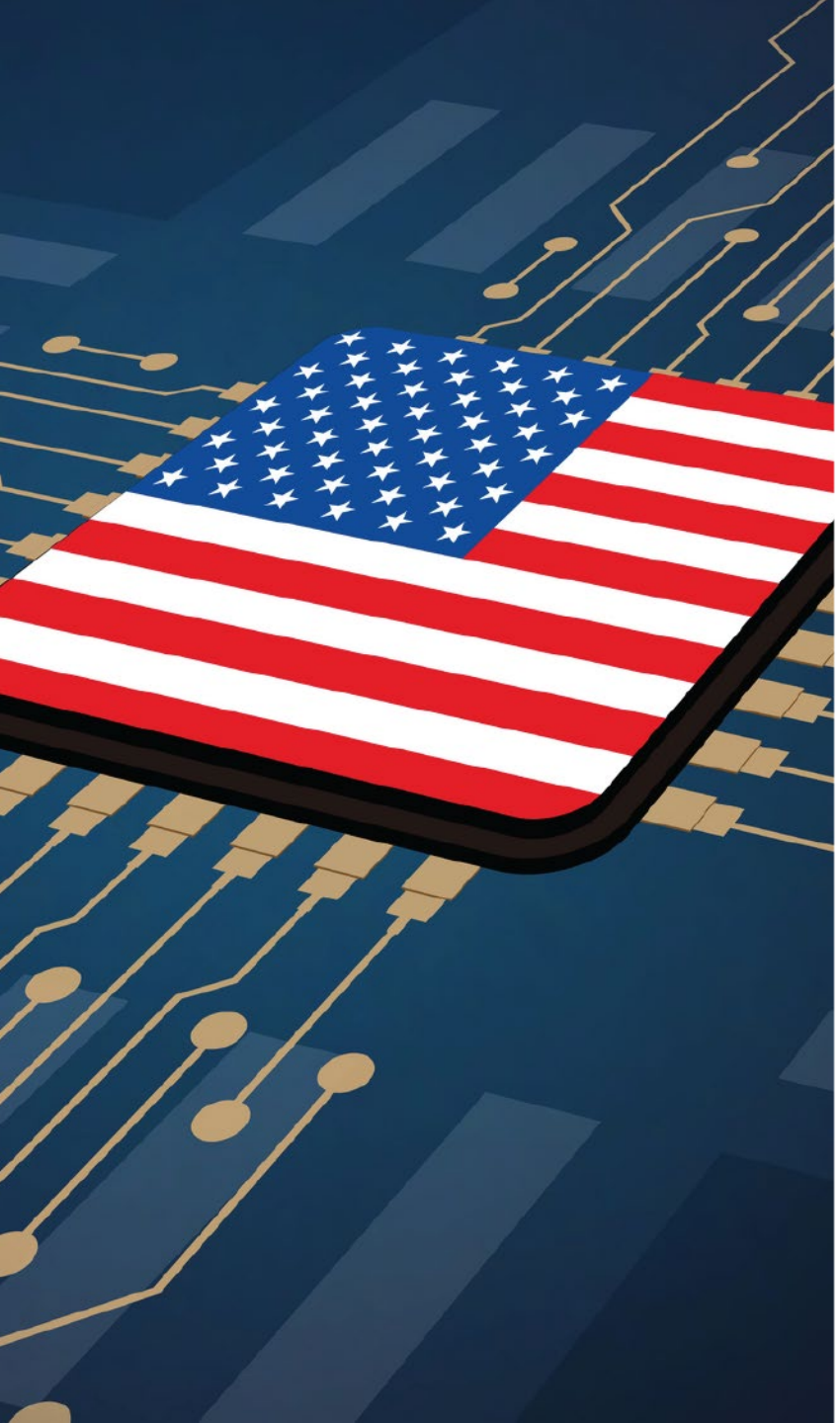
Eligible Subrecipients

- Institutions of higher education; for-profit organizations or non-profit organizations;
- State, local, territorial, and Tribal governments; Federally Funded Research and Development Centers; Federal entities;
- Foreign partners

Additional Requirements

- Eligible Applicants may only submit one concept paper under this NOFO
- Entities may be included as subrecipients on multiple concept papers and applications

Applicants should familiarize themselves thoroughly with the eligibility requirements within the NOFO



University-led Project Teams

RESPONSIVE APPLICATIONS MUST PROPOSE A COLLABORATION AMONG:

- One or more semiconductor industry companies,
- Research universities and/or national laboratories with demonstrated experience in AI/AE or in related fields, and
- At least one ERI (or a domestic non-profit or for-profit organization that manages a consortium of ERIs).

CHIPS R&D FURTHER ENCOURAGES COLLABORATIONS THAT INCLUDE:

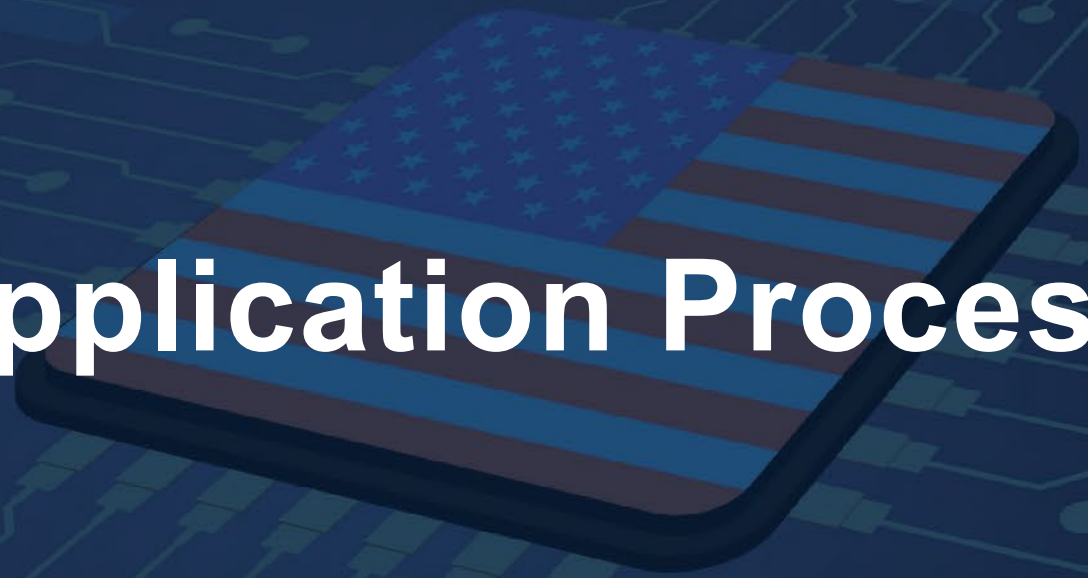
- Civil society or labor organizations focused on environmental sustainability or human health and safety, where appropriate.
- Multi-disciplinary, multi-organization project teams that collectively demonstrate the full range of expertise, experience, and development capabilities needed to achieve the objectives of this NOFO

CHIPS AI/AE for Rapid, Industry-informed Sustainable Semiconductor Materials and Processes (CARISSMA) NOFO

- Up to approximately **$100 million** in total funding
- Individual awards ranging from approximately **$20 million to $40 million**
- Expecting team of **universities and other research entities** with significant experience in AI-powered autonomous experimentation (AI/AE); semiconductor industry partners; emerging research institutions; and civil society organizations focused on environmental sustainability or human health and safety.

Key Dates

Application Process



Registration Requirements

System for Award Management (SAM.gov)

- Organizations must register with both SAM.gov and Grants.gov to apply.
- Receive Unique Entity Identifier (UEI), a 12-character alphanumeric ID assigned to an entity.
- SAM.gov registration process can take up to ten days.

Grants.gov

- All applications must be submitted through Grants.gov.
- Applicants should visit Grants.gov for information on any scheduled closures for routine maintenance.
- Large files take several minutes to upload into Grants.gov.

All concept papers due ***no later than*** 11:59 p.m. Eastern Time on **January 13, 2025**

Concept Paper Requirements

Section	Additional Details	Page in NOFO
SF-424 (R&R), Application for Federal Assistance	The SF-424 (R&R) must be signed by an authorized representative of the applicant's organization.	Pg. 51
Technical Content: Cover Sheet and Proposal	The Concept Paper Narrative must not exceed 10 pages with exclusions to page limit noted	Pg. 51
Concept Paper Quad Chart	One-page summary/abstract, suitable for dissemination to the public	Pg. 52
Budget Estimate	A rough order of magnitude estimate of the total project budget, including the lead applicant and any subrecipients. A full budget narrative is required for full applications, if invited.	Pg. 55
Letters of Commitment	Applicants should include letters of commitment from each planned team member (including any subrecipients and unfunded collaborators)	Pg. 55
Letters of Interest	(Optional, but encouraged) Letters of interest should indicate willingness from any third party to support this proposed effort	Pg. 55

Do not submit any classified materials. All "Proprietary" or "Sensitive Business Information" must be clearly marked

Nothing listed supersedes the NOFO. There are additional requirements for full applications detailed in the NOFO

Full Application Requirements

Section	Additional Details	Page in NOFO
SF-424 (R&R), Application for Federal Assistance	The SF-424 (R&R) must be signed by an authorized representative of the applicant's organization.	Pg. 56
Research & Related Budget (Total Fed + Non-Fed)	The budget must reflect anticipated expenses for the full term of the proposed project, considering all potential cost increases. A separate detailed R&R Budget must be completed for each project phase during the proposed award.	Pg. 57
CD-511	Certification Regarding Lobby is required	Pg. 57
SF-LLL, Disclosure of Lobbying Activities	Complete this form as applicable	Pg. 58
Technical Content: Cover Sheet and Proposal	The Concept Paper Narrative must not exceed 20 pages with exclusions to page limit noted; including, but not limited to, a detailed Project Team Description, Stakeholder Collaboration Study, IPRM, Research and Infrastructure Strategy, EWD Plan, and Broader Impacts Statement	Pg. 58
Executive Summary and Quad Chart	Summary and abstract, suitable for dissemination to the public	Pg. 58
Resumes/CVs	Resumes and CVs for all key personnel are required	Pg. 65
Budget Narrative and Justification	This written justification must include the necessity and the basis for the cost, as described below. Proposed funding levels must be consistent with the project scope, and only allowable costs must be included in the budget	Pg. 66
Letters of Commitment	Applicants should include letters of commitment from each planned team member (including any subrecipients and unfunded collaborators)	Pg. 68
Letters of Interest	(Optional, but encouraged) Letters of interest should indicate willingness from any third party to support this proposed effort	Pg. 69

Other Requirements not included in table: **Indirect Cost Rate Adjustment** (pg. 68), **Subaward Budget Form** (pg. 68), **Data Management Plan** (pg. 70), **Current and Pending Support Form** (pg. 70)

Concept Paper and Full Application Evaluation Criteria

The CHIPS R&D merit review process will assess concept papers against the following five criteria (1 and 2 will receive the greatest and approximately equal weight, 3-5 will receive approximately equal weight):

(1) Relevance to economic and national security

(2) Overall scientific and technical merit

(3) Project Management (Concept Paper)/Project Management, Resources, and Budget (Full Applications)

(4) Transition and impact strategy

(5) Education and workforce development

The evaluation will be qualitative, not numerical.

Nothing listed supersedes NOFO.
For more information, please reference pages 75-77 in the NOFO.

Concept Paper and Full Application Selection Factors

The selection factors in this competition are

(1) **Merit Review:** Results of the merit reviewers' evaluations, including technical comments, and the evaluation panel's evaluations and adjectival rankings

(2) **Relevance to Program and Mission:** Alignment with the objectives of this NOFO as well as the mission, goals, and priorities of the CHIPS R&D

(3) **Full application only Funding:** The amount available to be awarded under this NOFO is subject to the availability of funds and applications received. CHIPS R&D reserves the right to make no awards under this NOFO

(4) **Non-Duplication:** The degree to which the proposed project duplicates other projects funded by NIST or other Federal sources

(5) **Diversity of Projects and Participants**. The degree to which the proposed team and project provides for a diversity of proposed project topics, regional diversity, and institutional diversity (including small and medium enterprises, universities, non-profit research organizations, etc.) in the overall CHIPS R&D portfolio

(6) **Broader Impacts and Workforce Development**. The potential for the proposed project to contribute to broader U.S. research, development, innovation, manufacturing, education, workforce development, environmental responsibility, and regional economic development goals, including plans for broader impact

Nothing listed supersedes NOFO.
For more information, please reference pages 75-77 in the NOFO.

Program Structure

Program Structure *(continued)*

The Funding Opportunity is structured around:

- **Materials Classes and Applications**: Responsive applicants must propose focusing on specific material classes and applications relevant to semiconductor manufacturing
- **Three Operational Areas**: Responsive applicants must propose activities, milestones, and deliverables to address all three operational areas
- **Co-optimization Targets:** Responsive applications must propose to pursue targeted, industry-relevant materials and processes that co-optimize power- and performance-related materials, process, or device characteristics and sustainability targets
- **Programmatic Targets:** Responsive applications must propose to pursue improvements in the domestic capabilities for AI/AE research and in the research-trained semiconductor workforce. Responsive applications must further propose to pursue the domestic transfer of CHIPS-funded technologies.

Nothing listed supersedes NOFO.

Operational Areas

Responsive applications to this NOFO must propose activities, milestones, and deliverables to address the following three Operational Areas (OAs):

(1) **OA1: Convening, Roadmapping, and Technology Transfer**: Establishing lasting collaborations between stakeholders, refining Co-optimization and Programmatic Targets, and transferring research outputs for further use.

(2) **OA2: AI/AE Infrastructure and Research**: Establishing AI/AE capabilities, to include infrastructure at ERIs and other research universities or access to such infrastructure, and conducting basic and applied research into early technology readiness level (TRL) materials and processes that address semiconductor industry needs.

(3) **OA3: Education and Workforce Development**: Developing and expanding the total number of domestic researchers skilled in AI/AE methods relevant to the semiconductor industry materials and processes.

Proposals must address ALL three operational areas

Nothing listed supersedes NOFO.
For more information, please reference page 17 in the NOFO.

Materials Classes and Applications

- Applicants must propose focusing on specific material classes and applications relevant to semiconductor manufacturing.
- Proposals must demonstrate the expected impact on metrics related to both the sustainability of semiconductor manufacturing and to materials, process, or device performance characteristics, which may include device performance, power, area, and cost (PPAC).
- Proposals may seek to either improve existing materials an processes or enable realization of next-generation materials, processes, or devices.

Table 2. Non-Exhaustive List of Notional Materials Classes and Applications

• Abatement catalysts • Adhesives • Atomic Layer Deposition (ALD) • Antireflective Coatings • Chemical Mechanical Planarization (CMP) slurries • Dielectrics and insulators • Dopants • Epitaxy and deposition gases • Etch gases • Filters and membranes • Heat transfer fluids (HTFs) • Interconnects • Lubricants	• Memory materials • Metals and conductors • PFAS • Polymers and resins • Photonic materials • Photoresists • Photoacid generators (PAGs) • Redistribution Layer films (RDLs) • Solvents • Substrates • Surfactants • Thermal Interface Materials (TIMs) • Underfills • Wet etchants • 2D materials

Nothing listed supersedes NOFO.

Co-optimization Targets

- Co-optimization Targets are grouped into four Themes:
  - **Theme 1:** Materials, Process, or Device Power- and Performance- related Characteristics
  - **Theme 2:** Emissions and Hazardous Waste
  - **Theme 3:** Energy Consumption
  - **Theme 4:** Water Consumption
- Applicants must propose to pursue targeted, industry-relevant materials and processes that co-optimize power- and performance-related materials, process, or device characteristics (Theme 1) and sustainability targets (Theme 2–4)
- **Out of scope:** Applications that pursue manufacturing sustainability (Themes 2–4) without co-optimizing for Theme 1 and applications that improve device performance without addressing manufacturing sustainability will be considered out of scope.

For more information, please reference pages 18-20 in the NOFO.

Co-Optimization Targets (Themes 1-4)

Theme 1: Materials , Process, or Device Power- and Performance- related Characteristics **REQUIRED**

- Applications that pursue manufacturing sustainability (Themes 2–4) without co-optimizing for Theme 1 will be considered out of scope
- Co-optimization Targets based on industry-relevant materials, process, or device power- and performance-related characteristics, which may include PPAC and other related metrics such as yield, economic metrics, and supply chain resiliency metrics
- Develop materials and processes that result in similar or improved materials, process, and/or device characteristics compared to currently known materials and processes OR must demonstrate the industry-relevance of the proposal, such as through stakeholder Letters of Commitment/Interest.

Co-Optimization Targets (Themes 2-4)

Theme 2: Emissions and Hazardous Waste

- Co-optimization targets that demonstrate improvement related to green house gas (GHG) emissions, use of toxic substances, and generation of hazardous waste from current or future semiconductor manufacturing
  - Sample targets may include but are not limited to, for instance, the mass or volume of a substance (e.g., GHGs or PFAS) released into the environment per 300mm wafer manufactured.
  - Applicants may further propose to address targets related to the toxicity or human health and safety impact of semiconductor manufacturing-related emissions or hazardous waste

Co-Optimization Targets (Themes 2-4)

Theme 3: Energy Consumption

- Co-optimization targets that demonstrate improvement related to the amount of energy consumed by current or future semiconductor manufacturing.
- Sample target may include but are not limited to, for instance, kilowatt hours (kWh) per 300mm wafer manufactured.
- *Manufacturing energy consumption differs from the amount of power (energy) consumed by a manufactured device, which would be considered as a potential Theme 1 Co-Optimization Target.*

Co-Optimization Targets (Themes 2-4)

Theme 4: Water Consumption

- Co-optimization Targets that demonstrate improvement related to water consumed by current or future semiconductor manufacturing.
  - Targets may include, but are not limited to, targets related to amount of fresh water consumed from public utilities as well as targets related to recycling or reclamation of used process water.
  - Sample targets may include but are not limited to, for instance, gallons of water used per 300mm wafer manufactured.

Programmatic Targets

Applicants must propose **SMART** targets to pursue the following themes:

- **Theme 5: Research Capacity:** Applications must demonstrate how CHIPS-funded activities will increase the overall research capacity of the domestic semiconductor innovation ecosystem, particularly as it relates to AI/AE
- **Theme 6: Education and Workforce Development (EWD):** Applications must provide a plan to achieve improvements in the availability of state-of-the-art (SOTA) research-trained personnel
- **Theme 7: Domestic Technology Transfer:** Applications must demonstrate, with rigor increasing across the award period of performance, the ability for CHIPS-funded research outputs to successfully transfer to the domestic commercial marketplace

Nothing listed supersedes NOFO.

Programmatic Targets (Themes 5-7)

Theme 5: Research Capacity REQUIRED

- Programmatic Targets that demonstrate how CHIPS-funded activities will increase the overall research capacity of the domestic semiconductor innovation ecosystem, particularly as it relates to AI/AE.
  - Applications must specify the distribution of increased research capacity between ERIs and non-ERIs.
  - CHIPS R&D will favorably consider applications that demonstrate a substantial increase in research capacity and research leadership at ERIs.

Programmatic Targets (Organized by Theme)

Theme 6: Education and Workforce Development REQUIRED

- Programmatic Targets that represent improvements in the availability of research-trained personnel with experience on state-of-the-art (SOTA) capabilities.
- Applications must specify the distribution of EWD improvements between ERIs and non-ERIs. CHIPS R&D will favorably consider applications that demonstrate substantial EWD improvements at ERIs.

Programmatic Targets (Organized by Theme)

Theme 7: Domestic Technology Transfer REQUIRED

Applications must propose Programmatic Targets that demonstrate, with rigor increasing across the award period of performance, the ability for CHIPS-funded research outputs to successfully transfer to the domestic commercial marketplace.

- These targets must ensure consistency with the Commercial Viability and Domestic Production Plan (CVDP).
- CHIPS R&D strongly encourages applicants to work with industry partners when developing these targets.

By Whom?

Opportunity: AI/AE AI Powered Autonomous Experimentation, a.k.a. Self-Driving Labs

Gaps[1] (AMII 2024 workshop):

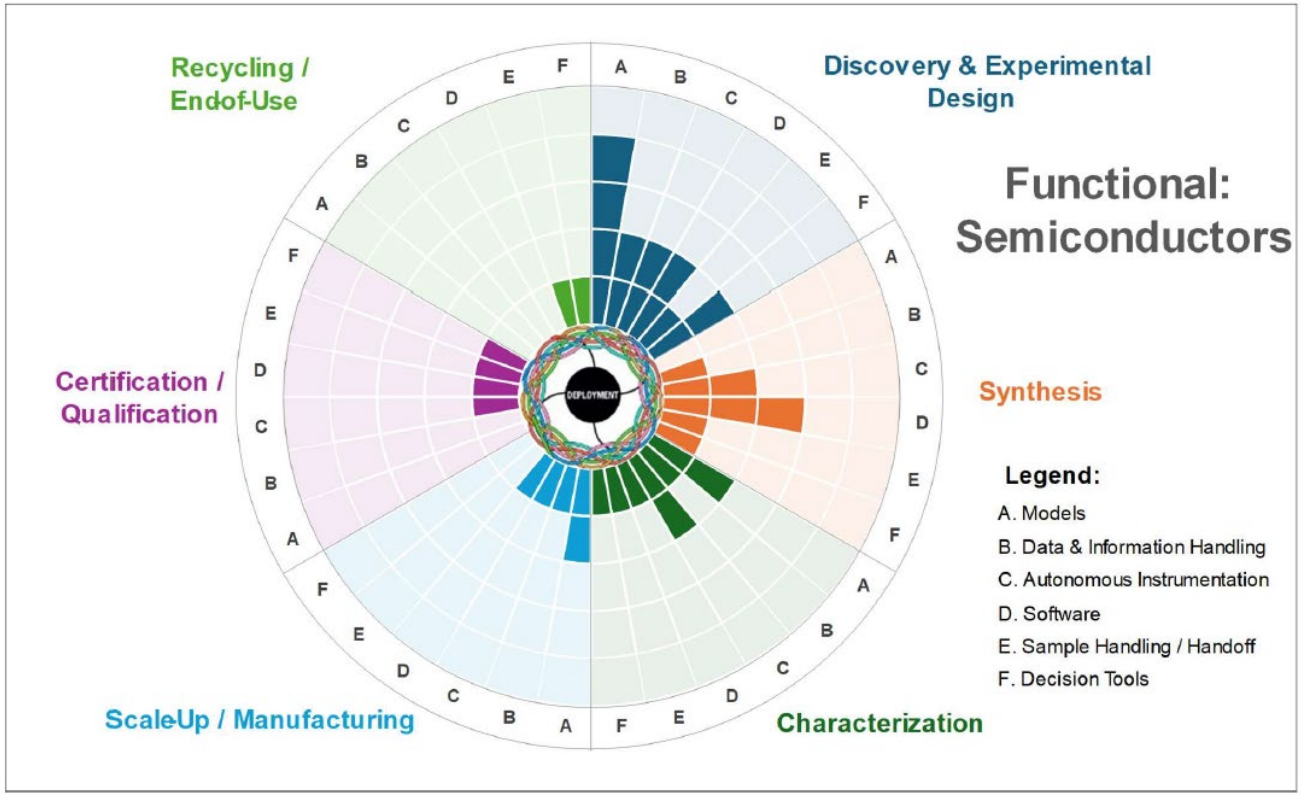
(1) Relatively **few organizations** have complete AI/AE capabilities at a "moderate" level or above

(2) There is a **gap in AI/AE-trained workers** with specialized skills in AI, materials, and sustainability

(3) While discovery efforts can identify new materials, there are **limited resources** for experimental verification

(4) Lack of physics-based materials synthesis models, lab scale characterization tools, and **partnerships for manufacturing scale-up**

AI/AE System Overview[1]

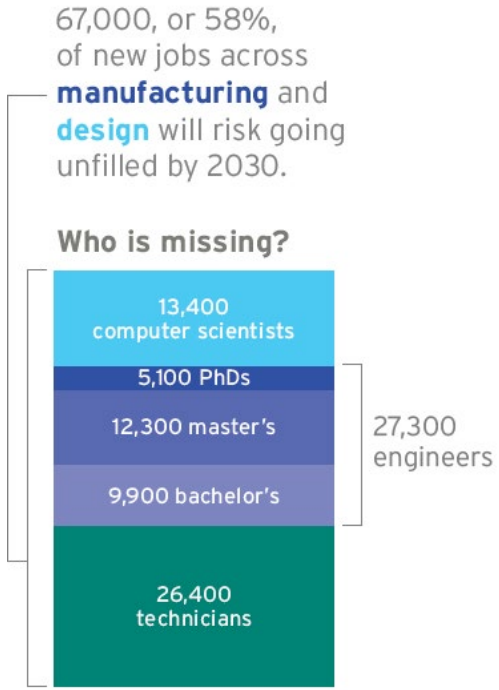


[1] Materials Genome Initiative, "Accelerated Materials Experimentation Enabled by the Autonomous Materials Innovation Infrastructure (AMII) A Workshop Report", July 2024 .

Opportunity: AI/AE AI Powered Autonomous Experimentation, a.k.a. Self-Driving Labs

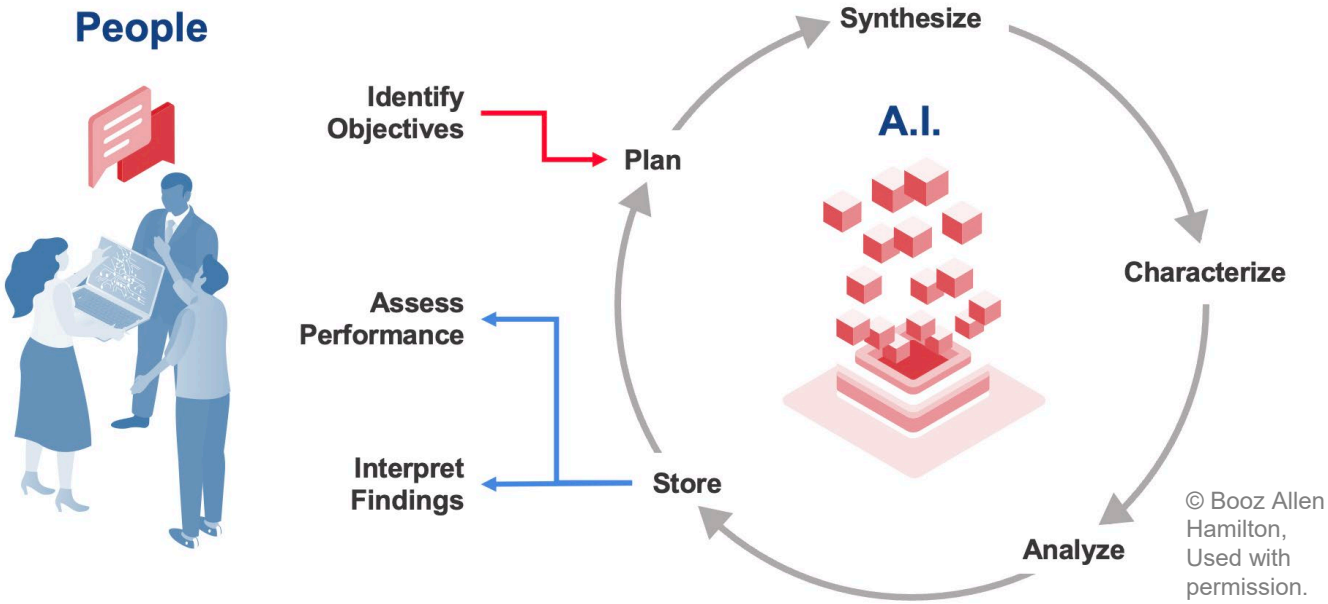
Gaps

(1) There is a **gap in AI/AE-trained workers** with specialized skills in AI, materials, and sustainability



While the chip industry seeks to close a ~40k gap in scientists and engineers, AI/AE must also compete to find AI-capable researchers.[1]

AI/AE System Overview



Humans initialize the closed-loop cycle, assess performance, and come to conclusions based on the reported results. The AI/AE system iteratively plans, experiments, and analyzes the data autonomously.

[1] Semiconductor Industry Association, "Chipping Away: Assessing and Addressing the Labor Market Gap Facing the U.S. Semiconductor Industry

Imagine doing it better!

- Instead of taking 10-25 years to design and deploy
  down to < 5 years with AI/AE
- We can achieve better perf
- We can co-op
- pate in AI/AE and in
- esearch collaborations between emerging
  federal labs
- exceptional cadre of university graduates and research faculty with
  R&D expertise

Goal: Demonstrate that new sustainable semiconductor materials, meeting industry needs, can be designed and delivered for industry testing within five years

Goal: Accelerate a step-change in the number of universities, researchers, and graduates participating in the U.S. semiconductor R&D ecosystem

Emerging Research Institutions (ERIs)

Challenge

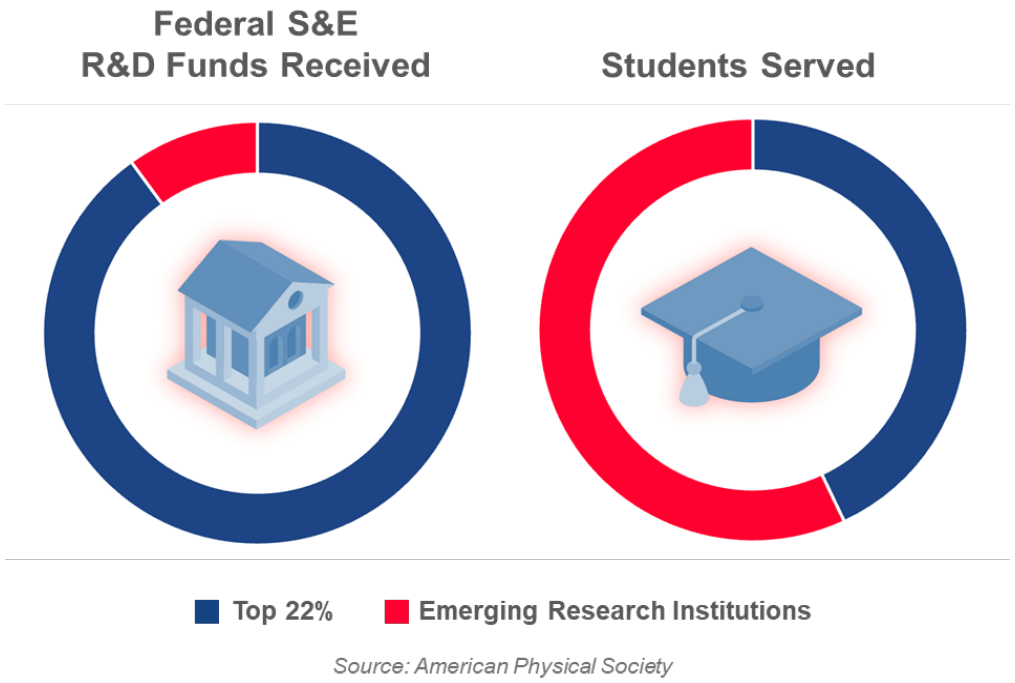
How can we dramatically increase ERI participation in semiconductor research, especially AI/AE materials research?

Opportunity

ERIs have untapped potential to bolster semiconductor research.

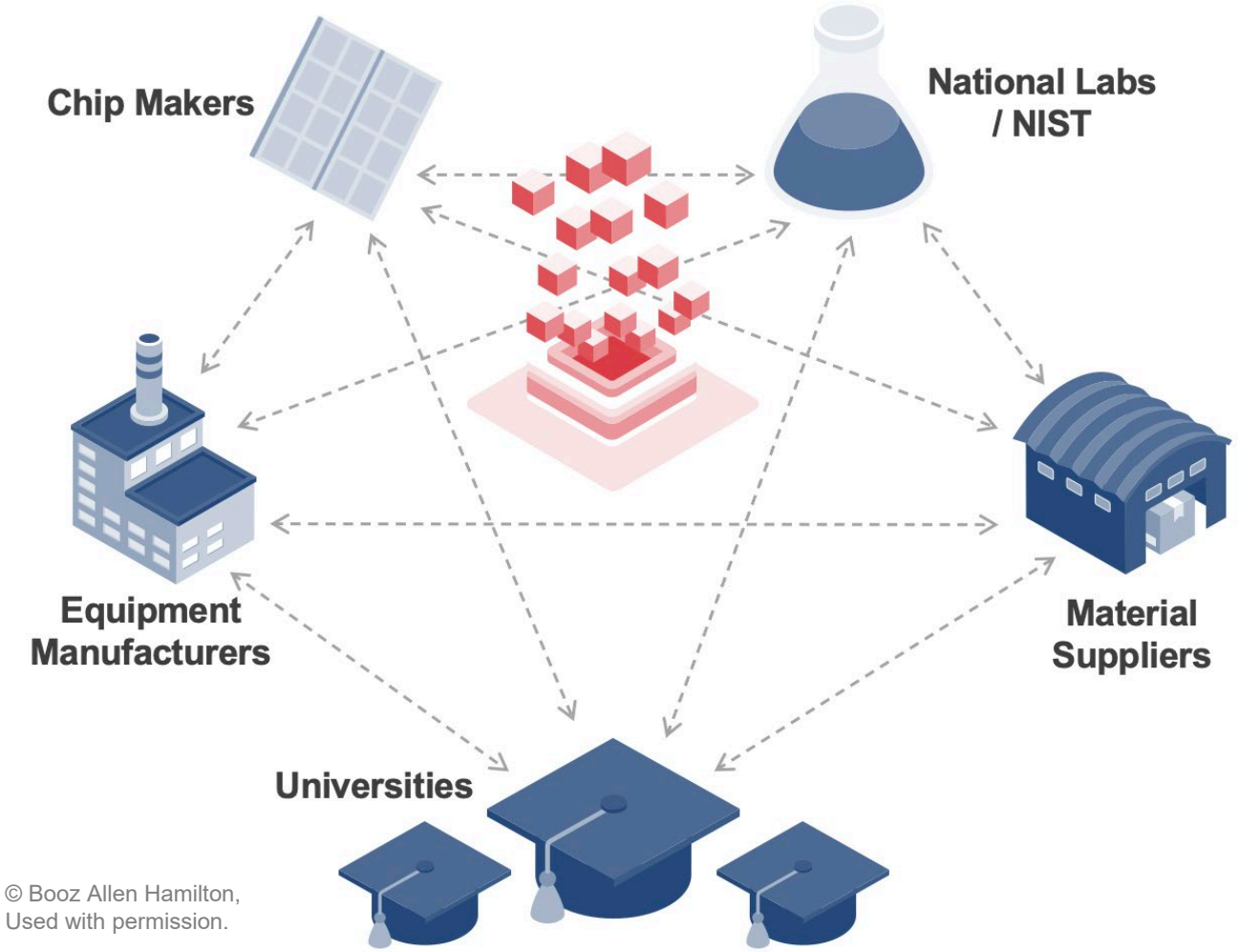
What is an ERI?

- An ERI is a higher education institution that receives less than $50M in federal research expenditure each year
- ERIs train the majority of undergraduate students yet receive a minority of federal R&D dollars
- ERI participation in grants is often limited to workforce development efforts
- Federal R&D at ERIs is growing, but additional funding and infrastructure are needed



Source: American Physical Society

Partnership and Collaboration Models (more on teaming this afternoon!)



Federated AI/AE

- Structures can range from a more centralized “hub” to a fully federated model
- Federation of the digital and physical infrastructure of AI/AE systems is both possible and potentially desirable
- AI/AE researchers can virtualize pieces of the workflow and digital objects (e.g., computer code, digital twins, data, and control software enabling remote operation)
- “Multi-agent” approach, which combines information from diverse research campaigns, can support AI/AE research strategies
- Ability to remotely access equipment hosted by collaborators from other institutions.

Phases, Milestones, and Outputs

Phases and Milestones

- Applications must propose thee phases of work with:
  - Phase 1 ranging in 12 to 18 months and each subsequent phase ranging in length from 12 to 24 months. The total period of performance may not exceed five (5) years.
  - SMART Milestones marking measurable progress towards demonstrating the Co-optimization Targets and achieving the Programmatic Targets
  - Go/no go decision points at the end of each phase

Notional Example of Project Phases

PHASE 1:
Stand up Program
(18 months)

- Finalize teaming structure, including for industry and civil society partner organizations
- Establish Research Advisory Board
- Refine Co-optimization and Programmatic Targets based on technoeconomic and lifecycle analyses
- Refine the Phase-specific Research Plan and CV, including a roadmap from R&D to industry adoption
- Determine AI/AE system components and workflow design
- Install, integrate, and test equipment and software
- Assemble project team with faculty, staff, students, and post-docs onboarded
- Refine EWD Plan and begin to develop and teach AI/AE curricula at participating universities
- Join CHIPS Manufacturing USA Institute and the NSTC, as appropriate

Notional Example of Project Phases

PHASE 2:
R&D Campaign
(18 months)

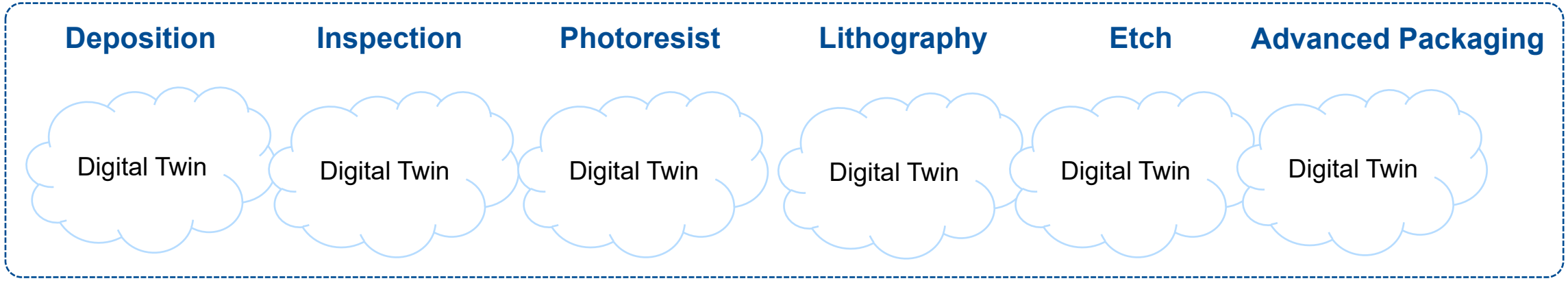
- Demonstrate an effective collaboration environment, workflow, throughput, and quality of R&D output of AI/AE systems
- Refine digital twins, custom software, application programming interfaces (APIs), and co-optimization algorithms
- Deploy preliminary materials digital twins
- Deliver first-round materials to industry for assessment with respect to Co-optimization Targets and AI/AE system performance
- Update EWD plan and continue to train students and post-docs using relevant AI/AE curricula

Notional Example of Project Phases

PHASE 3:
Delivery
(24 months)

- Conduct tests, led by industry, to establish the performance of multiple co-optimized sustainable semiconductor materials and processes
- Catalog and accelerate technology transfer and adoption by industry partners and secure industry commitments to deploy the technology
- Affirm the commercial viability, environmental impact, and supply chain impacts of potential research outputs
- Disseminate equipment and materials digital twins to industry, the CHIPS Manufacturing USA Institute, and the NSTC, as appropriate
- Execute plans to ensure sustained leadership, capabilities, and capacity for AI/AE at universities, including ERIs, and in the private sector
- Deliver final reports and best practice at CHIPS R&D

Vision for the CHIPS Manufacturing USA Institute



Semiconductor Manufacturing Flow

Complex Manufacturing

- **Co-design: function, process, materials, tools**
- 1000+ process steps
- 70+ masks
- **Hundreds of materials**
- Hundreds of different tools

Digital twin:

- Enables collaborative development across the country, creating new opportunities for participation.
- Speeding innovation in new materials, tools, processes.
- Leverage emerging A.I. technology to help accelerate the innovation in manufacturing and co-optimization.
- Significantly reduce costs by improving capacity planning, production optimization.

Networking Break

Please return at 10:20 AM

SUBMIT Questions for Q&A Session!

Scan the QR code or go to slido.com and enter code #CHIPSCARISSMA

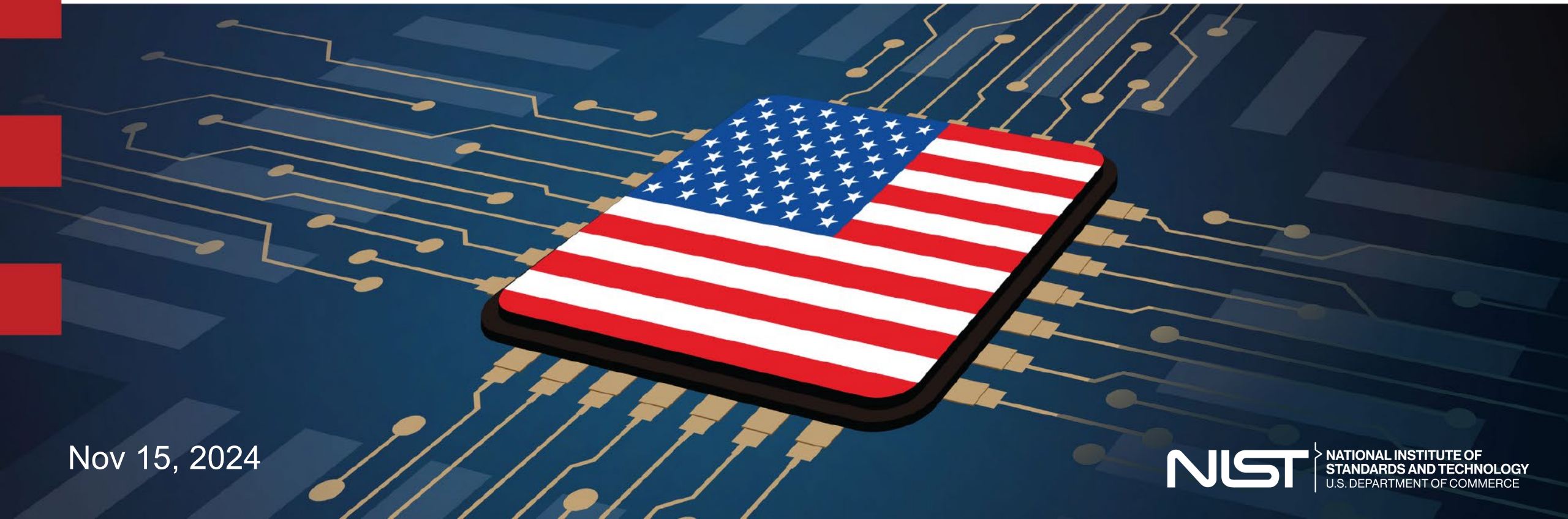
Manufacturing USA Overview

Eric Forsythe
Director
CHIPS Manufacturing USA Program

CHIPS Manufacturing USA Institute Digital Twin For Manufacturing

CHIPS AI/AE for Rapid, Industry-informed Sustainable Semiconductor Materials and Processes (CARISSMA) Proposer Day

Eric Forsythe, Ph.D Technical Director CHIPS Manufacturing USA Program
Michael McKittrick, Ph.D, Deputy Director CHIPS Manufacturing USA Program
Nancy Stoffel, Ph.D, Senior Technical Advisory CHIPS Manufacturing USA Program
Dillon Watring, Ph.D, Program Manager CHIPS Manufacturing USA Program
Christie Canaria,Ph.D, Senior Policy Advisor, CHIPS RD Office
Mahesh Mani, Ph.D, Technical Manager, Office for Advanced Manufacturing
Carol Handwerker, Ph.D CHIPS Incentives, Senior Technical Advisor the MFG USA
James Warren, PhD, NIST Materials and Measurement Lab, NIST

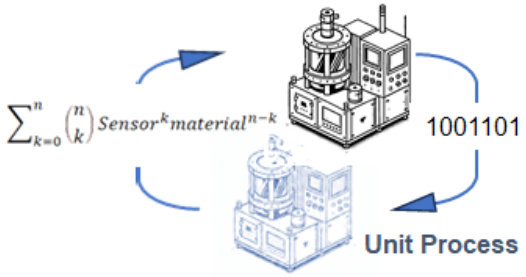


Nov 15, 2024

NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Technical Challenges Ahead

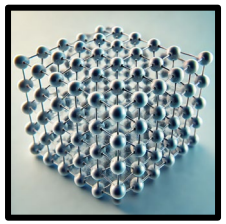
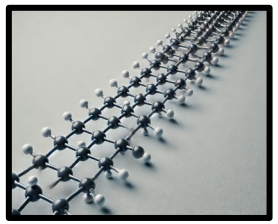
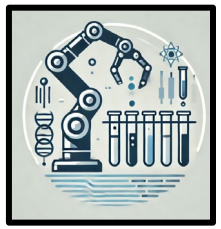
CHIPS Manufacturing USA institute



ManufacturingUSA

Network Opportunity

Collaborative Opportunity

AI/AE for Rapid, Industry-informed Sustainable Semiconductor Materials and Processes

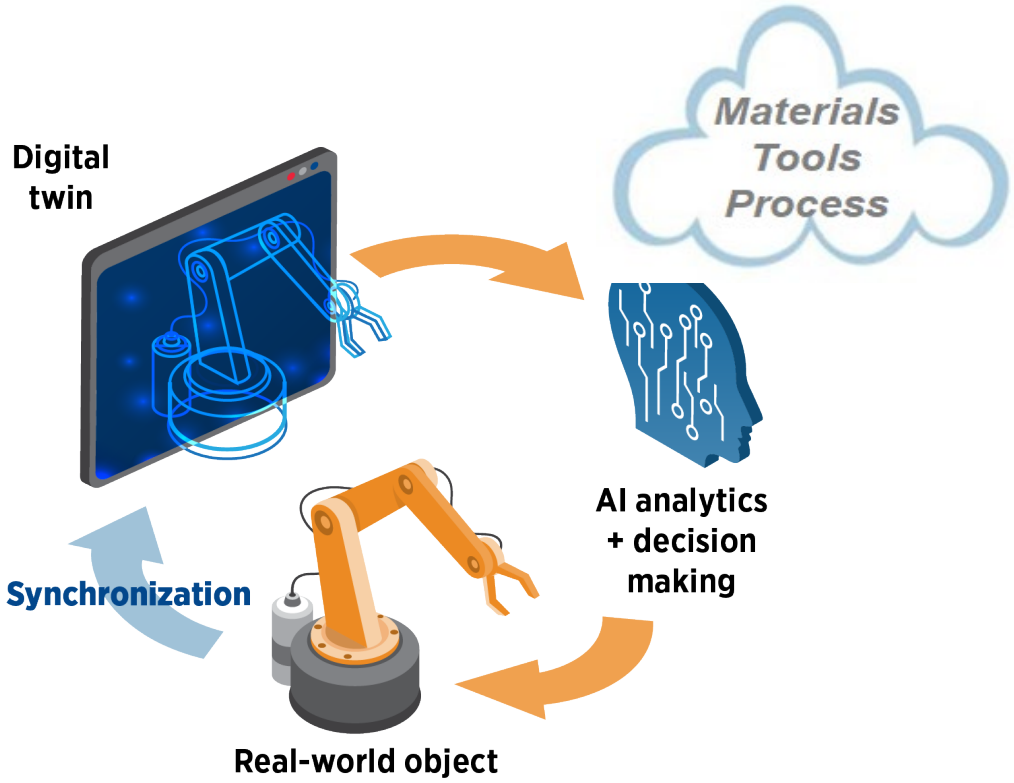
Collaborations, per the Digital Twin NOFO

- The Digital Twin institute will collaborate with CHIPS programs and related federal government programs
- The NOFO includes a roadmap and engaging members to refine on an annual basis.

CARISSMA NOFO Opportunity

- Recipients are required to be a collaborative partner with the CHIPS Manufacturing USA Institute
- Collaborate with the Manufacturing USA Network
- Technical members developing new materials could contribute to roadmaps
- The Manufacturing USA computational backbone could incorporate data from the AI/AE for Rapid, Industry-informed Sustainable Semiconductor Materials and Processes

The challenges for the Digital Twin Institute



A virtual representation or model that serves as the real-time digital counterpart of a physical object or process with real-time decision making

Objectives

- Innovate faster and at less manufacturing cost
- Access innovation from a diverse supply chain
- Shorten process design and validation times
- Improve facility performance and sustainability
- Enhance training modalities

Institute-level Challenges

- **Fragmentation** – Access **integrated data** needed to accelerate Digital Twin capabilities and deliver real-world solutions through AI tools
- **Lack of Trust** – Build **collaboration** through strong leadership, trust, shared risks, and mutual rewards.
- **High Barrier to Entry** – Significant **financial investment** needed limits innovation from small and medium-sized manufacturers, academia, gov't labs

CHIPS Manufacturing USA: Digital Twin Institute

Vision

Enable seamless integration of digital twin models into the U.S. semiconductor manufacturing, advanced packaging, assembly, and test industry, enabling the rapid development and adoption of innovations and enhancing domestic competitiveness for decades.

Mission

The CHIPS Manufacturing USA Institute will foster a collaborative environment within the domestic semiconductor industry, enabled by shared facilities; support industry-led solutions through funded research projects; accelerate technology towards commercialization through significant co-investment; and enable digital-twin workforce training.

Program Scope

Institute-level targets

Applicants proposed specific Institute-level technical targets, representing significant improvements over the current state of the art for semiconductor-industry digital twins and real-world semiconductor manufacturing.

- Technical targets
- Non-technical targets

Operational Areas

Consistent with the mission and objectives, responsive applications to this NOFO addressed each (of the 4) Operational Area (OA)

Activities

The applicant will develop activities for each operational area that will lead to the institute level targets.

Collaboration is Critical for Success

Active Participation from a wide-range of organizations

Network of Manufacturing USA Institutes

CHIPS R&D Programs

Relevant Federally funded efforts

We encourage you to begin identifying your research outputs and collaborative partnerships with the CHIPS Manufacturing USA Institute

Operational Areas

OA1

Institute Operations

Leadership across industry, academia, Govt

OA2

Shared Capabilities

Shared Access to physical and computational capabilities for interoperable solutions

OA3

Industry Solutions

Member-define solutions

OA4

Workforce Training

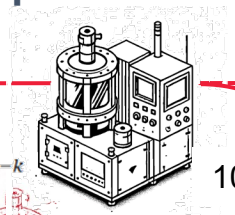
Workforce capacity increase

Technical Challenges Ahead

Short & Full-loops and Advanced Packaging

Deposition

$$\sum_{k=0}^{n} \binom{n}{k} Sensor^{k} material^{n-k}$$



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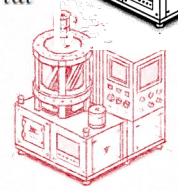
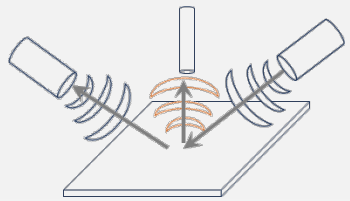
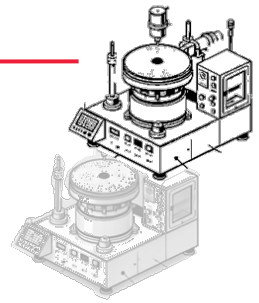


Unit Process

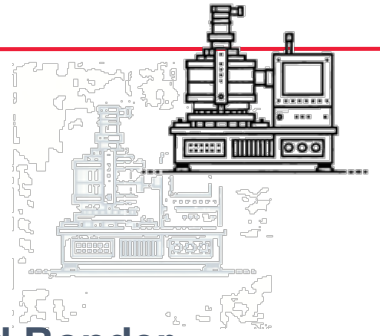
Inspection



Photoresist



Lithography



Etch

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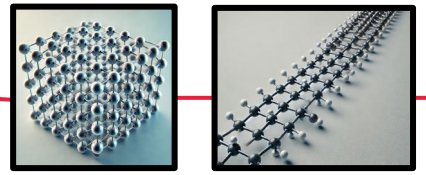
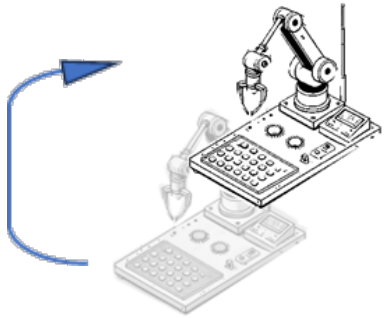
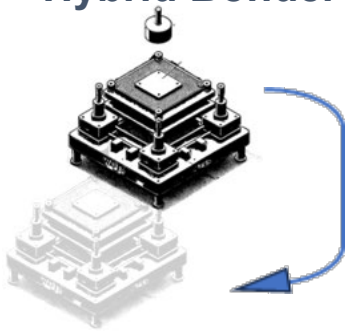
Materials Innovation



Pick and Place



Hybrid Bonder



Standards

Federated Data to HPC Cloud

Ontology Data Sets

Stacked Data for AI Models

Fab Performance
Sustainability simulation
Co-optimization design

CHIPS Manufacturing USA Institute Objectives

Convene stakeholders across the semiconductor production ecosystem

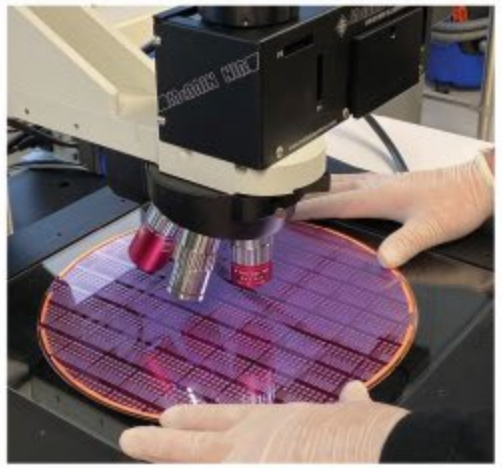
Improve the state of the art in manufacturing-relevant digital twins

Significantly reduce cost for U.S. chip development and manufacturing

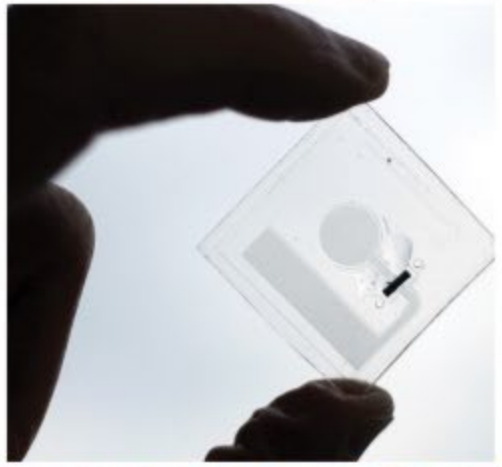
Improve development cycle times of semiconductor product innovation

Advance digital twin-enabled curricula for training a domestic semiconductor workforce

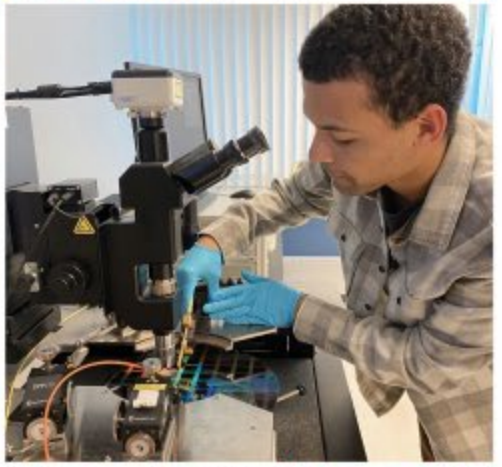
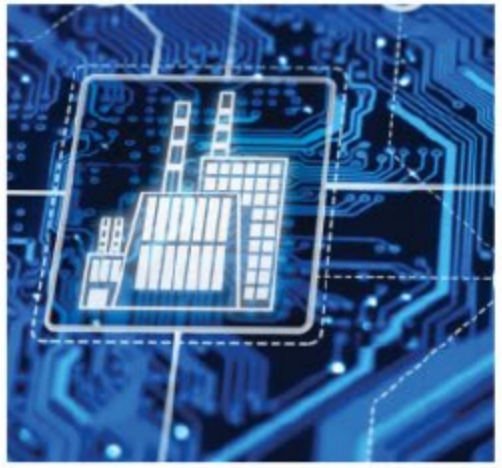
Create a digital twin marketplace for industry to access digital models



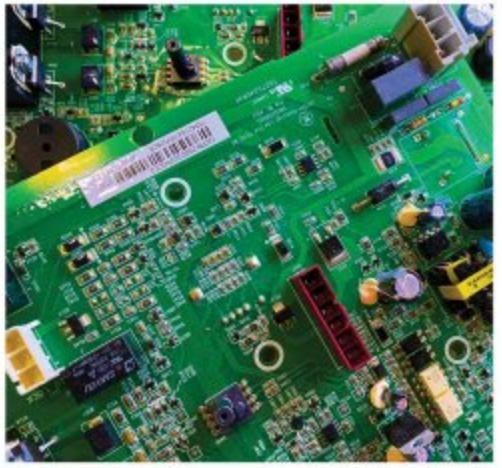


ManufacturingUSA





NSTC Overview

Scott Shepard
Technical Program Manager
CHIPS NSTC Program

The National Semiconductor Technology Center (NSTC)

The NSTC is a **public-private consortium** operated by **Natcast**, a purpose-built, non-profit entity. Natcast works in tandem with the CHIPS NSTC Program, which sits within the U.S. Department of Commerce.

15 USC 4656(c): “conduct research and prototyping of advanced semiconductor technology and grow the domestic semiconductor workforce to strengthen the economic competitiveness and security of the domestic supply chain”

Goals:

1. Extend U.S. leadership in foundational technologies for future applications and industries and strengthen the U.S. semiconductor manufacturing ecosystem.
2. Reduce significantly the time and cost to prototype innovative ideas for member organizations.
3. Build and sustain a semiconductor workforce development ecosystem.

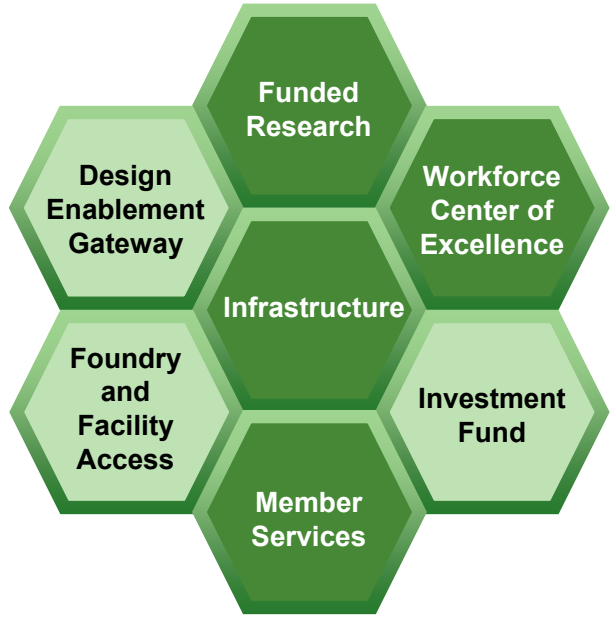



Image Credit: J. Stoughton/NIST

Sustainability –

the ability to meet the needs of the present without compromising the ability of future generations to meet their own needs

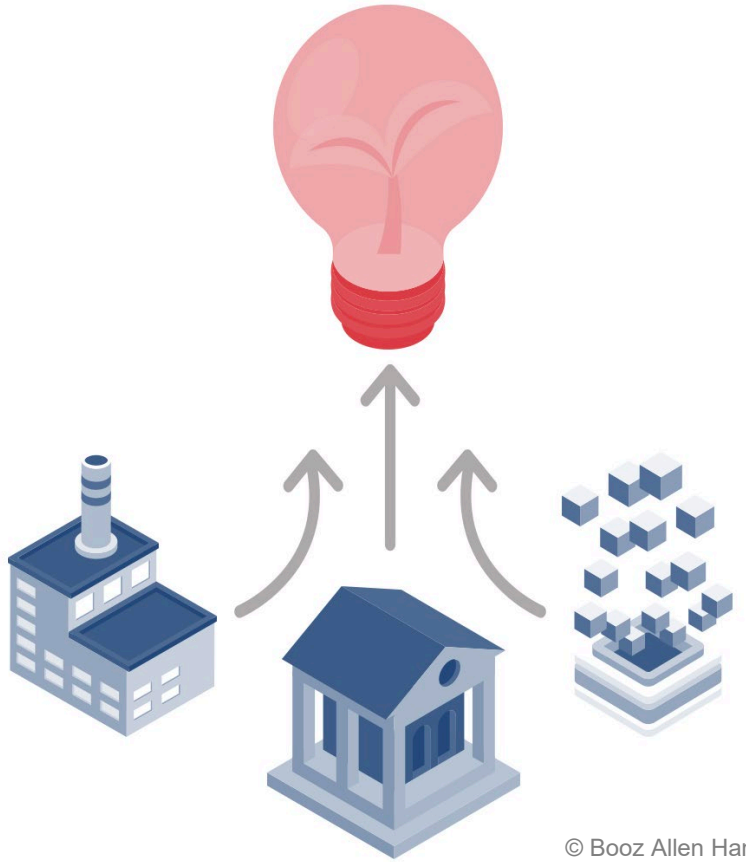
- Environmental Impact
- Economic Viability
- Human Health and Safety
- Supply Chain Readiness

Sustainable Semiconductor Manufacturing

Key Industry Sustainability Drivers

If not addressed, these create economic risk

- Manufacturing Processes
  - **Chip fabs use immense amounts of water and energy.**
  - Building and operating fabs is **expensive**
- Regulatory/Litigation Pressure
  - **Emissions:** 5 million metric tons of CO_2-equivalents emissions from F-GHGs in 2022.[1]
  - **Supply chain risk:** Suppliers of PFAS chemicals are exiting the market.[2]
- Products (Customer Driven)
  - **It is estimated that data centers consume 2% of all U.S. electricity**.[3]
  - Consumers want more efficient products!



[1] Environmental Protection Agency, "Fluorinated Greenhouse Gas Emissions and Supplies Reported to the GHGRP"
[2] 3M, "3M to Exit PFAS Manufacturing by the End of 2025"
[3] Semiconductor Research Corporation, "MAPT Microelectronics and Advanced Packaging Technologies Roadmap"

F-GHGs - Fluorinated-Greenhouse Gases PFAS - Perfluoroalkyl and polyfluoroalkyl substances.

CHIPS for America

$39 billion for incentives

Two component programs to:

1. Attract large-scale investments in advanced technologies such as leading-edge logic and memory, and advanced packaging
2. Incentivize expansion of manufacturing capacity for mature and other types of semiconductors

$11 billion for R&D

Four integrated programs to:

1. Conduct research and prototyping of advanced semiconductor technology
2. Strengthen semiconductor advanced packaging, assembly, and test
3. Enable advances in measurement science, standards, material characterization, instrumentation, testing, and manufacturing

Together with CHIPS initiatives from other agencies, including DOD, State, NSF, and Treasury

PRISM and CARISSMA Overview

PRISM

Focus

Characterize and mitigate PFAS emissions from semiconductor manufacturing without altering existing chemistries

Where to Apply

Natcast.org

Total Award Anticipated Funding

$35M, 8–15 anticipated awards

Lead Applicants

All organizations eligible for NSTC membership

CARISSMA

Focus

Leverage AI and Autonomous Experimentation (AI/AE) to advance innovation in new, sustainable materials

Where to Apply

Grants.gov

Total Award Anticipated Funding

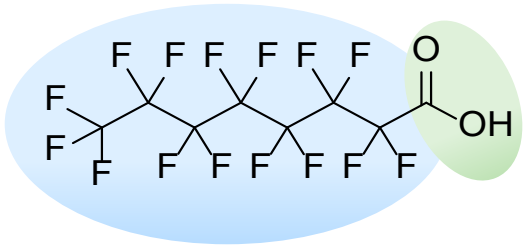
$100M, 2–5 anticipated awards

Lead Applicants

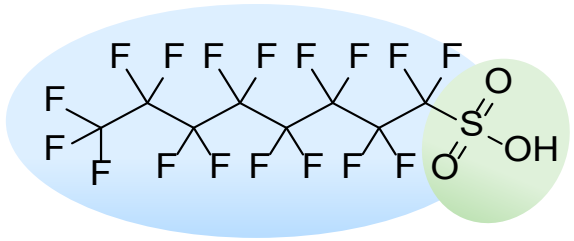
Universities and similar research institutions

Both Funding Opportunities Open Now!

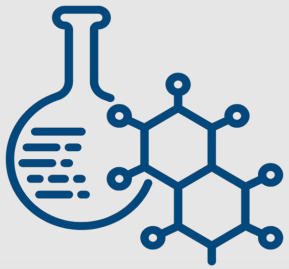
PFAS: Persistent and Bioaccumulative Chemicals



PFOA – C_8



PFOS – C_8



Chemistries

- Photoresists
- Anti-Reflective Coatings
- Top Coats for Immersion
- Wet Etchants
- Surface Treatments
- Etch/Chamber Clean Gases
- Heat Transfer Fluids
- Surfactants
- Surface Mount Materials

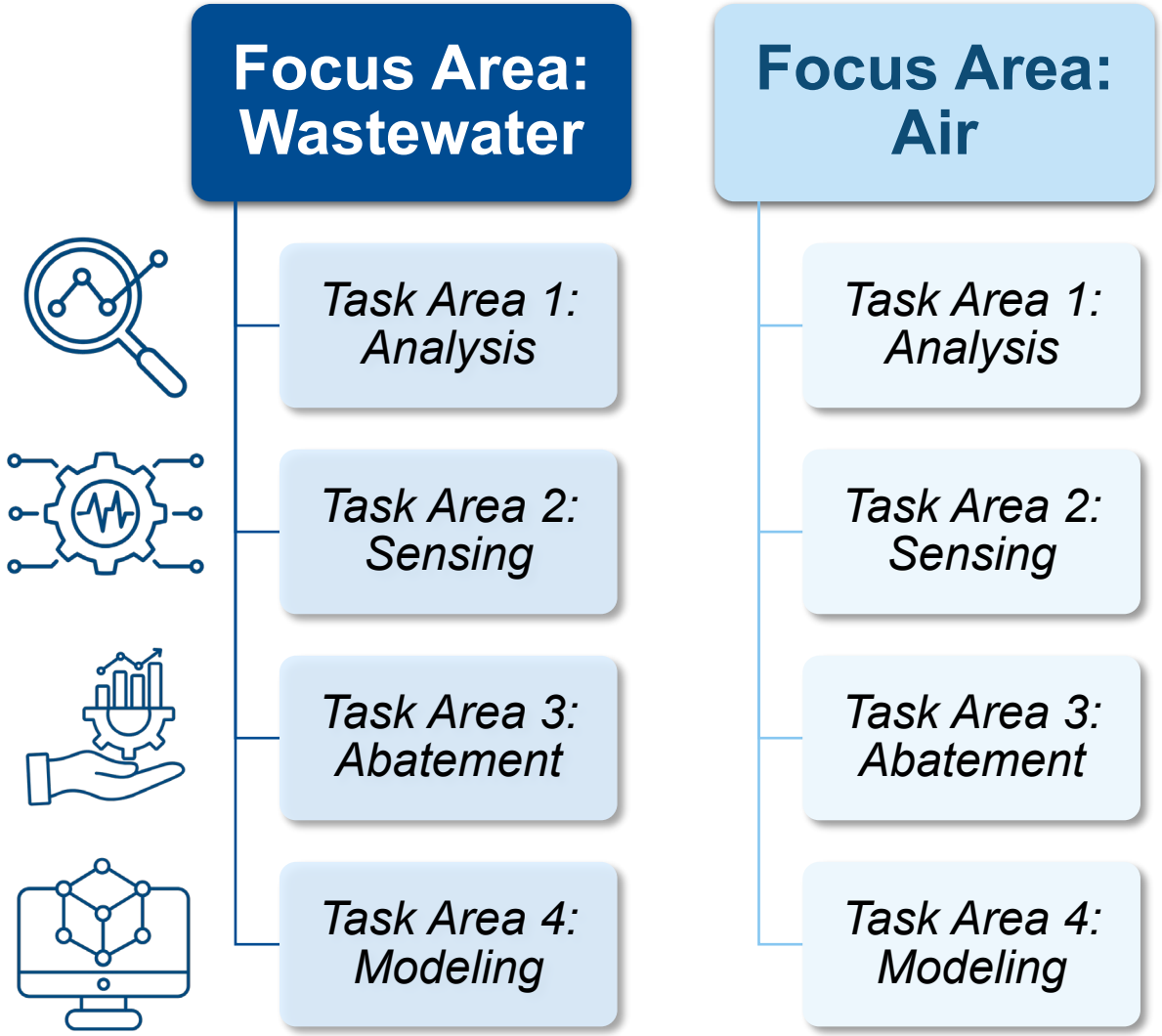
PFAS have unique properties which give them complex functions and performances…

- Fluorinated “super acid” for photolithography
- Low refractive index and surface energy
- Hydrophobicity and oleophobicity prevents intermixing between material layers
- Help achieve uniform coating on wafers
- Thermal and chemical stability

To address the challenge, we first need to understand…

- Which PFAS are being used in manufacturing processes and can we quantify them?
- Which PFAS are being emitted in wastewater and air?
- Which PFAS will need to be treated?

PFAS Reduction and Innovation in Semiconductor Manufacturing (PRISM)



2 Focus Areas

4 *Task Areas*

2 Project Phases

PRISM Program Details

NSTC

- **Anticipated Numbers:** Total program funding up to $35M with 8-15 awards anticipated
- **Eligibility:**
  - Must be NSTC members at the time of award
  - Must be eligible to become NSTC members to propose
- **Cost Sharing Requirements:** None

Anticipated Key Dates

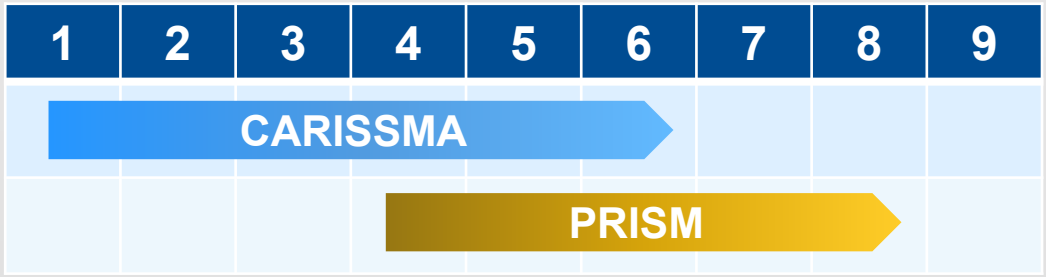
Call for Proposals Released	November 8, 2024
Proposers' Day	November 19, 2024
Concept Papers Due	December 4, 2024
Full Proposals Due	January 20, 2025
Target Project Start	June 2025

PRISM/CARISSMA Synergy

PRISM and CARISSMA are separate but complementary programs to enhance sustainability of semiconductor manufacturing.

- Addressing PFAS requires deployment of **abatement solutions** (PRISM) and **replacements research** (CARISSMA)
- CARISSMA also addresses broader sustainability goals than PFAS, including electricity and water consumption
- PRISM focuses specifically on technology development
- CARISSMA will also invest in research infrastructure and building capabilities

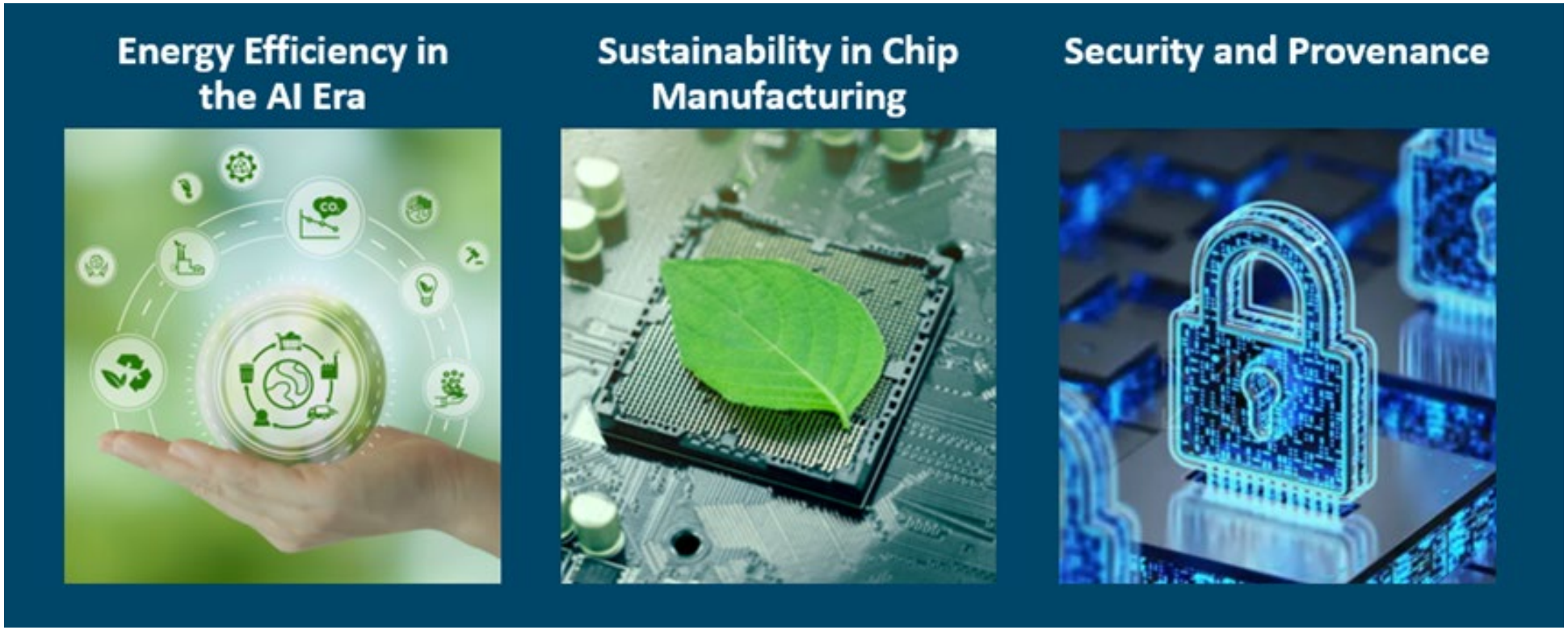
Technology Readiness Level (TRL)



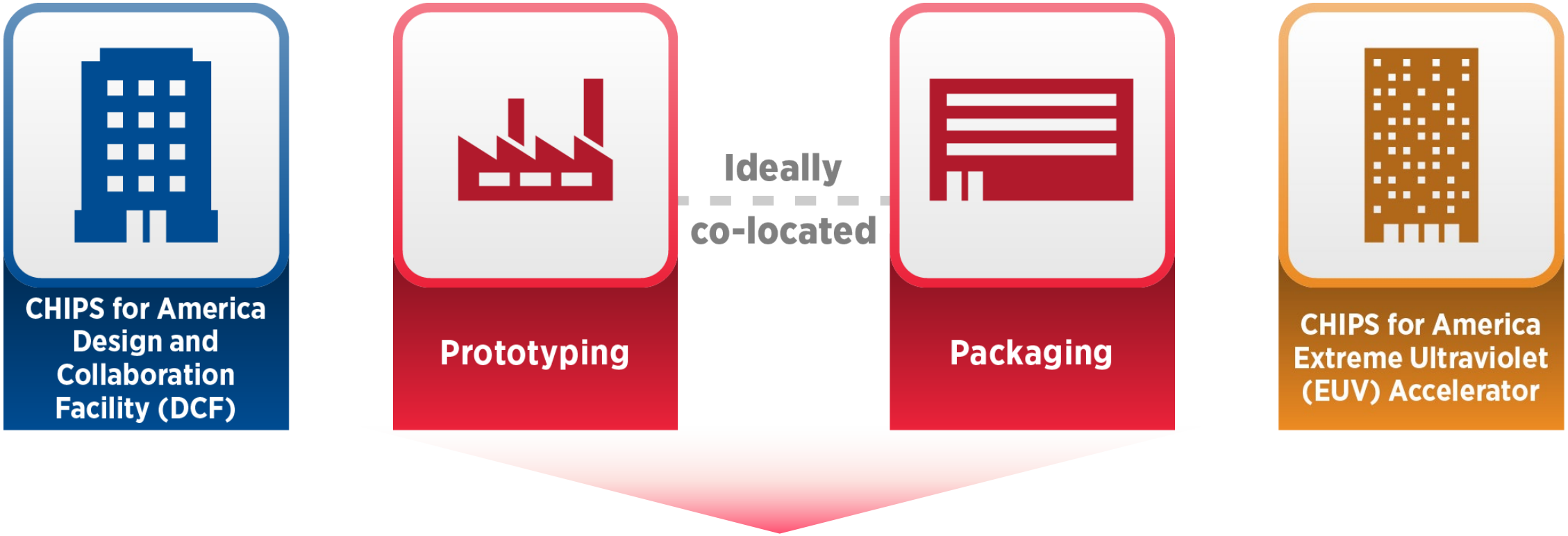
- CARISSMA will accelerate the discovery and validation of new materials to reduce time to deployment of early TRL innovations
- PRISM fill fund demonstration of rapidly deployable solutions already demonstrated at early TRLs

Future NSTC R&D

The NSTC has announced **Key Drivers of Economic and National Security** to help guide initial, future R&D. PRISM and CARISSMA will help bring the community together and produce data, results, and intellectual property to support future efforts in sustainability.



NSTC R&D Facilities Model



The CHIPS R&D facilities model recommends co-located R&D prototyping and advanced packaging capabilities to further both the NSTC and NAPMP programs.

Join the NSTC Community of Interest

Get Engaged

Sign up for email updates

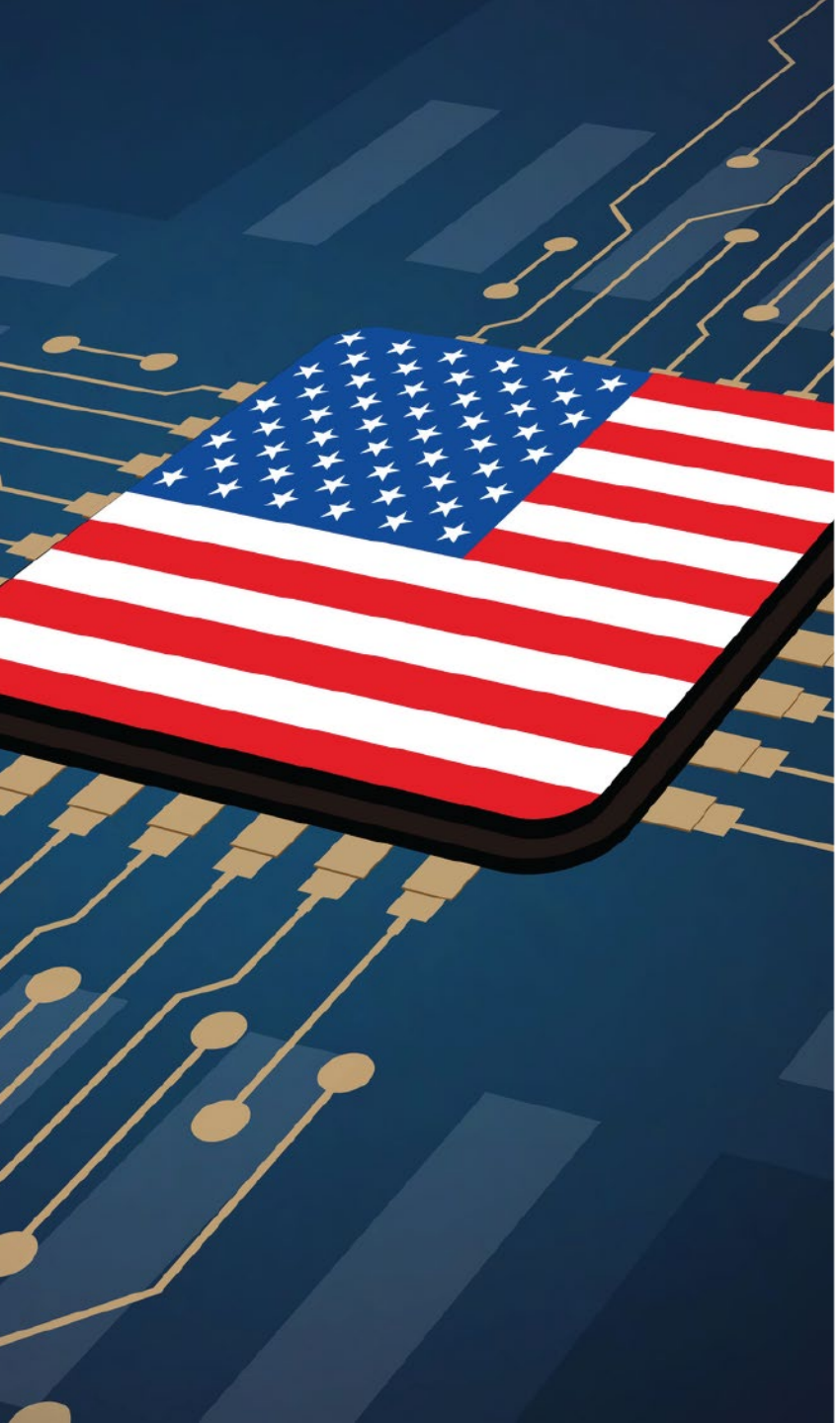
- CHIPS for America: CHIPS.gov
- Natcast: Natcast.org

Get in contact

- CHIPS: askchips@chips.gov
- Natcast: info@natcast.org

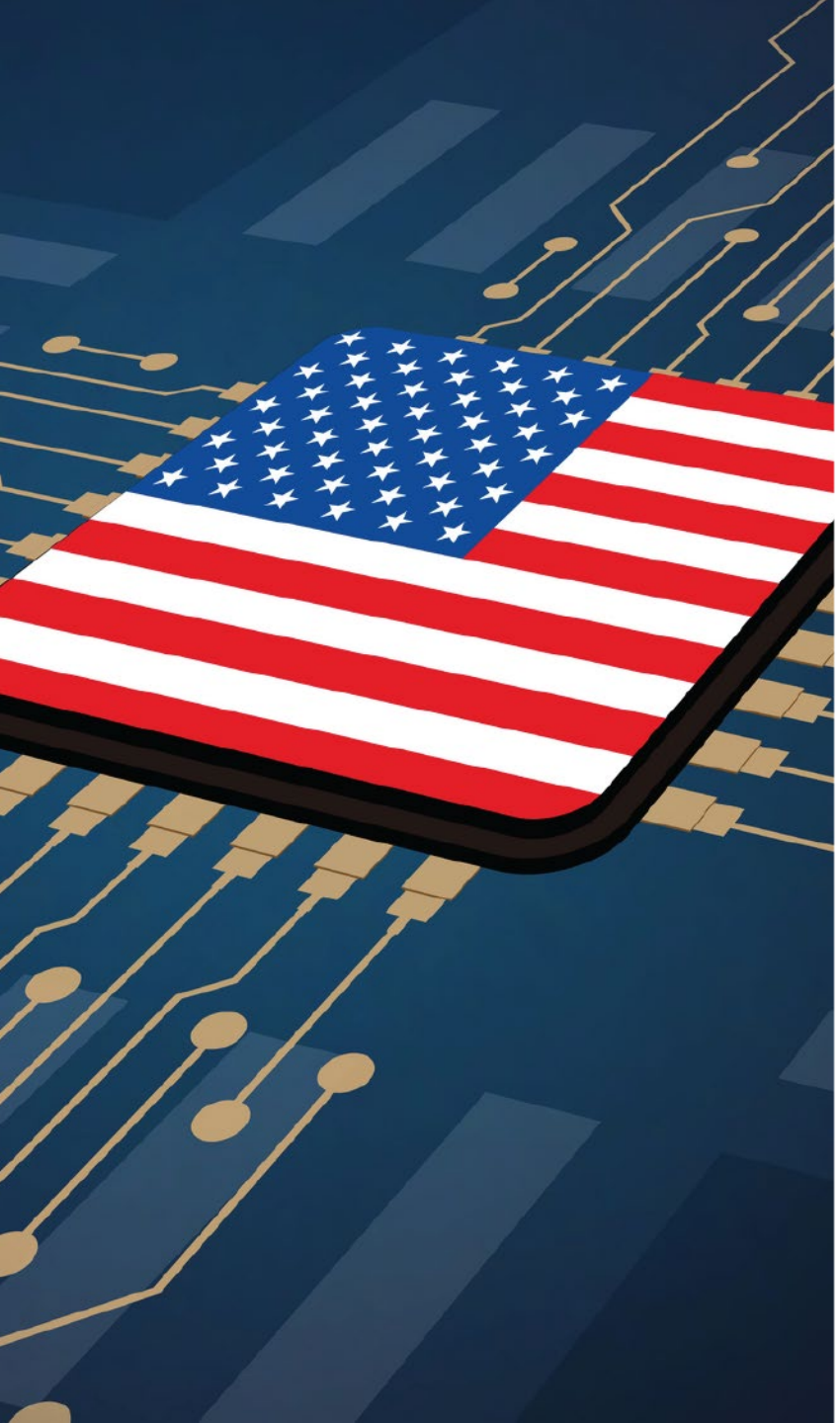
CHIPS CARISSMA: Teaming to Meet Program Goals

Carol Handwerker
Head of Technology Strategy
CHIPS Program Office



CARISSMA NOFO Objectives

1. **Accelerate research** into **and delivery** of targeted, industry-relevant, sustainable semiconductor materials and processes through the application of AI/AE;
2. **Propagate models for incorporating sustainability metrics** into semiconductor industry materials design and discovery, in addition to continued advancement in power, performance, area, cost, or other relevant technology metrics;
3. Expand the capabilities of emerging research institutions and other emerging R&D participants through **cohesive, innovative teams of universities, industry, government labs, and other stakeholders**; and
4. **Build an exceptional workforce** of university graduates and faculty with AI/AE R&D expertise.



CARISSMA NOFO Goals

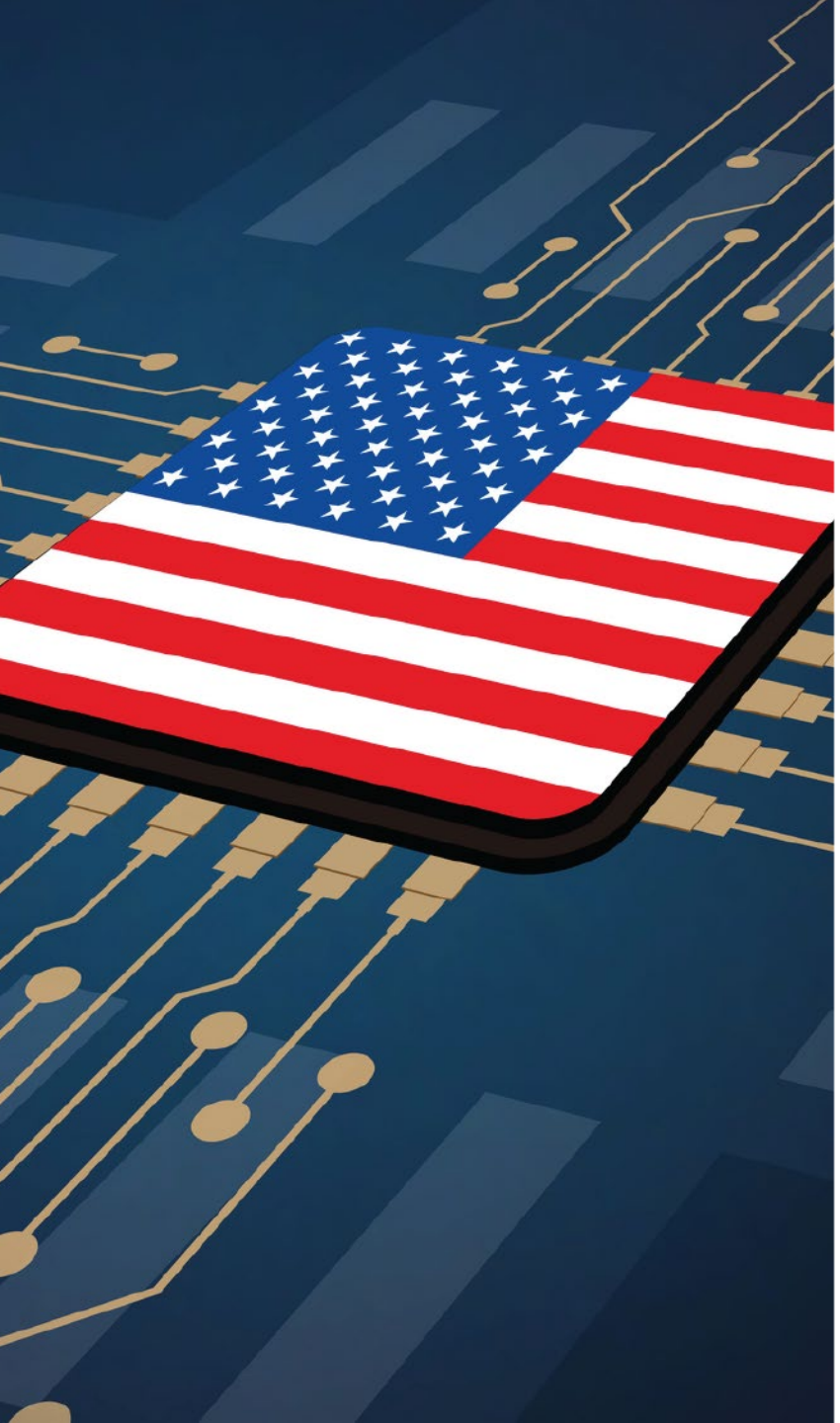
If successful, the NOFO will:

- Demonstrate that new sustainable semiconductor materials and processes, meeting industry needs, can be designed and adopted for industry testing within five years.

- Accelerate a step-change in the number of universities, researchers, and graduates participating in the U.S. semiconductor R&D ecosystem

To meet the goals and objectives:

- CHIPS R&D strongly encourages applications from multi-disciplinary, multi-organization project teams that collectively demonstrate the full range of expertise, experience, and development capabilities needed to achieve the objectives of this NOFO



University-led Project Teams

RESPONSIVE APPLICATIONS MUST PROPOSE A COLLABORATION AMONG:

- One or more semiconductor industry companies
- Research universities and/or national laboratories with demonstrated experience in AI/AE or in related fields
- At least one ERI R&D partner (or a domestic non-profit or for-profit organization that manages a consortium of ERIs)

RESPONSIVE APPLICATIONS ARE ENCOURAGED TO:

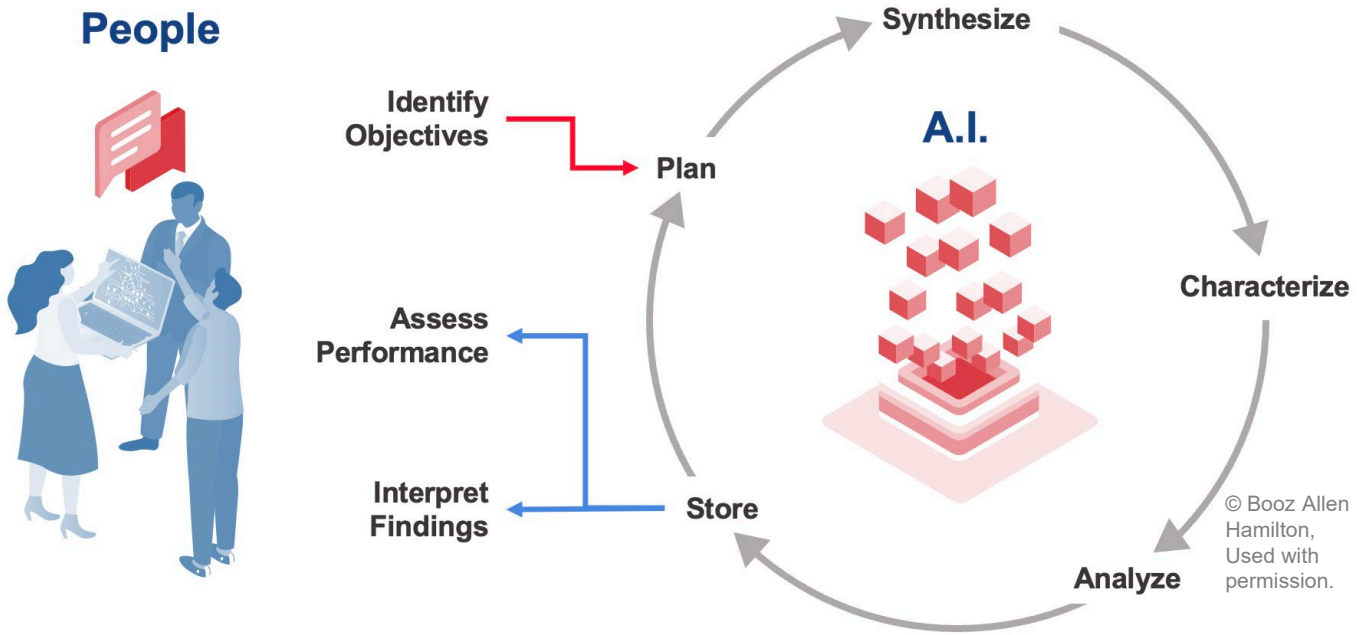
- Include civil society or labor organizations focused on environmental sustainability or human health and safety
- Involve multi-disciplinary, multi-organization project teams that collectively demonstrate the full range of expertise, experience, and capabilities needed to achieve NOFO objectives.

Opportunity: AI/AE AI Powered Autonomous Experimentation, a.k.a. Self-Driving Labs (continued2)

Background on Components of AI/AE Systems

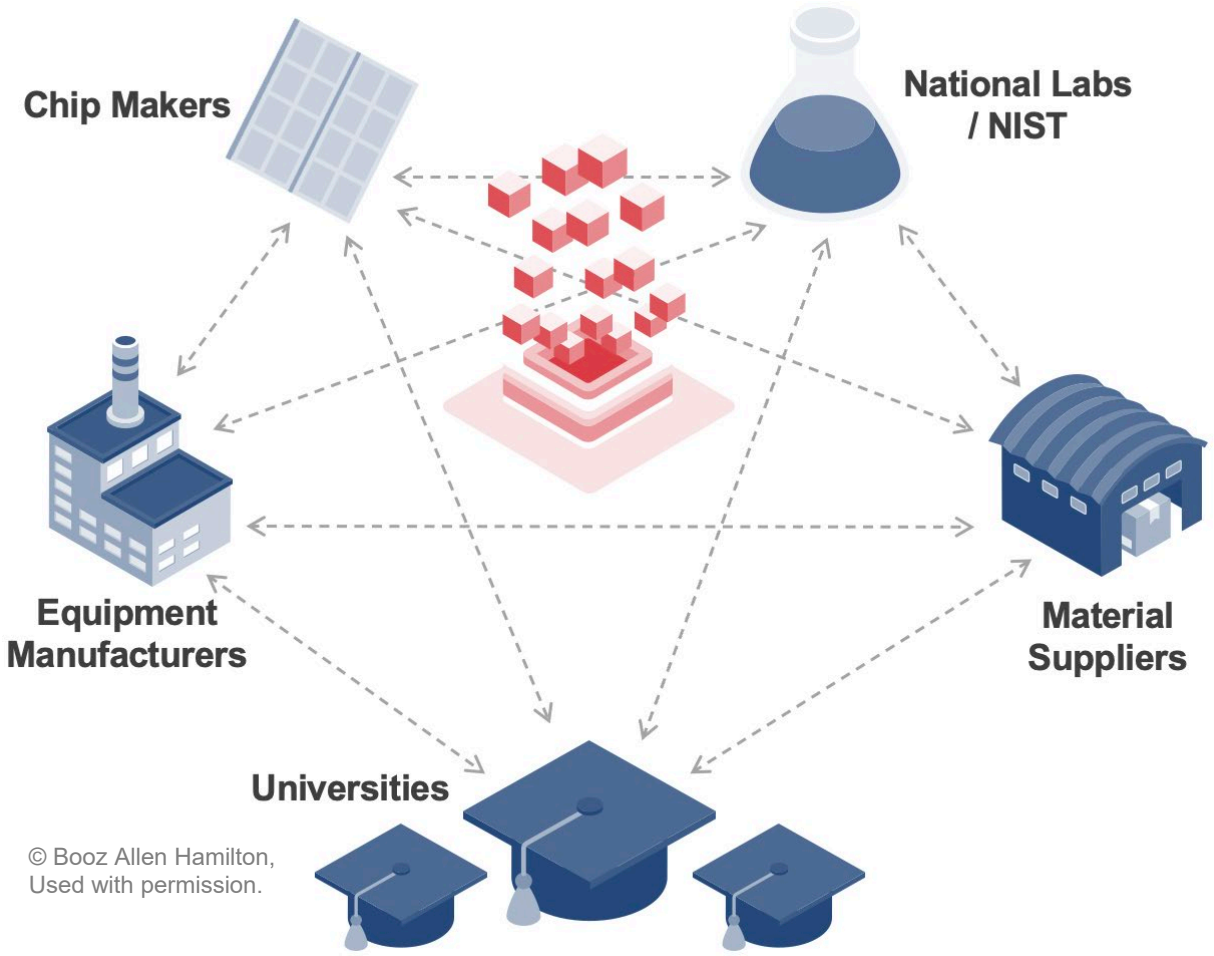
- ***AI/AE: What is it?***
  1. Automated (robotic) laboratory equipment
  2. Rapid/automatic characterization enabled by AI-trained pattern recognition
  3. Automated data storage and analysis
  4. Decision algorithms or planners to decide the next round of synthesis, (return to step 1 or go to step 5)
  5. Output: Materials for technical development by industry
- ***AI/AE Benefits***
  - Accelerate materials R&D
  - More time and resources for the researcher, while simultaneously reducing biases and errors
  - Simultaneous multi-dimensional or multi-parameter optimization

AI/AE System Overview



Humans initialize the closed-loop cycle, assess performance, and come to conclusions based on the reported results. The AI/AE system iteratively plans, experiments, and analyzes the data autonomously.

Partnership and Collaboration Models



Federated AI/AE

- Structures can range from a more centralized “hub” to a fully federated model
- Federation of the digital and physical infrastructure of AI/AE systems is both possible and potentially desirable
- AI/AE researchers can virtualize pieces of the workflow and digital objects (e.g., computer code, digital twins, data, and control software enabling remote operation)
- “Multi-agent” approach, which combines information from diverse research campaigns, can support AI/AE research strategies
- Ability to remotely access equipment hosted by collaborators from other institutions.

Highlight Teaming and Collaboration Model

- **Teaming and Collaboration Requirements**
  - Industry Organizations
  - Established Research Organizations
  - Emerging Research Institutions
  - Civil Society *(encouraged, not required)*
- **Examples of Federated Models**
  - Single problem, redundant exploration
  - Single problem, multiple pieces
  - Multiple problems, multiple pieces

Proposal Elements:

1. Project Team Description
2. Stakeholder Collaboration strategy
3. Broader Impacts Statement
4. Table of Funded Participants and Unfunded Collaborators
5. Letters of Commitment
6. Letters of Interest

"Responsive applications … **must propose establishing a collaboration** among one or more semiconductor industry companies, research universities or national laboratories with demonstrated experience in AI/AE or in related fields, and at least one ERI (or a domestic non-profit or for-profit organization that manage a consortium of ERIs)."

Teaming and Collaboration:
Industry, Civil Society, and Labor Organizations

Private sector organizations can ensure that **"Co-optimization Targets and the resulting Phase-specific Research Plans** meet industry needs and support both technology commercialization, environmental sustainability and human health and safety."

What might prospective team members provide?

- Establish the need for new materials and processes based on identified technology, economic, and sustainability goals and help set the research agenda
- Participate in R&D execution, including testing and lab-to-fab, and provide direct feedback on relevant material characteristics as well as human health, safety, and environmental impacts
- Inform techno-economic analyses, to show commercial viability and identify pathways to domestic production
- Join the Research Advisory Board
- Inform education and workforce development targets, and provide opportunities for student mentorship, internships, and hiring
- Provide optional co-investment, such as IP, staff, and facility access
- Organize the supply chain to accelerate adoption for industry testing within five years and domestic production

Where must we describe collaboration?

- Project Team Description
- Stakeholder Collaboration Strategy
- Physical Infrastructure Plan
- EWD Plan and CVDP Plan
- Table of Collaborators
- Letters of commitment

How will proposals be evaluated?

- *Economic Relevance*: Potential for industry adoption
- *Management*: Experts, facilities, and lasting collaborations
- *Impact Strategy*: Contribution to domestic manufacturing
- *Workforce*: Industry alignment

Teaming and Collaboration:
Established Research Organizations with Experience in AI/AE

Responsive applications must include " research, universities, or national laboratories with **demonstrated experience in AI/AE** or in related fields." Proposals must identify " key staff, leadership, and technical experts… with qualifications and experience appropriate to the proposed work."

What might prospective team members provide?

- Establish and manage high-performance teams with the needed expertise in AI/AE to meet the goals of the program
- Develop and execute models for interdisciplinary, multi-organization collaboration
- Leverage existing AI/AE systems and programs and extend them to sustainable semiconductor materials
- Provide access to existing data systems and materials characterization infrastructure
- Develop new infrastructure, as needed, for the sustainable semiconductor materials under investigation
- Leverage institutional resources for use in the program
- Provide guidance for accelerating R&D and technology transfer across the team, including linkages to industry
- Train next generation AI/AE researchers

How might we describe collaboration?

- Project Team Description
- Physical Infrastructure Plan
- Research and Infrastructure Strategy
- Table of Collaborators
- Letters of commitment

How will proposals be evaluated?

- *Economic Relevance:* Long-lasting domestic R&D capabilities
- *Technical Merit:* Knowledge of the current state of the art
- *Management:* Experts, equipment, and management structure
- *Workforce:* Rational and feasible targets

Emerging Research Institutions (ERIs)

Challenge

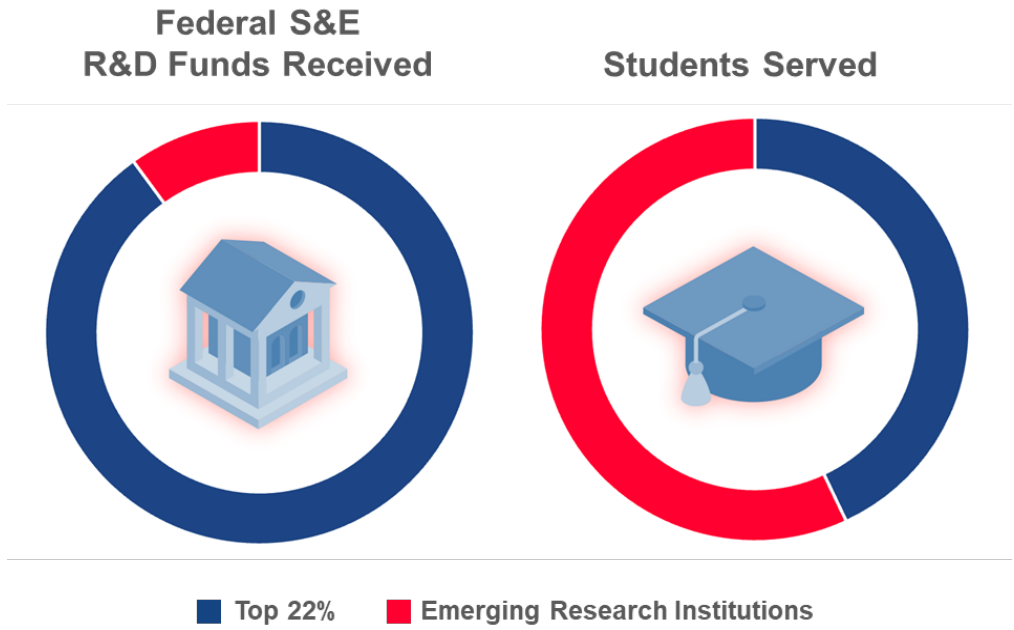
How can we dramatically increase participation of ERIs in semiconductor research, especially AI/AE materials research?

Opportunity

ERIs have untapped potential to bolster semiconductor research.

What is an ERI?

- An ERI is a higher education institution that receives less than $50M in federal research expenditure each year
- A list of ERIs is available via the Department of Energy Office of Science, as of September 2024 **(https://science.osti.gov/grants/Applicant-and-Awardee-Resources/Institution-Designations)**



Source: American Physical Society

Teaming and Collaboration:
Emerging Research Institutions

NOFO Requirement: “The Project Team Description must include faculty from one or more ERIs serving as a Principal Investigator or co-Principal Investigator relevant to [AI/AE Infrastructure and Research]”.

What might prospective team members provide?

- Lead or join an R&D partnership with established AI/AE research organizations and industry, providing one or more PIs/co-PIs
- Provide R&D expertise to high-performance teams to meet the goals of the program
- Leverage existing AI/AE systems and programs and extend them to sustainable semiconductor materials
- Strengthen the AI/AE R&D infrastructure at ERIs. Develop a model for interdisciplinary, multi-organization collaboration that supports R&D collaborations at ERIs
- Train the next generation of AI/AE researchers
- Provide guidance for accelerating R&D and technology transfer across the team

Where should we describe collaborations?

- Physical Infrastructure Plan (denote equipment at ERIs)
- Faculty Development Plan (show ERI research capacity growth)
- EWD Plan (specify targets at ERIs)
- Table of Collaborators
- Letters of Commitment (state ERI research role)

How will proposals be evaluated?

- *Economic Relevance:* Long-lasting domestic R&D capabilities at ERIs
- *Technical Merit:* Knowledge of the current state of the art
- *Management:* Experts, equipment, collaboration mechanisms
- *Workforce:* Rational and feasible targets

Highlight R&D Capability and Capacity Development

- **Teaming and Collaboration Requirements**
  - Industry Organizations
  - Established Research Organizations
  - Emerging Research Institutions
  - Civil Society *(encouraged, not required)*
- **Examples of Federated Models**
  - Single problem, redundant exploration
  - Single problem, split exploration
  - Multiple problems

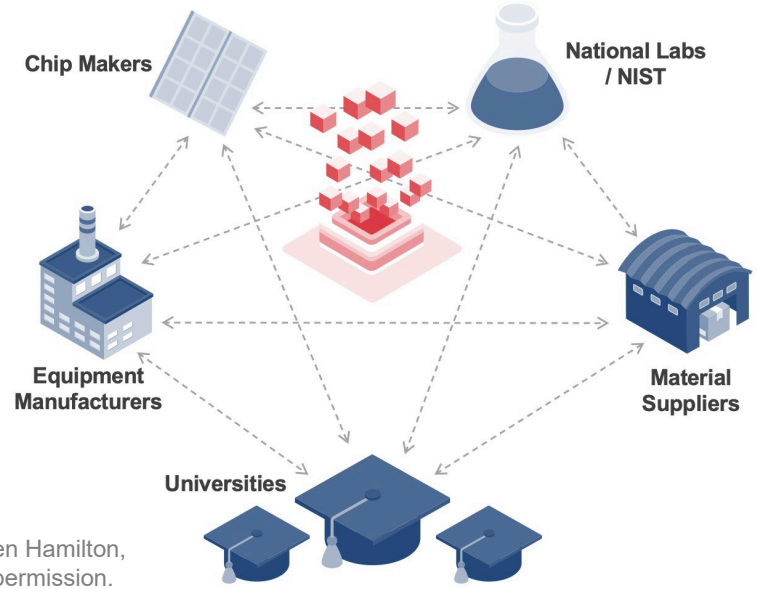
Proposal Elements:

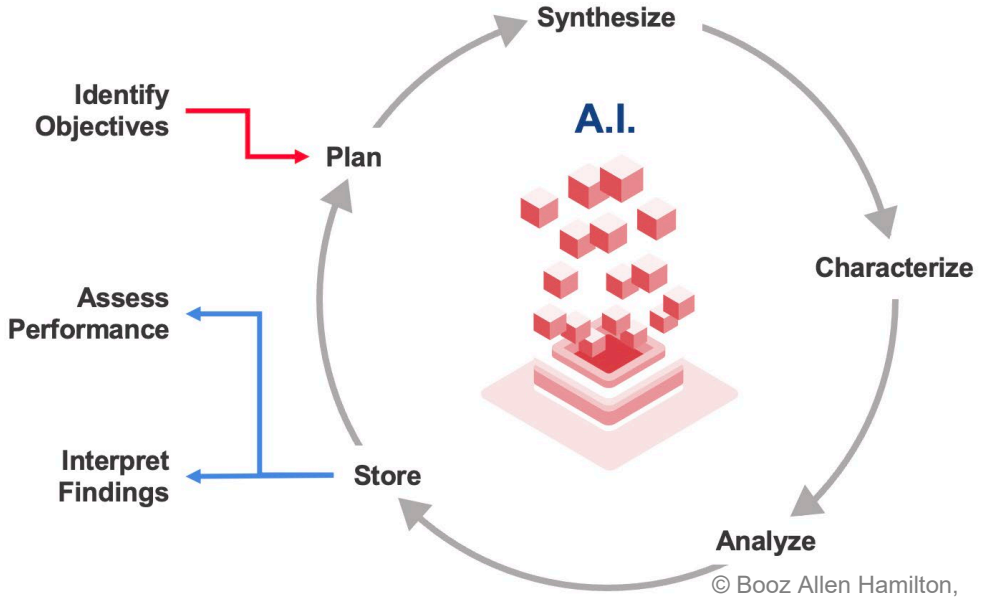
1. Physical Infrastructure Plan
2. Project Team Description
3. Faculty Development Plan

"Significant federation of the digital and physical infrastructure of an AI/AE system is both possible and potentially desirable. … CHIPS R&D encourages models that allow participating collaborators to remotely access equipment hosted by collaborators from other institutions. Other creative models … enabling federated research workflows are also encouraged."

Examples of Federated Models

“Applicants may propose different models for achieving this requirement while meeting their unique infrastructural needs.” The NOFO does not prescribe any single model; proposers should select a model that best meets their goals and objectives.

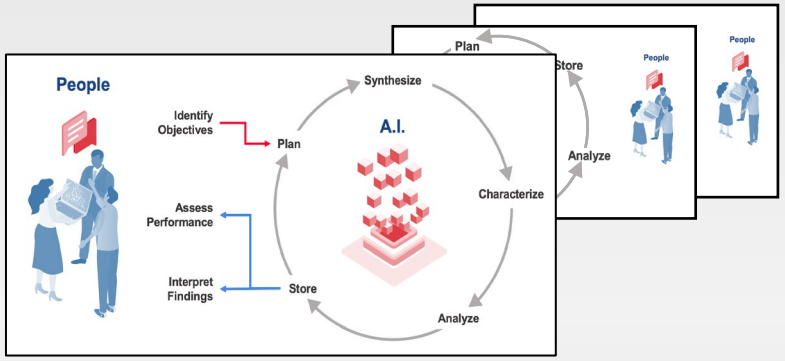




More information on AI/AE available from Materials Genome Initiative Strategic Plan, Report on Autonomous Experimentation for Materials R&D, and Impact Studies MGI.GOV

Examples of Federated Models

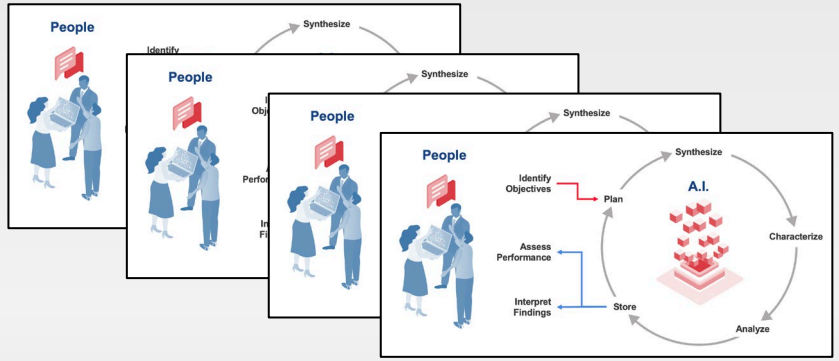
Option: One materials class
More centralized infrastructure



- Primary location (hub) for full-scale synthesis and characterization, with remote access to the necessary infrastructure
- Multiple locations (spokes) for experiment planning and analysis of results, with partial scale synthesis and characterization capabilities

Multiple options available in between

Option: Multiple materials classes
Fully federated infrastructure



- Multiple locations focused on different materials classes, guided by coordinated planning and analysis and shared data
- Multiple locations with infrastructure to conduct similar or different materials characterization and analysis

Proposal teams can select their own structure, so long as (1) the materials classes and applications are clear, (2) targets are achievable, and (3) participant institutions can conduct additional AI/AE campaigns after the completion of this project.

Recommendations from the 2004 NASEM Report on Accelerating Technology Transitions

- Quoted from the 2004 NASEM Report:
  - Focus on target technologies that have been **matched to compelling needs**
  - Determine with industry whether there is an **adequate business case**, including for the supporting supply chain
  - Create a culture that **fosters innovation, rapid development, and accelerated technology transition**, characterized by flexibility, a willingness to take risks, open communication without regard to hierarchy, a sense of responsibility that replaces unquestioned authority, and a commitment to success that goes beyond functional roles.
  - Use an **iterative process of development, implementation, and acceptance**, where technical team and product users are part of the end-to-end decision-making process **(such as AI/AE)**
  - **Empower individuals** to take risks, management must anticipate and plan for failure, and everyone must champion teamwork and collaboration over individual accomplishments
  - **Identify leaders** who can manage complex collaborative interactions, leaders who understand and respect the values, working styles, and goals of different groups and who can also effectively initiate and sustain communication among the stakeholders across all organizational and institutional boundaries.

ACCELERATING TECHNOLOGY TRANSITION
Bridging the Valley of Death for Materials and Processes in Defense Systems, NASEM, 2004

Up Next: Panel Q&A and Poster Session

Panel Q&A

James Warren, Nancy Stoffel, Scott Shepard, Carol Handwerker

SUBMIT Questions for Q&A Session!

Scan the QR code or go to slido.com and enter code CHIPSCARISSMA

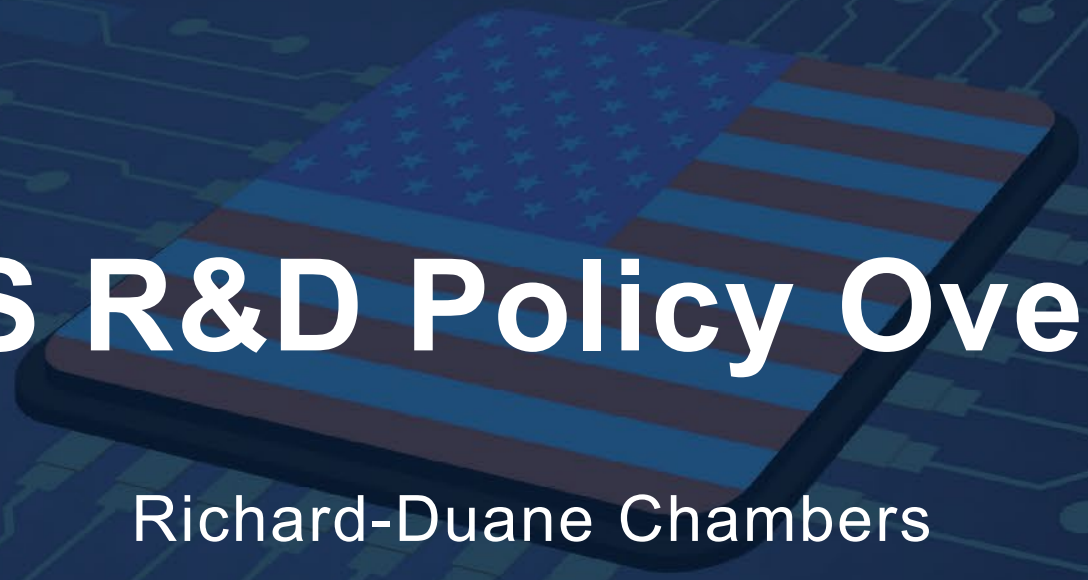
Poster Sessions and Lunch On-Going

In-Person Participants please return from Lunch by 1:50 PM

Virtual Participants please return at 2:35 PM

SUBMIT Questions for Q&A Session!

Scan the QR code or go to slido.com and enter code CHIPSCARISSMA

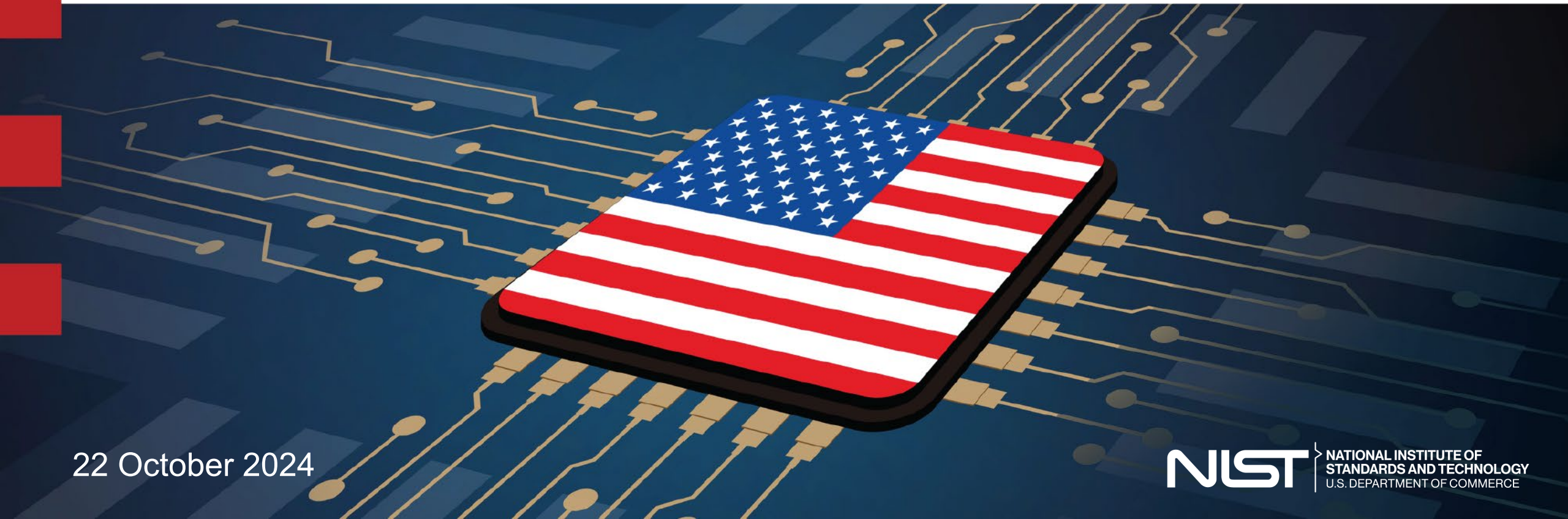


CHIPS R&D Policy Overview

Richard-Duane Chambers
Anita Balachandra

CHIPS for America
CHIPS R&D Office Policy Overview

Richard-Duane Chambers
Gregory Strouse



22 October 2024

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Policy Overview Agenda & Objectives

Agenda

- Overview of CHIPS R&D Office Goals
- International Collaboration
- Unique Directives Informing Work
- Key Required Plans
  - Intellectual Property Rights Management Plan
  - Commercial Viability and Domestic Production
  - Education and Workforce Development
  - Research Security

By the end, attendees should better understand

- CHIPS R&D objectives and policy context
- CHIPS R&D domestic and international research requirements
- Key required plans for proposals

Overview of CHIPS R&D Office Goals

Vision

A vibrant and self-sustaining U.S. domestic semiconductor ecosystem that revitalizes American manufacturing, grows a skilled and diverse workforce, and leads the world in semiconductor research and innovation.

Mission

Accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic tools, resources, workers, and facilities.

2030 Goals

- **U.S. Technology Leadership:** The United States improves its capacity to invent, develop, prototype, and deploy the foundational semiconductor technologies of the future.
- **Accelerated Ideas to Market:** The best ideas achieve commercial scale as quickly and cost effectively as possible.
- **Robust Semiconductor Workforce:** Inventors, designers, researchers, developers, engineers, technicians, and staff meet evolving domestic government and commercial sector needs.

Policy and National Security Context

Unique Directives

CHIPS and Science Act (2022)

- Prohibit Federal funding to participants in malign foreign talent recruitment programs
- Research security training
- Integration of workforce development into R&D efforts

CHIPS Act (2021)

- Domestic production requirements
- Domestic control requirements to protect intellectual property from foreign adversaries
- Workforce initiatives as a required component of most CHIPS-funded activities

Executive Order 14080 (2022)

- Prioritize strengthening and expanding regional manufacturing and innovation ecosystems

National Security Policy Memorandum 33 (2021)

- Research security program requirements
- Disclosure of conflicts of interest / commitment

Application Requirements

- ❑ Foreign Partner Justification
- ❑ Intellectual Property Rights Management Plan
- ❑ Commercial Viability and Domestic Production (CVDP) Plan
- ❑ Education and Workforce Development (EWD) Plan
- ❑ Research Security Plan

Domestic & Int'l Research Requirements

"NIST adheres to the principle that U.S. research leadership benefits from mutually beneficial international collaborations, including welcoming international scientists"

- **Lead applicant must be a domestic entity;** foreign organizations, excluding foreign entities of concern (FEOCs), can participate.
- **Funded R&D activity should occur in the United States** but CHIPS R&D may approve the completion of certain tasks outside the United States.
- **Any disbursement of funds** outside the United States **must be approved by CHIPS R&D.**

Justification for Foreign Participant:

- Foreign partner's involvement is essential to program objectives
- Applicant and foreign partner have adequate IP and data protection agreements in place.
- The partnership doesn't jeopardize the project's pathway to domestic production.
- Foreign partner is not based in a foreign country of concern.
- Foreign partner agrees to comply with nondisclosure agreements, laws and regulations and to undergo a security review.

Who is eligible to apply as the lead applicant?

- Domestic accredited institutions of higher education and domestic non-profit or for-profit organizations that manage consortia of accredited institutions of higher education are eligible to apply for this NOFO.
- A domestic entity is one that is incorporated within the United States (including a U.S. territory) with its principal place of business in the United States (including a U.S. territory). This includes non-profit organizations; accredited institutions of higher education; State, local, and Tribal governments; and for-profit organizations.

What is a foreign entity of concern?

Foreign entities of concern, as defined in 15 U.S.C. § 4651(8) and implementing regulation at 15 C.F.R. 231.104, include entities owned by, controlled by, or subject to the jurisdiction or direction of the governments listed in 10 U.S.C 4872(d): China, Russia, North Korea, or Iran.

An entity is owned by, controlled by, or subject to the jurisdiction or direction of a government of a foreign country where:

(i) The entity is: a citizen, national, or resident of a foreign country listed in 10 U.S.C. 4872(d); and located in a foreign country listed in 10 U.S.C. 4872(d);

(ii) The entity is organized under the laws of or has its principal place of business in a foreign country listed in 10 U.S.C. 4872(d);

(iii) 25 percent or more of the entity's outstanding voting interest, board seats, or equity interest is held directly or indirectly by the government of a foreign country listed in 10 U.S.C. 4872(d); or

(iv) 25 percent or more of the entity's outstanding voting interest, board seats, or equity interest is held directly or indirectly by any combination of the persons who fall within subsections (i)–(iii).

Domestic Control of Intellectual Property

15 U.S.C. 4656(g): "The head of any executive agency receiving funding under this section shall develop policies to require domestic production, to the extent possible, for any intellectual property (IP) resulting from microelectronics research and development conducted as a result of such funding and domestic control requirements to protect any such intellectual property from foreign adversaries."

Key Requirements

- At least one domestic entity must own or co-own any IP from the funded R&D and must have full rights to enforce the applicable IP for a period of years determined prior to the final award.
- The domestic entity must notify NIST before selling, transferring, or assigning ownership of the IP to another entity.
- IP from the funded R&D cannot be sold, transferred, or assigned to a foreign adversary, to include FEOCs and foreign countries of concern. IP cannot be licensed (except in certain limited circumstances) to a foreign adversary.

IP Rights Management Considerations

- Identify any pre-existing IP needed for the project, IP that may be developed with CHIPS R&D funding, and the path for accessing pre-existing or developed IP for new partners or associated recipients.
- Describe any desired deviations from standard IP regulations and terms.
- Describe how the proposed management and ownership of IP support the CVDP plan and any existing or planned protocols to ensure domestic control of CHIPS R&D-funded IP.
- Describe any additional desired licensing provisions.

Frequently Asked Questions

The NOFO states that at least one domestic entity must own or co-own any IP resulting from R&D conducted under the NOFO and have full rights to enforce applicable IP rights for at least a period of years, to be determined prior to the final award. What is a "period of years"?

CHIPS R&D will determine the "period of years" for which domestic control requirements are in effect on a case-by-case basis.

Commercial Viability and Domestic Production

"Applicants should propose measurable CVDP targets that demonstrate the viability of the proposed business model and of domestic production. Where relevant, CVDP milestones should complement technical milestones."

1. **Market Analysis Topics**
2. **Customer Analysis Topics**
3. **Financial Plan Topics**
4. **Domestic Production and Scale-up Topics**

Key Components:

- **Market Analysis:** A clear description of the value proposition of the proposed technology or product and identification of competitors.
- **Customer Analysis:** An assessment of demand for the funded innovation by current and potential customers or categories of customers, at volumes necessary for commercial viability.
- **Financial Plan:** A realistic and sustainable business model that considers cost, revenue, and access to capital.
- **Consensus Building:** Plans to collaborate (e.g., with standards bodies) to promote technology adoption

Key Point: Plans are intended to be an "initial assessment" or an "overview", with updates occurring across the award period. Applicants should not feel compelled to have all the answers before the research is complete!

Given this NOFO's focus on industry-informed, university-based collaborations, CHIPS R&D anticipates that CVDP targets may largely focus on strengthening industry partnerships, conducting technoeconomic analyses, and informing the CVDP through Phase 1. Certain CVDP elements, may be deferred until Phase 1 of the award.

Education and Workforce Development

CHIPS R&D recommends that EWD plans include the following elements, where applicable:

1. Workforce Needs
2. Metrics and Milestones
3. Industry-Relevant Training
4. Strategic Partnerships
5. Recruitment and Retention

Key Components:

- **SMART Targets:** A description of the specific goals EWD activities are expected to achieve and quantifiable metrics (e.g. students trained, graduated, hired, and retained) to demonstrate success toward EWD targets
- **Training Opportunities:** A description of the proposed EWD activities and demonstration of alignment with specific job opportunities and skills needs, consistent with the workforce needs assessment, and leverage known best practices
- **EWD Infrastructure and Curriculum Plan:** A detailed description of any physical or virtual infrastructure that will be made available to support EWD training programs, including research infrastructure as well as any new or modified curricula that will be developed or deployed
- **Recruitment and Retention Information**: A description of efforts to maximize access to and participation in the semiconductor workforce, including efforts to attract and retain a diverse student and trainee population such as supportive services and outreach to underserved communities.

Research Security Agenda & Objectives

Agenda

- Safeguarding CHIPS Science through Research Security
- NIST IR 8484 – Research Security Framework
- Research Security Plan
- Research Security Reviews of NAPMP Applications
- Selected FAQs
- Questions and Contact information

By the end, attendees should better understand

- What is Safeguarding Science and Research Security
- What is the NIST Research Security Framework
- What is a research security plan
- How will an application be reviewed
- Answers to the FAQs
- Who to contact regarding research security

Safeguarding CHIPS Research Science

Safeguarding Science facilitates open science and research security that values collaboration while protecting U.S. national security and economic security interests.

Research Security is protecting the means, know-how, and products of research until they are ready to be shared.

Risks to U.S. Scientific Research Advantages

- **National Security** – Transfer of research products accelerates foreign military applications
- **Economic Security** – Loss of technical advantages results in the loss of U.S. global market competitiveness
- **Intellectual Property** – Some governments violate core research integrity principles and facilitate the transfer of origin al ideas from the United States

NIST IR 8484 – Safeguarding International Science Research Security Framework

Framework Implementation

- Strikes a balance between scientific research security and fostering international collaboration
- Implements a methodology to review research and make risk balanced determinations

Research Security Program Implementation

- Strategic communication and training
- Composite multi-disciplined open-source analysis
- Risk-balanced determination and mitigation
- User friendly tools, checklists, and templates

NIST Internal Report
NIST IR 8484

Safeguarding International Science

Research Security Framework

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Research and Technology Protection
Commerce Office of Security

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Laboratory Programs

Mary Bedner
CHIPS Research and Development Program
CHIPS Program Office

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International and Academics Affairs Office
Director's Office

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August 2023

U.S. Department of Commerce
Gina M. Raimondo, Secretary

National Institute of Standards and Technology
Laurie E. Locascio, NIST Director and Under Secretary of Commerce for Standards and Technology

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Research Security Plan: Key Components

Provide a written plan describing internal processes or procedures to address foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity. Provide a point of contact on research security issues within the project leadership team.

- Establishing a Research Security Team and Policies
- Scope of Program – Assessing At-risk Technologies and IP
- Communication and Training Research Personnel and Staff
- Reviews, Risk Determination and Mitigation
- Reviewing Personnel Appointments
- Reviewing Foreign Travel Requests
- Reviewing Collaboration and Service Requests
- Implementing Technology Control (e.g., Data Mgmt and Export Controls)
- Cybersecurity

Research Security Reviews of CHIPS Applications

- **Understanding the research and type**
  - Fundamental or Proprietary
- **Implementation**
  - Open-source analysis of all relevant information by a multi-disciplined team
  - Risk Analysis (**RAFT**)
    - **R**ecruitment, **A**ffiliations, **F**unding, and **T**echnology
- **Risk Determination - Low, Medium, or High**
  - High does not always mean No
  - May include clarifications and/or mitigations
- **Clarifications and Mitigations**
  - Clarifications are questions that need answers prior to a final risk determination
  - Mitigations are changes that reduce initial risk determination

Standardized Review Process

Proposal

- Critical and Emerging Technology (CET)
- Mil/Civ applications
- Focus of an adversary
- Export control

Applicant Institutions

- Foreign entity of concern
- Foreign ownership, control and influence
- Export control
- Technology control plan
- Cyber-Physical security
- Research Security Plan

Covered Individuals

- Research integrity
- Foreign entity of concern
- Malign foreign affiliations
- Associations with foreign adversaries
- Conflicts of interest and commitment

Frequently Asked Questions

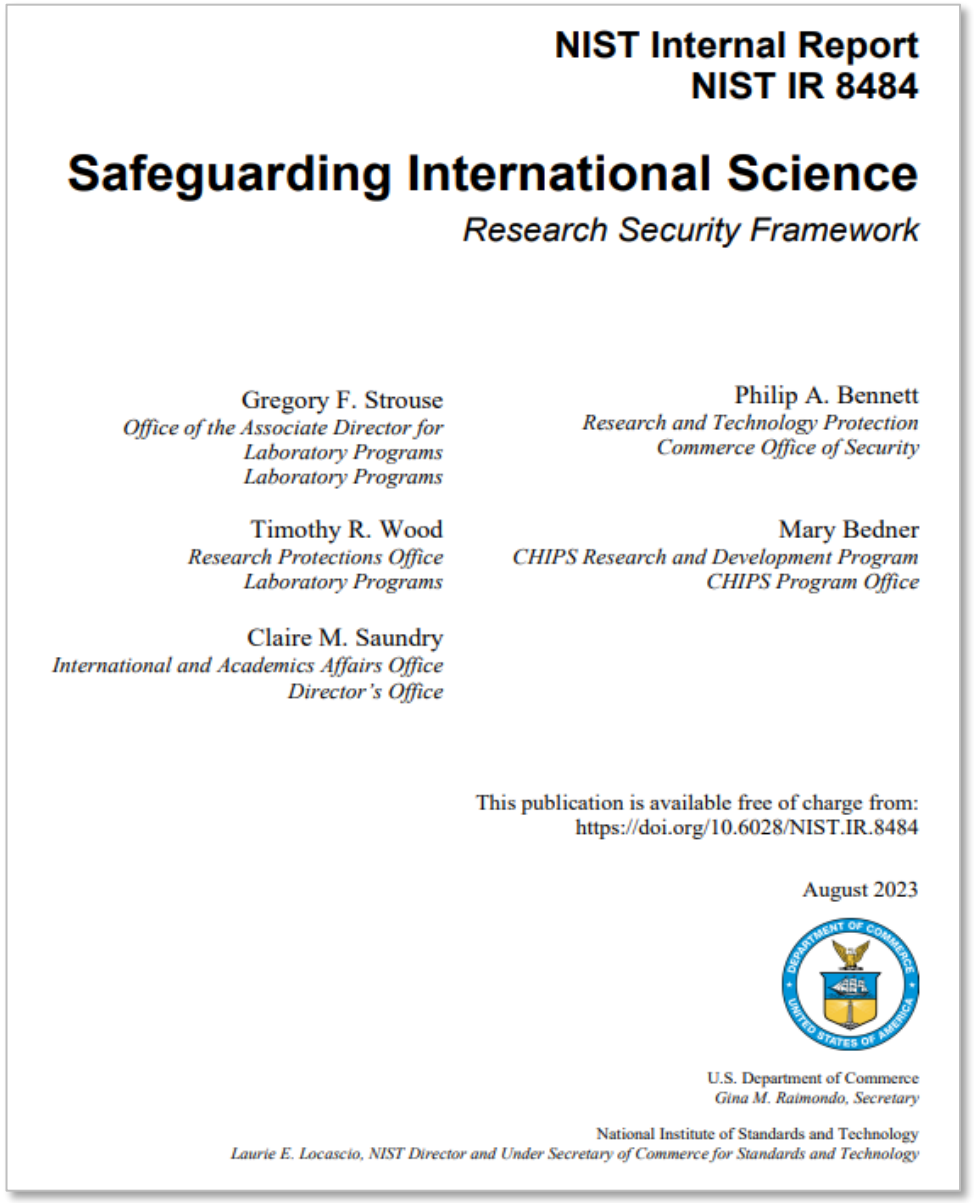
Do entities applying for CHIPS R&D research funds need to demonstrate that they have a research security program in place before applying for a research award and/or before receiving research funding?

- At present, CHIPS R&D does not require applicants to demonstrate the existence of a research security program in order to apply for or receive funding.
- However, applicants must provide a written plan (i.e., a research security plan) describing internal processes or procedures for addressing foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity, as applicable.

Frequently Asked Questions

Will CHIPS R&D provide funding or other resources to establish or improve a research security program or to the meet other CHIPS R&D research security requirements?

- To date, CHIPS R&D has not established any specific programs or set-asides to support the development of a research security program.
- However, limited funding may be available to implement a research security plan, subject to the objectives of the individual notice of funding opportunity (NOFO) and the approval of the relevant program director.
- For entities selected to receive funding, NIST may provide assistance to establish or improve research security activities consistent with NIST best practices (NIST IR 8484).



NIST Internal Report
NIST IR 8484

Safeguarding International Science

Research Security Framework

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Questions?

CHIPS for AMERICA

Contact Information

researchsecurity@nist.gov

Ready, Set, Submit! Application, Preparation, and Submission

Shanell Williams

Ready, Set, Submit!

Concept Paper & Invited Full Application Preparation & Submission

NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Financial Assistance Agreements Management Office

Agenda

PLAN AHEAD TO STAY AHEAD

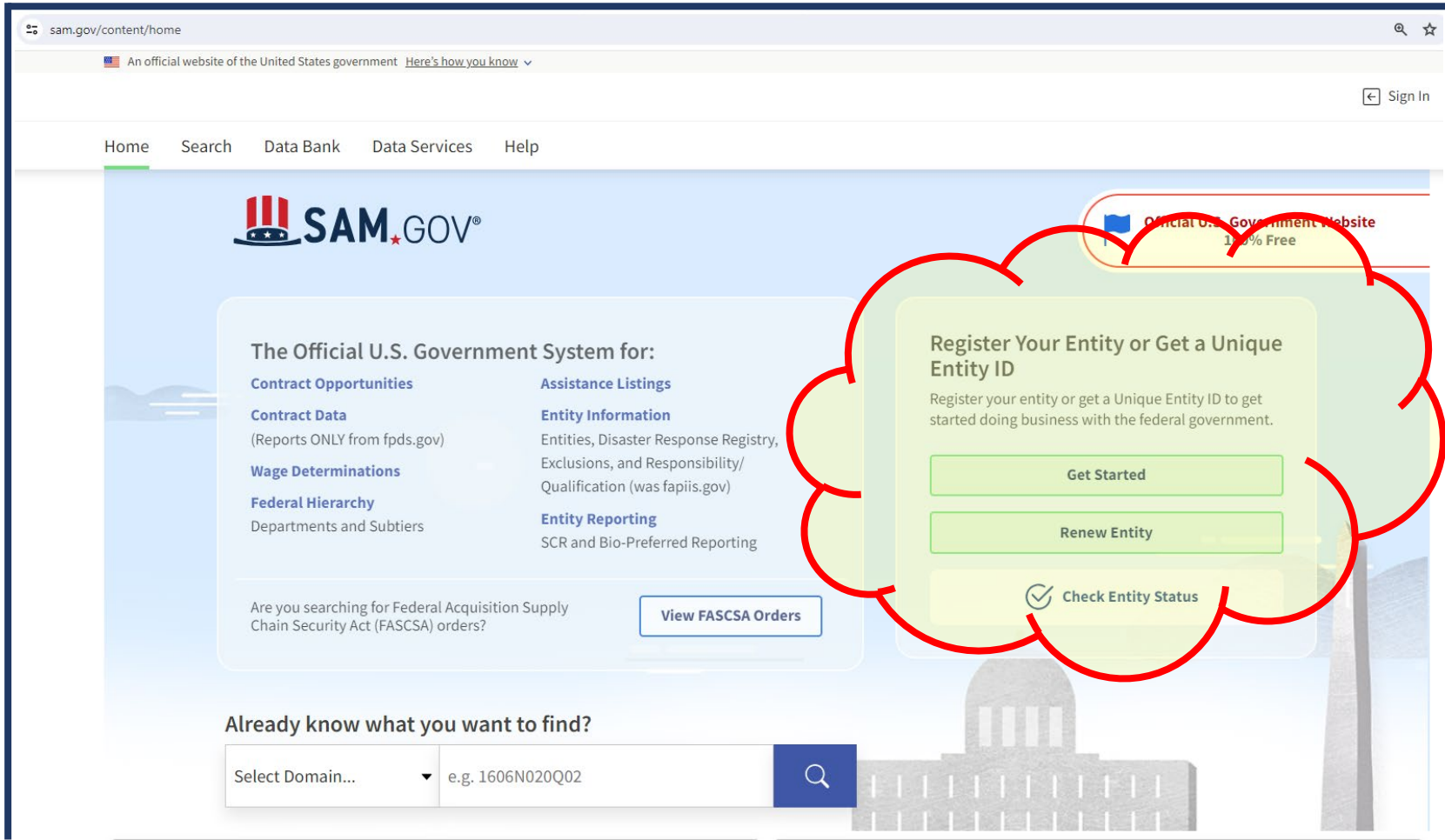
- SAM.gov Registration
- Grants.gov Registration
- Tips for Success

SAM.gov

Link: https://sam.gov/content/home

Help Desk: Monday - Friday from 8am - 8pm EST U.S. calls: 866-606-8220

- 100% FREE to register
- Must have an active account
- Unique Entity Identifier (UEI)
- Start Early: the process takes about 10 days, but can take up to 6 weeks!
- Complete the Representations & Certifications, especially the Financial Assistance Response page
- Register at SAM.gov before Grants.gov



Grants.gov

After obtaining a UEI for your organization from SAM.gov, you must register at Grants.gov. There is no fee to register at Grants.gov. Your organization's EBiz POC must:

1. Create a Grants.gov account with the same email address as used at SAM.gov for the EBiz POC; and
2. Add a profile at Grants.gov using the UEI obtained from SAM.gov.

The EBiz POC can then delegate administrative roles to other users. Read the Help article Manage Roles for Applicant for instructions.

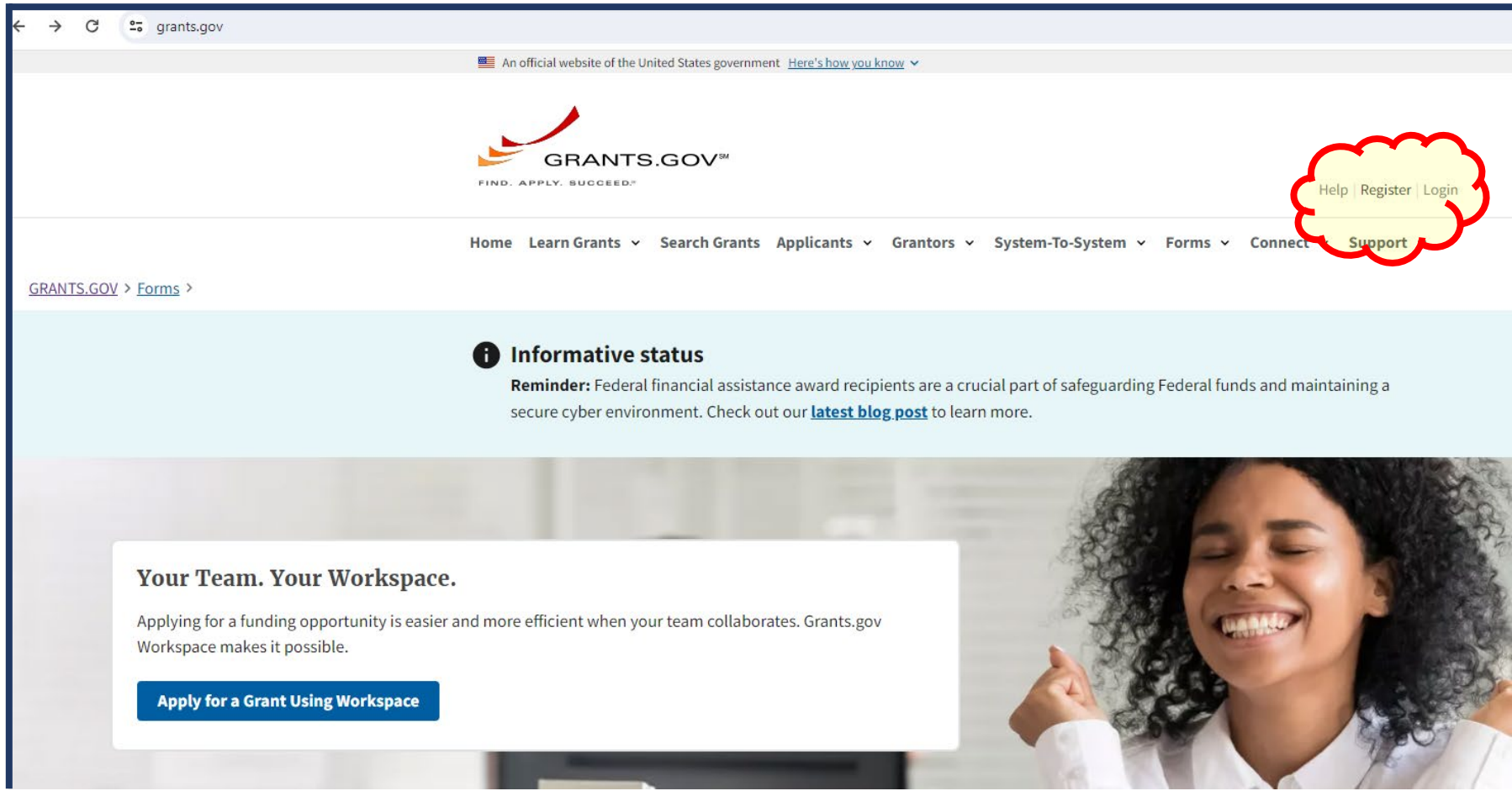
Visit the Grants Learning Center to find information about every phase of the grant management process, from applying and reporting to the award closeout.

Grants.gov *(continued)*

Link: https://www.grants.gov/applicants/applicant-registration

Help Desk: 1-800-518-4726 (24/7 excluding holidays) or support@grants.gov

- 100% FREE to register
- Grants.gov must be used to submit concept papers
- Separate instructions will be provided to applicants who are invited to submit full applications (after concept paper review)
- User Guide
- Applicant FAQs



On-Time Submission

- **All registrations, including SAM.gov, must be completed before the deadline**
  - **Concept Papers and Full Applications must be free of Grants.gov errors; corrective submissions must be made BEFORE the submission deadline and will overwrite previous submissions**

    - Errors stop application processing and must be corrected

    - Warnings do not stop application processing and are corrected at your discretion based on your circumstances

  - **Submit early to allow time to correct any unexpected errors or submission issues**
    - Depending on the size of the file, transmittal may take SEVERAL MINUTES to HOURS.
    - Don’t wait until the deadline date to submit. The system may be slow due to last minute submissions.

Tips for Success

- Understand the submission process stated in the NOFO
- Do NOT submit a full application at Grants.gov until invited
- SAM.gov registration must be active to apply in Grants.gov (Concept Paper & Full Application)
- Use correct UEI and EIN
- Designate the proper roles in the systems (e.g. - Authorized Rep in Grants.gov)
- Utilize “workspace” feature in Grants.gov to draft applications
- Limit the application file size / character limits / page limits per the NOFO
- Make sure you are using compatible software (e.g. - Adobe Reader)
- Do not pay to create accounts
- Late applications will not be accepted
- Register early at SAM.gov and Grants.gov!

Shanell V. Williams

Other Transaction Agreements Officer

E-mail: shanell.Williams@nist.gov with “2025-NIST-CHIPS-AIAE-Sustainability-01 Questions” in subject line

Panel Q&A

James Warren, Richard-Duane Chambers,
Anita Balachandra, Shanell Williams

SUBMIT Questions for Q&A Session!

Scan the QR code or go to slido.com and enter code CHIPSCARISSMA

CARISSMA NOFO Award Information and Timeline

- Up to approximately **$100 million** in total funding
- Individual awards ranging from approximately **$20 million to $40 million**
- Expecting team of **universities and other research entities** with significant experience in AI-powered autonomous experimentation (AI/AE); semiconductor industry partners; emerging research institutions; and civil society organizations focused on environmental sustainability or human health and safety.

Key Dates

Next Steps

- Verify your eligibility and complete all registration requirements.
- Download the NOFO and look through the full document, Contact NIST to address any questions.
- Review the Technical Targets, Co-optimization Targets, and Programmatic Targets. Review all Operational Areas
- Determine Project Team
  - ***Digital poster repository will be available for all Proposers' Day attendees after this meeting! Instructions for access have been or will be sent shortly***
- Draft your concept paper, ensuring all required sections are completed and identified needs are addressed.
- Apply via Grants.gov **by 11:59 p.m. Eastern Time on January 13, 2025.** Give yourself ample time to complete the application.

Resources

- **2025-AIAE-CHIPS-01 NOFO** link: grants.gov/search-results-detail/356912
- **NIST CARISSMA** page: https://www.nist.gov/chips/notice-funding-opportunity-carissma
- **NIST CARISSMA Frequently Asked Questions** (FAQs): https://www.nist.gov/chips/frequently-asked-questions-carissma-nofo
- **CHIPS R&D CARISSMA Program Proposers' Day**: https://www.nist.gov/news-events/events/2024/11/chips-rd-carissma-program-proposers-day
- **CHIPS R&D Funding Opportunities** page: https://www.nist.gov/chips/chips-rd-funding-opportunities
- **Strategic Opportunities in U.S. Semiconductor Manufacturing**: https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

Thank You!

For any questions, reach out to askchips@chips.gov