CHIPS for America Research & Development (R&D) Facilities Model & Process

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  - Are informational, pre-decisional, and preliminary in nature.
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CHIPS for America

$39 billion
for incentives

Invest in U.S. production of strategically important semiconductor chips, and assure a sufficient, sustainable, and secure supply of older and current generation chips for national security purposes and for critical manufacturing industries.

$11 billion
for R&D

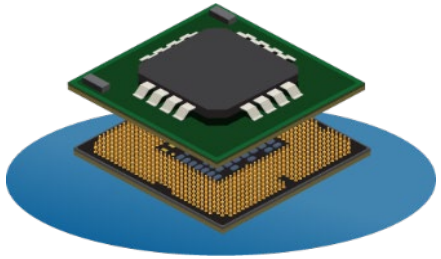
Strengthen U.S. semiconductor research and development (R&D) leadership to catalyze and capture the next set of critical technologies, applications, and industries.

$2 billion
for DoD Microelectronics Commons

A national network that will create direct pathways to commercialization for U.S. microelectronics researchers and designers from “lab to fab.”

Workforce Initiatives

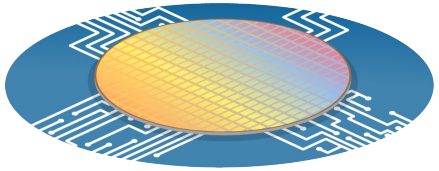
CHIPS R&D Programs



CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast

Natcast is a purpose-built nonprofit organization and operator of the NSTC consortium



CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

Manufacturing USA

CHIPS Manufacturing USA Program

CHIPS Metrology Program

Workforce Initiatives

The NSTC and NAPMP

NSTC

A **public-private consortium**, the National Semiconductor Technology Center (**NSTC**) is where members will have access to facilities, partners, and additional funding opportunities around R&D, an investment fund, and scaling up technologies and workforce activities.

The NSTC is operated by **Natcast**, a purpose-built, non-profit entity. Natcast works in tandem with the CHIPS NSTC Program, which sits within the U.S. Department of Commerce.

NAPMP

The National Advanced Packaging Manufacturing Program (**NAPMP**) is one of the programs within the **CHIPS for America Research & Development Office**. Its goal is to establish U.S. leadership in advanced packaging and provide the technology needed for packaging manufacturing in the U.S.

Within a decade, NAPMP-funded activities, will establish a vibrant, self-sustaining, profitable, high-volume, onshore packaging industry where advanced node chips manufactured in the U.S. are packaged in the U.S.

NSTC Roadmap: 4 Year View

2022

Setting the Foundation

- ✓ CHIPS Legislation Passed
- ✓ Released an RFI

2023

Engaging the Ecosystem

- ✓ Published NSTC Vision & Strategy
- ✓ Natcast, a non-profit organization, was independently established
- ✓ Engaged with thousands of stakeholders and participated in public events

Jan-Apr 2024

Establishing the NSTC

- ✓ Anticipated $5 billion investment
- ✓ Natcast selected as the NSTC operator
- ✓ Signed the consortium agreement
- ✓ Natcast launched the Community of Interest
- ✓ Hosted two public events with CHIPS & Natcast
- ✓ Natcast released an RFI on Facilities and Capabilities

May

NSTC Roadmap

- ✓ Facilities Model and Selection Process
- ✓ Workforce Partnership Alliance Program
- ✓ NSTC initial R&D funding call for proposals for AI-based RF design
- ✓ NSTC R&D Proposers' Day for AIDRFIC
- ❑ R&D funding call for proposals for development of test vehicles

We are HERE

Summer

- ❑ Update on Facilities Search
- ❑ NSTC R&D Proposer's Day for test vehicles
- ❑ Open Membership

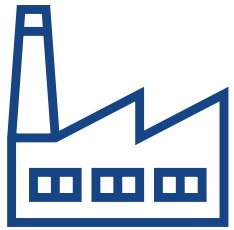
Fall

2025

Growing the NSTC

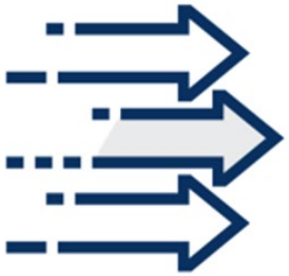
- ❑ Additional member services introduced

The Road Ahead



Facilities

Workforce Development



Jump Start Projects

Invite Members

Filling Key Gaps in the Ecosystem

Identified U.S. Market Gaps

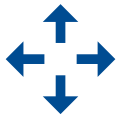
- Slow R&D cycle times for experiments with prototyping capabilities
- High costs and long wait times to facilities limit the speed of innovation
- Limited collaborative sites for leading researchers to access commercial tools
- No independent research packaging facilities to test prototypes
- Limited independent facility to mature technologies with new materials and architectures on a stable CMOS baseline

CHIPS for America R&D Facilities Solutions

- Faster cycles of learning with additional on-shore capability
- Unlock opportunities for frequent use of cutting-edge equipment and tools
- Central location to enable and encourage researchers to collaborate and test experiments on commercial tools
- Introduce at-scale advanced packaging research domestic capability
- Experimentation on full-flows at commercial-grade, including larger scale for “more than Moore” experiments

NSTC Facilities Key Principles

Accelerate Innovation: Enable world class R&D across the full range of microelectronics technical areas—including access to extreme ultraviolet (EUV) lithography, which is needed for research using the most advanced patterning technology



Create Differentiation: Ensure there is a clear value to the semiconductor ecosystem beyond existing comparable facilities

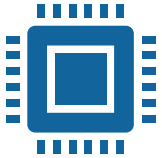
Financially Sustainable: Create enduring value for decades and attract investment from all types and sizes of companies

Be Independent and Neutral: Enable Natcast, on behalf of the NSTC, and the NAPMP to make strategic decisions about the operation of the facilities, and by ensuring that the facilities are places where all member entities and their employees have the opportunity to successfully innovate

Thriving and Vibrant Ecosystems: Provide, foster, and grow a talented workforce and a robust ecosystem of semiconductor companies, educational and research institutions, and local support to advance the mission

Ecosystem Feedback from RFI Respondents

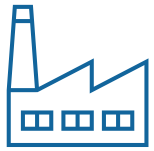
Industry	Partnership & Consortia	Educational Institutions	Government
52	9	17	1



High Interest in Packaging:

- Nearly all respondents indicated interest in advanced packaging access and increasing U.S. competitiveness

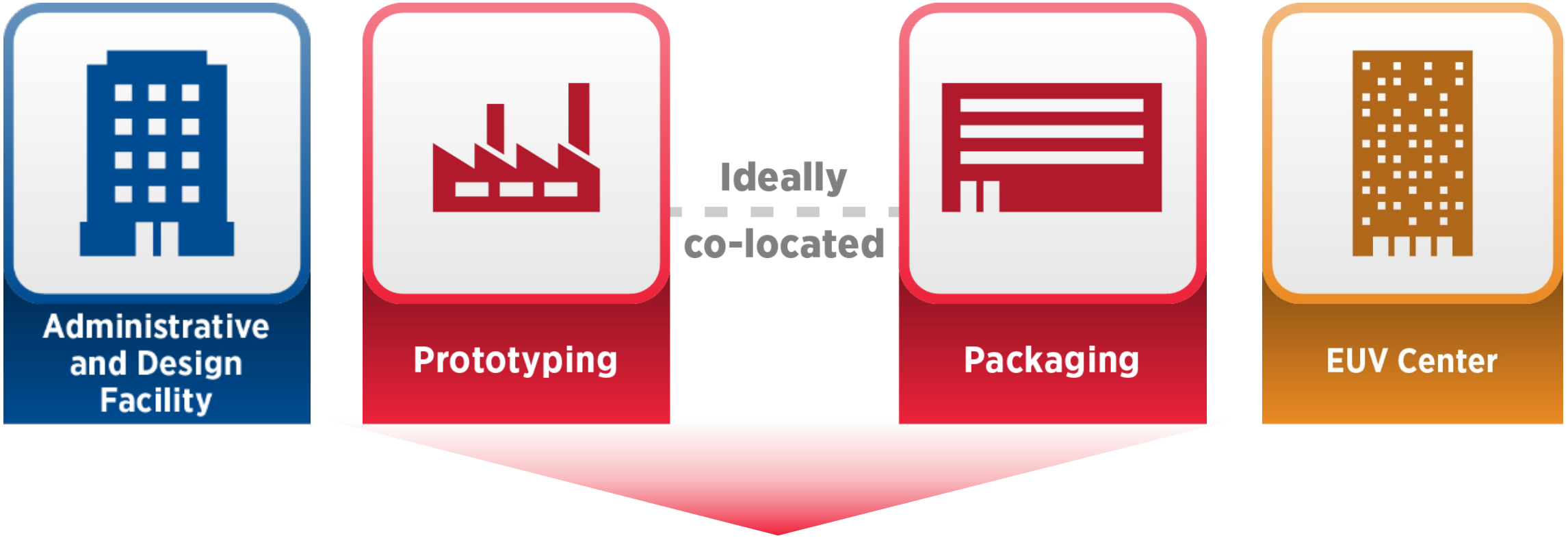
Need for Full-Flow (End-to-End) Wafer Processing Capabilities



At least three distinct process lines called out:

1) Specialized ‘300mm CMOS+X’ flow with end-to-end capability and flexibility
2) Wide-bandgap material line
3) 300mm advanced CMOS flow leveraging EUV lithography

R&D Facilities Model



The CHIPS R&D facilities model recommends co-located R&D prototyping and advanced packaging capabilities to further both the NSTC and NAPMP programs.

Selection Process: NSTC Administrative & Design Facility

Multi-functional facility, serving as the location for key operations of the NSTC, including: hosting Natcast administrative functions; convening consortium members; and conducting NSTC programmatic activity such as the Workforce Center of Excellence and the NSTC Design Enablement Gateway. The facility must be located in a region with a thriving and vibrant semiconductor ecosystem.

Phase 1 – Identification of Semiconductor Design Ecosystems

- Semiconductor Industry Value Chain
- Semiconductor Workforce, with focus on design
- Top Research Universities (R1 Universities) focused on Microelectronics
- Access to Relevant Functionality and Services

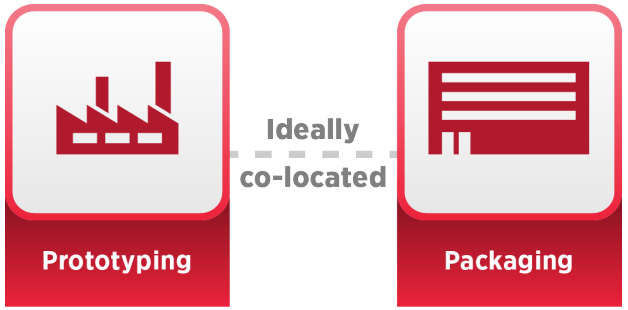
Phase 2 – Identification of Locations, Due Diligence, and Negotiations

- EDOs in select states/territories invited to provide proposed locations
- Evaluate site/facility characteristics, costs, timeline, partnership opportunities, incentives

Natcast has hired a third-party professional firm with commercial experience in site selections, including in the semiconductor industry, to support the process.

Selection Process

NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility



To achieve the ambitious goal of providing 300mm research, prototyping, and packaging capabilities by 2028, the NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility must be located in a region with a thriving and vibrant semiconductor ecosystem.

Phase 1 – Semiconductor Ecosystem Assessment

National search to identify thriving and vibrant semiconductor ecosystems.

- Ecosystem Questionnaire for States and Territories to Inform the Site Selection Process
- Applicants = Economic Development Organizations (EDO) of all 56 states, territories, and D.C.

Phase 2 – Site Evaluation

Invited states and territories can submit responses to site-specific questionnaire

- Provide detailed information about specific proposed sites
- Site-specific requirements, including the intention for the facility to be operational by 2028

Natcast has hired a third-party professional firm with commercial experience in site selections, including in the semiconductor industry, to support the process.

Phase 1 – Factors for Consideration

NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility

Industry Presence	Presence and planned growth of the semiconductor value chain, such as commercial semiconductor fabrication plants, advanced semiconductor packaging facilities, semiconductor equipment and material suppliers, and semiconductor design companies
Availability of Workers	Number of people currently working in semiconductor design, manufacturing, or closely-related fields and types of expertise
Education & Research	Number and caliber of university research and advanced degree programs focused on microelectronics
Workforce Development	Number and quality of semiconductor-focused training programs
Investment	Amount of private and public investments in the semiconductor industry in the previous decade
State/Territory Support	Number and type of benefits, incentives, and/or initiatives that benefit the semiconductor industry

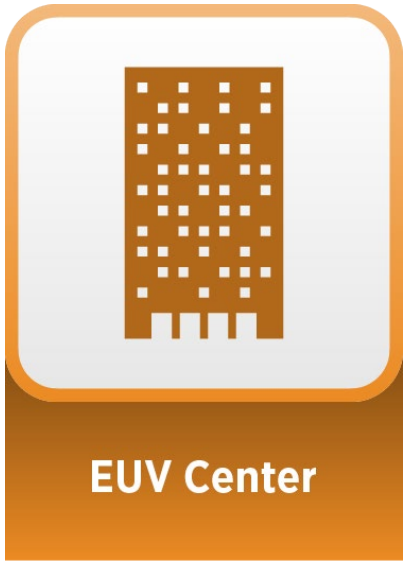
Phase 2 – Factors for Consideration

NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility

Real Estate & Infrastructure	Characteristics of the specific real estate proposed, including alignment to physical and technical specifications provided by Natcast and the Department; environmental factors; and the existence of certain utilities and other infrastructure
Costs	Key estimated one-time and operating costs for the facility
Operating Environment	Anticipated timing to achieve buildout and full-scale operations and potential operating risks for the specific site and location
Non-Federal Support	Extent and level of non-federal support such as state and local incentives and private capital
Proposed Partnership	Proposed partnerships with entities (e.g., companies, workforce providers, state and local governments) in the region to support the mission
Site-Specific Attributes	Whether the site will sufficiently benefit from the thriving and vibrant semiconductor ecosystem in the state or territory

Selection Process: NSTC EUV Center

The NSTC EUV Center will provide NSTC members with access to extreme ultraviolet (EUV) lithography technology to facilitate a wider range of research and path to commercialization, including technologies with the most challenging feature sizes.



Initially obtain access to EUV lithography as a service from an existing provider that meets NSTC requirements

- Limited number of existing U.S. entities who can provide the necessary EUV capabilities
- The Department of Commerce and Natcast to invite entities to participate in a selection and negotiation process
- Selected service provider will be the entity that is most advantageous to the objectives of CHIPS for America

Next Steps

Please email questions and relevant information to FacilitiesRFI@natcast.org

- Sign up for the CHIPS and Natcast mailing lists
- General CHIPS inquiries: askchips@chips.gov
- General Natcast inquiries: info@natcast.org

Join the NSTC Community of Interest

*Proposals received outside of the described processes **will not** be evaluated but rather redirected to the relevant channels.*


Thank you
Visit CHIPS.gov and Natcast.org for more information!