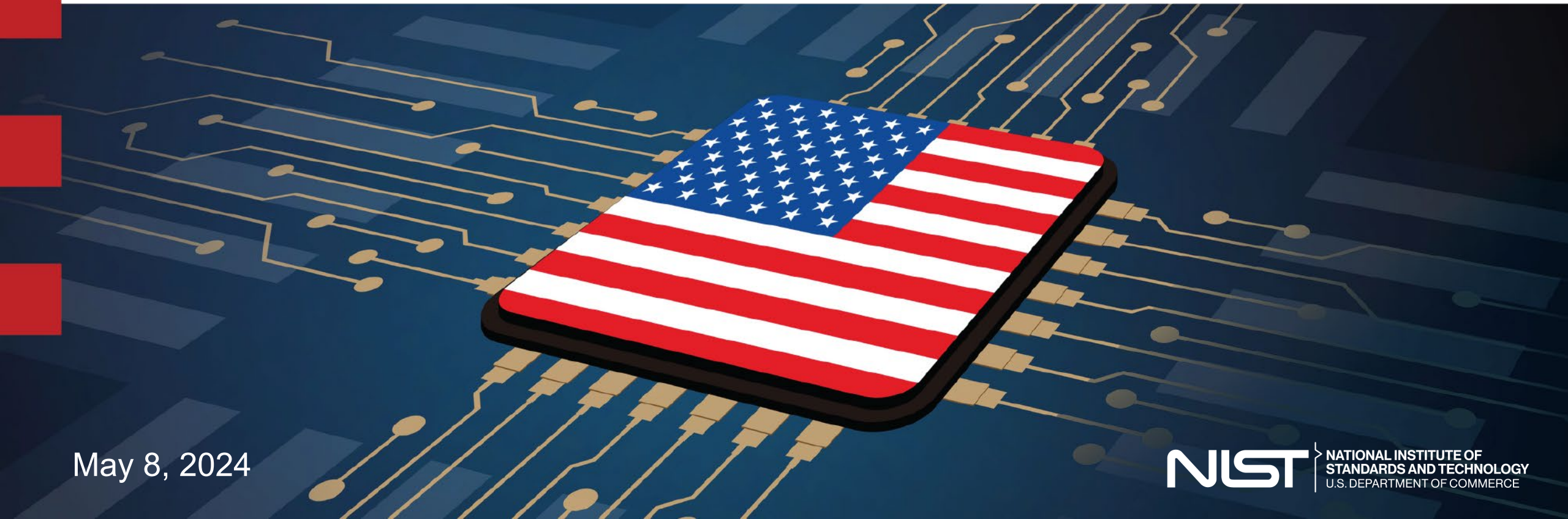
CHIPS Manufacturing USA Institute Funding Opportunity



May 8, 2024

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Disclaimer

The Notice of Funding Opportunity (NOFO) 2024-NIST-CHIPS-MFGUSA-01 document is the official competition document. The following presentation is only a summary of the NOFO document. Please review the NOFO thoroughly prior to starting the application process. Any apparent or actual conflict between the NOFO and this presentation must be resolved in favor of the NOFO.

Today's Speakers

Eric Forsythe
Technical Director
CHIPS Manufacturing USA

Mike McKittrick
Deputy Director
CHIPS Manufacturing USA

Webinar Expectations

Agenda

- CHIPS R&D Program
- CHIPS Manufacturing USA Digital Twin Institute
- Proposer's Day

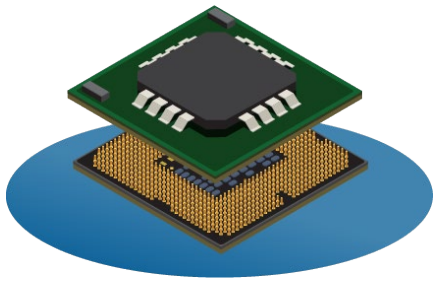
By the end, attendees should better understand

- Outcomes of the CHIPS Digital Twins Institute
- Key Dates in the Funding Opportunity
- Proposer's Day Details

CHIPS R&D Programs

Vision: A vibrant and self-sustaining U.S. domestic semiconductor ecosystem that revitalizes American manufacturing, grows a skilled and diverse workforce and leads the world in semiconductor research and innovation.

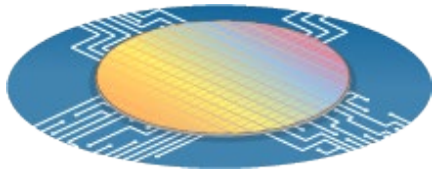
CHIPS Metrology Program



CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast

Natcast is an independent nonprofit organization and operator of the NSTC consortium



CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

Manufacturing USA

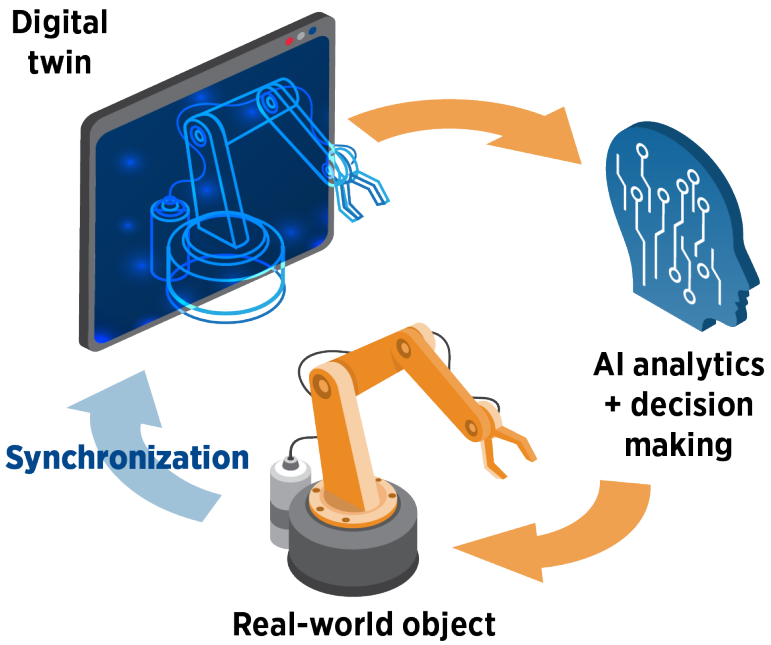
CHIPS Manufacturing USA Program

Workforce Initiatives

CHIPS Manufacturing USA
Digital Twin Institute

What is a digital twin?

- A **virtual** representation or model that serves as the real-time digital counterpart of a physical object or process.
- *Benefits*
  - Innovate faster and at less expense
  - Access feasible for small and medium businesses
  - Enhance training modalities
  - Shorten process design and validation times
  - Improve facility performance
- *Challenges*
  - *Fragmentation* – Being able to produce and access the **data** needed to validate digital twins and power machine learning and AI tools
  - *Lack of Trust* – Strategic industry **collaboration**, which requires a neutral convener to build trust and bring together all parties to share the risks and rewards of working across boundaries
  - *High Barrier to Entry* – Significant **financial investment**, which is out of reach for small and medium-sized manufacturers to do themselves



CHIPS Manufacturing USA: Digital Twin Institute

Vision

Enable seamless integration of digital twin models into the U.S. semiconductor manufacturing, advanced packaging, assembly, and test industry, enabling the rapid development and adoption of innovations and enhancing domestic competitiveness for decades.

Mission

The CHIPS Manufacturing USA Institute will foster a collaborative environment within the domestic semiconductor industry, enabled by shared facilities; support industry-led solutions through funded research projects; accelerate technology towards commercialization through significant co-investment; and enable digital-twin workforce training.

CHIPS Manufacturing USA Institute Objectives

Convene stakeholders across the semiconductor production ecosystem

Improve the state of the art in manufacturing-relevant digital twins

Significantly reduce cost for U.S. chip development and manufacturing

Improve development cycle times of semiconductor product innovation

Advance digital twin-enabled curricula for training a domestic semiconductor workforce

Create a digital twin marketplace for industry to access digital models

Operational Areas

OA1

Institute Operations

OA2

Shared Capabilities

OA3

Industry Solutions

OA4

Workforce Training

Example Institute-level targets

A substantial decrease in the time required to develop a specific new capability (e.g., a material, process, or tool) for semiconductor manufacturing, within two years of award.

A specific increase in the accuracy of a short loop of digital twins, leveraging artificial intelligence, within two years of award.

Establishing a production-representative digital twin of an end-to-end flow between semiconductor fabrication and advanced packaging, consisting of multiple interoperable digital twins validated with a pre-determined test vehicle, within five years of award.

Demonstrate applicability of one digital twin to another end-to-end flow, leveraging standards, within five years of award.

Achieving cost-share and co-investment commitments of more than three times the level of Federal investment, within two years of award.

Enabling the hiring or reskilling of a specific number of semiconductor industry workers, via EWD projects focused on credentialing, within the five-year Institute period of performance.

Applications are asked to propose Institute-level targets – these are provided as examples

CHIPS MFG USA – Approach

CHIPS R&D will invest up to $285M in Federal funds into four operational areas

	Phase 1. Stand up	Phase 2. Initial Performance	Phase 3: Advanced Performance	Phase 4: Transition Planning
5-yr Timeline	**6 – 18 mos**	**6 – 18 mos**	**6 – 18 mos**	**6 – 18 mos**
OA 1: Institute Operations	Establishing an Institute management and governance strategy, to include plans for outreach to a broad group of potential members			
OA 2: Shared Capabilities	Operating or providing member access to physical and virtual facilities, as appropriate.			
OA 3: Industry Solutions	Developing and supporting an Institute-funded portfolio of projects, to either improve the capabilities of digital twins or to impact real-world operations.			
OA 4: Workforce Training	Projects to either train the workforce to use digital twins or to leverage digital twin technology to deliver EWD services to diverse audiences of trainees.			
Milestones	• Stand up institute • Enroll members; build partnerships • Establish Shared Capabilities • Release project call(s)	• Demonstrate major manufacturing advances with digital twins • Refined policies and plans • Release project call(s) • Make project awards	• Increase performance with Digital Twin Backbone • Refined policies and plans • Release project call(s) • Make project awards	• Submit final reports • Increase performance with Digital Twin Backbone • Close out final project awards

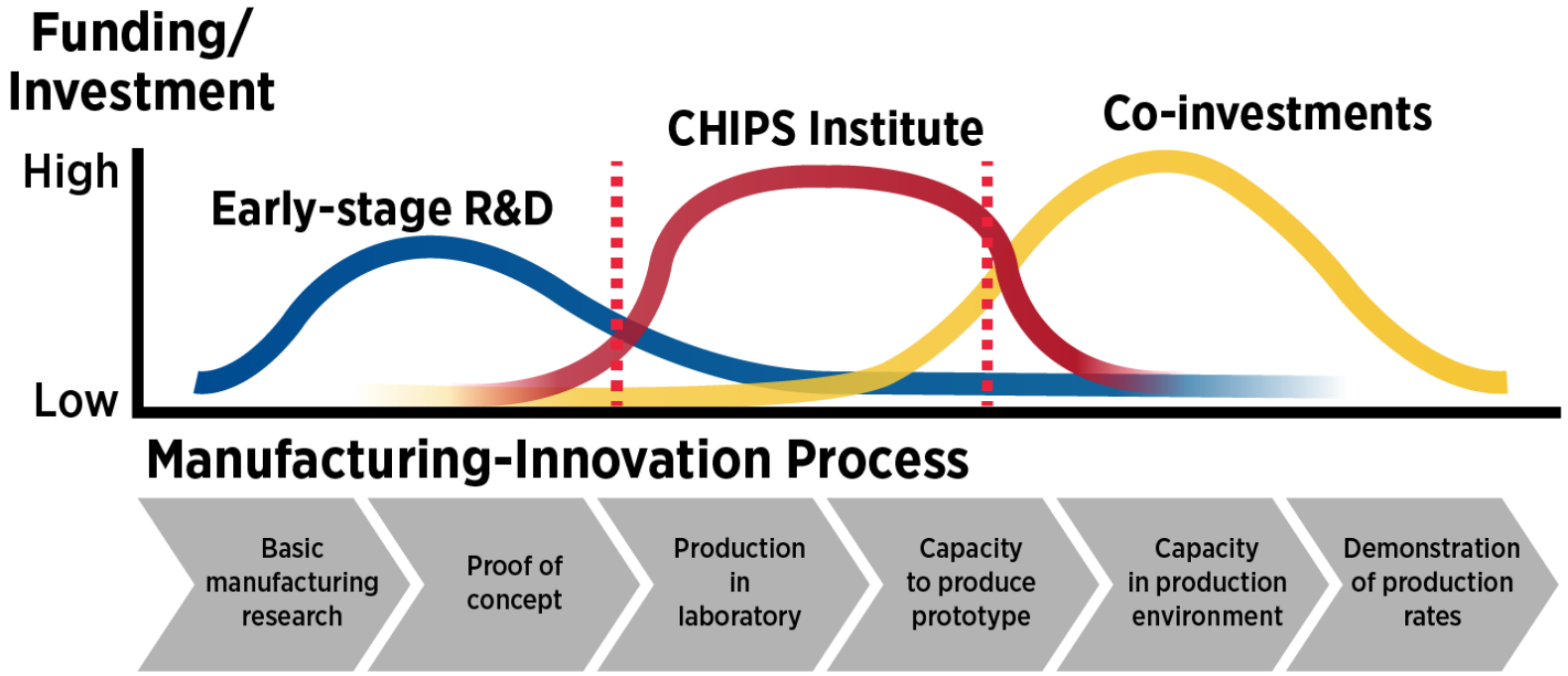
Commercial Scale-Up

▲ OA 1 Milestones ▲ OA 2 Milestones ▲ OA 3 Milestones ▲ OA 4 Milestones ★ Program Go/No-go decision

What might constitute non-Federal investment?

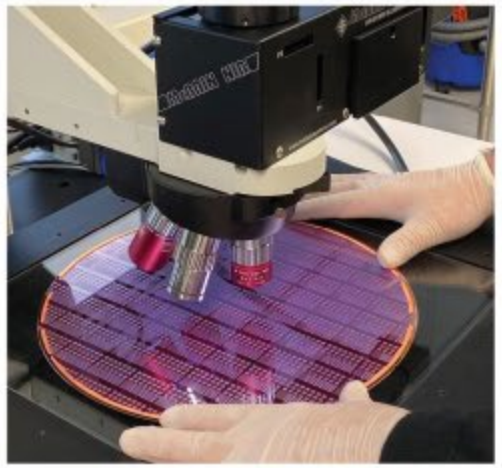
Member Dues	**Tools/Equipment on loan**	**State matching**
Software licenses	**Staff time**	**State facilities**
Facility access	**Materials**	**Philanthropy / Foundations**
Data	**Supplies**	**Follow-on funds (MRL 7 – 9)**

Acceleration to Commercialization

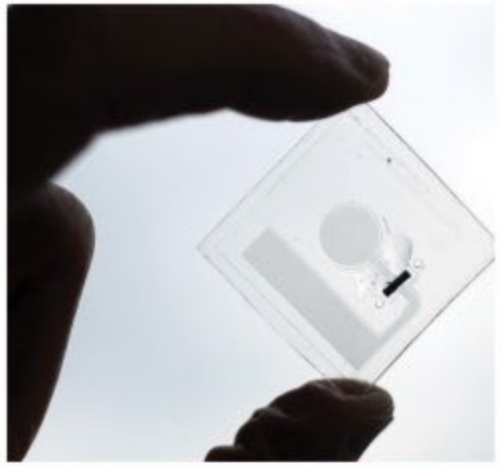


A key goal of the CHIPS Manufacturing USA Institute is to have a significant impact on the semiconductor industry.

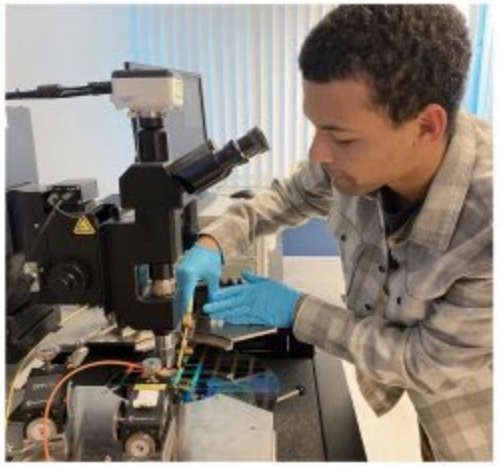
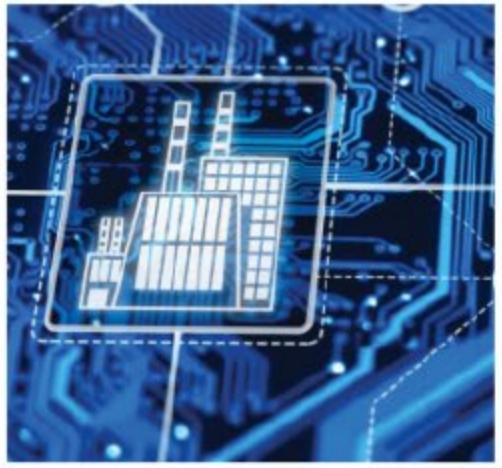
- Applicants should provide commitments from members to advance potential innovations from projects to higher MRLs.
- These commitments may involve late-stage technology development to commercialize digital twins or the application of digital twins to semiconductor manufacturing.
- Examples of co-investments may include those required to enable the scale-up, commercialization, and transition to domestic production of Institute-funded innovations.



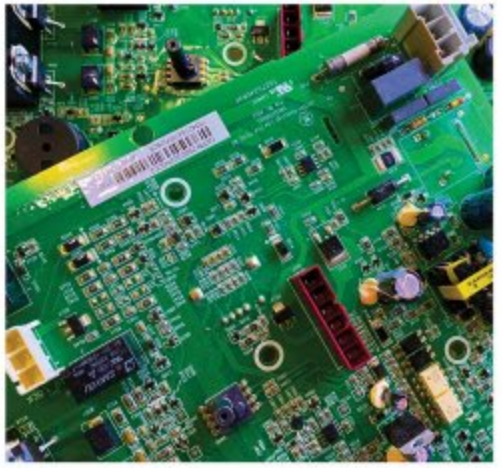


ManufacturingUSA





Collaboration is Critical for Success

Active Participation from a wide-range of organizations

Network of Manufacturing USA Institutes

CHIPS R&D Programs

Relevant Federally funded efforts

We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the CHIPS Manufacturing USA Institute

CHIPS Manufacturing USA Institute Funding Opportunity Details

- Follow QR code for full text of funding opportunity
- Highlighted NOFO Sections:
  - **Funding Opportunity Detailed Description** (*Institute activities, operational areas)*
  - **Institute-level Targets** (*innovations, workforce, co-investment*)
  - **Broader Impacts** (*future investments, support for other R&D, inclusive opportunities, environmental, and community impact*)
  - **Research Security**, **Intellectual Property, Eligibility**, and **Application Process**
- Encourage those interested to familiarize themselves and direct questions to askchips@chips.gov with "2024-NIST-CHIPS-MFGUSA-01 Questions“ in subject.

CHIPS for America QR Code: **CHIPS Manufacturing USA institute NOFO** (full text)

Key Dates

May 6, 2024

Digital Twin Institute Funding Opportunity (Released)

To establish and operate a CHIPS Manufacturing USA Institute focused on digital twins to tackle important semiconductor-industry manufacturing challenges.

May 16, 2024

Proposers Day

Share detailed information on the NOFO, in a collaborative atmosphere

Due: June 20, 2024

Concept Papers Review

Mandatory concept papers submitted by teams

Teams invited to submit full application

September 9, 2024

Full Application Due

The full application from applicants due

CHIPS for America QR Code: **CHIPS Manufacturing USA institute NOFO** (full text)

Next Steps

CHIPS Manufacturing USA Institute Proposers Day

- One day event on May 16, 2024
- Hilton Rockville Executive Meeting Center in Rockville, MD
- Hybrid Meeting, In-person attendance is strongly encouraged.
  - Plenary session describing Notice of Funding Opportunity requirements and submission process in detail
  - Breakout sessions to facilitate networking among attendees. Virtual attendees will have a breakout session.
- **Learn more and register at CHIPS.gov under Events**
- Registration will close May 13, 2024. Please Register!

CHIPS for America QR Code:
CHIPS Manufacturing USA Institute Proposers Day (event webpage)

Frequently Asked Questions

Frequently Asked Question 1

Can applicants receive money from both the $39 billion for incentives and the $11 billion for R&D?

Yes, applicants can receive funding from both programs if the applicant can show the Department how its proposed projects / uses of funding would advance the individual objectives of each program.

Frequently Asked Question 2

Can an organization participate in multiple concept papers?

- Eligible applicants may only submit one concept paper as the lead for the Institute award under this NOFO. Applicants are required to have an active registration in SAM.gov and are encouraged to begin the process of registering as early as possible.
- Entities are allowed to participate on multiple concept papers as subrecipients.
- Full applications will only be accepted from applicants invited after the concept paper stage.

Frequently Asked Question 3

Is there an opportunity to meet potential team members?

CHIPS R&D encourages collaborative proposals under this NOFO, as significant partnership will likely be required to meet the NOFO objectives.

The Proposers Day on May 16, 2024 will provide opportunities for networking.

Frequently Asked Question 4

What is the difference between cost share and co-investment?

- **Cost share** is the portion of the costs of a federally assisted project or program not borne by the Federal Government. The required cost share must, at a minimum, be equal to the total amount of federal funding provided through the lifetime of an award. 50% or more of the total funding for the Institute must come from non-federal sources.
- **Co-investments** are commitments made by Institute members to advance potential innovations from projects to higher Manufacturing Readiness Levels (MRLs). Examples of co-investments may include those required to enable the scale-up, commercialization, and transition to domestic production of Institute-funded innovations.

Thank You

Direct additional questions to **askchips@chips.gov** with 2024-NIST-CHIPS-MFGUSA-01 in subject.