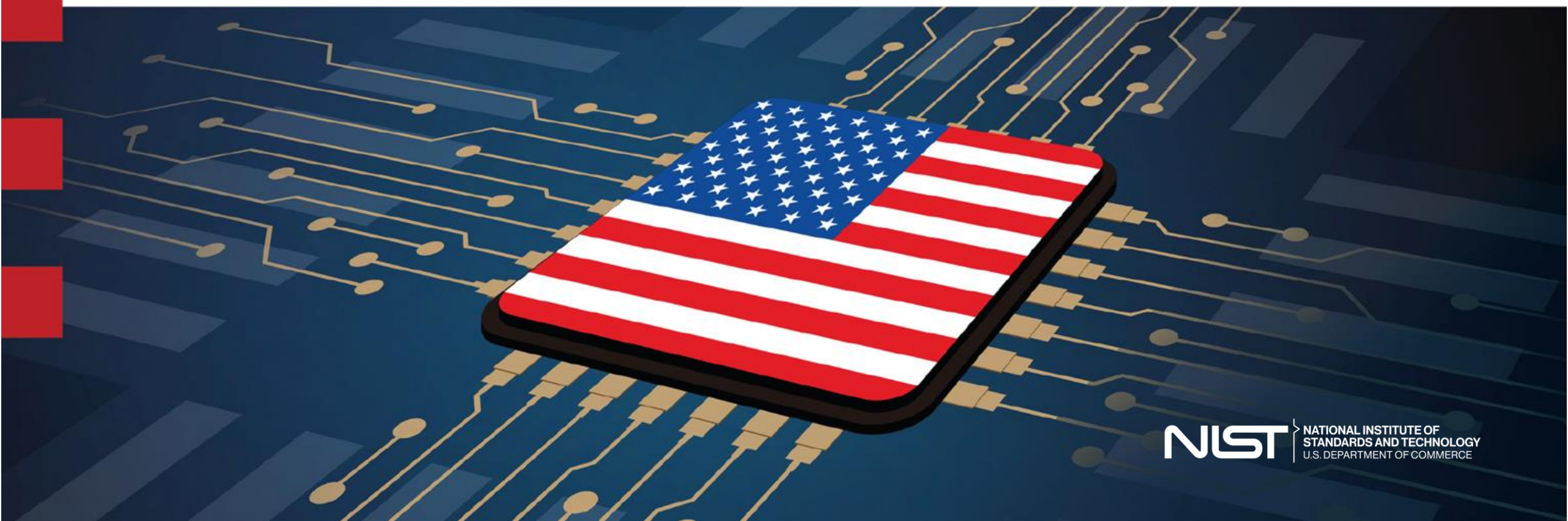


Updates on CHIPS Metrology Program

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Director, CHIPS Metrology Program



- Certain commercial entities, equipment, or materials may be identified in this document in order to describe an experimental procedure or concept adequately.
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CHIPS for America Vision



Economic Security

This act enables us to build more resilient supply chains for important components.



National Security

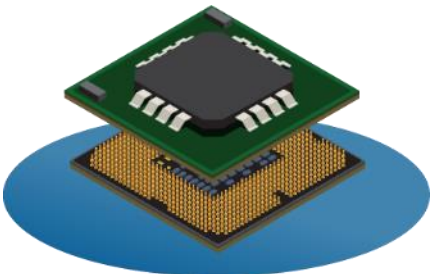
This act enables us to bring the most sophisticated technologies back to the U.S.



Future Innovation

Chips are key to the technologies and industries of the future, so we need to be at the forefront. This act will ensure long-term U.S. leadership in the sector.

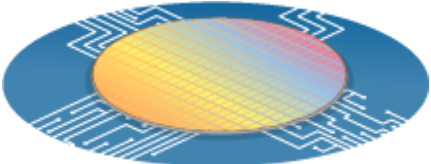
CHIPS R&D Programs



CHIPS National Semiconductor Technology Center (NSTC) Program



Natcast is a purpose-built nonprofit organization and operator of the NSTC consortium



CHIPS National Advanced Packaging Manufacturing Program (NAPMP)



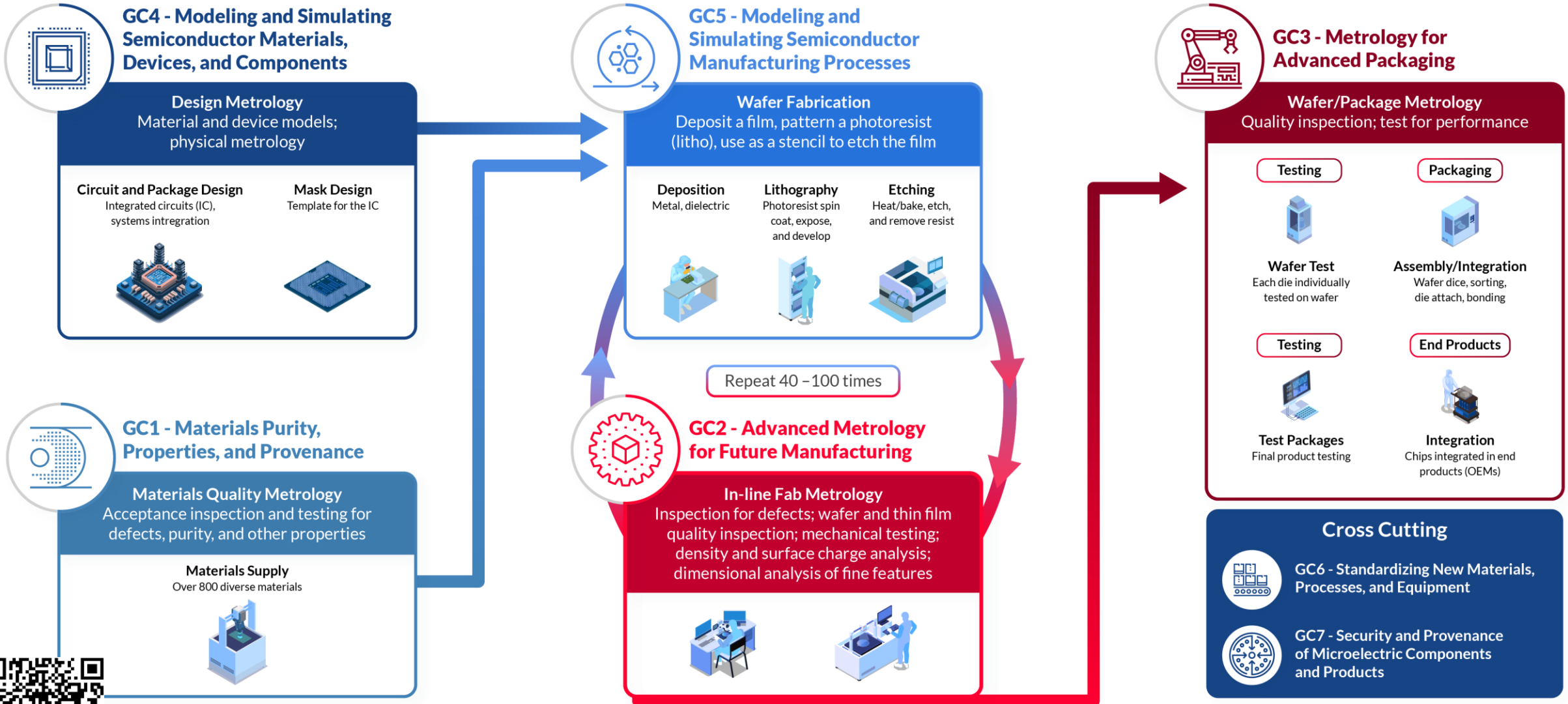
CHIPS Manufacturing USA Program



CHIPS Metrology Program

Workforce Initiatives

CHIPS Metrology Program Grand Challenges



CHIPS Metrology Program: How Far We've Come



CHIPS Metrology
R&D



CHIPS SBIR



CHIPS Metrology
Community



Metrology
Exchange to
Innovate in
Semiconductors

Grand Challenge (GC) Funded Research Projects

- Over **\$190 million** in funding has been provided to more than **40 approved research projects** in 6 Grand Challenges.
- Current projects are helping to develop new measurement instruments, measurement methods, and measurement-informed models and simulations for advanced microelectronics design and manufacturing.
- More information about the funded projects can be found on the CHIPS Metrology webpage. Additional project pages will be added this fall.

Industry and Academia Collaboration

- Research teams have proposed several distinct industry collaborators to provide materials and software and/or conduct joint research with researchers.
- Several collaborations with U.S. universities, nonprofit consortiums, research institutes, and associations related to the microelectronics industries have also been proposed.



[https://www.nist.gov/chips/
research-development-
programs/metrology-
program](https://www.nist.gov/chips/research-development-programs/metrology-program)

CHIPS Metrology Small Business Innovation Research (SBIR) Program



Encourage domestic small businesses to engage in research and development (R&D) with the potential for commercialization.

- Stimulate commercialization of technological innovation from the private sector through Federal R&D funding.
- Foster participation in innovation by socially and economically disadvantaged small businesses.

Funding across multiple topics on research projects for:

- Critically needed measurement services, tools, and instrumentation.
- Innovative manufacturing metrologies.
- Novel assurance and provenance technologies.
- Advanced metrology research and development (R&D) testbeds.

SBIR Awardees

- 17 small businesses across 9 states



<https://www.nist.gov/news-events/news/2024/09/biden-harris-administration-awards-nearly-5-million-small-businesses-bring>

CHIPS SBIR Awardees





CALIFORNIA

Sigray, Inc.
Concord



CALIFORNIA

Photon Spot, Inc.
Monrovia






CALIFORNIA

HighRI Optics, Inc.
Oakland



CALIFORNIA

Direct Electron LP
Rancho Bernardo






CALIFORNIA

Recon RF, Inc.
San Diego



CALIFORNIA

Photothermal Spectroscopy Corporation
Santa Barbara



CALIFORNIA

PrimeNano, Inc.
Santa Clara






COLORADO

Tech-X Corporation
Boulder



COLORADO

Vapor Cell Technologies
Boulder




COLORADO

Octave Photonics LLC
Louisville



MICHIGAN

Virtual EM, Inc.
Ann Arbor






OREGON

Provenance Chain™ Network
Portland



PENNSYLVANIA

Tiptek LLC
West Chester



TEXAS

Exigent Solutions
Frisco






VIRGINIA

Laser Thermal Analysis, Inc.
Charlottesville



WASHINGTON

Hummingbird Precision Machine Co.
dba Hummingbird Scientific
Olympia



WISCONSIN

Steam Instruments
Madison



The Community:

- Are **engagement groups** working to advance breakthrough measurements that are accurate, precise, and fit-for-purpose to produce microelectronic materials, devices, circuits, and systems.
- Facilitate collaborations to help **improve data and knowledge sharing** among all stakeholders in the semiconductor field.
- **Help stakeholders inform the industry standards** that are critical for enhancing U.S. economic or national security competitiveness to meet unprecedented demand for next generation networks.
- Help **close the cultural and knowledge gaps** between "fab," "lab," and equipment providers.



Credit: Adobe Stock

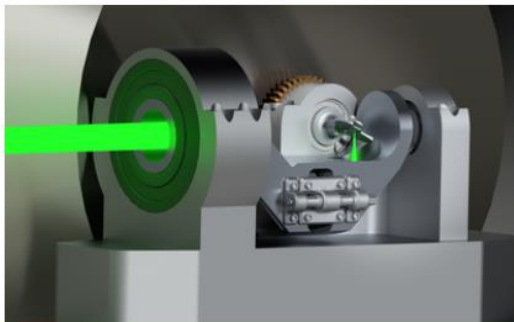


CHIPS for America QR Code:
<https://www.nist.gov/chips/metrology-community>

Metrology Exchange to Innovate in Semiconductors

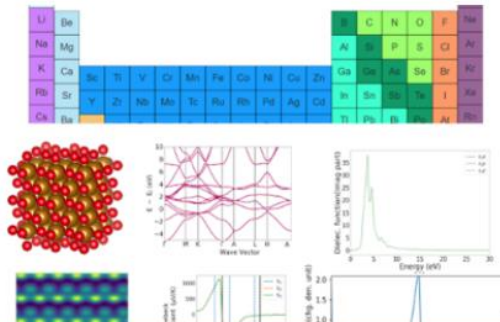


METIS will make research and data available in a manner that guards intellectual property, protects U.S. security interests, is aligned with the approach used by NIST for access to research results, and is self-sustaining to meet future needs.



**High Speed Metrology for
Magneto-electronic Devices and
Models**

[Access Data](#)



**Multiscale Modeling and Validation
of Semiconductor Materials and
Devices**

[Access Data](#)



CalNet

[Access Data](#)



CHIPS for America QR Code:
<https://www.nist.gov/metis>

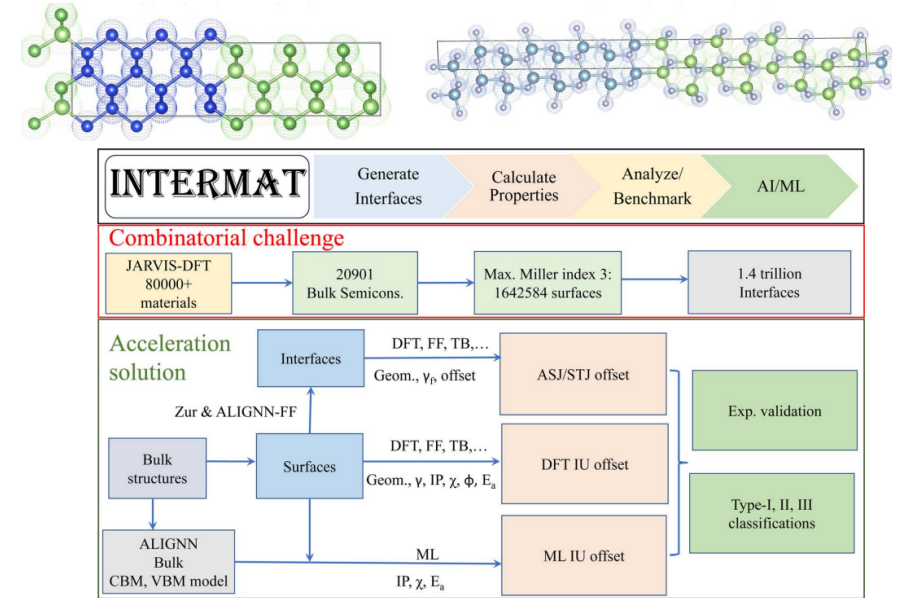
4.07 - Multiscale Modeling and Validation of Semiconductor Materials and Devices

Team member(s): Kamal Choudhary (642), Daniel Wines (642), Kevin Garrity (643), Brian DeCost (643), Lucas Hale (642), Eric Cockayne (643), Albert Davydov (642), Francesca Tavazza (643), Carrie Campbell (642)



Project Highlights:

- JARVIS-Leaderboard paper [1] enhances reproducibility and benchmarking for multi-scale modeling methods. The paper has 25k downloads.
- JARVIS-Tools software has half a million downloads and NIST-JARVIS, in general, has 150k users right now.
- The JARVIS dataset has close to 1 million downloads and 3k+ citations.
- InterMat project for semiconductor heterostructure design was published in Digital Discovery [2] and the code has been made publicly available.



Why Does it Matter?

- Enhance understanding of interfaces to improve device efficiency.
- Enhance understanding of defects to analyze device limitations.
- Multi-scale modeling tools accelerate advanced semiconductor device deployment.

Outcomes:

- Software tools and models can be used for evaluating materials and device configurations.
- Conversations with EDA software providers are ongoing to integrate InterMat in their software platform(s).

1. K. Choudhary, et al. "JARVIS-Leaderboard: a large scale benchmark of materials design methods." *npj Computational Materials* 10.1 (2024): 93. doi: 10.1038/s41524-024-01259-w
2. K. Choudhary and K. F. Garrity. "InterMat: accelerating band offset prediction in semiconductor interfaces with DFT and deep learning." *Digital Discovery* 3.7 (2024): 1365-1377. doi: 10.1039/D4DD00031E

A 3D graphic of an American flag, tilted and appearing to float above a dark blue background with a circuit board pattern. The text "Thank You!" is overlaid on the flag.

Thank You!

Questions? Email: askchips@chips.gov