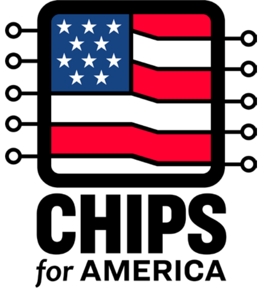
Chiplets



PM: Bapiraju Vinnakota

October 22, 2024

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

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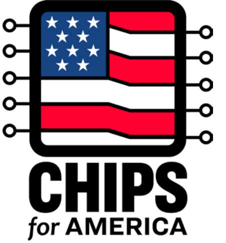

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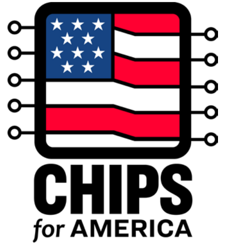
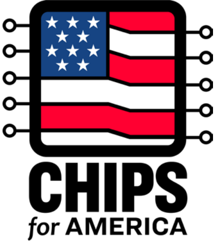
Key Dates



July 9, 2024	October 17, 2024	October 22, 2024	December 20, 2024	TBD	TBD
NOI (Released)	Advanced Packaging R&D (Released)	Advanced Packaging R&D Proposer's Day	Concept Papers Due Date	Invitation for Full Application Submission	Full Application Due

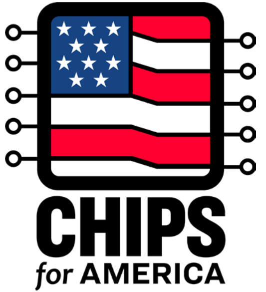
CHIPS for America QR Code:
CHIPS NAPMP NOFO 2
(full text)

Outline

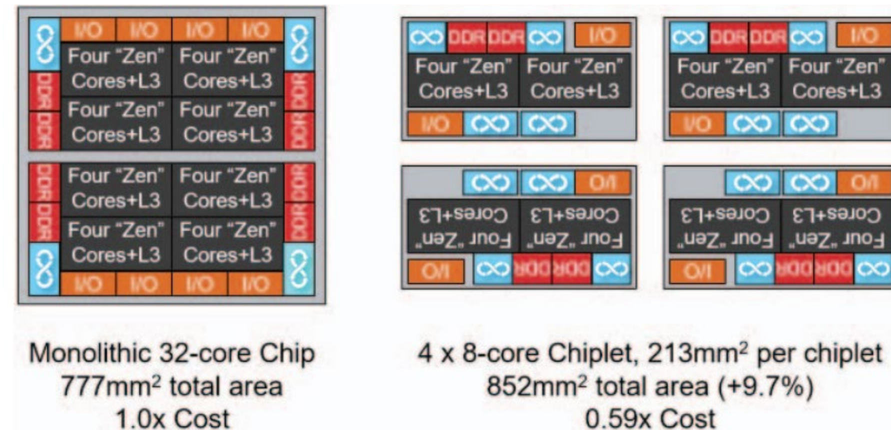


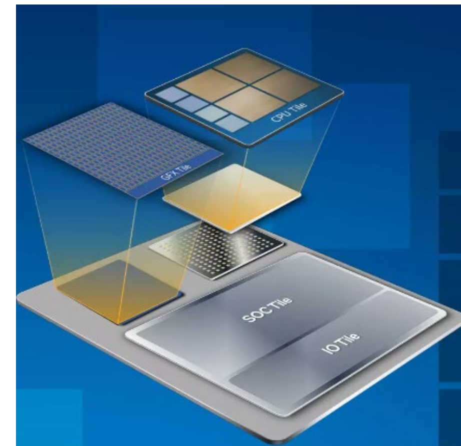
- Introduction
- Background and motivation
- Outcomes, Objectives, Tasks and targets
- Suggestions on how to respond to the Chiplets section
- Wrap up

Industry Moves to Chiplets



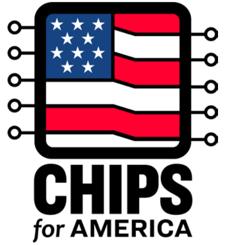
- **Chiplets**
  - A small, functionally targeted semiconductor chip that, when assembled at tight pitch and placement, results in a highly functional subsystem
  - A single product integrates and assembles multiple chiplets connected to one another through die-to-die interfaces
- **Motivation**
  - Build Big (Reticle busters)
  - Build Fast (Modularity, Reuse)
  - Build Better (Optimize function to process node)





Top: https://www.nextplatform.com/2021/06/09/amd-on-why-chiplets-and-why-now/
Bottom: https://www.tomshardware.com/news/intel-meteor-lake-cpus-for-desktops-incoming

A Chiplets/Systems Design Inflection Point Enabled by Advanced Packaging



Today: packages more like **boards**

Tomorrow: packages more like **chips**

fine line 5 trace layer PCB

Chip 1 Chip 2 Chip 3

FOWLP 5 trace layer RDL

10x wire density & growing

CHIPS R&D NAPMP Materials and Substrates Proposer's Day

NOFO1 10-layer subμ pitch

2nm, 2 upper metal layers

Estimated wire density in wires/mm

axis marks not to scale

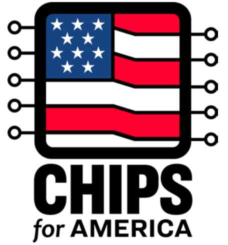
≈ 20 ≈ 500 ≈ 6,000 ≈ 20,000[2]

Wire Scarcity → **Wire Abundance**

Chiplets/Systems Today	With	Chiplets/Systems Tomorrow[3]
High-speed high-power interface	Wire abundance	**Scale-down** wire-like 2D/3D interface at 10μm and lower bond pitches
Monolithic wafer-scale	10-100x larger packages	**Scale-out** wafer-scale systems that exploit wire abundance
Board-like integration	Function & physical modularity	**Ecosystem** for IP-like heterogeneous chiplet integration

[1] P. Chiang,et al, "InFO_oSTechnology for Advanced Chiplet Integration," 2021 IEEE 71st ECTC, San Diego, CA, USA, 2021, pp. 130-135.
[2] Illustrative, approximate wire density numbers estimated from current state of the art.
[3] NAPMP Vision Paper: The Vision for the CHIPS for America National Advanced PackagingManufacturing Program (nist.gov)

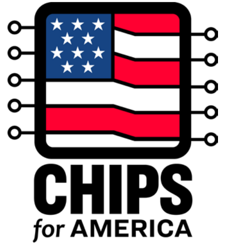
CHIPLETs Research & Design Area



- The R&D area focuses on new chiplet ecosystems that will fully leverage advanced packaging
  - “Wire abundance”: hundreds to thousands of wires between chiplets, instead of 10s to 100s
  - Ultra-large packages: hundreds to thousands of chiplets on package, more chiplets instead of bigger chiplets
  - Heterogeneous integration: function and physical chiplet modularity for faster, cheaper system development
- This investment in chiplets ecosystems is intended to achieve the following outcomes:
  - **3-5 years:** Demonstrated scaled-down, die-to-die (D2D) interfaces emerge that use wire abundance to enable a simpler connection between chiplets; implementations of powerful scale-out approaches such as a wafer-scale demonstrator that integrates several hundred chiplets; wafers of ecosystem-based chiplets that leverage 3D integration for use at the NAPPF and other advanced packaging facilities
  - **10 years:** Industry convergence around a set of chiplets ecosystems that leverage scale-down, scale-out and heterogeneous integration to reduce the cost and time to develop new products while offering greater power performance.

Long term: Ecosystems are self-sustaining, used and improved by industry and academia

Objectives



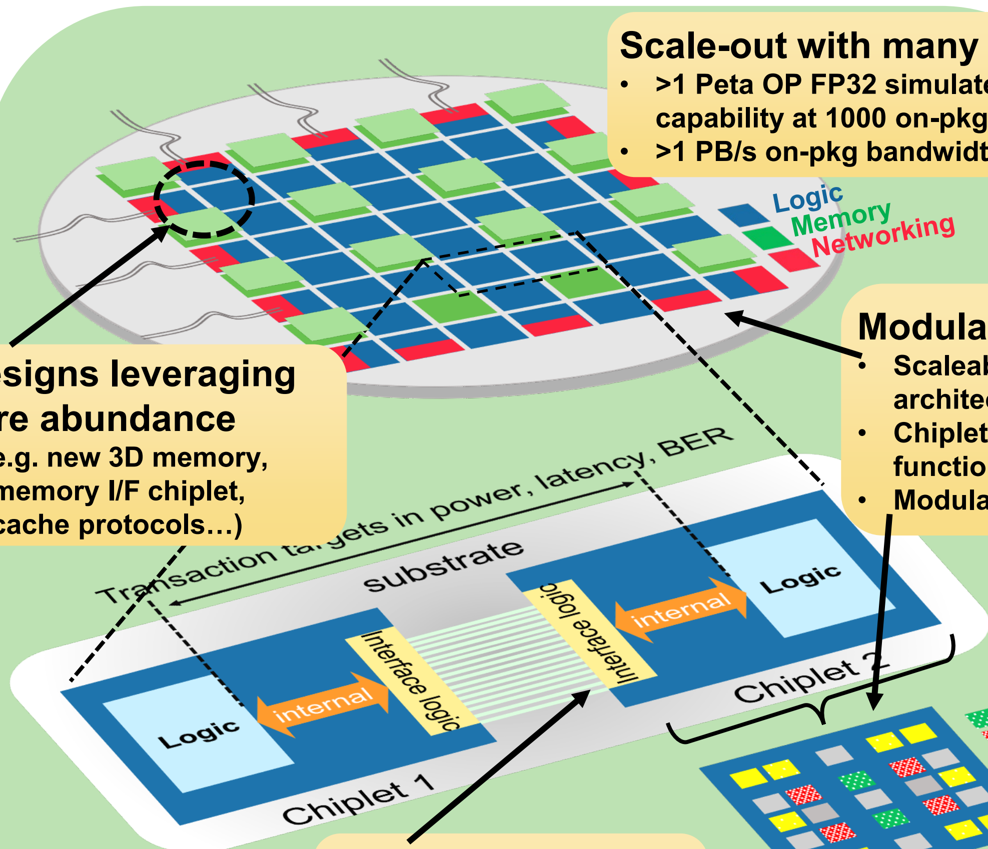
Scale Down	Scale Out	Ecosystem	Tech Demonstrator

• Advanced packaging enables hundreds to thousands of wires between chiplets
• Innovate on a simple low power, low latency wire-like D2D interface at 10μm and lower bond pitches
• Inflection point in function and system design
  • Designs that directly exploit wire abundance e.g. memory and/or memory management and/or interfaces
	• Develop technologies to enable scaling towards 100s-1000s of chiplets on ultra-large packages (HP only)
	• More chiplets instead of larger chiplets for high-performance systems.
	• Designs, algorithms & methods for scaled-out implementation & operation.
		• Develop a modular socket-based chiplet based reference architecture
		• Enable functional and physical modularity
		• Develop chiplet designs within this architecture
		• Define physical socket specifications for chiplet form factors
		  • physical parameters (e.g. dimensions, I/O, power)
			• Context for innovation of scale-down and scale-out principles
			• Demonstrate readiness for high-volume manufacturing
			• Fabricate and assemble a demonstrator with chiplets and packages at 10μm bond pitch aggregated into a system running meaningful applications
			• Applications must focus on one of two domains – high performance or low power.

Proposals must show an ability to leverage future expected bond pitch improvements from 10μm to 1μm

Example Targets: High Performance Domain

Innovations in Scale-Down, Scale-out and Ecosystem



Scale-out with many chiplets
- >1 Peta OP FP32 simulated capability at 1000 on-pkg chiplets
- >1 PB/s on-pkg bandwidth

Designs leveraging wire abundance
- e.g. new 3D memory, memory I/F chiplet, cache protocols…)

Modular Ecosystem
- Scaleable chiplet architecture
- Chiplet based, modular functionality
- Modular socket definition

Scale-down
- 100s-1000s wires
- ≤10 μm bond pad pitch
- Wire-like interface

implementations

context

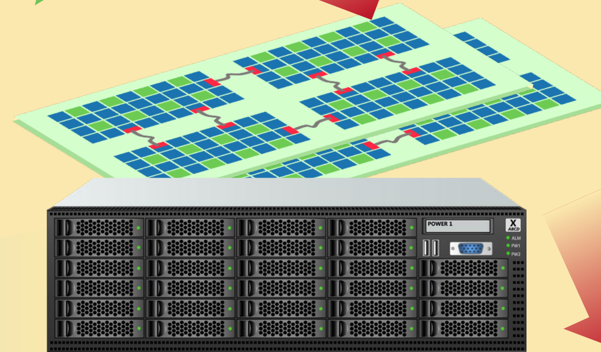
Technology Demonstrator

Baseline System

Variant System

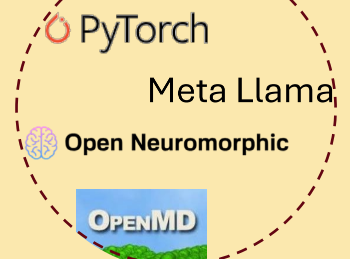
Domain specific accelerators

Unit Package
- 32 chiplets in a 3200 mm² Unit Pkg
- 2 chiplet differentiated variants
- ≤10 μm bond pad pitch



System Demonstrator
- 8 Unit packages aggregated into one system per variant

Application Demonstration
- 2 software application demonstrations per variant

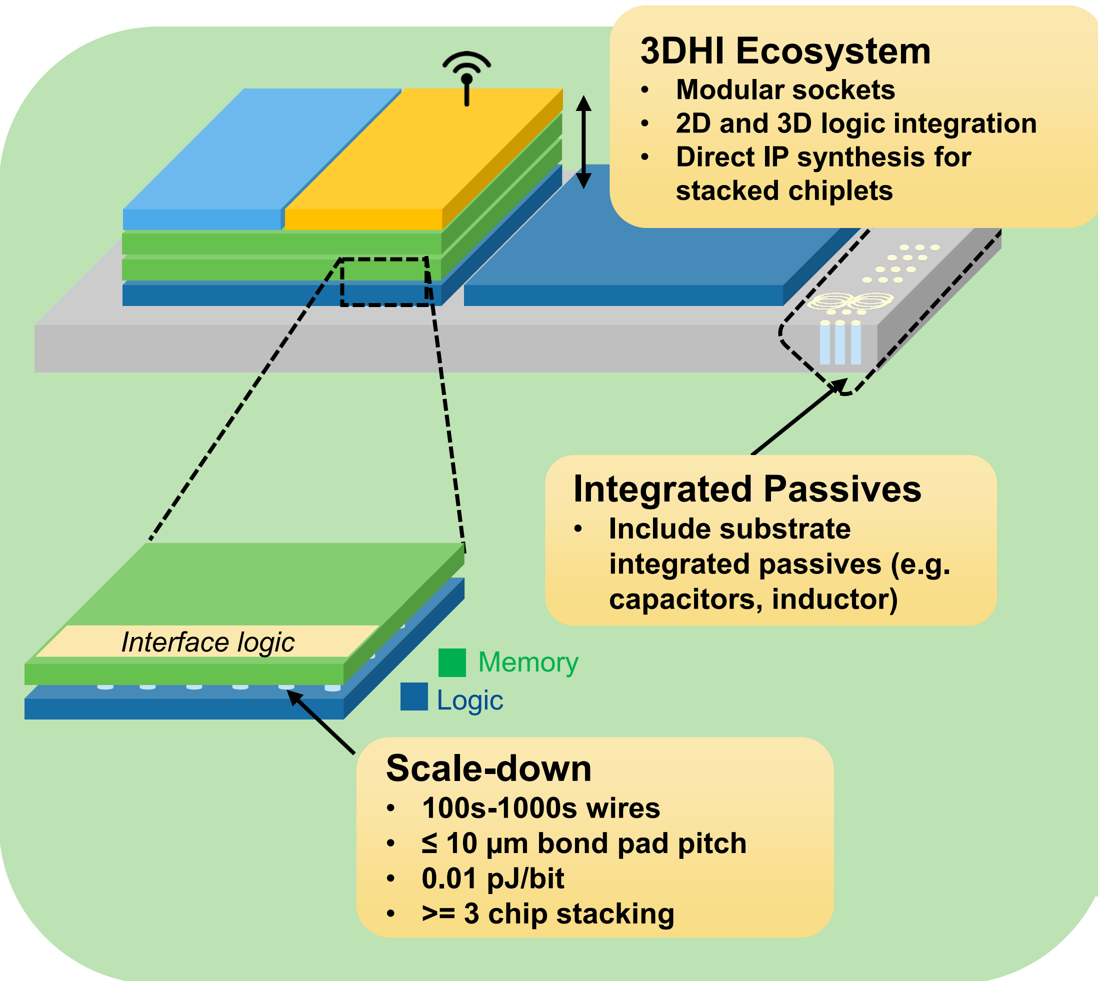


CHIPS for AMERICA

Example Targets: Low Power Domain

CHIPS for AMERICA

Innovations in Scale-Down and Ecosystem



3DHI Ecosystem
- Modular sockets
- 2D and 3D logic integration
- Direct IP synthesis for stacked chiplets

Integrated Passives
- Include substrate integrated passives (e.g. capacitors, inductor)

Scale-down
- 100s-1000s wires
- ≤ 10 µm bond pad pitch
- 0.01 pJ/bit
- >= 3 chip stacking

implementations

context

Technology Demonstrator

Baseline System

Variant System

Unit Package
- ≥ 3 stacked 10x10 µm die
- 2 chiplet differentiated variants
- ≤10 µm bond pad pitch

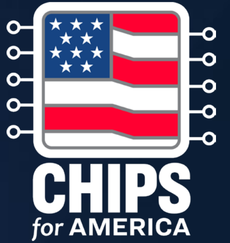
Demonstrator
- Wirelessly networked packages
- <5 W Active Power
- < 50 mW Standby

Application Demonstration
- 2 software application demonstrations per variant

IoT

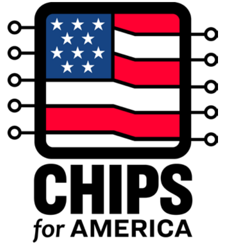
Biomedical

A/R



Suggestions to responding to the Chiplets RDA

Chiplets Concept Paper Response

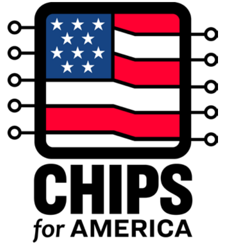


Applicants must focus a submission on one of two exemplar application domains, high-performance or low power.

For each technical target in the selected domain, applicants must indicate, in one consolidated table in the concept-paper submission, whether the project will meet, exceed, or not meet it. Proposals must address the following four required R&D output areas.

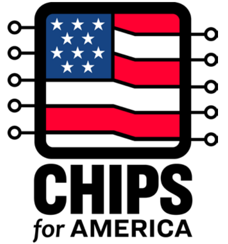
- **Scale-down** — Advances the state of the art to enable a simpler, cheaper, highly –parallel D2D interface and smaller chiplets made possible by wire abundance
- **Scale-out** (high-performance only) — Advances the state of the art to leverage scale-down and ultra-large packages to create systems of hundreds to thousands of chiplets
- **Ecosystem** — Advances the state of the art in modular design to cost-efficiently build and operate adaptable systems that leverage scale-down and scale-out
- **Technology Demonstrators** — Integrate outputs from Scale-down, Scale-out, and Ecosystem into a system demonstrating suitability and utility of outputs for use by U.S. industry and research.

Program Structure



- For the Chiplets Ecosystem R&D area, CHIPS R&D anticipates making available up to approximately $300,000,000 for funding multiple awards in amounts ranging from a minimum of approximately $10,000,000 to a maximum of up to approximately $75,000,000 in Federal funds per award for the high-performance domain and up to approximately $25,000,000 in Federal funds per award for the low-power domain.
- Applicants must propose a detailed project plan for achieving Project-Level Technical Targets. Projects should be divided into four (4) phases over a period of performance of five (5) years.
  - Phase 1 *(12 months)*
  - Phase 2 *(21 months)*
  - Phase 3 *(12 months)*
  - Phase 4 *(15 months)*

Phase Deliverables & Planning: Example



Year 1				Year 2				Year 3				Year 4				Year 5			
1Q	2Q	3Q	4Q	5Q	6Q	7Q	8Q	9Q	10Q	11Q	12Q	13Q	14Q	15Q	16Q	17Q	18Q	19Q	20Q

- **CH Phase 1:** Scale-down design, scale-out / ecosystem specifications
- **CH Phase 2:** Scale-down verification, scale-out implementation and tapeout
- **CH Phase 3:** System bring-up, integration
- **CH Phase 4:** Technology demonstration

Scale-down: D2D Spec, D2D macro+ test chip design → D2D testchip 1 tapeout, assembly bringup → (optional) Designs unique to wire abundance e.g. memory, mem mgmt… → TD Firmware R1 → Variant Integration → App 2 R1 Integ-ration

HP-Only

Scale Out: Algorithms, design, protocols. → Wafer-scale package design → Perf. Analysis → Communication, compute primitives → TD Firmware Alpha → TD Firmware 1 Beta

Ecosystem: Sockets & Architecture Analysis → Arch& Socket Spec → TD Chiplet Design → System simulation / Validation → Chiplets tapeout+ fab → Chiplets + TD Unit Package Assembly& Bring up → TD Integ-ration

Tech Demonstrator: Specification and Planning → **Tech Demonstrator:** System Spec → Baseline TD Unit Package Design → Chiplet Bringup Package

Application Perf Analysis → Application Software Architecture → Sys Dev Environment → Application Beta → App 1 R1 and Integration

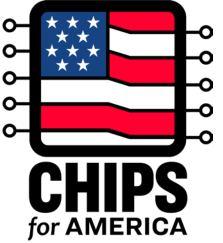
Baseline Demo

Variant Demo

- Performers expected to provide a detailed development plan
  - Suggested deliverables include functional test vehicles
- Intent is to cooperate across performers
  - Will require coordination

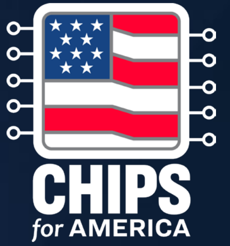
Design & Implementation Effort | Analytical Effort | Reports/Specs

Proposals must take advantage of advanced packaging technologies



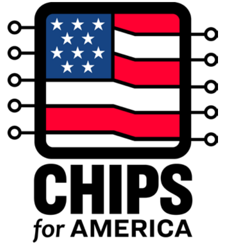
Out of scope for this R&D area are:

- Chiplet designs that are extensions of conventional approaches, based on commodity packaging that do not directly leverage advanced packaging in their architecture
- Chiplet designs with D2D interfaces tightly coupled to the choice of a SoC-bus (system-on-chip bus) or other high-level protocols
- Standalone chiplet designs for any function not coupled to a chiplet ecosystem.
- Proposals that focus on unmodified reuse of existing chiplets, target the development of new chiplets to integrate with existing chiplets
- Use wire-bonding for D2D interconnect.



Wrap Up

Chiplets Research and Development Area



RDA Drivers

- Leverage Advanced Packaging attributes:
  - “Wire abundance”: Hundreds to thousands of wires between chiplets as an inflection point that influences system design
  - Ultra-large packages: Build systems from hundreds to thousands of chiplets in one package
  - Heterogenous integration: incorporation of separately manufactured components

Critical Objectives

- Scale-down: Die-to-die interfaces based on hundreds/thousands of wires between chiplets at bond pitches of 10μm and lower
- Scale-out: Wafer-scale systems built with hundreds to thousands of chiplets
- Ecosystem: Unique functional and physical modularity for heterogeneous integration
- Technology Demonstrators: Implement and demonstrate innovations in chiplets and packaging. In one of either High-Performance or Low-Power domains.

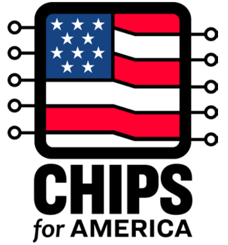
Key Outputs

- Technology demonstrators with packages/chiplets at 10μm bond pitch to show value of advanced packaging for applications
  - Optional: Chiplets/system designs that uniquely exploit wire abundance
- “Wire-like” low-power low-latency die-to-die interface implemented.
- Specification for functional and physical modular socket-based ecosystem.
- Analytical study on scale-out capabilities

Out of Scope

- Chiplet designs that are extensions of conventional approaches
- Unmodified reuse of existing chiplets
- Standalone chiplet designs for any function not coupled to a chiplet ecosystem
- Target the development of new chiplets to integrate with existing chiplets
- Chiplet designs based on commodity packaging
- Wire bonding for D2D interconnect,

Collaboration with Other Research and Development Areas



- Chiplet sizes
- Fiduciaries and alignment

- Reference architecture
- Socket specifications

- Socket specifications
- Reference architecture

- Substrates for prototyping
- Substrate models and analysis

Equipment, tools, processes, and process integration

Power delivery, and thermal management

Materials and substrates

Connectors (Photonics & RF)

Chiplets ecosystem

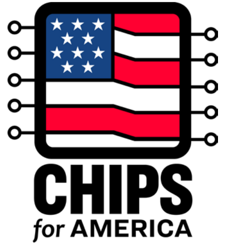
Co-design/ Electronic Design Automation

National Advanced Packaging Piloting Facility

Prototype packaging and assembly

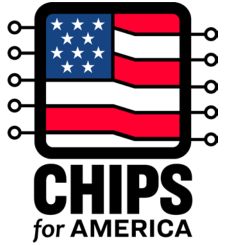
- PDK and models
- Design and analysis tools

Collaboration is Critical for Success



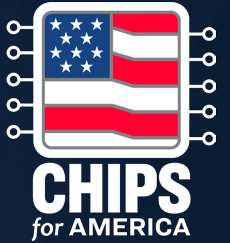
- System houses and end users
- EDA vendors
- Chiplet designers
- Chiplet fabricators
- Materials and substrate suppliers
- Equipment and tool vendors
- Educational institutions
- Thermal and connector solutions
- OSATS and IDMs
- Prototypes

Successful execution will require collaboration between proposers and each R&D Area. Proposers must clearly understand the ideas presented in each R&D Area. We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the NAPMP.



Next Steps

- NOFO 2: Concept papers due 12/16
- Visit CHIPS.gov for resources, including:
  - Upcoming R&D Area Webinars
  - FAQs
  - Funding opportunities and NOFO updates
- Join our mailing list
- Contact us
  - askchips@chips.gov – general inquiries
  - apply@chips.gov – application-related inquiries



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