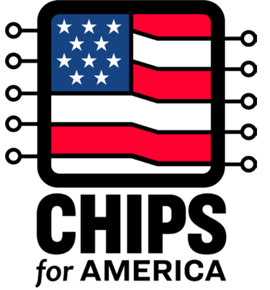
Co-Design EDA



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October 22, 2024

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

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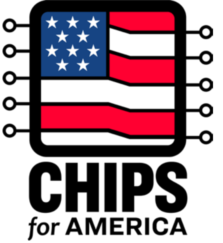

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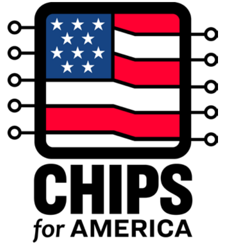
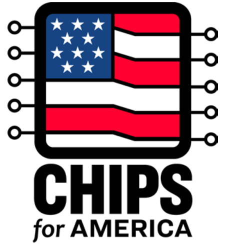
Key Dates



Date	Milestone
July 9, 2024	NOI (Released)
October 17, 2024	Advanced Packaging R&D (Released)
October 22, 2024	Advanced Packaging R&D Proposer's Day
December 20, 2024	Concept Papers Due Date
TBD	Invitation for Full Application Submission
TBD	Full Application Due

CHIPS for America QR Code:
CHIPS NAPMP NOFO 2
(full text)

EDA RDA Drivers



RDA Drivers

- Scale-out Advanced Packaging designs containing hundreds of Chiplets on a single substrate are complex physical objects and systems that exceed the capabilities of existing EDA solutions. New EDA abstractions and capabilities are needed for wafer-scale Chiplet-based AP systems.

Critical Objectives

- Design Implementation and Verification (Design)
- Embedded Security (Security)
- Test, Repair, Resilience, Reliability, and Fault Tolerance (Resilience)
- Independent Integration, Verification and Validation (IV&V)

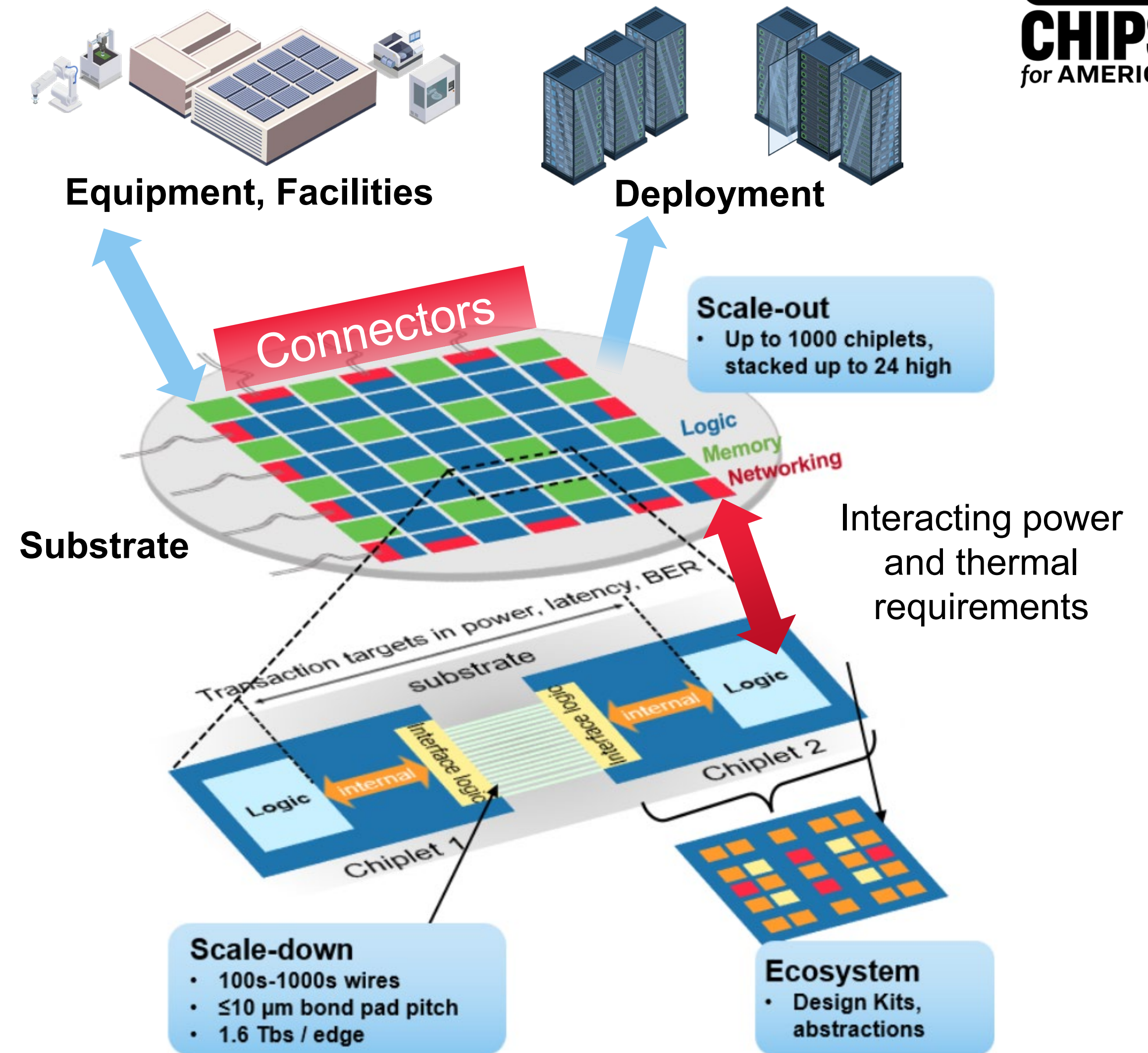
Key Outputs

- A Chiplet-level layer of abstraction
- Documented Design, Security, and Resilience Platform architectures and tools;
- Demonstrations of functionality for each tool and;
- Objective specific outputs as described in the NOFO

Chiplets ecosystem | Connectors (Photonics & RF) | Power delivery, and thermal management | Equipment, tools, processes, and process integration | Materials and substrates

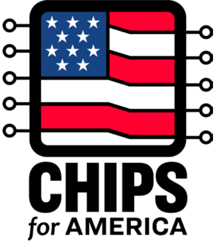
EDA RDA Drivers

- A scale-out, scale-down package is a highly complex physical object
  - Encapsulates electro-thermal-mechanical interactions across a wide range of distance and time scales
- A scale-out, scale-down package is a highly complex system of chiplets
  - Requires new layers of abstraction, new approaches to design, verification, security, and resilience
- Critical R&D Objectives
  - **Design** Implementation and Verification
  - Embedded **Security**
  - Test, Repair, **Resilience**, Reliability, Fault Tolerance
  - Independent Integration, Verification and Validation (**IV&V**)



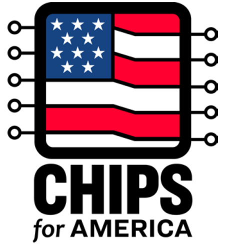
CHIPS for AMERICA

Covered Designs



- Developed solutions must be able to handle, as a single entity:
  - Designs built on any substrate
  - Up to 1000 chiplets of different X, Y, Z dimensions
  - Stacks up to 24 high
  - Heterogenous interacting subsystems including digital, analog, RF, and optical
  - Chiplets, connectors, thermal structures, embedded passives, interposers, and/or bridges up to wafer/panel scale
- See NOFO section 1.6.5.3.1 for full description

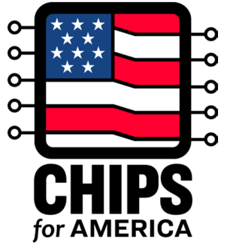
Critical Objectives



Proposals for this R&D area must address: *A)* at least one of Objectives 1-3, or *B)* Objective 4

Objective	
1. Design Implementation and Verification (Design)	(1) a documented Design Platform architecture; (2) a set of tools developed in accordance with that architecture; (3) system-based demonstrations of functionality; and (4) a built Design Platform system based on the architecture and integrating the tool sets produced in the project.
2. Embedded Security (Security)	(1) a documented Security Platform architecture; (2) a set of tools developed in accordance with that architecture; (3) simulation-based and system-based demonstrations of functionality; and (4) a built Security Platform based on the architecture and integrating the tool set.
3. Test, Repair, Resilience, Reliability, and Fault Tolerance (Resilience)	(1) a documented Resilience Platform architecture; (2) a set of tools developed in accordance with that architecture; (3) demonstrations of functionality for each tool; and (4) a built Resilience Platform system based on the proposed architecture and integrating the proposed tool set.
4. Independent Integration, Verification and Validation (IV&V)	(1) a documented IV&V Platform architecture; (2) a set of tools developed in accordance with that architecture; (3) demonstrations of functionality for each tool; (4) a built IV&V Platform system based on the proposed architecture and integrating the proposed tool set; and (5) a set of IV&V evaluations for Objectives 1-3 using the Platform.

Key Elements of EDA Solutions



The advanced end-to-end EDA solutions intended to emerge from this R&D investment comprise four elements:

1) **Design Platform** providing a full suite of design implementation and verification capabilities and serving as the primary working interface for design teams engaged in wafer scale Chiplet advanced packaging

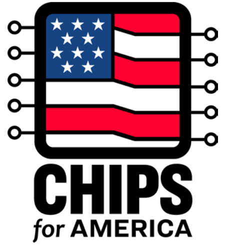
2) **Security Platform** enabling verifiable secure-by-design capabilities for trustworthy products.

3) **Resilience Platform** providing all-life-stages test, repair, resilience, reliability, and fault tolerance design capabilities for reliably resilient products

4) **Process and Assembly Design Kit** (PADK) encapsulating all relevant data for advanced package co-design and EDA solutions developed throughout the RDAs

In order to develop a design ecosystem that will interface with the NAPPF

EDA RDA Schedule & Dependencies: Summary



Year 1				Year 2				Year 3				Year 4				Year 5			
1Q	2Q	3Q	4Q	5Q	6Q	7Q	8Q	9Q	10Q	11Q	12Q	13Q	14Q	15Q	16Q	17Q	18Q	19Q	20Q

CD Phase 1: Architecture

CD Phase 2: Alpha Implementation

CD Phase 3: Beta Implementation

CD Phase 4: Productization

Design: Alpha Design

Security: Alpha Design

Resilience: Alpha Design

IV & V: Alpha Design

Beta Designs

Final Designs

Built Instances

Test infra.

PADK

Chiplets ecosystem

Connectors (Photonics & RF)

Power delivery, and thermal management

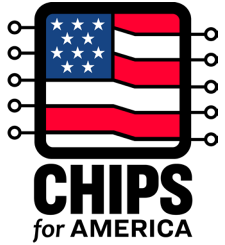
Equipment, tools, processes, and process integration

Materials and substrates

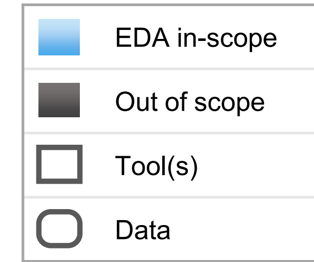
Prototypes

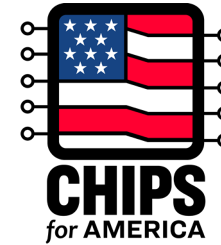
Facilities

Collaboration with Other RDAs



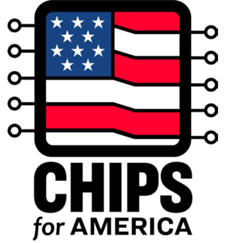
Co-Design and EDA scope





Cloud Computing

Massively Parallel Independent Processing



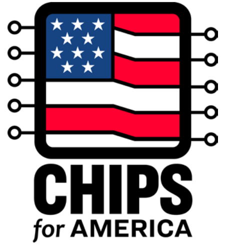
The Co-Design and EDA RDA is focused on cloud-native algorithms that consist of:

- Inherently distributed file systems
- Scalable capacity
- Massively distributed computation
- Container-based compute
- API level communication

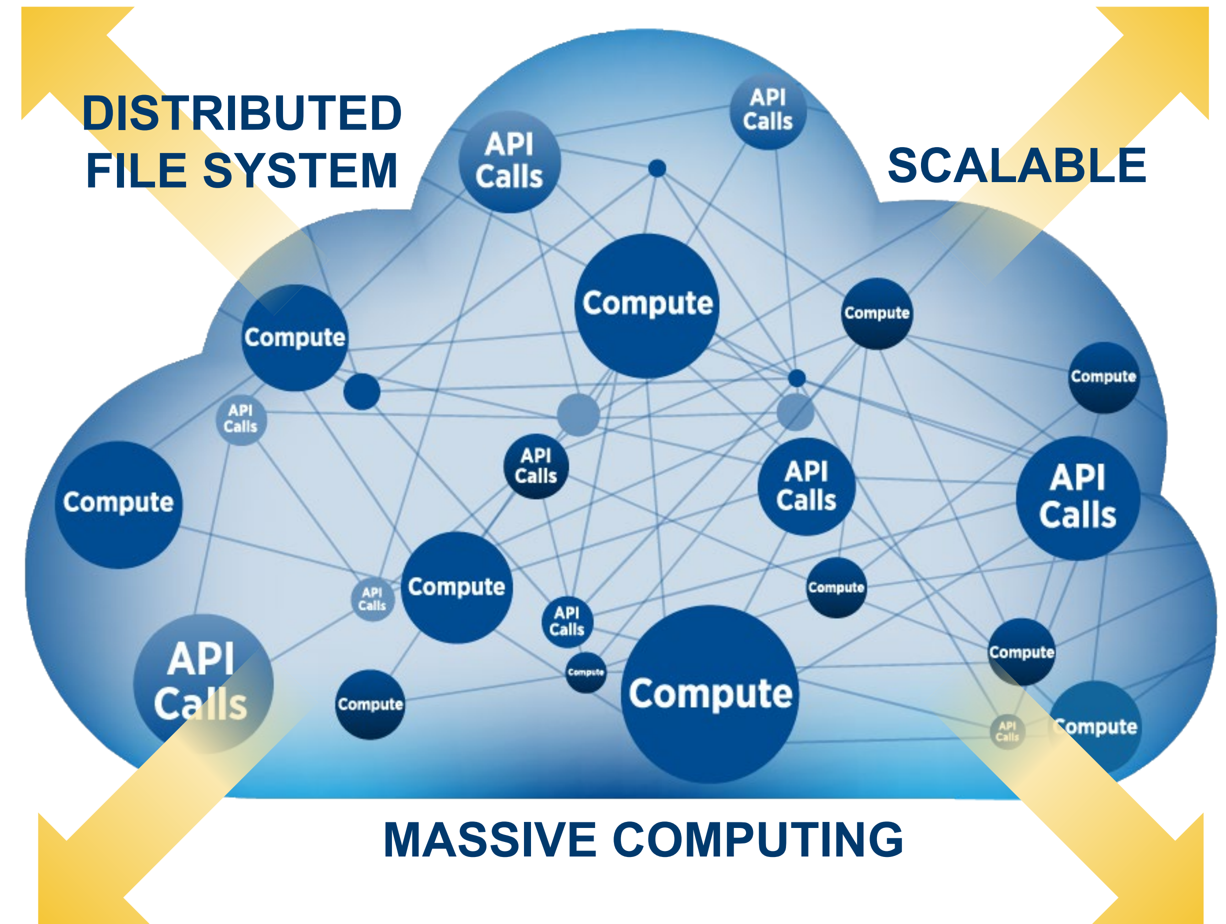
The Co-Design and EDA RDA creates a paradigm shift for EDA by:

- Developing innovative algorithms that scale with systems
- Utilizing the advantages of cloud both now and in the future
- Using scale to focus on system-wide co-design and optimization instead of point solutions

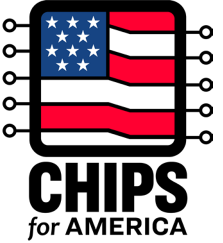
Cloud-based tools



1. **Cloud-based design exploration framework:**
    - Uses chiplets as an abstraction layer
    - Enables evaluation of tradeoffs in power, thermal, performance, area, cost and other relevant metrics
    - Execution time of no more than **2 hours per cycle** for 1000 chiplet design
    - vCPU needs that scale linearly with the number of chiplets
2. **Cloud-based design implementation framework:**
    - Fully automated package and system-of-chiplet mechanical design, floorplanning, placement, full ultrafine pitch routing, power and clock delivery, timing, simulation, multiphysics analysis, verification, validation, visualization, LVS/DRC
    - Execution time of no more than **8 hours per cycle** for 1000 chiplet design
    - vCPU needs that scale linearly with the number of chiplets
3. **Cloud-based design sign-off framework:**
    - Automated generation of all deliverables needed for manufacturing
    - Execution time of no more than **24 hours per cycle** for 1000 chiplet design
    - vCPU needs that scale linearly with the number of chiplets

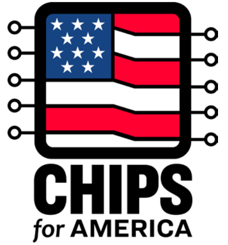


Use of AI/ML in proposed solutions



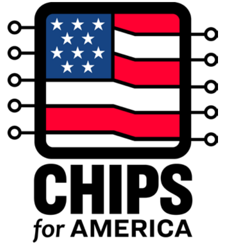
- AI/ML can be proposed as a portion of a solution
- Applicants must describe the expected models and training data along with an overview of any expected gains/limitations compared to an approach not using AI/ML
- Incorporating AI/ML early on, rather than retrofitting it later, has the potential to fundamentally change how these solutions work

Co-Design, yield and resilience



- Example output for Resilience Objective from the NOFO
  - A design exploration tool using chiplets as an abstraction layer that enables evaluation of tradeoffs between **manufacturing test, redundancy/repair/isolation capability, fault/error tolerance, and graceful degradation/failure** for systems that may include digital, analog, RF and/or photonic components.
- Building working, resilient advanced packaging systems involves the co-design of many different capabilities and a corresponding need to develop infrastructure to gather and analyze relevant data throughout the manufacturing process and device operation

EDA RDA Objective Out of Scope



Out of Scope Design

- Design capabilities for purely monolithic systems, silicon tapeout or core circuit IP block development
- Development of any chiplet-level application, operating system (OS), or driver software
- System architecture, neuromorphic solutions, and solutions primarily focused on chiplet-level EDA

Out of Scope IV&V

- Proposals that feature hardware or manufacturing demonstrations
- Proposals that are based around non-cloud computing platforms
- Proposals that seek to alter or replicate rather than integrate and evaluate deliverables from other Objectives

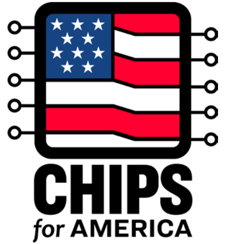
Out of Scope Resilience

- Proposals primarily focused on new test equipment or intra-chiplet DFT techniques
- Communication standards conformance demonstrations, including bit error rate (BER) demonstrations
- Fault tolerant system architectures
- New information coding techniques
- Demonstrated compliance with ISO 26262 or other domain-specific functional safety standards is not required

Out of Scope Security

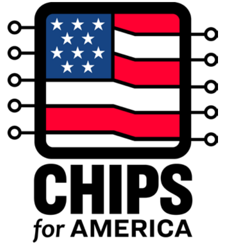
- Software security (e.g. software-based pointer checks)
- System security service functionality (e.g., encryption services)
- Secure communications protocols
- Encryption techniques including fully homomorphic
- Explainable AI
- Anything subject to national security classification
- Developing or managing external asset management capability
- Intra-chiplet hardware security techniques (e.g., physically unclonable functions, logic locking)

Program Structure



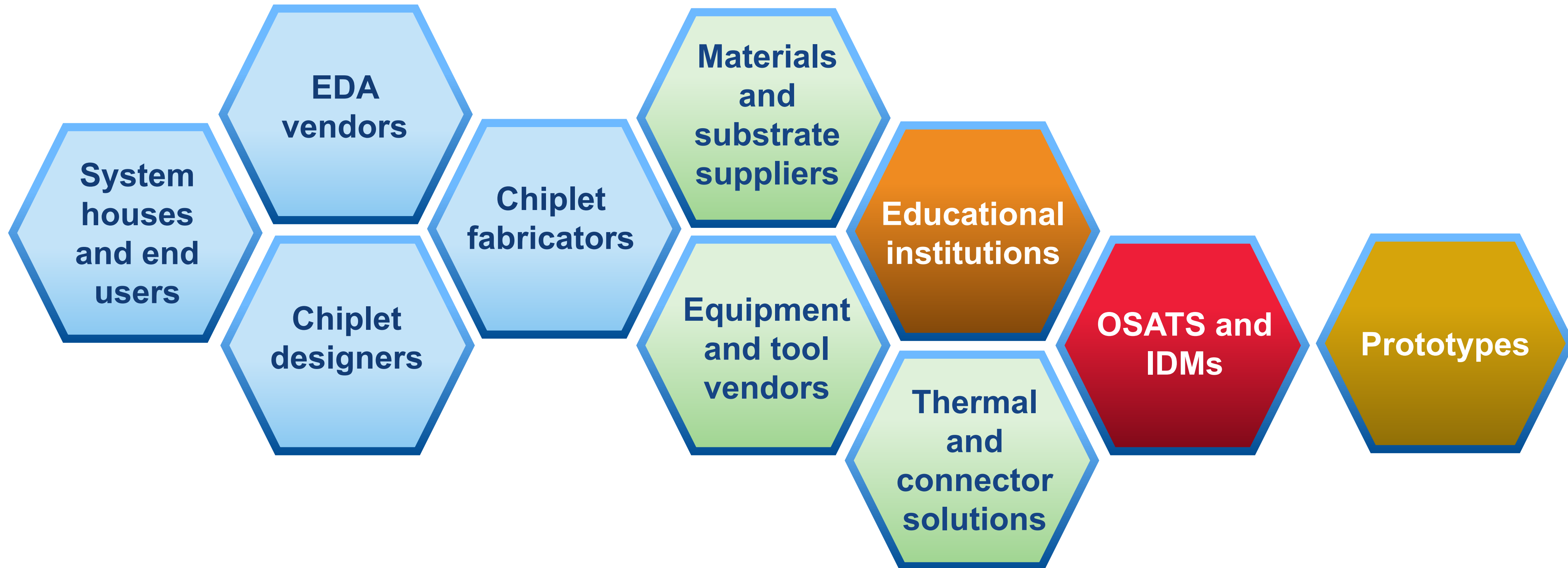
- For the Co-design/Electronic Design Automation (EDA) R&D area, CHIPS R&D anticipates making available approximately $250,000,000 for funding multiple awards in amounts ranging from a minimum of approximately $10,000,000 to a maximum of approximately $100,000,000 in Federal funds per award.
- Multiple awards for projects varying in scope and funding amount are expected under this NOFO, with a period of performance of five (5) years per award.
  - Projects should be divided into four (4) phases over a period of performance of five (5) years.
    - Phase 1 (12 months)
    - Phase 2 (18 months)
    - Phase 3 (18 months)
    - Phase 4 (12 months)
  - While cost share is not be required, CHIPS R&D will give preference to applications that demonstrate credible cost share commitments. Cost share generally consists of labor, materials, equipment, software, facilities costs, and other investments directly related to the project.

Co-Design and EDA Summary

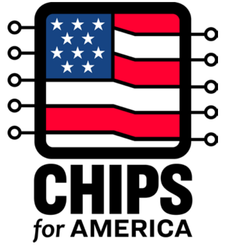


- Advanced packages containing systems of hundreds of chiplets need a new abstraction layer to support innovative EDA tools and design flows.
- Co-designing all aspects of package and system as a single entity will lead to improved optimizations and eventually enable new architectures
- The Co-Design and EDA RDA includes four Objectives:
  1. **Design Implementation and Verification (Design)**
  2. **Embedded Security (Security)**
  3. **Test, Repair, Resilience, Reliability, and Fault Tolerance (Resilience)**
  4. **Independent Integration, Verification and Validation (IV&V)**
- Proposals for this R&D area must address at least one of Objectives 1-3, or Objective 4
- Refer to the Notice of Funding Opportunity (NOFO) for details.

Collaboration is Critical for Success

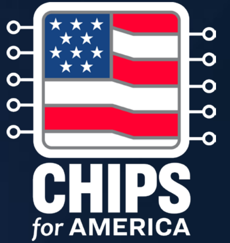


Successful execution will require collaboration between proposers and each R&D Area. Proposers must clearly understand the ideas presented in each R&D Area. We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the NAPMP.



Next Steps

- NOFO 2: Concept papers due 12/16
- Visit CHIPS.gov for resources, including:
  - Upcoming R&D Area Webinars
  - FAQs
  - Funding opportunities and NOFO updates
- Join our mailing list
- Contact us
  - askchips@chips.gov – general inquiries
  - apply@chips.gov – application-related inquiries



Thank you for attending

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