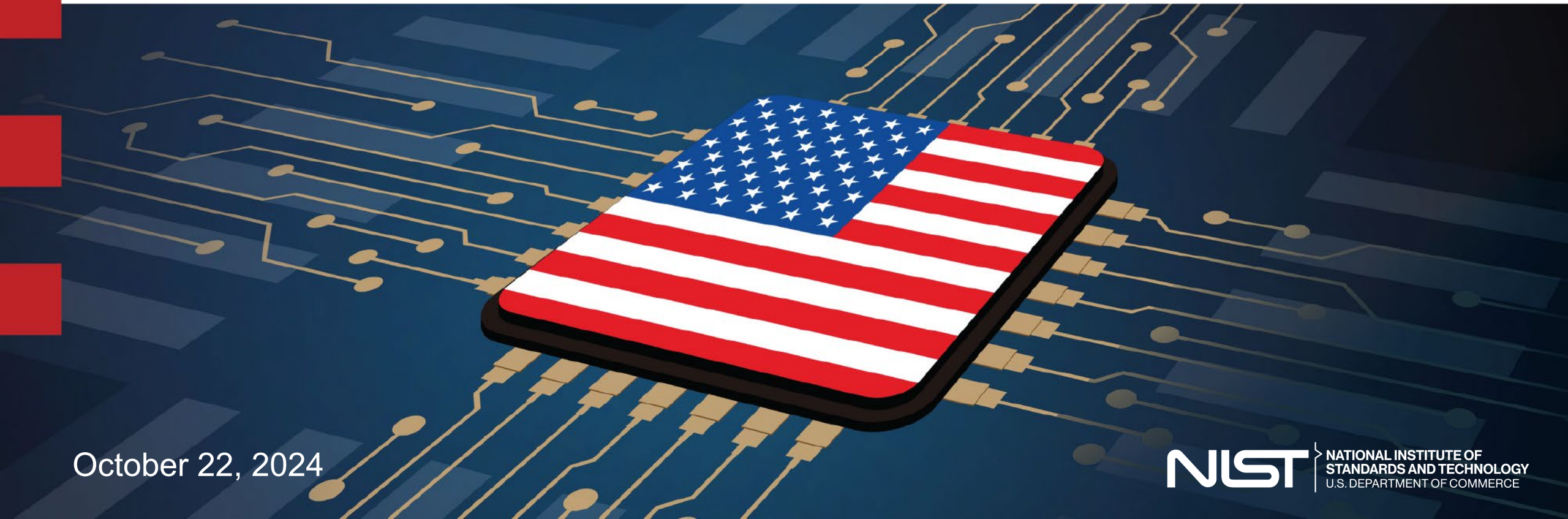
Equipment, Tools, Processes and Process Integration

PM: Robert J. Soave, PhD



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CHIPS for AMERICA

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

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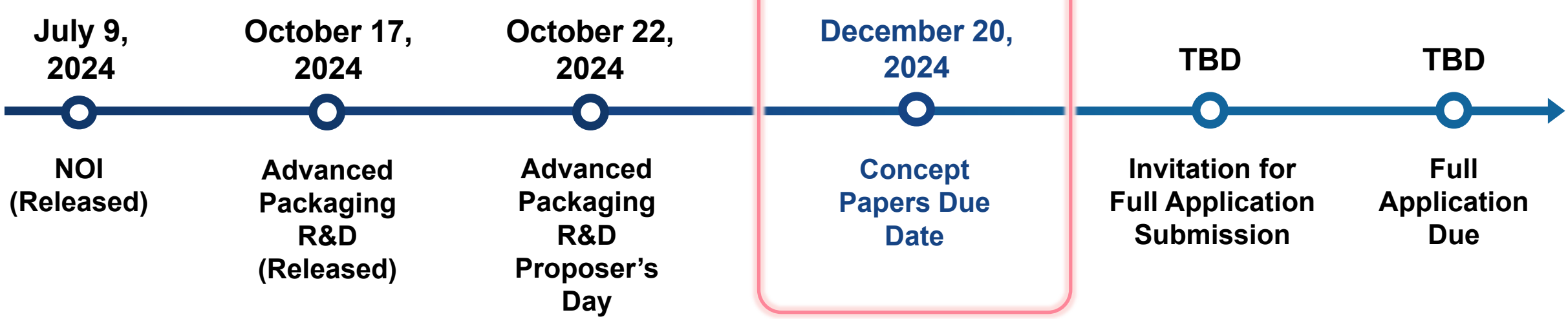
Key Dates



CHIPS for America QR Code:
CHIPS NAPMP NOFO 2
(full text)

Equipment, Tools, Processes and Process Integration (ETPI) R&D Area

- Advances in packaging processes and equipment are required to achieve the scaled down dimensions set out in the previous NAPMP Materials and Substrates NOFO, and to enable innovative, manufacturable advanced packaging flows suitable for adoption by U.S. industry
- The processes and equipment that are the focus for this R&D area are those that will enable end-to-end advanced packaging flows suitable for high-volume manufacturing, customized manufacturing, piloting, and prototyping
- This investment is intended to achieve the following outcomes:

  3-5 years:

  - New tools, processes, and integrated flows are **installed in the NAPPF** to assess efficacy and extendibility, and to gather insights into suitability for commercial adoption
  - Tools and processes are incorporated in NAPPF prototyping flows
  - Programs are established to improve tool and process performance and packaging flow manufacturability

  10 years: Robust production equipment and integrated advanced packaging processes for chiplet-based manufacturing at commercial scale are available and in use by U.S. industry

ETPI R&D Drivers

- Develop, demonstrate and deliver advanced processes and equipment that achieve the scale-down dimensions and scale-out assembly targets required for advanced packaging
- Develop innovative, manufacturable end-to-end integrated process flows (IPF) that leverage these newly developed capabilities
- Install resulting tools, process technologies and integrated process flows in the NAPPF as primary vehicles for development and prototyping
- Key tool and process R&D focus areas include:
  - Advanced alignment and bonding methods to connect chiplet arrays with fine-pitch connection points
  - Flexible, manufacturable fine-pitch assembly methods to produce dense chiplet arrays and advanced 3DHI chiplet stacks
  - Equipment to run processes at commercial scale and handle the substrates, wafers and dies

Two Categories Within This RDA

Process Cluster Development

- Tools and processes required for key parts of an advanced packaging flow
- Category is further sub-divided into 5 process clusters (descriptions follow)
- Respondents may submit proposals to one or more of the 5 process clusters

End-to-End Integrated Packaging Flows

- Sequencing multiple clusters into end-to-end packaging process flows to create a functional, testable packaged system or subsystem
- Includes designing and implementing a comprehensive Bring-up Assembly Vehicle with test structures and diagnostics to demonstrate and optimize the flow

Respondents may submit proposals for one or both categories

Equipment and Process Development: Process Clusters

Development organized around five (5) **process clusters**, defined as a sequence of steps that enable a key part of the packaging flow:

1) **Chiplet Singulation:** Low-damage, high-precision methods to singulate incoming wafers patterned with dies, to produce chiplets ready for the assembly process
2) **Chiplet to Substrate Assembly and Bonding:** Positioning and attaching chiplets with ultra-fine pitch bonding pads to substrates, in dense arrays with close chiplet-to-chiplet spacing
3) **Three-Dimensional Heterogeneous Integration (3DHI):** Forming heterogeneous chiplet stacks with ultra-fine-pitch chiplet-to-chiplet connections
4) **Collective Chiplet Processing:** Methods to simultaneously process an array of chiplets using a handler wafer or other suitable substrate
5) **Finishing:** Incorporating advanced power delivery, passivation, thermal management, and connectors, including photonics, into the packaged device

Process Cluster Development Proposals (Category 1)

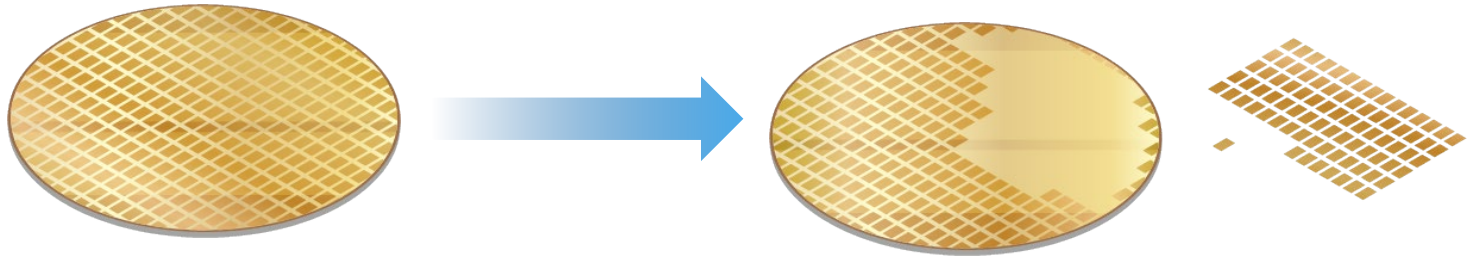
- Applicants may submit proposals that address full tool and process solutions for one or more of the 5 clusters
- Successful proposals will present a comprehensive R&D approach encompassing integrated tool and process development, interactions between process steps, and step sequencing within each cluster and between clusters as appropriate
- Proposals must describe metrology methods and proposer-supplied test vehicles that will be used to characterize, optimize, and validate process, tool, and cluster efficacy
- CHIPS R&D strongly encourages applications from multi-disciplinary, multi-organization project teams that collectively demonstrate the full range of expertise, experience, and development capabilities needed to achieve the technical objectives
- *Applicants are strongly encouraged to incorporate in their proposals innovative and potentially transformative technologies to improve cluster performance, capabilities and manufacturability*

Process Cluster Descriptions

(Note: Illustrations depict notional examples)

Process Cluster Overview: Cluster 1

Cluster 1
Chiplet Singulation



R&D Objective: Develop advanced, manufacturable process flows and associated equipment to dice incoming wafers and produce singulated chiplets ready for the assembly process

Scale-Down and Scale-Out Requirements

- Bonding surfaces free from defects and contaminants that impact bond quality, yield and reliability
- Precise chiplet dimensions and defect-free sidewalls to enable close chiplet-to-chiplet spacing
- Flexible tools and processes to singulate a variety of incoming wafer sizes and materials, including bonded wafer stacks

R&D Focus: Center on advanced, high-precision, low damage dicing / separation methods

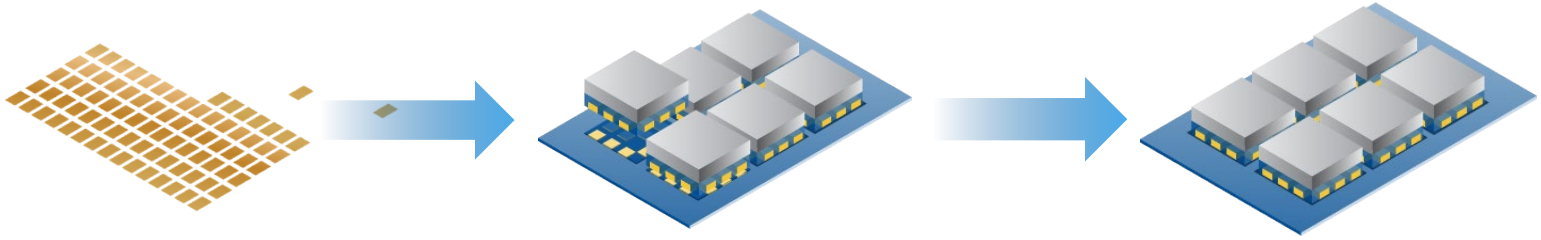
Out of Scope:

- Extensions to conventional saw blade dicing

➢ Note: Multi-step processes requiring a saw-blade step to meet cluster requirements are permitted

Process Cluster Overview: Cluster 2

Cluster 2
Assembly and Bonding



R&D Objective:

- Develop full tool and process solutions to position and connect dense arrays of heterogeneous chiplets on substrates, with ultra-fine-pitch connection points and close chiplet-to-chiplet spacing
- This is an essential capability to develop and establish manufacturable advanced packaging flows suitable for adoption by U.S. industry

R&D Focus

- Center on advanced bonding processes, alignment techniques and fine pitch assembly methods to achieve program targets for connection pitch, positioning precision, and chiplet spacing
- Integrated tool and process approach to develop and optimize all factors related to assembly and bonding
- Wafer-to-wafer, chiplet-to-substrate and chiplet-to-chiplet bonding all have applications in advanced packaging and 3DHI, and are therefore in scope. Alternate assembly methods will be considered.
- Respondents to this cluster are strongly encouraged to include a proposal for an End-To-End Packaging Flow

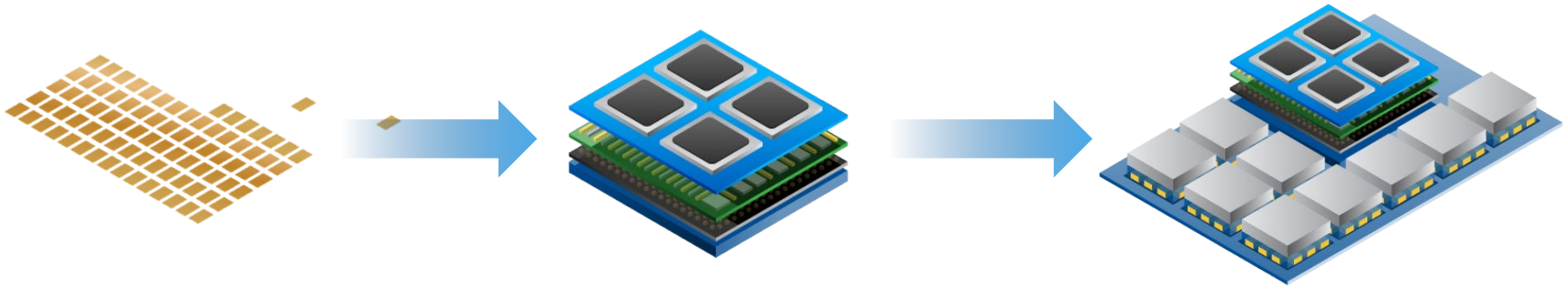
Out of scope

- Extensions to solder-based assembly used in conventional packaging

➢ Note: Enhancements to the bond interface metallurgy that yield measurable benefits are permitted

Process Cluster Overview: Cluster 3

Cluster 3
3DHI



R&D Objectives:

- Develop manufacturable integrated process flows to produce stacks of heterogeneous chiplets with ultra-fine-pitch die-to-die connection points
- Integrate these stacks into the packaging assembly or subassembly
- Significantly advance 3DHI manufacturing technology for adoption by U.S. industry

R&D Focus

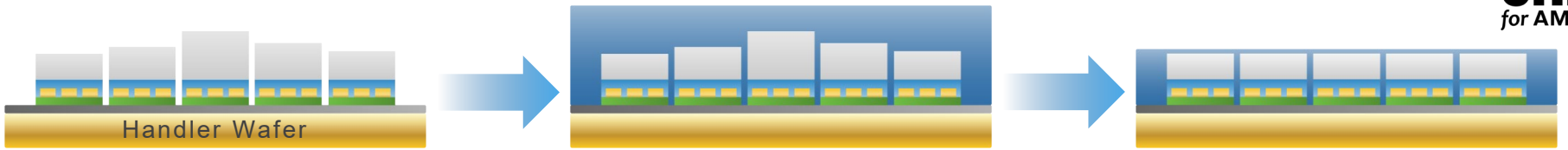
- Integrated approach to develop and optimize the 3DHI process flow, from incoming chiplet preparation, to stack assembly, to stack testing, to integration into the package subassembly
- Integrate Thermal Management and Power Delivery innovations developed in R&D Area 2
- Respondents to this cluster are strongly encouraged to include a proposal for an End-To-End Packaging Flow

Cross-Program Coordination

- This 3DHI cluster will require many of the tool and process technology elements developed in other process clusters and R&D Areas. CHIPS R&D will work with successful 3DHI applicants to coordinate with these cluster and RDA teams, so project results collectively contribute to advancing 3DHI packaging architectures.

Process Cluster Overview: Cluster 4

Cluster 4
Collective Chiplet Processing

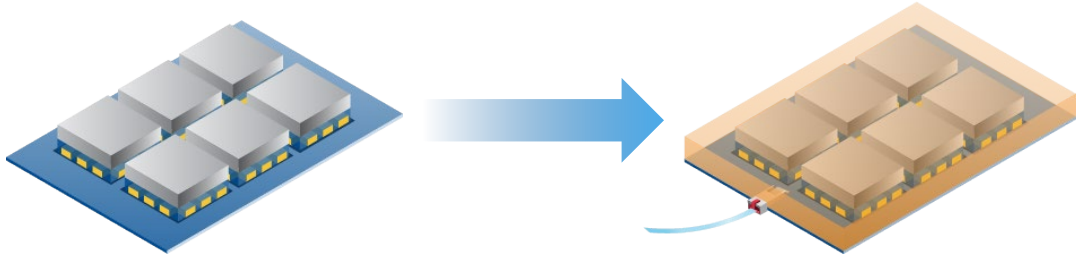


R&D Objective: Develop manufacturable methods to process groups of chiplets through operations within the packaging flow using a handler or other suitable substrate

- Examples of operations that may benefit from collective processing include without limitation:
  - Applying materials such as gap fill and passivation layers to a chiplet array (depicted above)
  - Backside thinning and polishing to produce chiplets with uniform thickness (depicted above)
  - TSV formation and reveal
  - Bonding surface CMP
  - Wet cleaning and surface preparation
  - Chiplet array reconstitution
  - Using a handler wafer to simultaneously bond a chiplet array to a packaging substrate
- Handler attachment based on for example tape, spin-on applied adhesives, and multi-layer adhesive systems are in scope, as are attachment methods that do not require an adhesive
- Equipment and methods for chiplet-to-handler placement, temporary bond and de-bond are all in scope

Process Cluster Overview: Cluster 5

Cluster 5
Finishing



R&D Objective: Develop equipment, processes, and methods that enable advanced finishing operations for substrates that have completed the assembly and bonding cluster

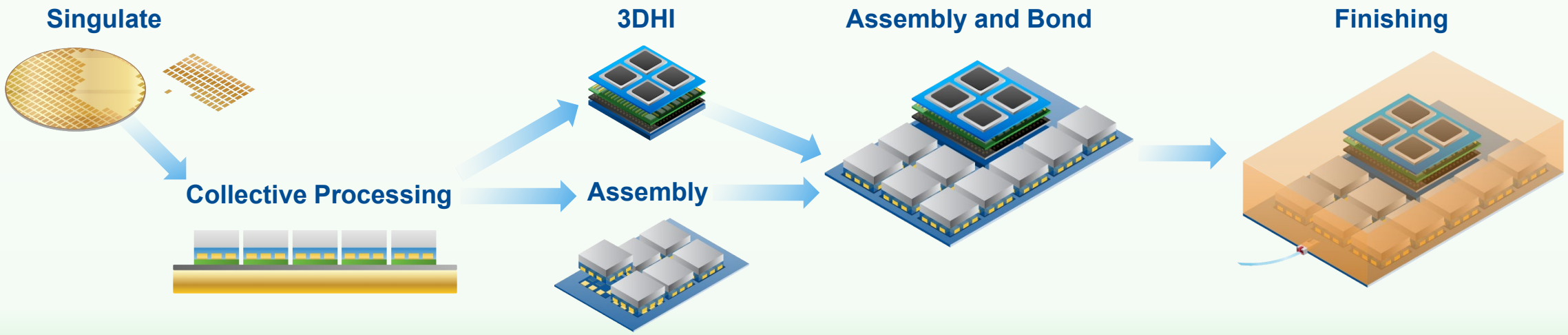
- Incorporating power delivery and thermal management elements developed in R&D Area 2
- Integrating and attaching the advanced connectors developed in R&D Area 3
  - Note: Respondents to R&D Area 2 and R&D Area 3 are encouraged include in their proposals activities to integrate the resulting innovations into the packaged device under this Finishing cluster
- Passivation – Protection and encasement of the bonded chiplets and other elements incorporated in the package Examples include without restriction:
  - Films to encase dense heterogeneous chiplet arrays
  - Highly conformal films for passivating elements in restrictive geometries
  - Corrosion protection and reliability enhancement
- Testing the chiplet assembly for functionality at a level sufficient to proceed with finishing operations
- Substrate singulation

End-to-End Packaging Flows (Category 2)

R&D Objective:

- Develop manufacturable end-to-end integrated packaging flows (IPF) to create a functional, testable packaged system (or subsystem) with performance characteristics that leverage the advanced packaging constructs being funded
- Successful proposals will be based on sequencing and integrating the process clusters and technology elements developed in this ETPI R&D Area

Notional example: Integrated packaging flow from sequencing process clusters



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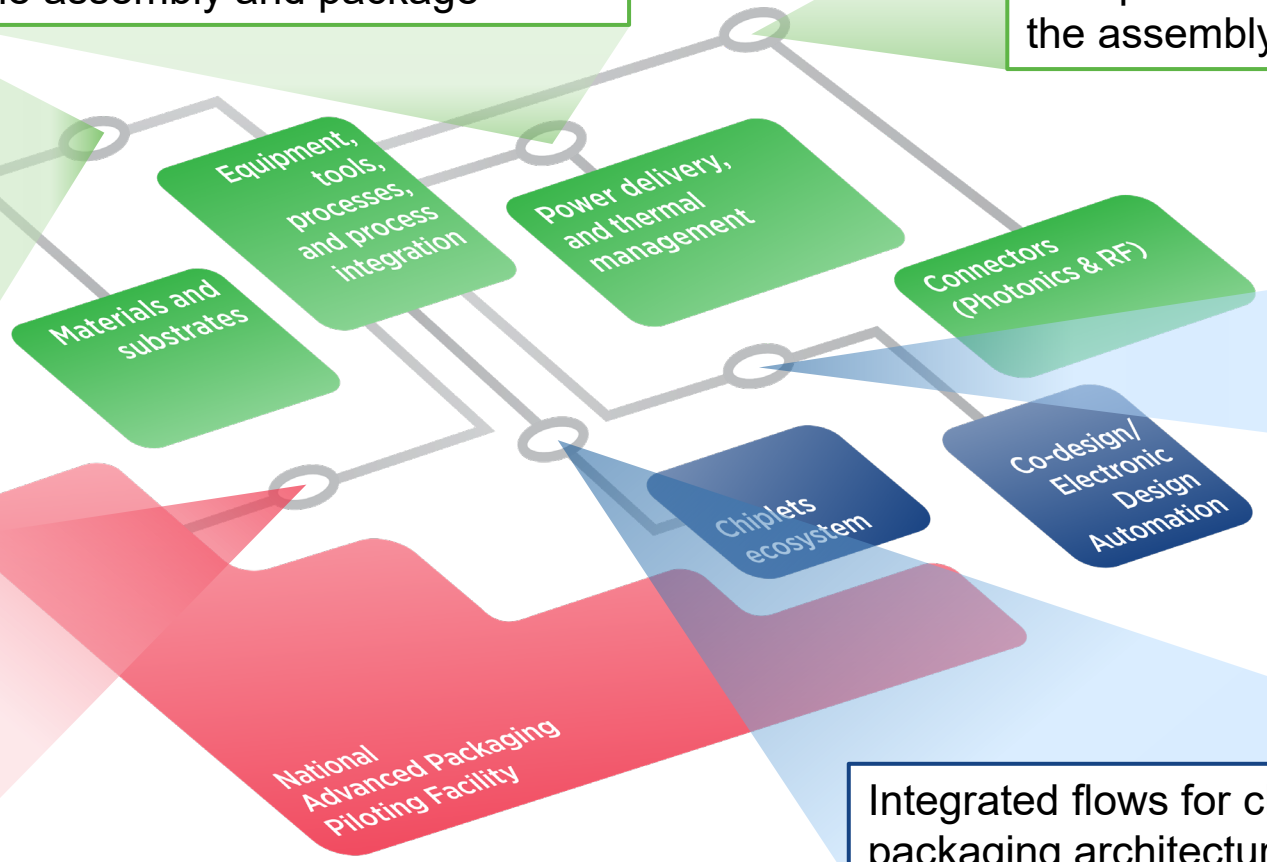
- Successful proposals will be based on sequencing and integrating the process clusters and technology elements developed in this ETPI R&D Area
- Proposals should include a **bring-up assembly vehicle** comprised of test chiplets designed to verify and characterize cluster and IPF efficacy
- IPFs will be installed as baseline flows in NAPPF as primary vehicles for optimization and development
- The bring-up assembly vehicle will be run on these baseline flows, with continuous improvements and periodic feature scaling, similar to the scaling model that drove Moore's Law
- Major cluster development programs are encouraged to include plans for an integrated packaging flow

Coordination and Alignment with Other RDAs

Tools and methods to incorporate thermal and power solutions in the assembly and package

Tools and methods to incorporate connectors in the assembly and package

Assembly and bonding compatible with fine scale connections and embedded features

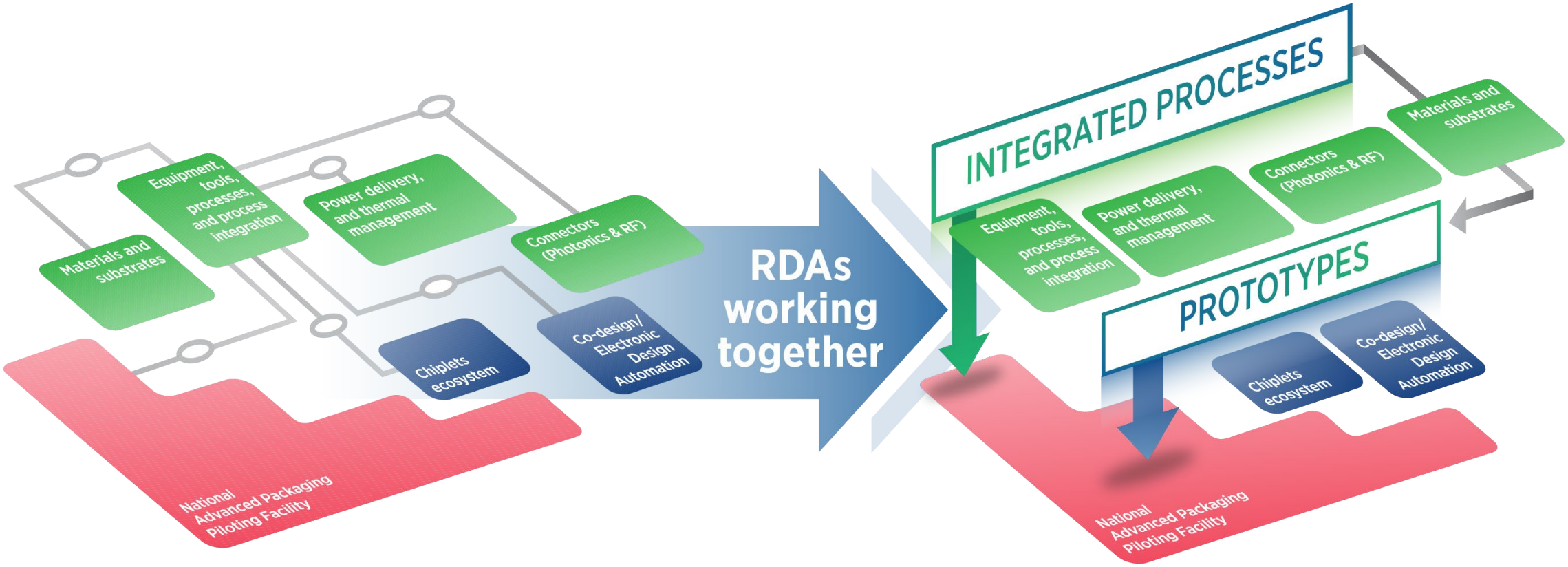


Process and alignment data for advanced models

Equipment and process infrastructure for development and prototyping

Integrated flows for chiplet-based packaging architectures

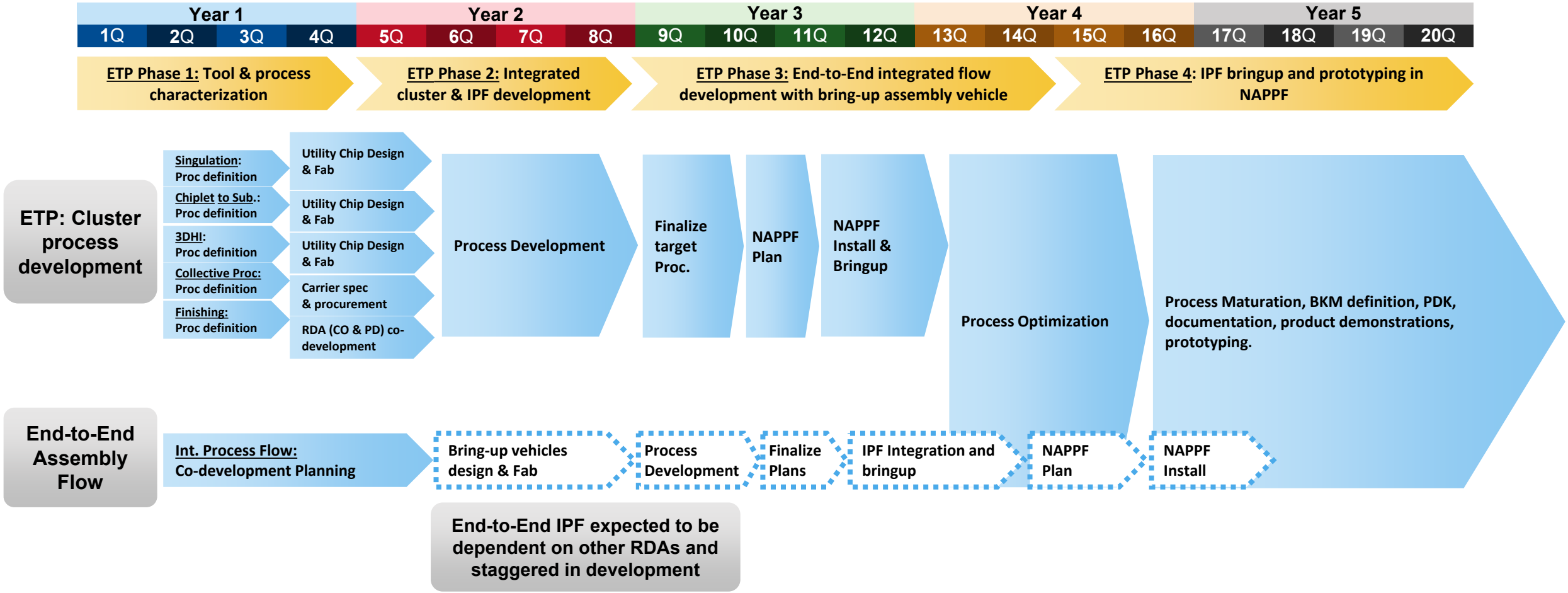
Enabling the NAPMP Vision



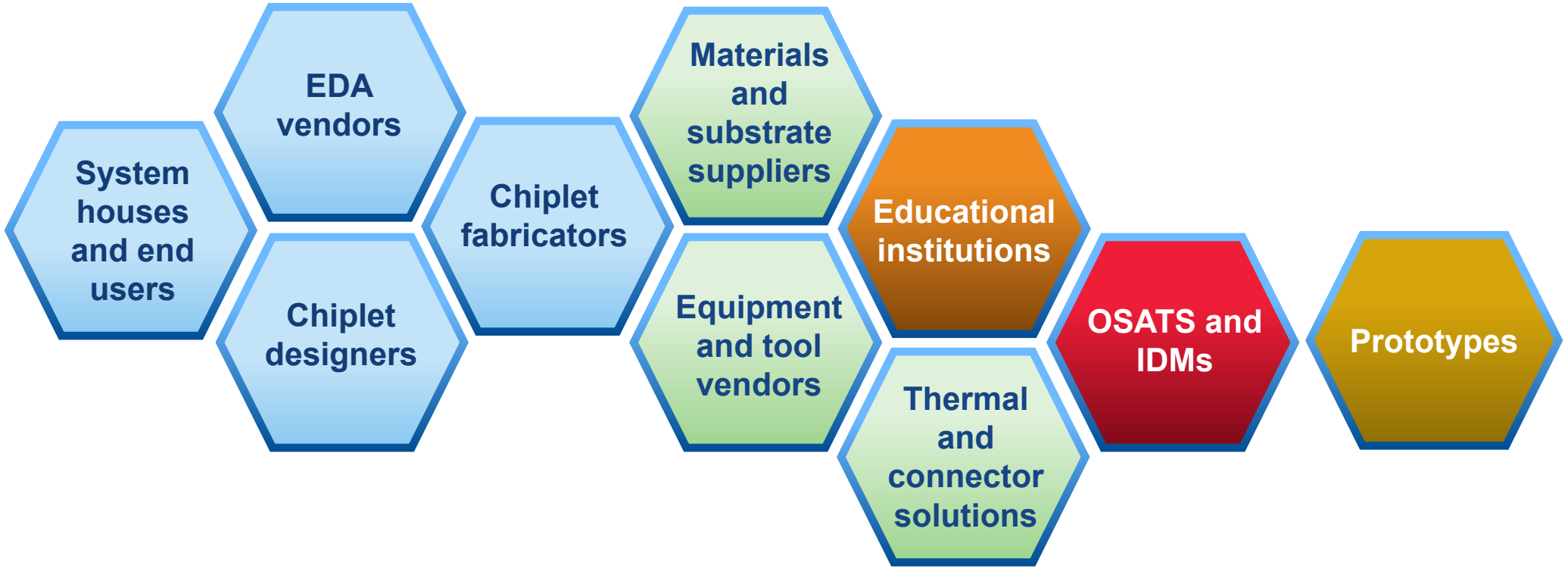
Program Structure

- Multiple awards varying in scope and funding are expected
  - Up to approximately $450,000,000 anticipated for funding multiple awards in amounts ranging from a minimum of approximately $10,000,000 up to a maximum of approximately $150,000,000
- CHIPS R&D strongly encourages multi-disciplinary, multi-organization project teams that collectively demonstrate the expertise, experience, and development capabilities to achieve the technical objectives
  - Collective team experience developing, demonstrating, and delivering advanced packaging equipment and integrated processes for forward-looking technology nodes will be a key factor in proposal evaluation
- Applicants must propose a detailed project plan for achieving Project-Level Technical Targets
- Projects should be divided into 4 phases over a period of performance of up to 5 years
  - Phase 1 *(12 months)*
  - Phase 2 *(12 months)*
  - Phase 3 *(18 months)*
  - Phase 4 *(18 months)*
- While cost share is not be required, CHIPS R&D will give preference to applications that demonstrate credible cost share commitments. Cost share generally consists of labor, materials, equipment, software, facilities costs, and other investments directly related to the project.

Example of Phased Project Plan



Collaboration is Critical for Success



Successful execution will require collaboration between proposers and each R&D Area. Proposers must clearly understand the ideas presented in each R&D Area. We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the NAPMP.

Next Steps

- NOFO 2: Concept papers due 12/16
- Visit CHIPS.gov for resources, including:
  - Upcoming R&D Area Webinars
  - FAQs
  - Funding opportunities and NOFO updates
- Join our mailing list
- Contact us
  - askchips@chips.gov – general inquiries
  - apply@chips.gov – application-related inquiries

Thank you for attending

Visit CHIPS.gov for future updates and additional information