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DEPARTMENT OF COMMERCE

CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

Advanced Packaging Research and Development

AGENCY: National Institute of Standards and Technology, Department of Commerce

ACTION: Notice of Intent (NOI)

SUMMARY: The CHIPS Research and Development Office (CHIPS R&D) intends to announce, via a Notice of Funding Opportunity (NOFO), an open competition for new research and development (R&D) activities to establish and accelerate domestic capacity for semiconductor advanced packaging. The technical focus and R&D goals of the NOFO are expected to be informed by recent industry roadmaps, which share the common theme that emerging applications like high performance computing and low power electronics, both needed for artificial intelligence (AI), require leap-ahead advances in microelectronics capabilities, including advanced packaging. Advanced packaging allows manufacturers to make improvements in performance and function and to shorten time to market. Additional benefits include a reduced physical footprint, lower power, increased chiplet reuse, and potentially decreased costs. Achieving these goals requires coordinated investments to support integrated R&D activities to establish leading-edge domestic capacity for semiconductor advanced packaging.

The purpose of this NOI is to offer preliminary information to potential applicants, facilitating the development of meaningful partnerships and strong, responsive proposals relevant to one or more of five R&D areas: (1) Equipment, Tools, Processes, and Process

Integration; (2) Power Delivery and Thermal Management; (3) Connector Technology, Including Photonics and Radio Frequency (RF); (4) Chiplets Ecosystem; and (5) Co-design/Electronic Design Automation (EDA).

In addition to the R&D areas, the NOFO is expected to include a specific opportunity for prototype development in exemplar application areas. These exemplar applications are likely to focus on areas such as high-performance computing and low-power systems needed for AI. Prototypes should be designed to demonstrate and validate research advances and new packaging flows resulting from projects supported through this NOFO.

More information about the expected CHIPS R&D NAPMP Advanced Packaging Research and Development NOFO will be available on the CHIPS for America website at https://www.nist.gov/chips/chips-rd-funding-opportunities.

FOR FURTHER INFORMATION CONTACT: Questions may be directed via email to askchips@chips.gov with "2024-NIST-CHIPS-NAPMP-Advanced Packaging" in the subject line, or via phone to Bill Burwell at 240-224-4335. All answers to questions, provided at the sole discretion of CHIPS R&D, will be posted on the CHIPS R&D website at https://www.nist.gov/chips/chips-rd-funding-opportunities, with further information provided on this site once the open competition has been announced.

SUPPLEMENTARY INFORMATION:

Purpose. The CHIPS Research and Development Office (CHIPS R&D) intends to announce, via a Notice of Funding Opportunity (NOFO), an open competition for new research and development (R&D) activities to establish and accelerate domestic capacity for semiconductor advanced packaging. CHIPS R&D anticipates awarding a total of up

to approximately $1,600,000,000 in cooperative agreements and other transaction agreements in amounts up to approximately $150,000,000 in federal funds per award. Multiple awards for projects varying in scope and funding amount are expected within this NOFO, with a period of performance of up to 5 years per award. While co-investment will not be required, CHIPS R&D will give preference to applications that demonstrate credible co-investment commitments. The purpose of this NOI is to offer preliminary information to potential applicants, facilitating the development of meaningful partnerships and strong, responsive proposals relevant to one or more of the R&D research and prototype[1] development areas described below.

CHIPS R&D Mission. The CHIPS and Science Act appropriated approximately $50 billion to the Department of Commerce – $39 billion in incentives to onshore semiconductor manufacturing and $11 billion to advance U.S. leadership in semiconductor R&D. Within CHIPS for America, the mission of CHIPS R&D is to accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic research efforts, tools, resources, workers, and facilities.

NAPMP Objectives. NAPMP, one of multiple CHIPS R&D initiatives, seeks to drive U.S. leadership in advanced packaging and provide the technology and skilled workforce needed for packaging manufacturing in the United States. Within a decade, NAPMP-funded activities, coupled with CHIPS manufacturing incentives, will establish a vibrant, self-sustaining, profitable, domestic packaging industry where advanced node chips

[1] The term "prototype" is used throughout to refer to a functional system produced through an end-to-end advanced packaging process flow for the purpose of demonstrating the characteristics of that flow and the prototype design, including packaging process characteristics such as process stability, yield, reliability, and defectivity; and prototype characteristics such as functionality, performance, power/energy consumption, and thermal dissipation.

manufactured in the United States and abroad can be packaged in appropriate volumes within the United States and innovative designs and architectures are enabled through leading-edge packaging capabilities. In combination with other CHIPS for America education and workforce efforts, NAPMP-funded activities will also produce the diverse and capable workforce needed for the success of the domestic packaging sector.

Advanced Packaging Research and Development NOFO Objective. The intended objective of the NOFO will be to enable, through R&D, innovative new advanced packaging flows suitable for adoption by U.S. industry. To pursue this objective, CHIPS R&D expects to design the NOFO with the following elements. First, the NOFO is expected to set out R&D areas to be supported in addressing key challenges and technology gaps in advanced packaging. Second, it is expected to provide for coordinated R&D efforts aligned through common technical targets so that results collectively contribute to composable and implementable advanced packaging flows. Finally, it is expected to provide for demonstrating the benefits of R&D results through a combination of prototypes and baseline packaging flows.

Background. The technical focus and R&D goals of this NOFO are expected to be informed by a series of industry roadmaps, including the 2024 IEEE Heterogeneous Integration Roadmap (https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2024-edition.html) and International Roadmap for Devices and Systems (https://irds.ieee.org/editions), the Semiconductor Research Corporation (SRC) Microelectronics Advanced Packaging Technologies Roadmap (https://srcmapt.org/); the UCLA and SEMI Manufacturing Roadmap for Heterogeneous Integration and Electronics Packaging (https://chips.ucla.edu/page/MRHIEP Project/MRHIEP Final

Report); and the iNEMI 5G/6G mmWave Materials and Electrical Test Technology Roadmap (https://www.inemi.org/article_content.asp?adminkey=cc22bf8eb1bfb8248c594509fe54dd9b&article=275). Collectively, these roadmaps emphasize that emerging technologies like high performance computing and artificial intelligence, advanced telecommunications, biomedical devices, and autonomous vehicles require leap-ahead advances in microelectronics capabilities.

In the past, the semiconductor industry has largely addressed performance needs by increasing the number and density of transistors on a chip, a process known as miniaturization. However, the previous pace of miniaturization, as expressed by Moore's Law, is slowing and cannot alone provide the performance improvements needed for emerging microelectronics technologies. Improving all aspects of system performance to support the breadth of new semiconductor applications will require innovations in advanced packaging.

Semiconductor packaging serves two general purposes. One is to protect the chip mechanically, thermally, and environmentally. The other is to enable reliable inter-chip communication and data processing, power delivery, and a stable test and system integration platform. Advanced packaging and related capabilities, such as heterogeneous integration, are designed to increase all aspects of system performance by linking multi-component-assemblies with large numbers of interconnects to achieve a degree of integration that blurs the line between chip and package.

Program Drivers: In designing proposals, applicants should consider in their planning activities the below five program drivers guiding the design of this NOFO.

1. Scale-down and Scale-out
2. Heterogeneous Integration, including Chiplets
3. End-to-End Advanced Packaging Flows
4. Prototypes for Demonstrating Functionality
5. Aligned R&D efforts for Implementable Advanced Packaging Flows

These program drivers are aligned with the industry roadmaps referenced above and the objectives outlined in the Vision for the National Advanced Packaging Manufacturing Program (https://www.nist.gov/system/files/documents/2023/11/19/NAPMP-Vision-Paper-20231120.pdf). The drivers are outlined below and are expected to be relevant to all R&D areas under this NOFO. Review, evaluation, and selection criteria for the NOFO are expected to include consideration of these drivers.

The first program driver is the ability in advanced packaging to **"scale-down and scale-out."** Scaling-down refers to shrinking the size of the features on the package and increasing interconnect densities. Scaling out refers to increasing the number of chips assembled on the substrate and overall functional density in both 2-dimensional (2D) and 3-dimensional (3D) architectures. Examples of scaling down goals and targets can be found in the MRHIEP roadmap (https://chips.ucla.edu/page/MRHIEP%20Project/MRHIEP%20Final%20Report). Applicants should consider in their planning activities interdisciplinary approaches that contribute to scaling-down and scaling-out in advanced packaging.

> *The primary driver for advanced 2D and 3D packaging technologies is the need for increased interconnect densities to support* [heterogeneous integration] *and deliver increasing bandwidth in a power efficient manner while enabling efficient power delivery*. IEEE Heterogeneous Integration Roadmap 2024 (https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2024-edition.html)

The second driver is advancing capabilities for **heterogeneous integration (HI), including chiplets**.[2] This driver focuses on the NAPMP objective for "creating an advanced packaging ecosystem based on heterogeneous chiplet technology to promote widespread and easy use of the technologies developed."[3] Applicants should incorporate considerations for heterogeneous integration and chiplets-based architectures in their research planning.

> *Heterogeneous Integration is essential to maintain the pace of progress with higher performance, lower latency, smaller size, lighter weight, lower power requirement per function, and lower cost.* IEEE Heterogeneous Integration Roadmap 2021 (https://eps.ieee.org/images/files/HIR_2021/ch01_overview.pdf)

> [T]*he exponential growth in package pin counts and I/O power consumption, domain-specific architectures, technical and business models of* [intellectual property] *reuse, and mixed technology node chiplets will drive advances in HI and advanced packaging*. SRC MAPT Roadmap (https://srcmapt.org/wp-content/uploads/2024/03/SRC-MAPT-

[2] The term "chiplets" refers throughout to the design of small, functionally targeted semiconductor chips that, when assembled at tight pitch and placement, result in a highly functional subsystem. Examples of chiplets in an ecosystem include common functions such as CPU, input/output devices, memory, domain-specific accelerators, etc.
[3] The Vision for the National Advanced Packaging Manufacturing Program (NAPMP Vision Paper, https://www.nist.gov/document/vision-national-advanced-packaging-manufacturing-program), Nov. 2023

Roadmap-2023-v4.pdf)

The third program driver is enabling **end-to-end advanced packaging flows** suitable for adoption by industry. This driver addresses the NAPMP objective to "develop packaging platforms capable of both high-volume and customized manufacturing."[4] To address this driver, applicants should plan for implementing their research outputs in a full packaging flow.

The CHIPS Research and Development Office has designed the NAPMP to include an Advanced Packaging Piloting Facility ([N]*APPF) where successful development efforts will be transitioned and validated for scaled transition to U.S. manufacturing*. NAPMP Vision Paper (https://www.nist.gov/document/vision-national-advanced-packaging-manufacturing-program)

The fourth driver is **demonstrating functionality in prototypes** to provide evidence for new capabilities, increased efficiencies, lowered production costs, reduced environmental impact, or other benefits resulting from research advances. This driver addresses the NAPMP objective to "enable successful advanced packaging development efforts to be validated and transitioned at scale to U.S. manufacturing."[5] NAPMP expects to support projects to design prototypes in application areas such as high-performance computing and artificial intelligence and low-power systems under the NOFO.

The final driver is **aligning R&D** efforts so that R&D results are not isolated or incompatible, but instead collectively contribute to implementable advanced packaging flows. Successful applicants should expect to participate in coordination and information-

[4] Ibid.
[5] Ibid.

sharing across projects in all R&D areas. The NOFO is expected to include provisions for coordination and cooperation activities connecting all of the R&D projects.

Advanced Packaging Research and Development NOFO Objectives: Consistent with the research incentives areas identified in the NAPMP Vision Paper (https://www.nist.gov/document/vision-national-advanced-packaging-manufacturing-program), the NOFO is expected to focus on proposals in one or more of five R&D areas with the potential to strategically enhance domestic advanced packaging capabilities through innovation in:

1. Equipment, Tools, Processes, and Process Integration;
2. Power Delivery and Thermal Management;
3. Connector Technology, Including Photonics and Radio Frequency (RF);
4. Chiplets Ecosystem; and/or
5. Co-design/Electronic Design Automation (EDA).

Within these areas, CHIPS R&D intends to fund R&D activities that establish and promote relevant domestic capability and capacity, with the following objectives:

1. Accelerate domestic R&D and innovation in advanced packaging;
2. Transition advanced packaging innovation into U.S. manufacturing, such that these technologies are available to U.S. manufacturers and customers, including to significantly benefit U.S. economic and national security;
3. Support the establishment of a robust, sustainable, domestic capacity for advanced

packaging R&D, prototyping, commercialization, and manufacturing; and

4. Promote a pipeline of skilled and diverse workers for a sustainable domestic advanced packaging industry.

To ensure that funded R&D meets the above objectives, CHIPS R&D expects to specify technical targets for applicants to achieve within each of the five R&D areas described below. Individual proposals may address one or more of the R&D areas. Note that these R&D areas are aligned with the relevant research investment areas set out in the NAPMP Vision Paper (https://www.nist.gov/document/vision-national-advanced-packaging-manufacturing-program).

R&D Area 1: Equipment, tools, processes, and process integration: This R&D area is expected to include developing: (1) end-to-end packaging flows that enable a chiplet-based advanced packaging architecture suitable for commercial adoption; (2) advanced, flexible, extensible process technologies required to produce a packaged subassembly; and (3) new packaging equipment needed to run the packaging processes and to handle the required substrates, wafers and dies, all at the scaled down dimensions set out in the previous NAPMP Materials and Substrates NOFO, located at https://www.nist.gov/document/nofo-national-advanced-packaging-manufacturing-program-napmp-materials-substrates (see Table 2, page 14) and designed for use at commercial scale.

R&D in this area is expected to focus on five packaging process clusters, with a cluster defined as a sequence of steps that enable a key part of the packaging flow. The five process clusters expected to be relevant to this NOFO are:

1. Chiplet Singulation: Producing singulated chiplets from incoming wafers that are fully patterned with dies, for subsequent assembly.

2. Chiplet to Substrate Bonding: Positioning and attaching chiplets with ultra-fine-pitch bonding pads to substrates, in dense arrays with close chiplet-to-chiplet spacing. This includes bonding techniques designed to improve bond quality, positioning precision, process flexibility, process efficiency, and overall cluster efficiency. Examples include thermal compression bonding, fusion bonding, hybrid bonding, multi-step sequences, and other methods.

3. Chiplet Reconstitution: Placing and attaching singulated chiplets on a carrier. Reconstitution should be compatible with the scaled down dimensions set out in the previous NAPMP Materials and Substrates NOFO, located at https://www.nist.gov/document/nofo-national-advanced-packaging-manufacturing-program-napmp-materials-substrates (see Table 2, page 14).

4. 3-Dimensional Integration (3DI): Forming heterogeneous chiplet stacks with ultra-fine bonding pad pitches.

5. Finishing: Incorporating advanced power delivery, passivation, thermal management, and connectors, including photonics, into the packaged device.

NAPMP expects that proposals within this R&D area may address one or more of these clusters, including the relevant equipment, tools, and processes. The NOFO is expected to call for comprehensive R&D approaches that encompass interactions between steps and step sequencing within each cluster. The NOFO is also expected to include proposals addressing cluster assembly, i.e., sequencing of multiple clusters for end-to-end

packaging process flows suitable for use in advanced packaging of prototypes. Note that the specific processes and sequence of steps within each cluster are expected to be driven by the requirements of the prototype to be packaged.

R&D Area 2: Power delivery and thermal management: The expected focus of this R&D area is to address the challenges introduced by advanced packaging in terms of power delivery, power efficiency, and thermal management.

Examples of the associated research challenges expected to be considered in this R&D area include the following.

1. New thermal solutions – for implementation with advanced substrates, 3D heterogeneous integration (3DHI), and other design aspects – to reduce hotspots, maintain thermal targets, and enable reliability in multilayer stacks without constraining connectivity.

2. Innovative approaches for delivering power at high density with efficient voltage regulators and dynamic power management schemes for 3DHI devices, including modular designs and devices for use with a variety of chiplets.

3. Validated, higher fidelity models and accelerated learning using artificial intelligence and machine learning (AI/ML) to accurately predict power and thermal distribution across chiplet stacks and enable advanced system design and evaluation.

4. Integrated power and thermal management to reach efficiency and power density goals with modular designs for use with fine-pitch, bonded stacks of chiplets.

It is expected that proposals within this area may consider related research challenges

within other R&D areas, such as Co-design/Electronic Design Automation and Chiplets Ecosystem. Expected to be in scope are vertical heat extraction, local heat spreading, advanced methods for active and passive cooling of 3DHI devices to reliably operate at higher power density, wide bandgap chiplets for 3DHI, and advanced materials and architectures to achieve specific thermal and power goals such as low-resistance thermal interfaces. Expected to be out of scope are discrete packaged wide bandgap devices and conventional cooling approaches.

R&D Area 3: Connector Technology, Including Photonics and RF: The expected goal for this R&D area is innovation for high data-rate, low latency, small footprint, error-free, and energy-efficient connections between packaged sub-assemblies. It is expected that the intended sub-assemblies will be chiplet populated substrates where the substrates have the characteristics set out in Section 1.5 of the NAPMP Materials and Substrates NOFO, located at https://www.nist.gov/document/nofo-national-advanced-packaging-manufacturing-program-napmp-materials-substrates.

NAPMP expects that, depending on the distance between the packaged assemblies, the mode of data transfer may be via flexible wire, such as serializer/deserializer (SerDes) with or without repeaters; wireless, including RF; or low-loss photonics via optical fiber arrays. It is also expected that projects may address one or more of these modes of data transfer. RF transceivers and optical engines are expected to be provided using chiplet-based technology or embedded directly into the advanced substrates. Potential applicants are encouraged to focus on new scale-down and scale-out technologies for connections that enable secure communications and provide for mechanical, electrical, and thermal reliability.

It is expected that chiplet sub-assemblies to substrate connectors will be in scope for this R&D area. Expected to be out of scope are traditional ball grid array (BGA) or land grid array (LGA) connectors and conventional wire bonding.

R&D Area 4: Chiplets Ecosystem: This R&D area is expected to focus on developing a comprehensive set of novel technologies for chiplet ecosystems that leverage advanced packaging to enable application-specific integrated packages that go beyond the capabilities of conventional monolithic ASICs (application-specific integrated circuits). It is expected that chiplets in an application-specific integrated package will need to communicate and operate together. For this NOI, the term "chiplet ecosystem" is used to refer to: (1) a set of chiplets that can be used to form application-specific integrated packages and (2) the set of requirements new chiplets have to follow to be added to the ecosystem. Consistent with this definition, chiplets in an ecosystem can be combined in multiple ways to form diverse products.

It is expected that successful proposals should develop a chiplet ecosystem that meets as many of the following goals as is possible.

- The ecosystem provides for increasing performance over time by continually leveraging the tighter bond pitch and more intimate interaction that will be made possible by fine-pitch packaging, starting at a bond pitch of ~10 microns.
- The ecosystem enables designs that consist of a discrete number of chiplets, include support for 3D stacks, and are based on a chiplet integration layer specification that is not adequately addressed in current open systems and reduces the cost of adding new chiplets.

- System performance in the ecosystem can be increased by increasing the number of chiplets. For example, a high-performance chiplet ecosystem can be scaled up by increasing the number of chiplets rather than by developing new larger chiplets. This scaling up strategy enables going from a multi-chiplet device design comparable to a monolithic ASIC to a "rack 'n' pack" device (i.e., an application-specific integrated package comparable to a wafer-scale processor).
- The ecosystem enables designers to address all supported design requirements with provisions to accommodate yield loss in packaging assembly and optimize power and energy to meet performance requirements with the available system resources.

It is expected that proposals should be centered around exemplar applications in the areas of high-performance computing/AI, and low-power applications. It is expected that the NOFO will require applicants to plan for making chiplets resulting from funded project research available for purchase at cost in prototype quantities and in wafer form for research use at the National Advanced Packaging Piloting Facility (NAPPF).

It is expected that, in addition to ecosystem development, chiplets for packaging process development that support any of the other five R&D areas will be in scope. Memory is also expected to be in scope but must be at fine bond pitch consistent with NAPMP scale-down goals (see Section 1.5 of the NAPMP Materials and Substrates NOFO, located at https://www.nist.gov/document/nofo-national-advanced-packaging-manufacturing-program-napmp-materials-substrates).

Expected to be out of scope for this R&D area are: designs that are extensions of conventional approaches based on commodity packaging and that do not directly

leverage advanced packaging in their architecture; designs tightly coupled to the choice of an SoC-bus (system-on-chip bus) or other high-level protocols; or standalone chiplet designs for any function not coupled to a chiplet ecosystem. Also expected to be out of scope are ecosystem design proposals that: focus on unmodified reuse of existing chiplets; target the development of new chiplets to integrate existing chiplets into new architectures; do not leverage advanced packaging; or do not provide for the delivery of chiplets and application-specific integrated packages.

R&D Area 5: Co-design/Electronic Design Automation: The expected focus of this R&D area is co-design with automated tools of multi-chiplet subsystems for advanced packaging in scaled-down and scaled-out designs (see NAPMP Materials and Substrates NOFO Table 2, page 14 for insights into relevant dimensions and capabilities, located at https://www.nist.gov/document/nofo-national-advanced-packaging-manufacturing-program-napmp-materials-substrates). This includes innovations in EDA interoperability; EDA-enabled incorporation and co-optimization of chiplets of different sizes in a large platform design including logical electrical, photonic, thermal, and mechanical models; and advances in seamless integration of the chip to package. Additional areas could include the use of artificial intelligence/machine learning (AI/ML) in package design and design approaches for test, repair, security, and reliability including graceful failure through designs that enable continued operation at a reduced performance level after failure of one or more components. Applicants should address comprehensive co-design capabilities that include a detailed understanding of the substrate and processes used for assembly, including power and thermal management, and connector solutions.

It is expected that EDA that addresses purely monolithic applications without

consideration of chiplets, heterogeneity and the multi-scale, multi-physics packaging environment will be out of scope for this R&D area.

Prototype Development: In addition to the five R&D areas listed above, the NOFO is expected to include opportunities for prototype development in exemplar application areas such as high-performance computing and artificial intelligence, and low-power systems applications. The goal in prototype development is to establish new advanced packaging flows that leverage the technologies being developed across the five R&D areas. Functionality will be a requirement, and prototypes should be designed to provide a means for assessing relevant packaging characteristics such as yield and preliminary reliability.

Commercial Viability and Domestic Production: In accordance with 15 U.S.C. § 4656(g), the NOFO will include requirements for a commercial viability and domestic production plan (https://www.nist.gov/system/files/documents/2024/03/12/CHIPS%20R%26D%20Commercial%20Viability%20and%20Domestic%20Production%20CVDP%20Plan%20Guidebook.pdf), describing activities to be funded as part of the proposed project and, potentially, additional commercialization activities beyond the period of performance. The CVDP plan must include a realistic business model for the funded innovations, include a technology transition plan, and describe pathways to benefitting national and economic security, such as through the domestic availability of the technology and successful adoption by commercial or defense partners.

Education and Workforce Development: The NOFO is expected to include requirements for an education and workforce development plan,

(https://www.nist.gov/system/files/documents/2024/06/17/CHIPS%20RD%20Education%20and%20Workforce%20Development%20Plan%20Guidebook-508C.pdf), that leverages capabilities supported through the proposed project to address domestic advanced packaging workforce needs, including educational opportunities arising from engaging students in research. NAPMP encourages applicants to, in providing an Education and Workforce Development (EWD) plan, describe any efforts to attract and retain a diverse student and trainee population and to demonstrate that the EWD efforts are worker centered, industry-aligned, and promote good jobs with working conditions consistent with the Good Jobs Principles (https://www.dol.gov/general/good-jobs/principles), published by the Department and the U.S. Department of Labor.

National Advanced Packaging Piloting Facility: The CHIPS Research and Development Office has designed the NAPMP to include a NAPPF, where successful research and development efforts will be implemented and validated for suitability for volume-scaled manufacturing. The specific tools and capabilities of the NAPPF will be aligned with the "scale down and scale out" strategy described in the NAPMP Vision Paper (https://www.nist.gov/document/vision-national-advanced-packaging-manufacturing-program). Additional details regarding the NAPPF will be posted to the CHIPS for America web site (https://www.nist.gov/chips/chips-rd-funding-opportunities) as they are announced.

Where applicable, proposers responding to the NOFO are expected to be asked to implement their research outputs in the NAPPF once established. NAPMP program managers will work with applicants in the post-award phase to facilitate work with the NAPPF.

Technical Targets: Each R&D area is expected to include technical targets selected by CHIPS R&D for their potential to guide innovation toward the scale-down and scale-out goals of the program. Applicants should review the previous NAPMP Materials and Substrates NOFO, located at https://www.nist.gov/document/nofo-national-advanced-packaging-manufacturing-program-napmp-materials-substrates, which provides detailed insights into the NAPMP "scale down and scale out" targets. Sections 1.4.3, Technical Areas, and 1.5, Project-level Technical Targets, provide detailed information about substrate materials and technical targets.

Eligible Use of Funds. Funded activities are expected to include, but not necessarily be limited to, basic and applied research, development of relevant advanced packaging manufacturing-scale equipment and processes, the design and demonstration of prototypes, commercial viability and domestic manufacturing preparation, workforce education and training, and pilot-level fabrication.

Eligibility. CHIPS R&D expects eligible lead applicants and subrecipients will include for-profit organizations; non-profit organizations; accredited institutions of higher education, including community and technical colleges and minority serving institutions; and state, local, territorial, and Tribal governments. Entities that operate Federally Funded Research and Development Centers (FFRDCs) may be eligible to receive this funding as subrecipients to an eligible applicant to the extent allowed by law, based on the unique and specific needs of the project. It is expected that the NOFO will require that applicants must be domestic entities, meaning entities incorporated in the United States (including U.S. territories) with their principal place of business in the United States, including U.S. territories, and will potentially be subject to other eligibility

requirements.

Subrecipients are those who are designated by the lead applicant as subrecipients, included in the proposed budget, and whose activities are a continuing part of ongoing project activities with their work tailored to specific project goals, such as research and development activities, education and workforce activities, and other integral project efforts. Vendors selling goods and services to award recipients in the ordinary course of business are not considered subrecipients.

It is expected that foreign organizations may be permitted to participate as members of a project team, as sub-subrecipients or contractors, subject to CHIPS R&D approval based on a written justification that the foreign partner's involvement is essential to advancing program objectives, among other considerations.

R&D Collaboration: CHIPS R&D expects that applicants assembling teams (i.e., with a lead applicant from industry or academia and one or more subrecipients) may be best suited to collectively provide the full range of expertise and capabilities needed to achieve the program objectives and to successfully strengthen U.S. advanced packaging innovation. Equally important, effective partnerships can promote inventiveness, clarify future demand, improve transparency and security, solidify business and domestic manufacturing plans (including plans for technology adoption by defense and commercial partners), help educate the future workforce, mitigate the risk of future chip shortages or oversupply, and support a more productive, efficient, and self-sustaining semiconductor ecosystem.

CHIPS R&D therefore strongly encourages applications from teams that demonstrate collaboration across the innovation, manufacturing, supply chain, and customer

landscape, as well as across the industry, non-profit, and academic sectors. Applications that do not include teams may be required to include a justification for the proposed single-entity approach.

Application Process and Award Information. The envisioned application process consists of a mandatory concept paper and a required full application. CHIPS R&D anticipates a due date for concept papers of approximately 60 days after the date of NOFO publication. Full applications would only be accepted from applicants invited to apply after the concept paper stage. Submissions from entities other than those specifically invited to submit a full application would not be reviewed or considered in any way.

CHIPS R&D expects to host a webinar series after this NOI is released to provide additional opportunities to learn about the Notice of Intent. Details regarding the time and date of webinar events will be posted on the CHIPS R&D website at https://www.nist.gov/chips/chips-rd-funding-opportunities. Participation in webinars is not a prerequisite for submitting a concept paper or application.

Additionally, to provide the public with an opportunity to learn more about the NOFO, CHIPS R&D expects to host a Proposers Day after the NOFO is released to familiarize potential applicants with the NOFO objectives and program structure. CHIPS R&D will announce details regarding the date and location of Proposers Day via the CHIPS R&D website at https://www.nist.gov/chips/chips-rd-funding-opportunities. Attendance is not a prerequisite for submitting a concept paper or application.

Competition Information. Once the open competition has been announced, further information may be found at https://www.nist.gov/chips/chips-rd-funding-opportunities.

System for Award Management. In anticipation of the NOFO, CHIPS R&D encourages potential applicants to complete the following steps, which are required to submit concept papers and full applications for Federal assistance:

- Register with the System for Award Management (SAM) at https://www.sam.gov. CHIPS R&D strongly encourages applicants to register for SAM.gov as early as possible. While this process ordinarily takes between three days and two weeks, in some circumstances it can take six or more weeks to complete due to information verification requirements. Recipients will be required to maintain an active registration in SAM and re-validate registration annually.
- Register for a Grants.gov (http://www.grants.gov) account. It is advisable also to go to "manage subscriptions" on Grants.gov and sign up to receive automatic updates when amendments to a funding opportunity are posted.

Disclaimer. This NOI does not constitute a solicitation. No applications may be submitted in response to this NOI. Any inconsistency between information within this Notice and the eventual NOFO announcing CHIPS R&D/NAPMP Advanced Packaging awards competition shall be resolved in favor of the NOFO.

Authority. DOC CHIPS activities are authorized by Title XCIX—Creating Helpful Incentives to Produce Semiconductors for America of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Pub. L. 116–283, often referred to as the CHIPS Act).

Dated:

Alicia Chambers,
NIST Executive Secretariat.