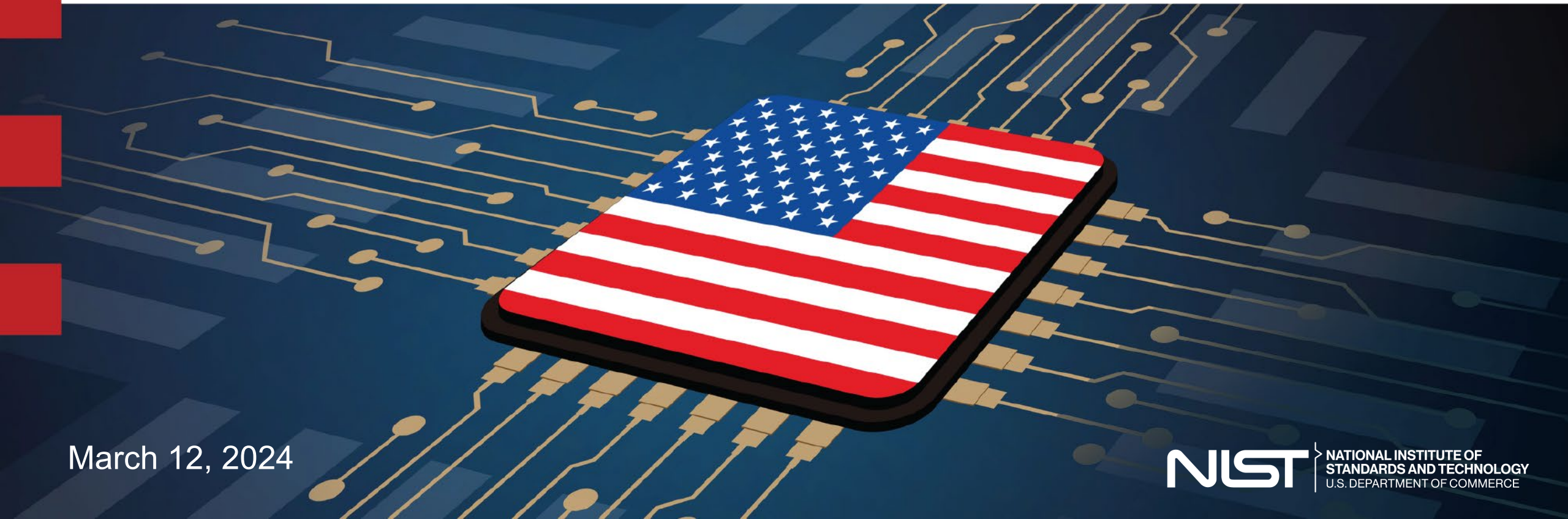
CHIPS for AMERICA

Materials and Substrates Proposer's Day



March 12, 2024

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Welcome

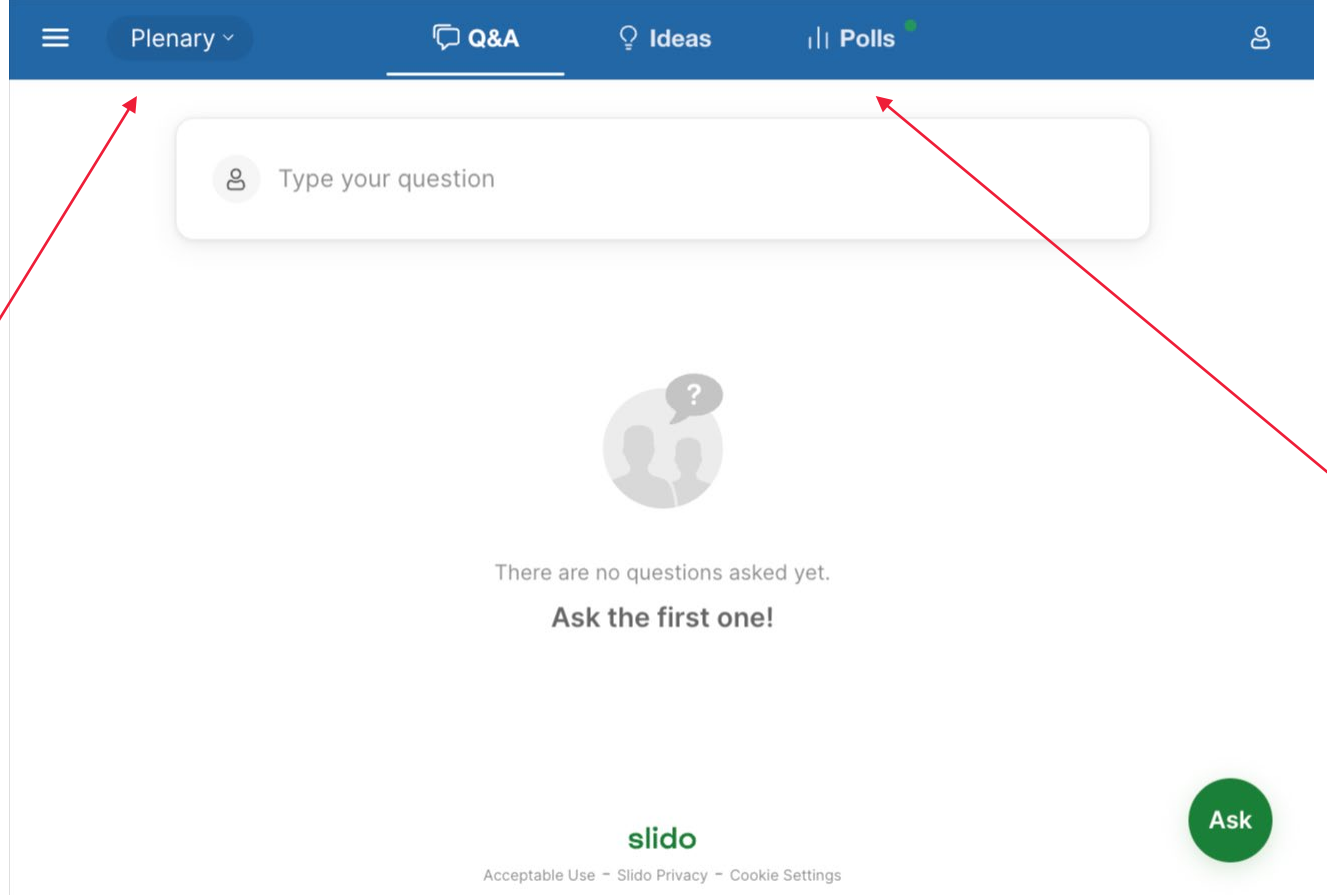
HOUSEKEEPING ITEMS

- Lots of Information to share!
- Did you get a sticker/lanyard when you picked up your credentials? If not, please do at break.
- Visit CHIPS.gov
  - Get the Notice of Funding Opportunity
  - Access additional resources for applicants and stakeholders: Frequently Asked Questions: National Advanced Packaging Manufacturing Program (NAPMP) Funding Opportunity | NIST is a living document

CHIPS for America QR Code: **CHIPS NAPMP Materials and Substrates NOFO** (full text)

Slido

You can change rooms any time using this dropdown menu



Toggle between functions, as needed

Scan the QR code or go to slido.com and enter code NAPMP

Proposer's Day Expectations

Agenda

- NAPMP Program Overview
- Overview of Materials and Substrates NOFO
- CHIPS R&D Policy Overview
- Grants Management Division
- Answers to Questions
- Breakouts – Networking and Team Building
- Next Steps for NAPMP

By the end, attendees should better understand

- Outcomes of the Materials and Substrates Program
- Requirements and Stages/Phases of the Materials and Substrates Program
- How to apply to Materials and Substrates NOFO
- The importance of teamwork!

Morning Agenda (AM ET)

Time	Session	Speaker
8:30AM – 8:40AM	Welcome	Under Secretary **Laurie Locascio**
8:40AM – 8:50AM	Expectations for Day	**Dan Berger** Associate Director, CHIPS NAPMP
8:50AM – 9:20AM	NAPMP Team Introductions NAPMP Program Overview	**Subramanian Iyer** Director, CHIPS NAPMP
9:20AM – 10:00AM	Materials and Substrates NOFO Overview	**Aaron Forster** Program Manager, Materials and Substrates
10:00AM – 10:45AM	CHIPS R&D Office Policy Overview	**Richard-Duane Chambers** Director of Policy and Integration **Greg Strouse** NIST Safeguarding Science Research Security Director
10:45AM – 11:00AM	Ready, Set, Submit! Application, Preparation, and Submission	**Michael Teske** Grants Management Officer **Blase Etzel** Other Transaction Agreement Officer
11:00AM – 11:30AM	Networking/Break	
11:30AM – 12:00PM	Question and Answer Panel	**Moderator:** George Orji **Panel:** Dan Berger, Aaron Forster, Richard-Duane Chambers, Greg Strouse

Afternoon Agenda (PM ET)

Time	Session	Speaker
12:00PM – 1:30PM	Lunch (on own)	
1:30PM – 1:45PM	Afternoon Instructions Importance of Teaming	**Dan Berger** Associate Director, CHIPS NAPMP
1:45PM – 3:00PM	Breakout Sessions 1	*Technical Area Focus*
3:00PM – 3:30PM	Networking/Break	
3:30PM – 4:50PM	Breakout Sessions 2	*Teaming Focus*
4:50PM – 5:00PM	Break/Return to Plaza Ballroom	
5:00PM – 5:30PM	What is next for NAPMP	**Subramanian Iyer** Director, CHIPS NAPMP
5:30PM	Adjourn	

NAPMP Leadership

Subramanian Iyer
Director
NAPMP

Dan Berger
Associate Director
NAPMP

George Orji
Deputy Director
NAPMP

NAPMP Program Managers

Aaron Forster
Program Manager
Materials and Substrates

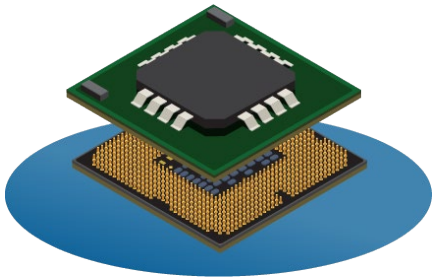
David LaVan
Program Manager
Thermal and Power Management

Emily Kinser
Program Manager
Photonics and Connectors

Bapiraju Vinnakota
Program Manager
Photonics and Connectors

CHIPS R&D Programs

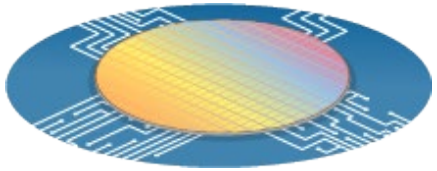
CHIPS Metrology Program



CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast

Natcast is an independent nonprofit organization and operator of the NSTC consortium



CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

Manufacturing USA

CHIPS Manufacturing USA Program

Workforce Initiatives

Establishing Advanced Packaging in the U.S.

Packaging Roadmaps

- NIST-sponsored roadmaps: MRHIEP, MAESTRO and MAPT
- Other roadmaps: HIR and IRDS

Technology Investment Areas

- All aspects of technologies required to develop a leading-edge on-shore advanced packaging manufacturing capability

The National Advanced Packaging Piloting Facility (NAPPF)

- Key to facilitating high-volume manufacturing
- Piloting and prototyping functions

The Chiplet and Design Ecosystem

- Chiplet discovery, disaggregation and reaggregation methodologies, protocols, standards, fabrication and warehousing design for test, repair and reliability, and holistic design tools and methodologies

Design in the U.S., build in the U.S., and sell worldwide

- Successful development efforts will be transitioned and validated for scaled transition to U.S. manufacturing

NAPMP Priority Research Investment Areas

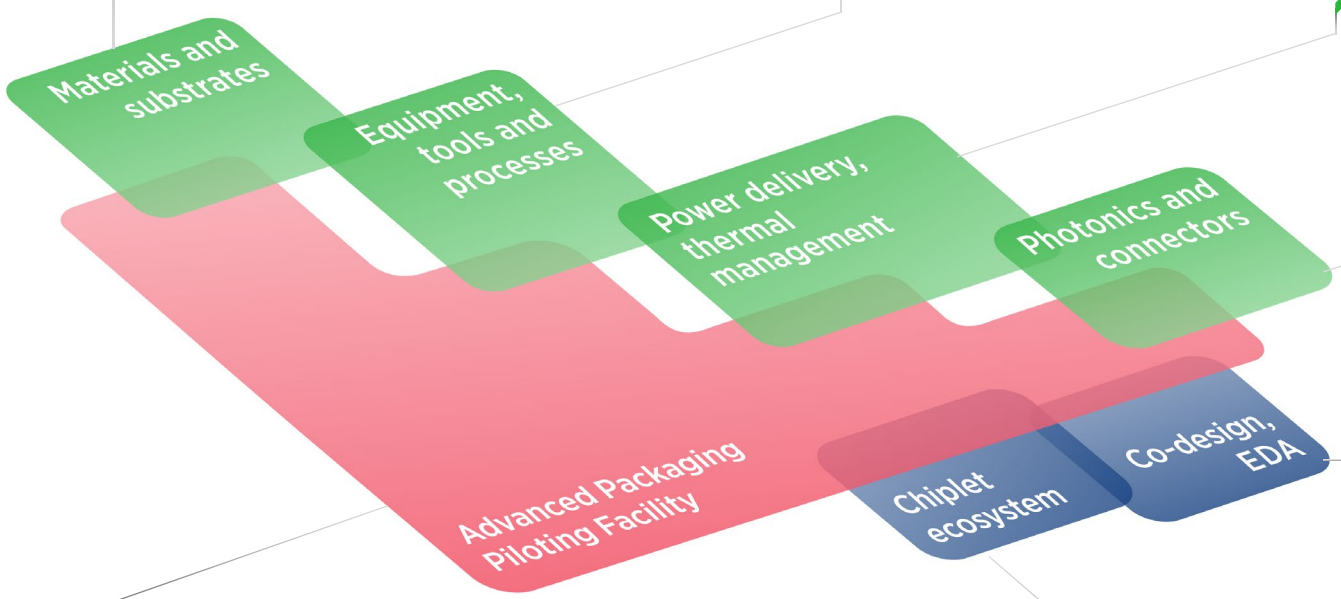
Materials and substrates are the platform for heterogeneous integration of dielets

Equipment, tools, and processes are needed to pattern substrates and assemble dielets and passivate assemblies

Thermal management and efficient power delivery are critical needs

Photonics and connectors allow the assembly to interact with the outside world

Automated design for test, repair, security, and reliability; substrate and process dependent



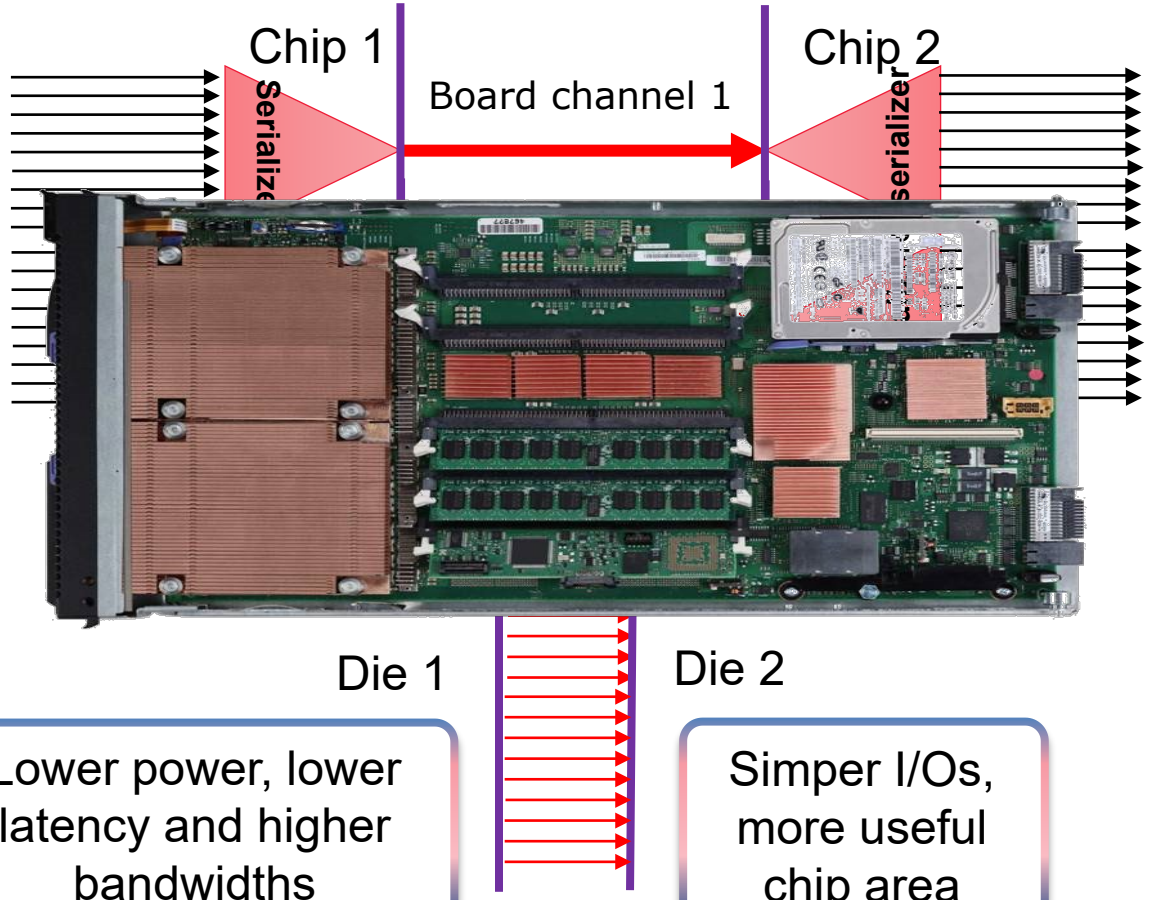
The NAPPF provides a test bed for integration of the different investment areas and also functions as a piloting and prototyping facility

The chiplet ecosystem is crucial for any implementation of advanced packaging

NAPPF: National Advanced Packaging Piloting Facility

Advanced packaging is all about scale

The difference now is scale:



Lower power, lower latency and higher bandwidths

Simper I/Os, more useful chip area

- More Channels on the package
  - Finer ”bump/pillar” pitch
  - Approach on-chip via pitches (<1 μm)
- Finer Trace Pitch
  - Approach on-chip wiring pitches
- Shorter inter die distance
  - ~ μm

Scale Down

- Significantly more intimately connected Silicon

Scale Out

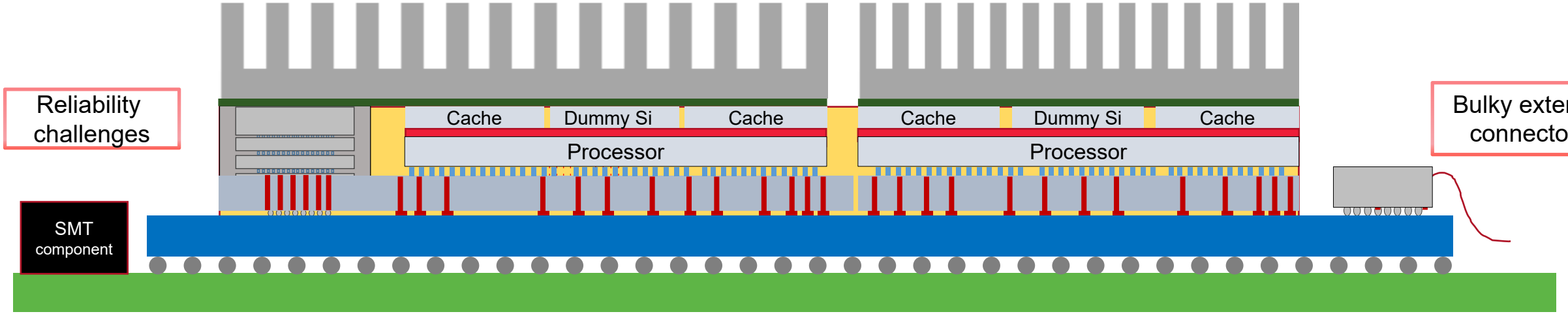
We do it today — but with complexity and added hierarchy

Materials with large CTE mismatches and high stresses

Known good die, testing and rework challenges

Thermal and hot spot challenges
Power delivery challenges

Reliability challenges



Bulky external connectors

Increasingly complex hierarchies (e.g.: interposers) and assembly techniques

Organic substrates and laminates with large warpage and coarse pitches with embedded and SMT passives and expensive interposers

Simplify packaging and make it cost effective to manufacture in the US

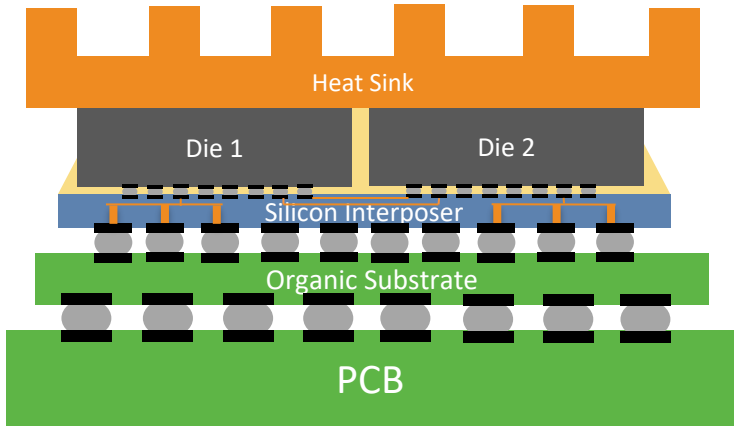
CTE: coefficient of thermal expansion; SMT: surface mount technology

Substrates

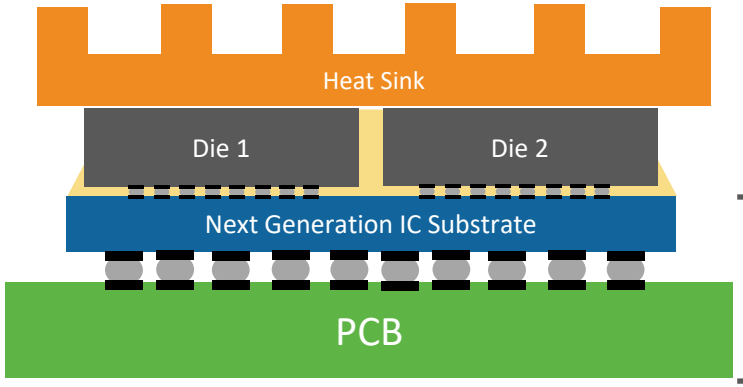
- Substrates are the platform on which chips are integrated
- Organic substrates (including Laminates and PCBs) dominate
  - Off-shore manufacturing dominates this space, and this supply chain was and continues to be vulnerable today
  - This industry migrated offshore at a time when pitches were coarse and substrate sizes were small and the emphasis was on cost rather than function
  - However, in the last several years, these substrates have become more complex, and the process has become more sophisticated, but this know-how is now off-shore
- Packaging itself has evolved in the last several years beyond what these substrates can achieve and has led to the development of interposer technology as an additional level in the packaging hierarchy
  - But interposer technology has also shifted offshore leaving US system houses and chip manufacturers vulnerable
- Is there a way to rethink substrates and achieve a simpler packaging hierarchy and process?

Substrate evolution

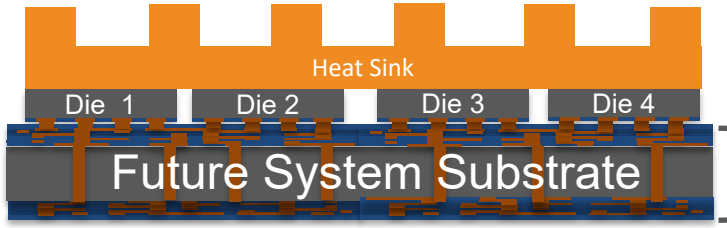
Towards a simpler hierarchy



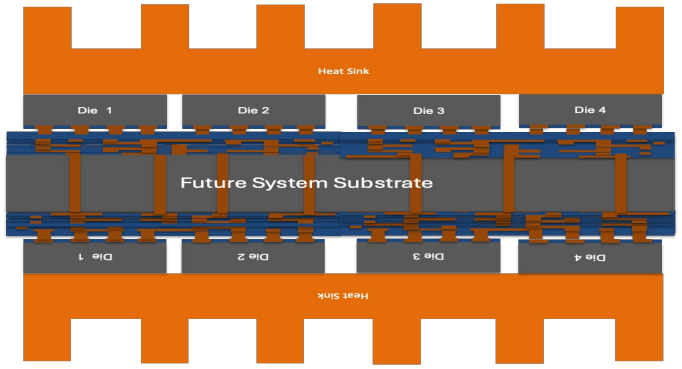
3 Level Package



2 Level Package



1 Level Package



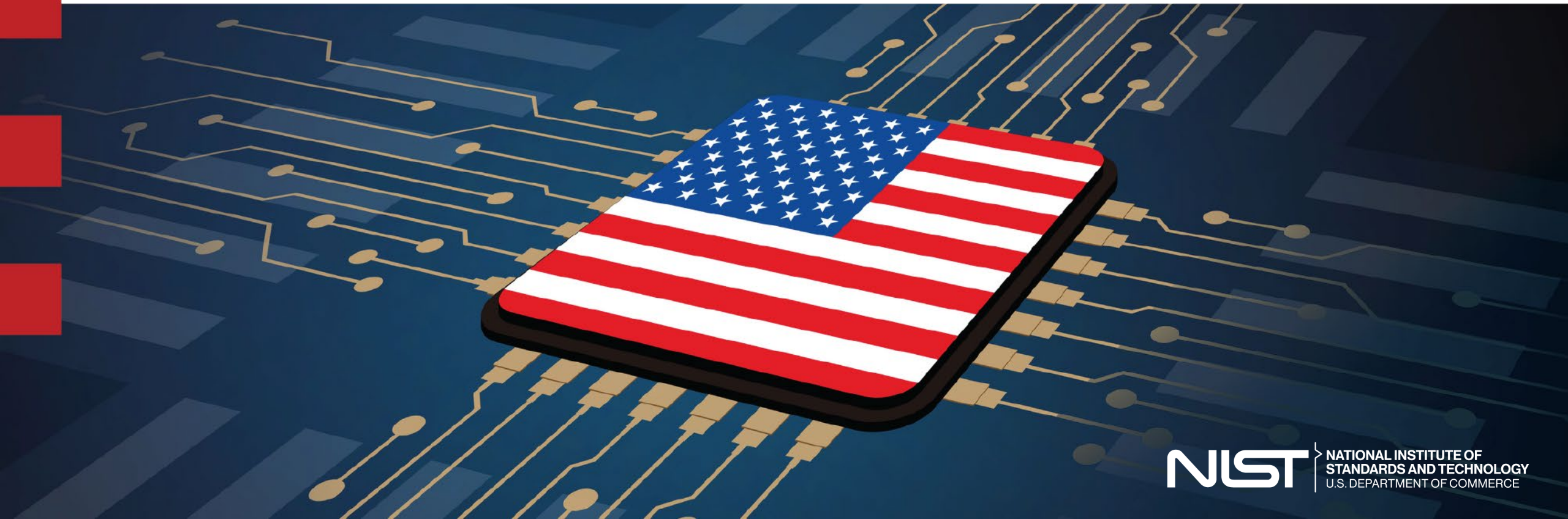
1 Level double sided Package

Disclaimer

- Statements and responses to questions about advanced microelectronics research and development programs in this webinar:
  - Are informational, pre-decisional, and preliminary in nature.
  - Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
  - Are subject in their entirety to any final action by NIST or the Department of Commerce.
- Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or Notices of Funding Opportunity, which are controlling.

CHIPS for America
The Materials and Substrates
Notice of Funding Opportunity

CHIPS for AMERICA



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Substrates and Substrate Materials Program

Vision & Mission

- The Program vision is to drive **U.S. leadership** in advanced substrates manufacturing for advanced packaging in the United States
- The program mission is to develop **critical and relevant innovations** for advanced substrates to enable **cutting edge advanced packaging applications** and **scale up** substrate innovations **into U.S. manufacturing**

Objectives

1. Accelerate domestic R&D and innovation in advanced packaging materials and substrates;
2. Translate domestic materials and substrate innovation into U.S. manufacturing, such that these technologies are available to U.S. manufacturers and customers, including to significantly benefit U.S. economic and national security;
3. Support the establishment of a robust, sustainable, domestic capacity for advanced packaging materials and substrate R&D, prototyping, commercialization, and manufacturing; and
4. Promote a skilled and diverse pipeline of workers for a sustainable domestic substrate manufacturing sector.

Approach

1

Scale down: shrinking features on a package:

- ✓ Making the features on the package approach those at the top level on a monolithic CMOS chip
- ✓ Reducing the distance between dies that are assembled on a multi-chip package to approach the distance between IP blocks on a monolithic chip

2

Scale out: increasing the areal density of chips on a package

- ✓ Accommodate a larger number of closely packed heterogeneous die
- ✓ Address the power delivery, thermal dissipation and external connection challenges
- ✓ Develop standards and protocols to accommodate a large and diverse set of chips (chiplets)

3

R&D that leads to sustainable manufacturing at appropriate volume

- ✓ Translate domestic materials and substrate innovation into U.S. manufacturing
- ✓ Promote a skilled and diverse pipeline of workers for a sustainable domestic substrate manufacturing sector

Program Scope

3 Technical Areas

- TA1: Organic substrates, including fan-out.
- TA2: Glass-based substrates
- TA3: Semiconductor-based substrates

Flexible and substrates for biomedical applications

Applicants can propose to one or more technical areas

Activities

TECHNICAL

- Basic and applied R&D
- Substrate development
- Demonstration device development

NON-TECHNICAL

- Commercial viability
- Workforce development
- Domestic Production

Awards

- $300 Million total over 5 years
- Individual awards up to $100 Million

Co-investment encouraged.

Substrates and Substrate Materials

What is within program scope?

- Substrate wiring
- Via pitches
- Through substrate vias
- Number of levels on both sides of the substrate
- One or more passive or active components embedded in the substrate for enhanced functionality

What is NOT within program scope?

- Traditional boards
- Interposers
- Small area substrates

CHIPS R&D Specified Technical Targets

Technical Target Category	CHIPS R&D-specified Technical Targets		
	TA 1 (Organic)	**TA 2 (Glass)**	**TA3 (Semiconductor-Based)**
1. Minimum Line Width, Spacing, and Pitch	1 μm line width, 1 μm line spacing, 2 μm pitch	0.5 μm line width, 0.5 μm line spacing, 1 μm pitch	0.25 μm line width, 0.25 μm line spacing, 0.5 μm pitch
2. Coplanarity at Die Attach (Bonding Area)	Below 0.5 μm over dielet area, where dielet area can vary between 1 mm x 1 mm to 10 mm x 10 mm	Below 0.5 μm over dielet area, where dielet area can vary between 1 mm x 1 mm to 10 mm x 10 mm	Below 0.5 μm over dielet area, where dielet area can vary between 1 mm x 1 mm to 10 mm x 10 mm
3. Interlevel via diameter	1 μm	0.5 μm	0.25 μm
4. Through substrate via diameter	Less than 100 μm	Less than 100 μm	Less than 100 μm
5. Max wire thickness	Equal to wiring pitch	Equal to wiring pitch	Equal to wiring pitch
6. Max number of Layers (hierarchical)	10+10 (side 1 + side 2), or 15 single sided for Fan Out wafer level packaging	10+10 (side 1 + side 2)	15+15 (side 1 + side 2)
7. Composite coefficient of thermal expansion (CTE)	6 to 10 parts per million (ppm) -77 °C to 350 °C	6 to 10 parts per million (ppm) -77 °C to 350 °C	6 to 10 parts per million (ppm) -77 °C to 350 °C
8. Max substrate size	500 mm x 500 mm	500 mm x 500 mm or 300 mm diameter	210 mm x 210 mm or 300 mm diameter
9. Max thickness	3 mm	2 mm	1 mm
10. Warpage	Should be consistent with lithographic requirements for specified minimum line width and spacing		
11. Applicant-Defined Target(s)	If consistent with the objectives of this NOFO, the Applicant may propose one or more additional technical targets, such as targets addressing environmental sustainability.		

- *Technical targets selected for potential to **improve performance, manufacturability, sustainability, and sustainable production** of advanced substrates*
- *Applicants may propose additional Project-Level Targets*
- *Applicants must describe, whether they expect to:*
  - ***(1) exceed the target;***
  - ***(2) meet the target;***
  - ***(3) partially meet the target; or***
  - ***(4) not need to meet the target***
- *Applicant should **carefully explain how proposed approach represents a significant technical advance relevant to the global state of the art, accomplishes CHIPS R&D mission and goals, and specific objectives of this NOFO.***

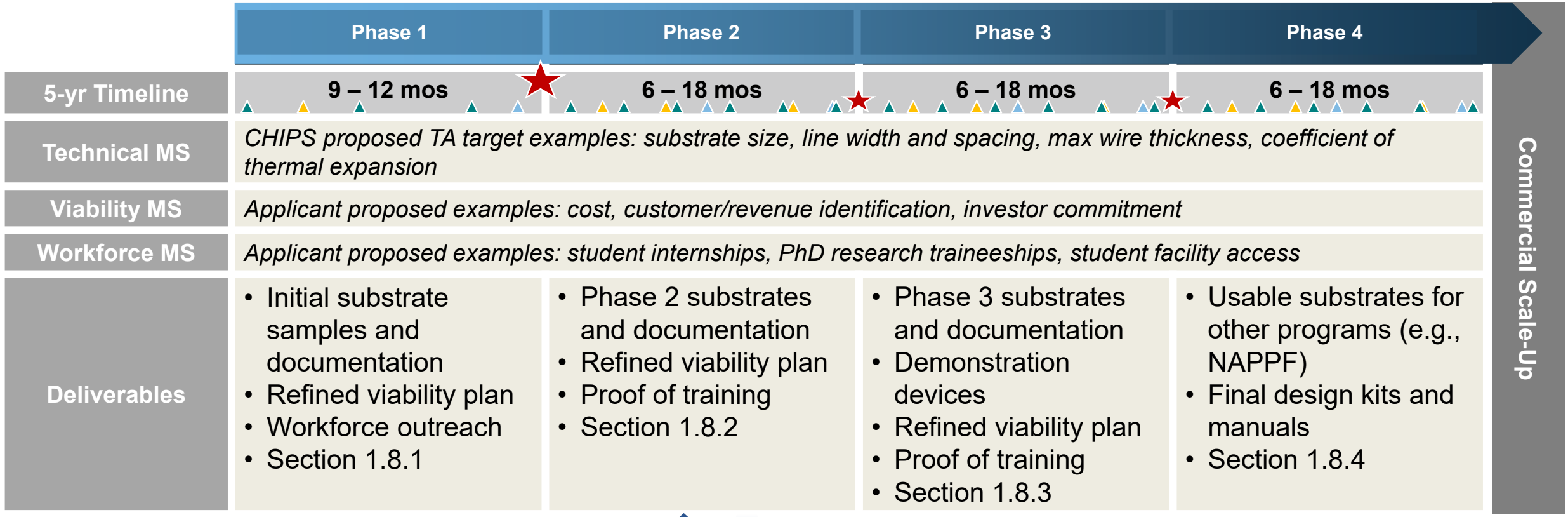
Embedded Substrate Features:
Active and Passive Devices

- *Applicants **may include one or more passive or active components embedded** in the substrate for enhanced functionality*
- *Applicants **are strongly encouraged to consider including these features that advance/enhance U.S. leadership in substrate offerings***

- Advanced voltage regulation structures
- Advanced RF Antenna structures
- Advanced substrate thermal solutions
- Advanced high density decoupling capacitors
- Substrate inductor or resistor structures
- Cross substrate waveguides and/or TLV

- Substrate trackability/ traceability structures or substrate tags
- Substrate radiation shielding structures
- Substrate cavity, curvature, biocompatibility, or geometric flexibility provisions

Example of a Phased Program Approach



Phase specific targets

Inform

★Program Go/No-go decision

▲ Technical Milestones
▲ Commercial Viability Milestones
▲ Education/Workforce Milestones

Broader Impacts

Commitment and Support to future investment in R&D Programs

- During Phase 4, CHIPS R&D aims to provide substrates developed under this NOFO to research projects in other areas of packaging research that would benefit from access to advanced substrates.
- CHIPS R&D will favorably consider applications that demonstrate a commitment to participating in the NSTC, the NAPPF, the NIST Manufacturing USA Institute on Digital Twins; NIST Metrology; NSTC Workforce Center of Excellence; DoD ME Commons, NSF semiconductor education initiatives
- CHIPS R&D will favorably consider applications that identify metrics and milestones that demonstrate the capability of funded technologies to improve upon **environmental** outcomes of current methodologies and minimize the potential for adverse impacts on health, the environment, and the local community.

Project Structure

Focus on one or more Technical Targets

- Organic
- Glass
- Semi-conductor

Propose specific Project-level Targets…

- Technical Milestones
- Technical Targets
- Non-Technical Milestones
- Non-Technical Targets

Provide for supplying substrate samples and demonstration devices

- Substrate samples
- Demonstration devices

Sub-divide projects into 4 phases, 3-18 months

- Pilot-scale production of substrates in Phase 4
- Period of Performance not to exceed 5 years

SMART
(Specific, Measurable, Achievable, Relevant, and Time-Bound)

Substrate Samples

Project Assessments

- Do manufactured substrates possess features described in technical targets?

Substrates

- Substrates for evaluation including relevant documentation such as process assumptions, design manuals, PDK, reliability criteria, and electrical specifications.
- Phase dependent lot and batch sizes.

Demonstration Device

Project Assessments

- Is the substrate design suitable for integration into a simple, functional, testable package?

Demonstration Device

- Describe the design of a demonstration device appropriate to the intended substrate design and suitable for demonstrating the ability to successfully integrate substrate into a functional and testable package.

Eligibility

Eligible Applicants

- ☐ Domestic for-profit organizations
- ☐ Domestic non-profit organizations
- ☐ Accredited institutions of higher education including community and technical colleges
- ☐ State, local, territorial, and Indian tribal governments

Eligible Participants

- ☐ FFRDC as subrecipients or contractors with additional justifications
- ☐ Federal Entities as Subrecipients or contractors
- ☐ Foreign Organizations as members of project team, subrecipients or contractors, CHIPS R&D Approval with written justification.

Additional Requirements

- ☐ Lead Institution is applicant entity for full application: ***substrate prototyping capabilities or plan to achieve in 3 months***
- ☐ Entities may only apply as **Lead Institution** 1 full application
- ☐ Entities may be included as subrecipients on no more than 2 applications

Co-investments

- ☐ Strongly encouraged
- ☐ Described in 2 CFR § 200.306
- ☐ Other investments must be allocable and necessary

Applicants should familiarize themselves thoroughly with the eligibility requirements within the Materials and Substrates NOFO 2024-NIST-CHIPS-NAPMP-01, Section 3

Funding Restrictions

Highlight

- Construction activities are not an allowable cost under this program. However, costs related to internal modifications of existing buildings that would be necessary to carry out the proposed research tasks may be allowed, at NIST discretion.
- In addition, recipients and subrecipients may not charge profits, fees, or other increments above cost to an award issued pursuant to this NOFO

Materials and Substrates Application Process

Step	Description
1 Concept Paper	**Mandatory Concept paper broadly describes approach to technical area, impact, plans, project team, capabilities, and budget estimates.** There is a 10 page limit on concept paper narrative. A merit assessment of eligible, complete, and responsive concept papers. Successful applicants will be invited to submit full applications. Submission instructions contact research@chips.gov with opportunity number 2024-NIST-CHIPS-NAPMP-01 in subject.
2 Full Application	**Full Applications are a detailed proposal describing project description, impacts, team, technical plan, EWD, Research Security, CVDP, and IP management. This is not an exhaustive list.** Submission of full applications will be through Grants.gov.
3 Evaluation	**Merit Reviews will be conducted for both Concept Papers and invited Full Applications**. Reviews will consider criteria: Relevance to economic and national security; Overall scientific and technical merit; Project management; and transition and impact strategy.

Nothing listed supercedes NOFO.

Concept Paper Requirements

	Key Forms and Documents	Description
A	**Cover Sheet**	A one-page document that does not contribute to concept paper narrative page limit
B	**Executive Summary**	Executive Summary is a one page summary/abstract suitable for dissemination to the public. It should be a self-contained document that broadly describes project team, objectives, impacts, and education/workforce goals.
C	**Quad Chart**	Quad chart format selected by applicant that contains problem statement, proposed solution, concept of project, technical objectives and key participants.
D	**Table of Contents**	For concept paper narrative, does not contribute to page limit
E	**Concept Paper Narrative**	A 10 page limit description of project impact statement, project plan, project team, planned role for additional team members, team capabilities, budget estimate, and letters of interest. *Applicants and recipients should have an active registration in SAM.gov*

Submission instructions contact research@chips.gov with opportunity number 2024-NIST-CHIPS-NAPMP-01 in the subject line. Nothing listed supercedes NOFO.

Concept Paper Evaluation Criteria

1	**Relevance to Economic and National Security**	• This criterion addresses relevance of the proposal to enhancing U.S. economic or national security competitiveness and to achieving the CHIPS R&D mission and goals, as expressed in Section 1.1.1.
2	**Overall Scientific and Technical Merit**	• This criterion addresses the quality, innovativeness, and feasibility of the proposed Concept Paper Narrative and the potential for meeting the objectives of this NOFO, as expressed in Section 1.1.3.
3	**Project Management**	• This criterion addresses the degree to which applicants demonstrate that they have the appropriate personnel and access to required equipment and facilities
4	**Transition and Impact Strategy**	• This criterion addresses the project's potential for supporting the commercialization and domestic production of funded semiconductor innovations, as well as beneficial impacts to workforce development and the broader domestic research, development, and innovation ecosystem.

Nothing listed supercedes NOFO.

Concept Paper Review Process

1	**Initial Review**	• Concept papers and full applications received by the respective deadlines will be reviewed to determine eligibility, completeness, and responsiveness to this NOFO and stated program objectives.
2	**Review of Concept Papers**	• Merit Review, Evaluation Panel, Adjectival Rating,
3	**Selection of Successful Concept Papers**	• Selection of Successful Concept Papers and Invitations to Submit Full Applications.

Nothing listed supercedes NOFO.

Full Application Requirements

	Key Forms and Documents	Description
A	**Forms**	SF-424, Research & Related Budget, CD-511, Research and Related Other Project Information, SF-LLL
B	**Project Narrative**	The Project Narrative is a word-processed document of no more than twenty (20) pages (single-spaced between lines), which is responsive to the program description and the evaluation criteria.
C	**Resume(s) or CV(s)**	Not to exceed 2 pages per individual. These do not contribute to the Project Narrative page limit. Resumes or CVs are required for all key personnel including the principal investigator(s).
D	**Budget Narrative and Justification**	Not to Exceed 5 pages. These do not count against the Project Narrative page limit. There is no set format for the Budget Narrative and Justification; however, the written justification should include the necessity and the basis for the cost, as described in NOFO.
E	**Additional Documents**	Indirect Cost Rate Agreements, Subaward Budget Form, Letters of Commitment and/or Interest, Data Management Plan, Current and Pending Support Forms

Nothing listed supercedes NOFO.

Full Application Evaluation Criteria

1	**Relevance to Economic and National Security**	• This criterion addresses relevance of the proposal to enhancing U.S. economic or national security competitiveness and to achieving the CHIPS R&D mission and goals (See Section 1.1.1).
2	**Overall Scientific and Technical Merit**	• This criterion addresses the quality, innovativeness, and feasibility of the proposed Concept Paper Narrative and the potential for meeting the objectives of this NOFO, as expressed in Section 1.1.3.
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Full Application Evaluation Criteria

1	**Relevance to Economic and National Security**	• This criterion addresses relevance of the proposal to enhancing U.S. economic or national security competitiveness and to achieving the CHIPS R&D mission and goals (See Section 1.1.1).
2	**Overall Scientific and Technical Merit**	• This criterion addresses the quality, innovativeness, and feasibility of the proposed Project Narrative and the potential for meeting the objectives of this NOFO, as expressed in Section 1.1.3. Specifically, the proposal must be clear and concise and identify the core innovation, technical approach, and major technical hurdles and risks, as well as clearly establish the feasibility of the project through adequately detailed plans linked to major technical barriers.
3	**Project Management, Resources, and Budget**	• This criterion addresses the reasonableness, appropriateness, and cost-effectiveness of the proposed budget, management strategy, and resources, relative to the work and objectives of the Project Narrative.
4	**Transition and Impact Strategy**	• This criterion addresses the project's potential for supporting the commercialization and domestic production of funded semiconductor innovations, as well as beneficial impacts to workforce development and the broader domestic research, development, and innovation ecosystem.

Nothing listed supercedes NOFO.

Full Application Review Process

1	**Merit Review**	• At least three (3) independent, objective reviewers, who may be Federal employees or non-Federal personnel, with appropriate professional and technical expertise relating to the topics covered in this NOFO.
2	**Evaluation Panel**	• Following the merit review, an evaluation panel consisting of CHIPS R&D staff and/or other Federal employees with the appropriate technical expertise will conduct a panel review of the ranked applications.
3	**Pre-Selection Interviews and Site Visits**	• At CHIPS R&D's discretion, applicants may be requested to participate in Pre-Selection Interviews and/or Site Visits during the evaluation panel phase, either at CHIPS R&D, the applicant's site, or a mutually agreed upon location, or via conference call or webinar.
4	**Adjectival Rating**	• The evaluation panel will provide a final adjectival rating and written evaluation of each full application to the Selecting Official for further deliberation.
5	**Selection and Federal Awarding Agency Review of Risk Posed by Applicants**	• The Selecting Official will make final award recommendations. NIST will also conduct the research security review described in Section 2.7.6 and the results will be provided to the Selecting Official.

Nothing listed supercedes NOFO.

Materials and Substrates NOFO: key dates

February 28, 2024

Materials and Substrates Funding Opportunity (Released)

For R&D activities that will **establish and accelerate domestic capacity for advanced packaging substrates and substrate materials**

March 12, 2024

Materials and Substrates Proposer's Day

Share detailed information on Materials and Substrates NOFO, in a collaborative atmosphere

Due: April 12, 2024 11:59 pm EST

Concept Papers Review

Mandatory concept papers submitted by teams

Teams invited to submit full application

July 3, 2024

Full Application Due

The full application from applicants due

CHIPS for America QR Code: **CHIPS NAPMP Materials and Substrates NOFO** (full text)

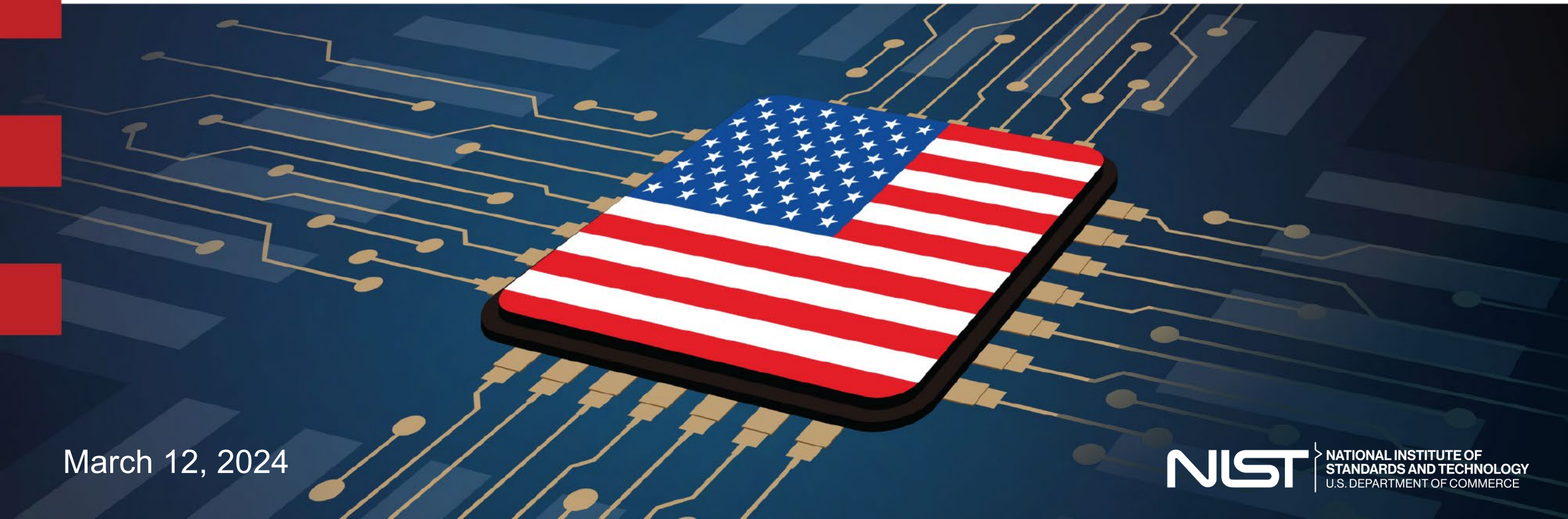
Policy and Integration Speakers

Richard-Duane Chambers
Director, Policy and Integration
CHIPS R&D Office

Greg Strouse
NIST Safeguarding Science
Research Security Director

CHIPS for America
CHIPS R&D Office Policy Overview

Richard-Duane Chambers
Gregory Strouse



March 12, 2024

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Policy Overview Agenda & Objectives

Agenda

- Overview of CHIPS R&D Office Goals
- International Collaboration
- Unique Directives Informing Work
- Key Required Plans
  - Domestic Control and Intellectual Property Rights
  - Commercial Viability and Domestic Production
  - Education and Workforce Development
  - Research Security

By the end, attendees should better understand

- CHIPS R&D objectives and policy context
- CHIPS R&D domestic and international research requirements
- Key required plans for proposals

Overview of CHIPS R&D Office Goals

Vision

A vibrant and self-sustaining U.S. domestic semiconductor ecosystem that revitalizes American manufacturing, grows a skilled and diverse workforce, and leads the world in semiconductor research and innovation.

Mission

Accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic tools, resources, workers, and facilities.

2030 Goals

- **U.S. Technology Leadership:** The United States establishes the capacity to invent, develop, prototype, and deploy the foundational semiconductor technologies of the future.
- **Accelerated Ideas to Market:** The best ideas achieve commercial scale as quickly and cost effectively as possible.
- **Robust Semiconductor Workforce:** Inventors, designers, researchers, developers, engineers, technicians, and staff meet evolving domestic commercial-sector and government needs.

Policy and National Security Context

Unique or Emerging Directives

CHIPS and Science Act (2022)

- Prohibit malign foreign talent recruitment programs
- Research security training

CHIPS Act (2021)

- Domestic production requirements
- Domestic control requirements to protect intellectual property from foreign adversaries

National Security Policy Memorandum 33 (2021)

- Research security program requirements
- Disclosure of conflicts of interest / commitment

Application Requirements

- **Domestic Research and Development Requirements**
- **Commercial Viability and Domestic Production Plan**
- **Domestic Control and Intellectual Property Rights Management Plan**
- **Research Security Plan**

Domestic & Int'l Research Requirements

"NIST adheres to the principle that U.S. research leadership benefits from mutually beneficial international collaborations, including welcoming international scientists"

- **Lead applicant must be a domestic entity;** foreign organizations, excluding foreign entities of concern (FEOCs), can participate.
- **Funded R&D activity should occur in the United States** but CHIPS R&D may approve the completion of certain tasks outside the United States.
- **Any disbursement of funds** outside the United States **must be approved by CHIPS R&D.**

Justification for Foreign Participants (excluding FEOCs):

- Foreign partner's involvement is essential to program objectives and doesn't jeopardize the project's pathway to domestic production.
- Applicant and foreign partner have adequate IP and data protection agreements in place.
- Foreign partner agrees to comply with laws and regulations and undergo a national security review.

Domestic Control of Intellectual Property

15 U.S.C. 4656(g): "The head of any executive agency receiving funding under this section shall develop policies to require domestic production, to the extent possible, for any intellectual property (IP) resulting from microelectronics research and development conducted as a result of such funding and domestic control requirements to protect any such intellectual property from foreign adversaries."

Key Requirements

- At least one domestic entity must own or co-own any IP from the funded R&D and must have full rights to enforce the applicable IP for a period of years determined prior to the final award.
- The domestic entity must notify NIST before selling, transferring, or assigning ownership of the IP to another entity.
- IP from the funded R&D cannot be sold, transferred, or assigned to a foreign adversary, to include FEOCs and foreign countries of concern. IP cannot be licensed (except in certain limited circumstances) to a foreign adversary

IP Rights Management Considerations

- Identify:
  - Key preexisting IP
  - IP the funded R&D will generate
  - How new partners can access the above IP
- Describe:
  - Additional licensing provisions to protect IP
  - Existing or planned protocols to ensure domestic control of the IP
  - How the IP supports commercial viability and domestic production

What is a foreign entity of concern?

Foreign entities of concern include entities owned by, controlled by, or subject to the jurisdiction or direction of the governments listed in 10 U.S.C 4872(d): China, Russia, North Korea, or Iran.

An entity is owned by, controlled by, or subject to the jurisdiction or direction of a government of a foreign country where:
(i) The entity is: a citizen, national, or resident of a foreign country listed in 10 U.S.C. 4872(d); and located in a foreign country listed in 10 U.S.C. 4872(d);
(ii) The entity is organized under the laws of or has its principal place of business in a foreign country listed in 10 U.S.C. 4872(d);
(iii) 25 percent or more of the entity's outstanding voting interest, board seats, or equity interest is held directly or indirectly by the government of a foreign country listed in 10 U.S.C. 4872(d); or
(iv) 25 percent or more of the entity's outstanding voting interest, board seats, or equity interest is held directly or indirectly by any combination of the persons who fall within subsections (i)–(iii).

Frequently Asked Questions

What is a “domestic entity”?

For the purposes of this NOFO, at a minimum, a domestic entity is one that is incorporated in the United States. NIST may also consider other factors, such as whether the entity has its principal place of business in the United States.

Note: CHIPS R&D expects funding recipients to exercise appropriate due diligence to determine whether a potential project partner may qualify as a foreign entity of concern or foreign country of concern and therefore be subject to prohibitions on participation.

Frequently Asked Questions

The NOFO states that at least one domestic entity must own or co-own any IP resulting from R&D conducted under the NOFO and have full rights to enforce applicable IP rights for at least a period of years, to be determined prior to the final award. What is a "period of years"?

CHIPS R&D will determine the "period of years" for which domestic control requirements are in effect on a case-by-case basis.

Commercial Viability and Domestic Production

"Applicants should propose measurable CVDP targets that demonstrate the viability of the proposed business model and of domestic production. Where relevant, CVDP milestones should complement technical milestones.."

Market Analysis Topics

1) Current State-of-The-Art
2) Value Proposition
3) Technical Milestones

Customer Analysis Topics

1) Market Size
2) Customer Engagement Strategy

Financial Plan Topics

1) Cost Structure
2) Revenue Streams
3) Access to Capital

Domestic Production and Scale-up Topics

1) Scale-up
2) Supply Chain
3) Workforce
4) Regional Ecosystem
5) Standards and Regulatory Compliance

Are there considerations that would allow for non-domestic production?

CHIPS R&D does not require production to occur exclusively within the United States. However, applicants should explain why they are unable to conduct certain production activities in the United States, considering factors such as:

- Lack of domestic production capabilities
- Relative cost of domestic vs. foreign production
- Potential economic or national security benefits from having distributed production among US and overseas sites
- Potential risks of US-based production such as market acceptance or value proposition

Research Security Agenda & Objectives

Agenda

- Safeguarding CHIPS Science through Research Security
- NIST IR 8484 – Research Security Framework
- Research Security Plan
- Research Security Reviews of NAPMP Applications
- Selected FAQs
- Questions and Contact information

By the end, attendees should better understand

- What is Safeguarding Science and Research Security
- What is the NIST Research Security Framework
- What is a research security plan
- How will an application be reviewed
- Answers to the FAQs
- Who to contact regarding research security

Safeguarding CHIPS Research Science

Safeguarding Science facilitates open science and research security that values collaboration while protecting U.S. national security and economic security interests.

Research Security is protecting the means, know-how, and products of research until they are ready to be shared.

Risks to U.S. Scientific Research Advantages

- **National Security** – Transfer of research products accelerates foreign military applications
- **Economic Security** – Loss of technical advantages results in the loss of U.S. global market competitiveness
- **Intellectual Property** – Some governments violate core research integrity principles and facilitate the transfer of original ideas from the United States

NIST IR 8484 – Safeguarding International Science Research Security Framework

Framework Implementation

- Strikes a balance between scientific research security and fostering international collaboration
- Implements a methodology to review research and make risk balanced determinations

Research Security Program Implementation

- Strategic communication and training
- Composite multi-disciplined open-source analysis
- Risk-balanced determination and mitigation
- User friendly tools, checklists, and templates

NIST Internal Report
NIST IR 8484

Safeguarding International Science

Research Security Framework

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Office of the Associate Director for Laboratory Programs
Laboratory Programs

Philip A. Bennett
Research and Technology Protection
Commerce Office of Security

Timothy R. Wood
Research Protections Office
Laboratory Programs

Mary Bedner
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CHIPS Program Office

Claire M. Saundry
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Director's Office

This publication is available free of charge from:
https://doi.org/10.6028/NIST.IR.8484

August 2023

U.S. Department of Commerce
Gina M. Raimondo, Secretary

National Institute of Standards and Technology
Laurie E. Locascio, NIST Director and Under Secretary of Commerce for Standards and Technology

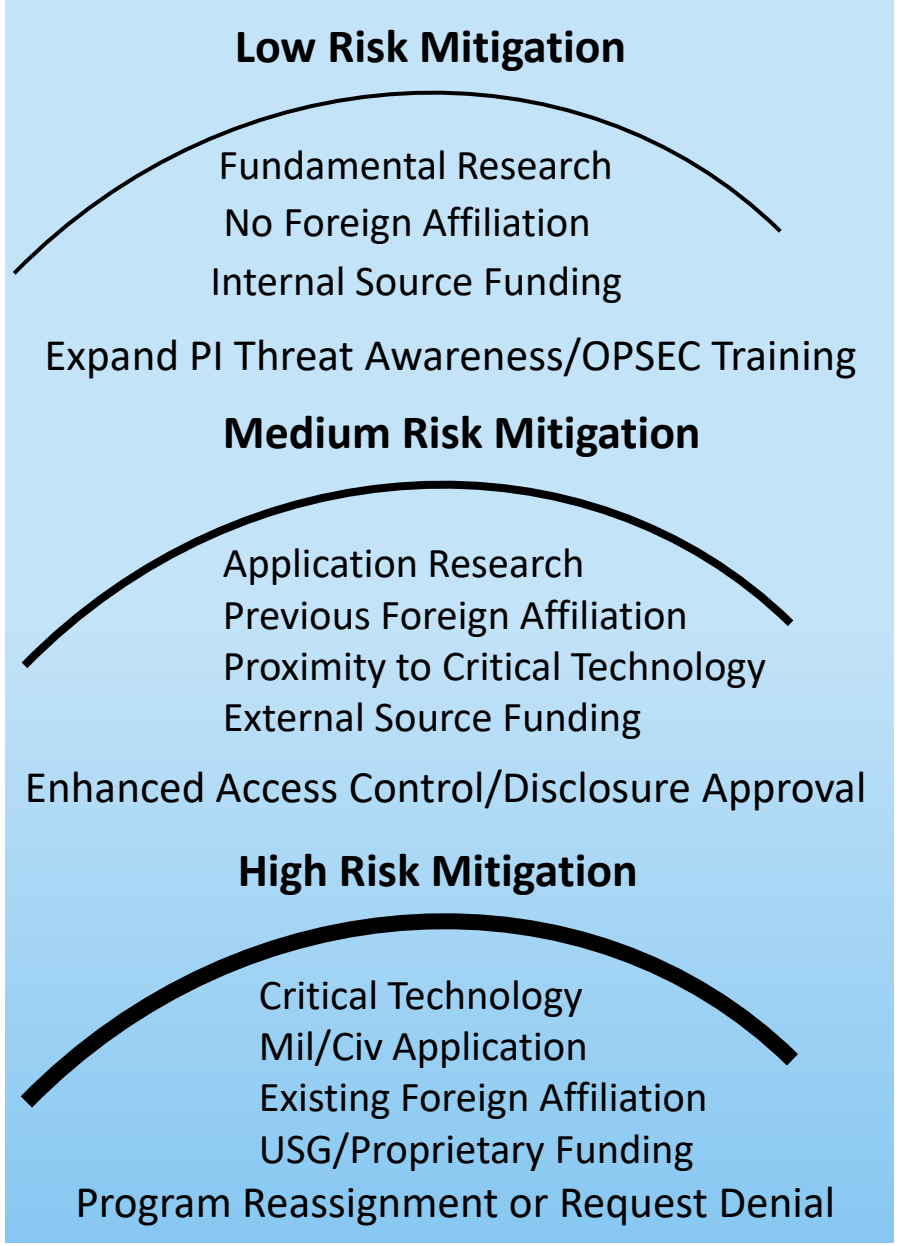
https://doi.org/10.6028/NIST.IR.8484

Research Security Plan: Key Components

"Provide a written plan describing internal processes or procedures to address foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity. Provide a point of contact on research security issues within the project leadership team."

- Establishing a Research Security Team and Policies
- Scope of Program – Assessing At-risk Technologies and IP
- Communication and Training Research Personnel and Staff
- Reviews, Risk Determination and Mitigation
- Reviewing Personnel Appointments
- Reviewing Foreign Travel Requests
- Reviewing Collaboration and Service Requests
- Implementing Technology Control (e.g., Data Mgmt and Export Controls)
- Cybersecurity

Research Security Reviews of NAPMP Applications



- **Understanding the research and type**
  - Fundamental or Proprietary
- **Implementation**
  - Open-source analysis by multi-disciplined team
  - Risk Analysis (**RAFT**)
    - **R**ecruitment, **A**ffiliations, **F**unding, and **T**echnology
- **Risk Determination and Mitigation**
  - Does the Benefit Outweigh the Risk?
  - Consensus risk-balanced determination with countermeasures to mitigate levels of anticipated risk
- **Program Maintenance (if awarded)**
  - Recurring Case Review
  - Partnership Oversight

Frequently Asked Questions

Do entities applying for CHIPS R&D research funds need to demonstrate that they have a research security program in place before applying for a research award and/or before receiving research funding?

- At present, CHIPS R&D does not require applicants to demonstrate the existence of a research security program in order to apply for or receive funding.
- However, applicants must provide a written plan (i.e., a research security plan) describing internal processes or procedures for addressing foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity, as applicable.

NIST Internal Report
NIST IR 8484

Safeguarding International Science

Research Security Framework

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https://doi.org/10.6028/NIST.IR.8484

Questions ?

CHIPS for AMERICA

Contact Information

researchsecurity@nist.gov

Frequently Asked Questions

Will CHIPS R&D provide funding or other resources to establish or improve a research security program or to the meet other CHIPS R&D research security requirements?

- To date, CHIPS R&D has not established any specific programs or set-asides to support the development of a research security program.
- However, limited funding may be available to implement a research security plan, subject to the objectives of the individual notice of funding opportunity (NOFO) and the approval of the relevant program director.
- For entities selected to receive funding, NIST may provide assistance to establish or improve research security activities consistent with NIST best practices (NIST IR 8484).

Grants Management Division Speakers

Blase Etzel
NIST Grants Management

Michael Teske
NIST Grants Management

Ready, Set, Submit!

Invited Full Application Preparation & Submission

NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Grants Management Division

Agenda

PLAN AHEAD TO STAY AHEAD

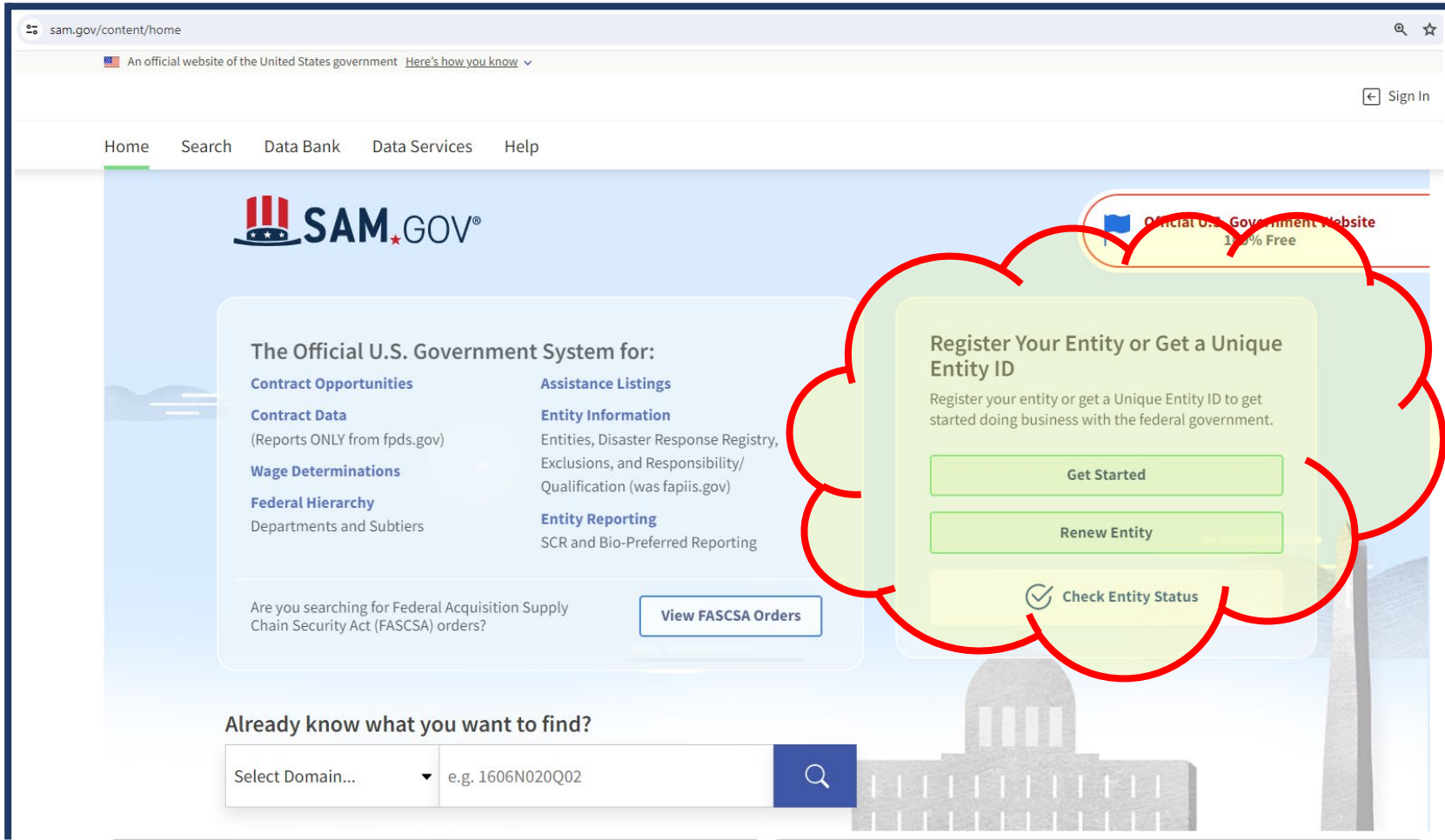
- SAM.gov Registrations
- Grants.gov Registrations
- Tips for Success

SAM.gov

Link: https://sam.gov/content/home

Help Desk: Monday - Friday from 8am - 8pm EST U.S. calls: 866-606-8220

- 100% FREE to register
- Create an active account
- Get a Unique Entity ID
- Register to SAM.gov before Grants.gov
- Start Early: the process takes about 10 days, but can take up to 6 weeks!
- Make sure Certifications and Representations are complete

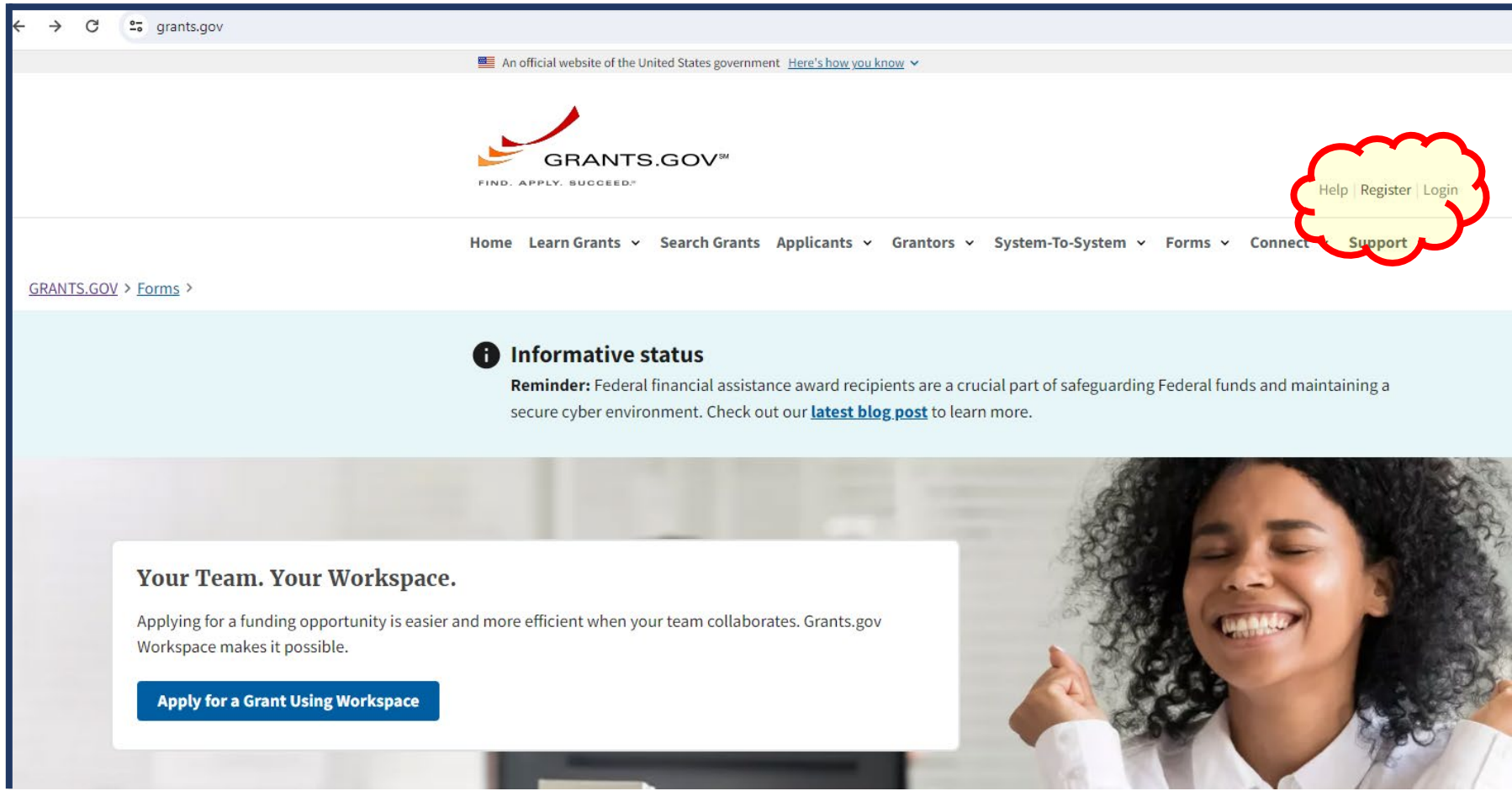


Grants.gov

Link: https://www.grants.gov/applicants/applicant-registration

Help Desk: 1-800-518-4726 (24/7 excluding holidays) or support@grants.gov

- 100% FREE to register
- Grants.gov will be used for full applications only
- See NOFO for Concept Paper submission process
- User Guide
- Applicant FAQs



Grants.gov

After obtaining the UEI for the organization from SAM.gov, you must return to Grants.gov to continue registration. There is no fee for registering with Grants.gov. Your organization's EBiz POC must:

1. Create a Grants.gov account with the same email address as used in SAM.gov for EBiz POC, and
2. Add a profile with Grants.gov using the UEI obtained from SAM.gov.

The EBiz POC can then delegate administrative roles to other users. Read the Help article, Manage Roles for Applicant for instructions.

Visit Learn Grants to find information about every phase of the grant management process, from applying and reporting to the award closeout.

On-Time Submission

- Deadline for Invited Full Application is *July 3, 2024, by 11:59 p.m. Eastern Time*

- **All registrations including SAM.gov must be completed before the deadline**
- **Application must be free of Grants.gov errors; corrective submissions must be made BEFORE the submission deadline and will overwrite previous submissions**

- Errors stop application processing and must be corrected

- Warnings do not stop application processing and are corrected at your discretion based on your circumstances

- **Submit early to allow time to correct any unexpected errors or submission issues**
  - Depending on the size of the file, transmittal may take SEVERAL MINUTES to HOURS.
  - Don’t wait until the deadline date to submit. The system may be slow due to last minute submissions.

Tips for Success

- Do NOT apply with a full application in Grants.gov until invited
- Understand submission process in NOFO
- SAM.gov registration must be active to apply in Grants.gov
- Designate the proper roles in the systems (ie: Authorized Rep in Grants.gov)
- Utilize “workspace” feature in Grants.gov to draft applications
- Do not pay to create accounts
- Limit application to file size / character limits / page limits
- Late applications will not be accepted
- Use correct UEI and EIN
- Make sure you are using compatible software (ex: Adobe Reader)
- Register to SAM.gov and Grants.gov early!

Lunch Options

- On your own
  - Olives restaurant in the hotel lobby
  - Olives restaurant "grab & go options" in the hotel lobby
  - Venture out to one of the local restaurants:
    - https://www.google.com/maps/d/edit?mid=1udE_t1I0vEh3adeRn9HtqTQkbSnd8KM&usp=sharing
    - QR code links to map of local eateries, may want to order ahead:

Panel Question & Answer

George Orji
Deputy Director
NAPMP
Moderator

Dan Berger
Associate Director
NAPMP

Richard-Duane Chambers
Director, Policy and Integration
CHIPS R&D Office

Aaron Forster
Program Manager
Materials and Substrates

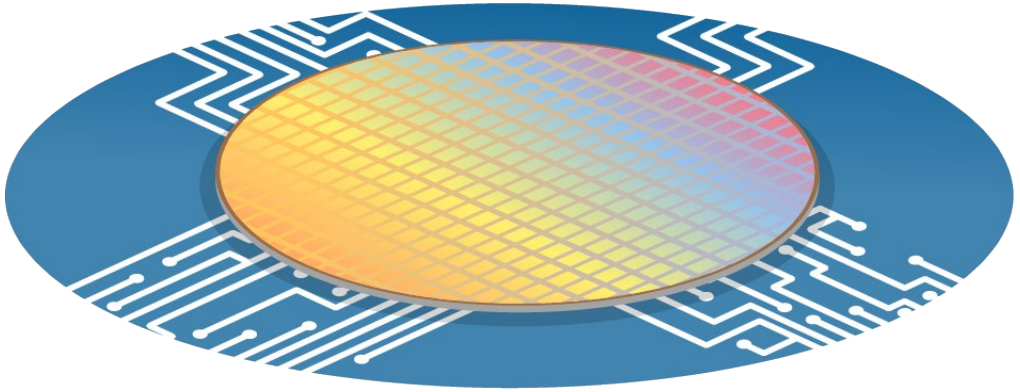
Greg Strouse
NIST Safeguarding Science
Research Security Director

Lunch Options

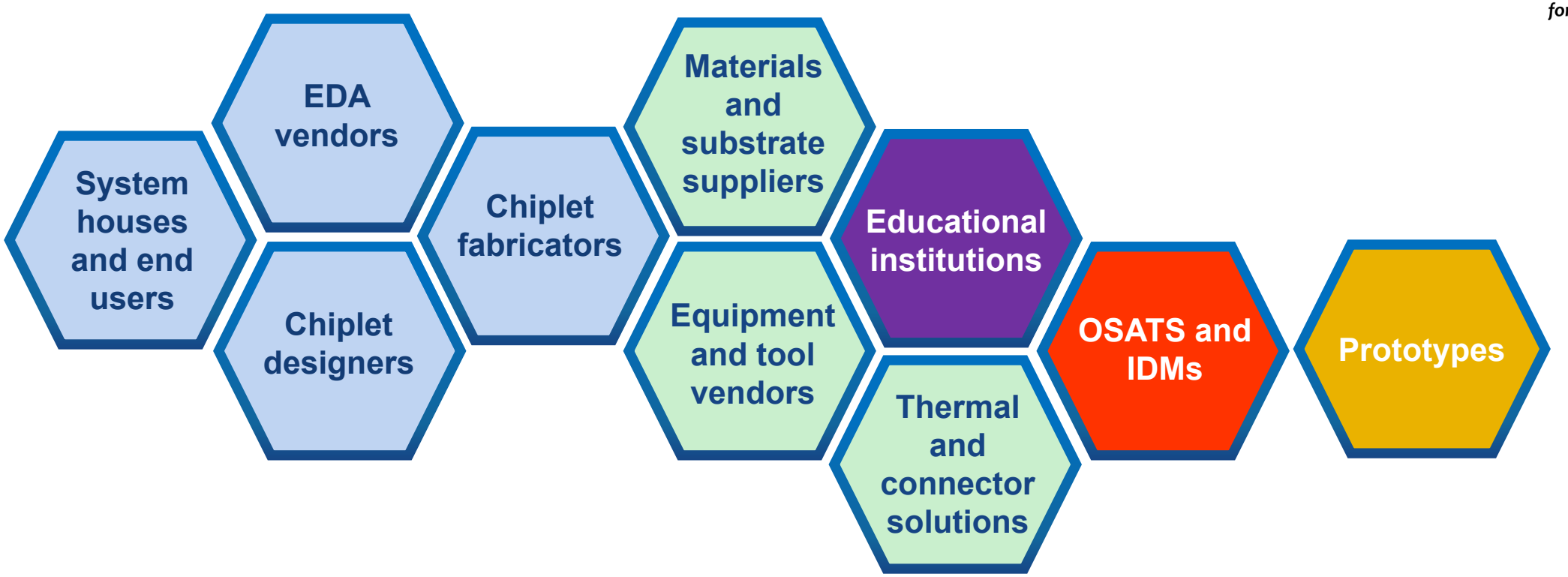
- On your own
  - Olives restaurant in the hotel lobby
  - Olives restaurant grab & go options in the hotel lobby
  - Venture out to one of the local restaurants:
    - https://www.google.com/maps/d/edit?mid=1udE_t1I0vEh3adeRn9HtqTQkbSnd8KM&usp=sharing
    - QR code links to map of local eateries, may want to order ahead:

Possible benefits of teaming:

- Complementary skillsets
- Shared goals
- Trust and commitment
- Diversity of experiences, backgrounds, locations and even work status
- Open communication
- Inclusive



Collaboration is Critical for Success



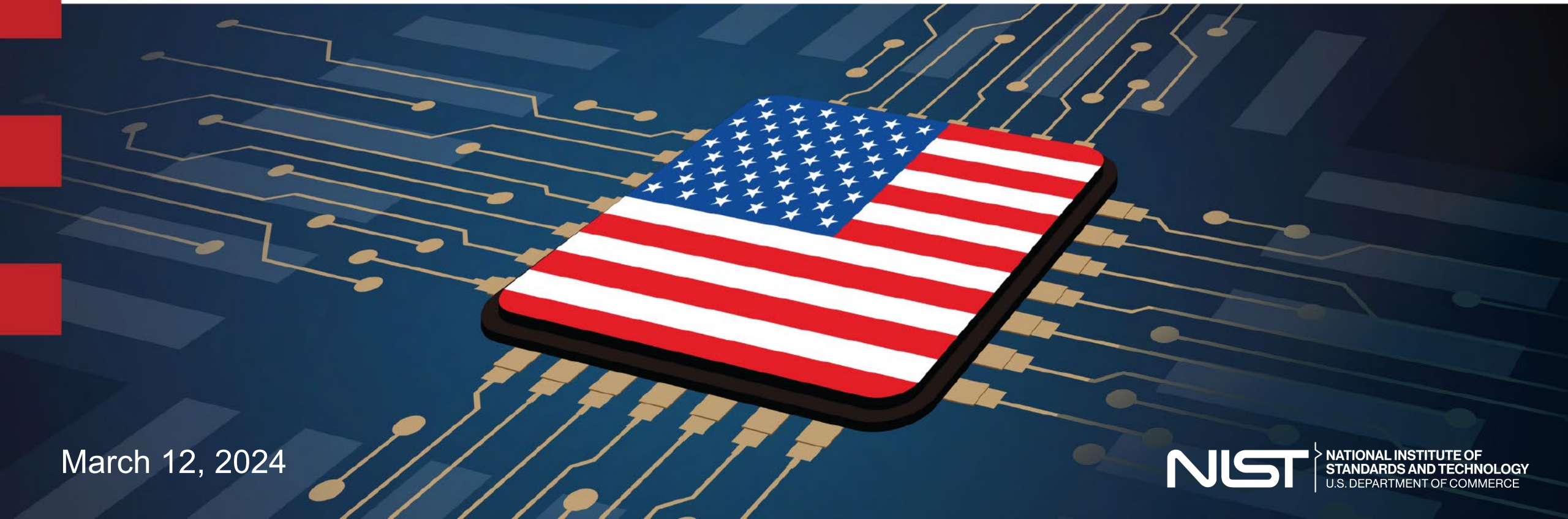
We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the NAPMP.

Afternoon Breakout Sessions

- Successful outcomes are proposer's forming strong and diverse teams.
- There are two sessions in three different rooms
  - Breakout Session 1: Discussions with a Technical Area Focus
    - Blue Lanyard/Organic, fan out sticker – XXX room
    - Black Lanyard/Glass sticker – YYYY room
    - Red Lanyard/Semiconductor – ZZZZ room
    - Virtual attendees will remain together in Zoom meeting room.
  - Networking Break: Virtual attendees have opportunity to go to smaller rooms. After break go directly to session 2.
  - Breakout Session 2: Discussions with a Teaming Focus
    - There are three different rooms: XXX, YYY, ZZZZ
    - Please try out a different room to network with a new group of people

National Advanced Packaging Manufacturing Program - Next Steps

Subramanian Iyer



March 12, 2024

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Disclaimer

Statements and responses to questions about advanced microelectronics research and development programs in this webinar:

- Are informational, pre-decisional, and preliminary in nature.
- Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
- Are subject in their entirety to any final action by NIST or the Department of Commerce.

Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or Notices of Funding Opportunity, which are controlling.

The Role of the package

Mechanical protection
- Handling
- Stability

Environmental protection
- Moisture
- Hermeticity
- Corrosion

Thermal protection
- Heat spreading
- Heat sinking
- Hotspot reduction

To protect and to serve

Connect electrically to other chips

Deliver power

Stable test and integration platform

“Scale Down, Scale Out and then Scale Up”

Packaging Roadmaps

- NIST sponsored roadmaps: MRHIEP, MAESTRO and MAPT
- Other roadmaps: HIR and IRDS

Technology Development Thrusts

- All aspects of technologies required to develop a leading-edge on-shore advanced packaging manufacturing capability

The Advanced Packaging Piloting Facility (APPF)

- Validates & practices NAPMP thrusts
- Piloting and prototyping functions

The Chiplet and Design Ecosystem

- Chiplet discovery, disaggregation and reaggregation methodologies, protocols, standards, fabrication and warehousing design for test, repair and reliability and holistic design tools and methodologies

Design in the U.S., build in the U.S., and Sell Worldwide

- Product-like prototyping exercise to be built and “qualified” in the APPF

NAPMP Structure: six hardware and eco-system thrusts + piloting facility + prototyping challenges

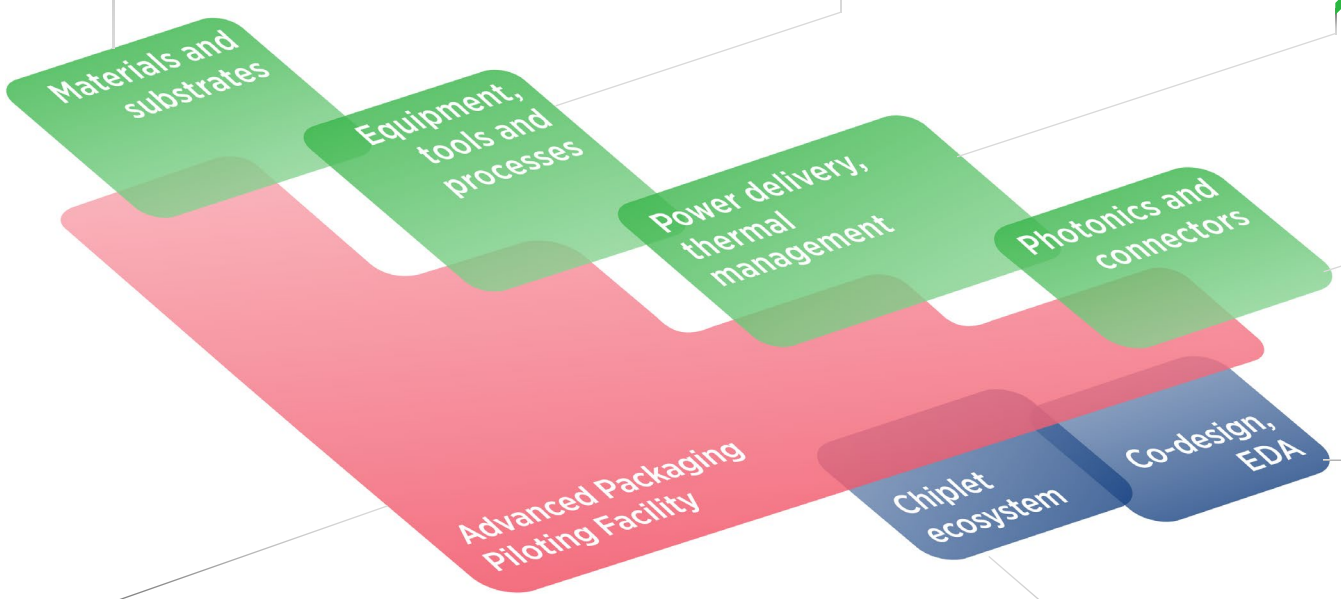
Materials and substrates are the platform for heterogeneous integration of dielets

Equipment, tools, and processes are needed to pattern substrates and assemble dielets and passivate assemblies

Thermal management and efficient power delivery are critical needs

Photonics and connectors allow the assembly to interact with the outside world

Automated design for test, repair, security, and reliability; substrate and process dependent



The NAPPF provides a test bed for integration of the different investment areas and also functions as a piloting and prototyping facility

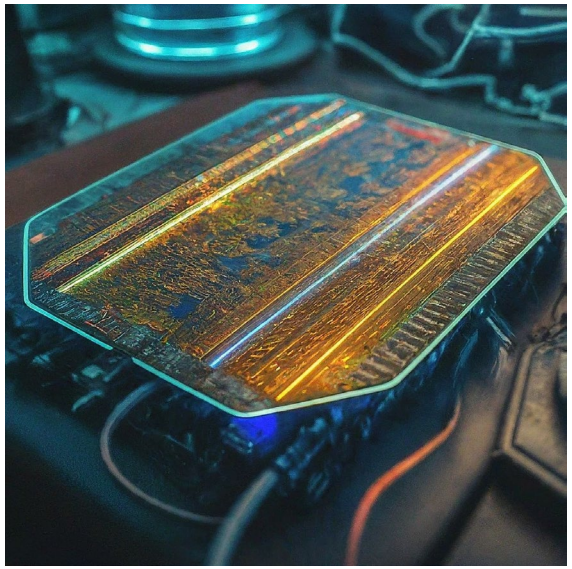
The chiplet ecosystem is crucial for any implementation of advanced packaging

NAPPF: National Advanced Packaging Piloting Facility

The National Advanced Packaging Piloting Facility (NAPPF) – Where it all comes together

- Investment Area Thrusts should connect activities with the APPF
- NAPPF will be focused on integrated process flows that can reach commercial scale
- NAPPF will be focused on validating new technology specifications, compatibility with other processes, yield, and reliability
- The NAPPF will be focused on assessing technologies for scaled transition to U.S. manufacturing including yield and reliability
- We will do this with baseline processes and prototyping and piloting exemplars

Choosing exemplars and corresponding baseline processes



AI and HPC

Low power edge communication devices

Medical Electronics

Others: auto, extreme ……

We could probably run two or three baseline processes in the NAPPF based on our three substrate types

We look forward to your thoughts on these topics.

Thank you for your participation!

Thank you for attending

Visit CHIPS.gov for future updates and additional information