CHIPS R&D Update

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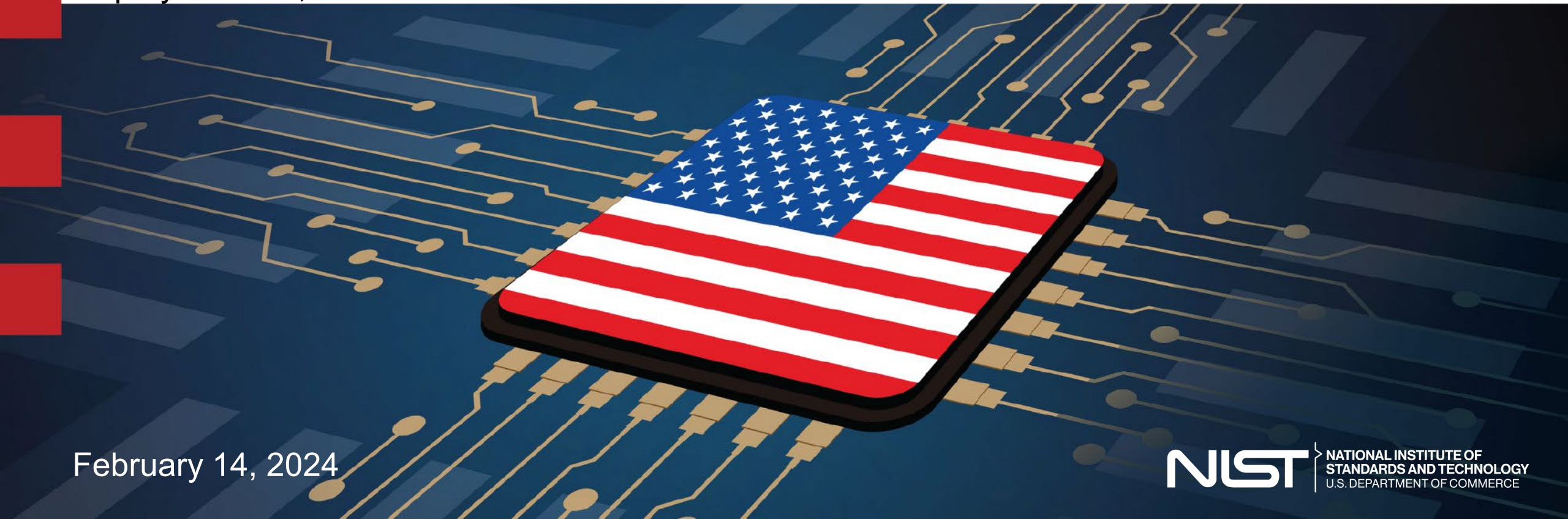


February 14, 2024

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

CHIPS for America

$39 billion
for incentives

Two component programs to:

1. Attract large-scale investments in advanced technologies such as leading-edge logic and memory, and advanced packaging
2. Incentivize expansion of manufacturing capacity for mature and other types of semiconductors

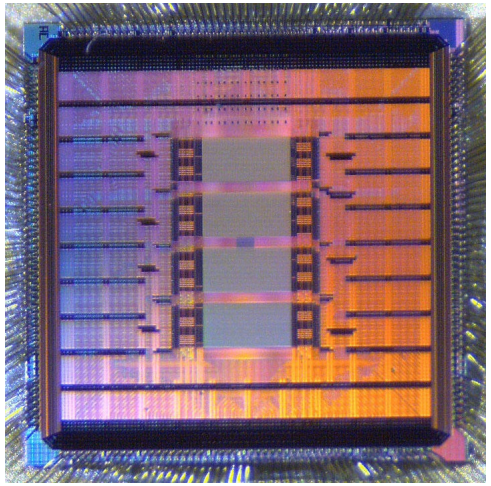
$11 billion
for R&D

Four integrated programs to:

1. Conduct research and prototyping of advanced semiconductor technology
2. Strengthen semiconductor advanced packaging, assembly, and test
3. Enable advances in measurement science, standards, material characterization, instrumentation, testing, and manufacturing

Plus CHIPS initiatives from other agencies, including DOD, State, NSF, and Treasury

Vision for Success



U.S. Technology Leadership

The United States establishes the capacity to invent, develop, prototype, and deploy the foundational semiconductor technologies of the future.

Accelerated Ideas to Market

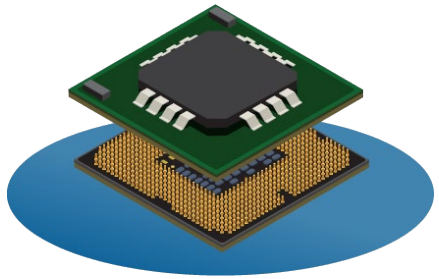
The best ideas achieve commercial scale as quickly and cost effectively as possible.

Robust Semiconductor Workforce

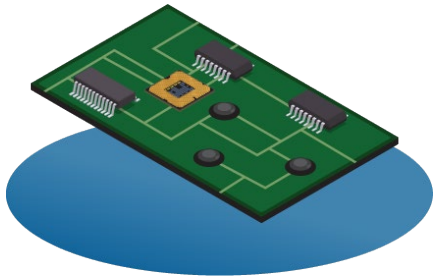
Inventors, designers, researchers, developers, engineers, technicians, and staff meet evolving domestic government and commercial-sector needs.

CHIPS R&D Programs

Metrology



National Semiconductor Technology Center



National Advanced Packaging Manufacturing Program

Manufacturing USA

Manufacturing USA Institute

Workforce Initiatives

CHIPS R&D Timeline

	FALL 2023	WINTER 23/24	Spring 2024
NSTC	Establish NSTC	Natcast.org / CEO	Membership / Programs
NAPMP	NAPMP vision and strategy	Notice of Intent	Notice of Funding Opp (~$300M)
Manufacturing USA institute(s)	Announce selected topic(s)	Notice of Intent	Notice of Funding Opp (min. $200M)
Metrology	3 Grand Challenges Funded	Communities of Practice	
Standards	Standards Summit	• Digital Twin Data • Chiplets	• Digital Twin Data • Supply Chain Trust Data

Updates

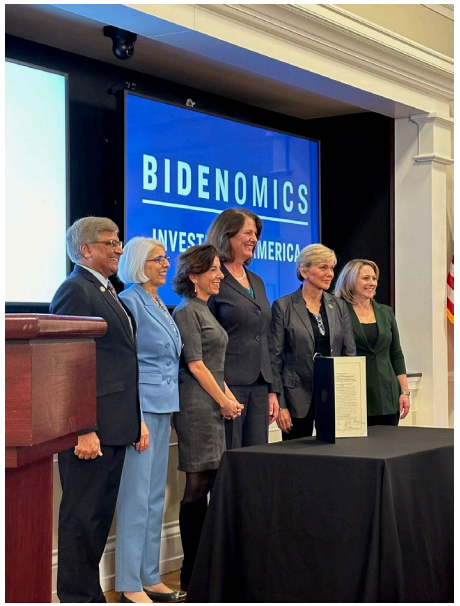
- National Semiconductor Technology Center Consortium
  - Feb 9, 2024
  - Signing ceremony at White House Executive Office Bldg.
  - Commerce, Energy, Defense, NSF, Natcast
  - Natcast CEO, Deirdre Hanford

- HBCU CHIPS Network kick-off (Feb 8, 2024)
  - At Department of Commerce

- Inside CHIPS Metrology (Jan 16, 2024)

- National Advanced Packaging Manufacturing Program Vision
  - Nov 27, 2023

- Building the U.S. Semiconductor Workforce (Nov 15, 2023)



Natcast

NAPMP Vision, Mission, and Outcomes

Vision

The National Advanced Packaging Manufacturing Program will drive **U.S. leadership** in advanced packaging and provide the technology needed for packaging manufacturing in the United States.

Mission

NAPMP will develop **critical and relevant innovations** for advanced packaging technologies and **accelerate their scaled transition** to U.S. manufacturing entities

Outcomes

- Within the decade NAPMP funded activities, **coupled with CHIPS manufacturing incentives,** will establish a vibrant, self-sustaining, profitable, high-volume, onshore packaging industry where advanced node chips manufactured in the USA are packaged in the USA.
- We expect the technology developed to be leveraged in new applications and market sectors

NAPMP Priority Research Investment Areas

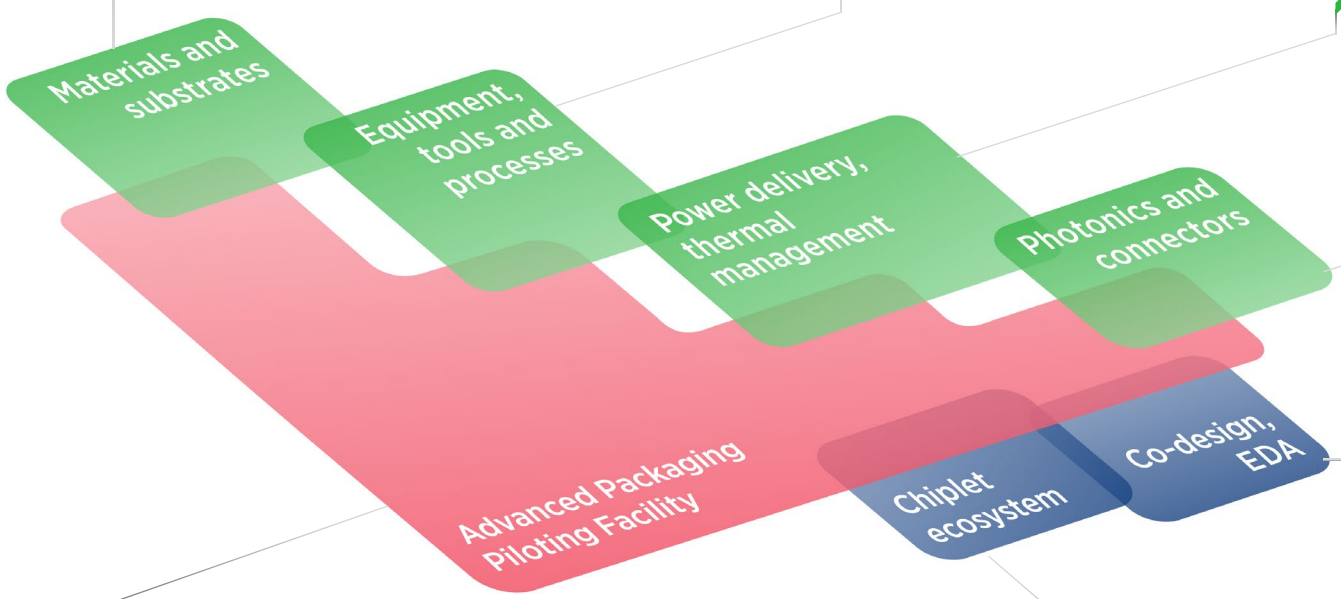
Substrates & materials are the platform for heterogeneous integration of dielets

Equipment, tools & processes are needed to pattern substrates and assemble dielets and passivate assemblies

Thermal management and efficient power delivery are critical needs

Photonics and connectors allow the assembly to interact with the outside world

Automated design for test, repair, security, and reliability; substrate and process dependent



The APPF provides a test bed for integration of the different investment areas and also functions as a piloting and prototyping facility

The chiplet ecosystem is crucial for any implementation of advanced packaging

APPF: advanced packaging piloting facility

CHIPS Manufacturing USA Institute

- Establish one Institute with the potential for significant impact on semiconductor manufacturing
- Topic = Digital twins

- For general planning, minimum expected NIST commitment ~$200 million over a five-year period
- Anticipate a greater than 1:1 cost share

- Analysis of RFI responses, industry feedback, listening sessions across 15+ engagements, and technology opportunities across the CHIPS R&D portfolio.

Digital Twin Institute

Vision

Enable **seamless integration of digital twin models** into the U.S. semiconductor manufacturing, advanced packaging, and assembly industries, enabling rapid adoption of innovations and enhancing domestic competitiveness for decades.

Mission

Foster a **collaborative environment** within the domestic semiconductor industry, enabled by the world's first **shared** semiconductor Digital Twin process **validation facility**, industry-relevant research projects, and digital-twin supported workforce training.

Digital Twin Institute Objectives

Reduce the time and cost for chip development and manufacturing

Accelerate the adoption of semiconductor manufacturing innovations

Increase access to semiconductor manufacturing training through the adoption of digital twin-enabled tools

Expand access to digital twin tools, solutions and frameworks

Digital Twin Institute Approach

A physical facility and digital framework, integrated with industry-led research projects

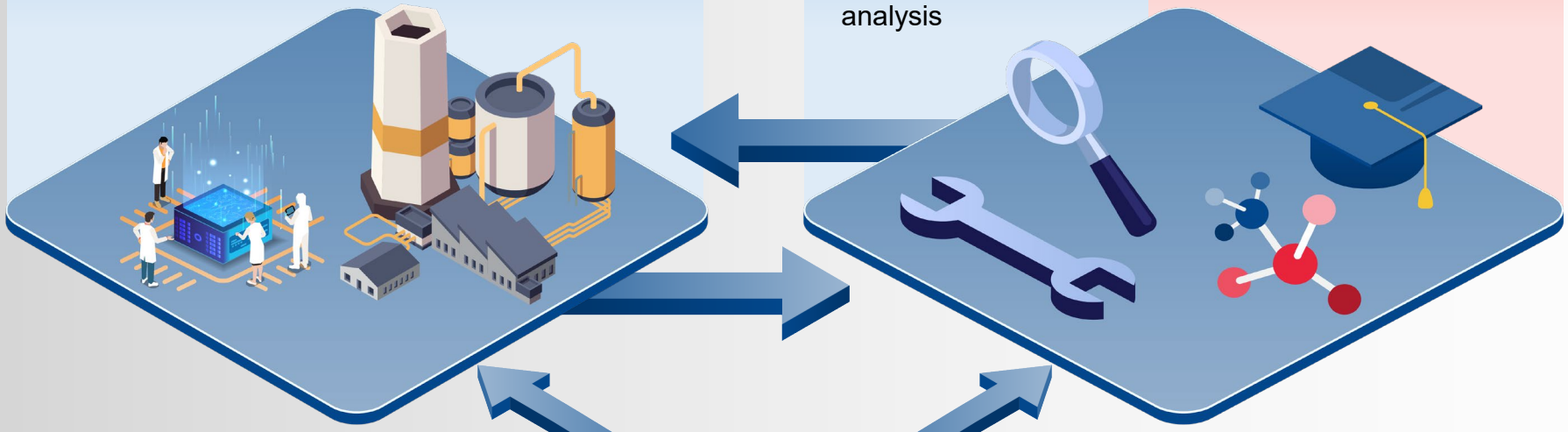
1 Establish a **shared physical facility**

Expected activities:
- Baseline facility testbed
- Digital emulation hardware
- Core technical & operations staff

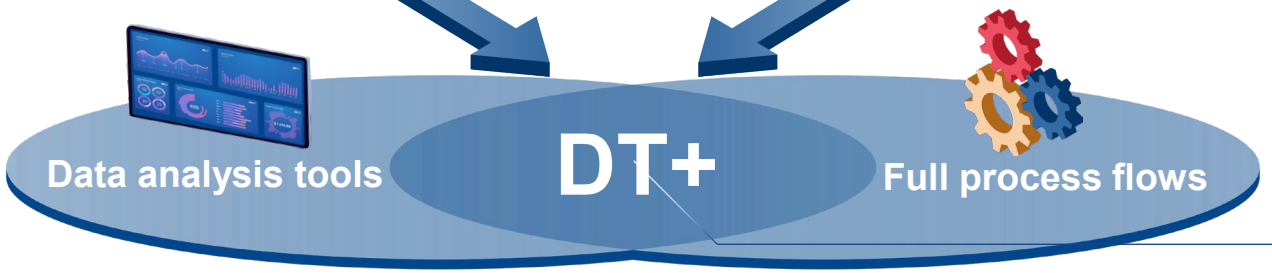
2 Competitively fund **industry-led technical and workforce development projects**

Deliver technical solutions, de-risk new tools, and conduct data analysis

Develop and test education & workforce development tools enabled by digital twins



3 **Digital framework** for interoperable data and models



4 Create a **shared marketplace** of digital twin models