


Impact of the ITRS Metrology Roadmap



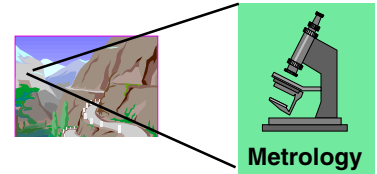
Where am I going and how will I get there ?

Alain Diebold

AGENDA

- ITRS Overview

- Metrology Roadmap Overview



- Lithography Metrology



- Front End Processes Metrology



- Interconnect Metrology

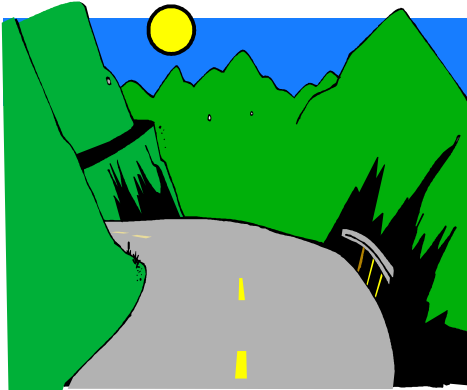


- Integrated Metrology

- Materials & Contamination Characterization

- The Future

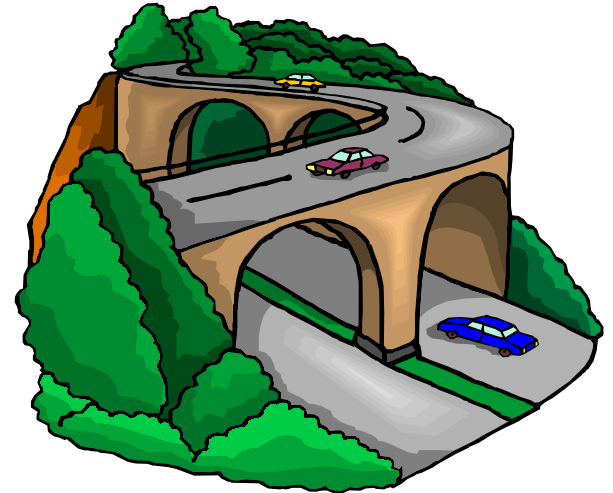
ITRS Focused Roadmaps



Lithography



Front End Processes



Interconnect



**Process Integration,
Devices. & Structures**

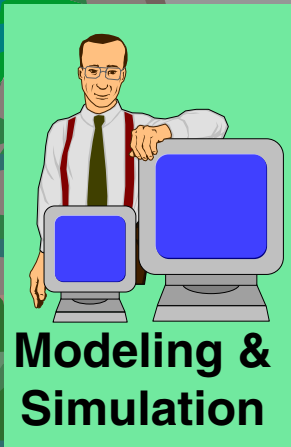


Packaging

ITRS Cross-cut Roadmaps

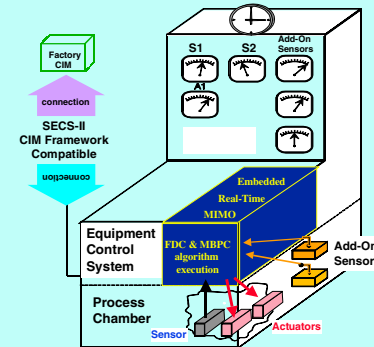
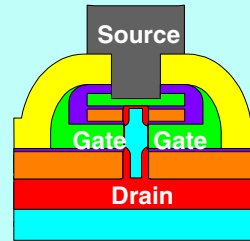
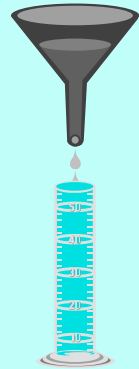


Defect Reduction Technology



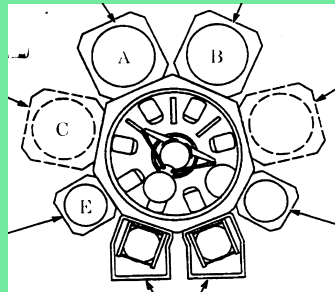
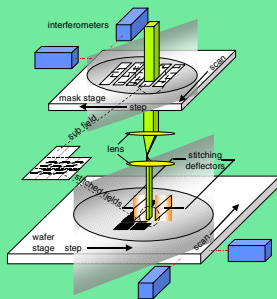
Three ITRS views of the future

New Materials, Structures, & Process Timing



High/Low k, USJ, beyond CMOS

New Process Tool Timing



Litho λ , cluster, wafer size

IC Node and Capability Timing

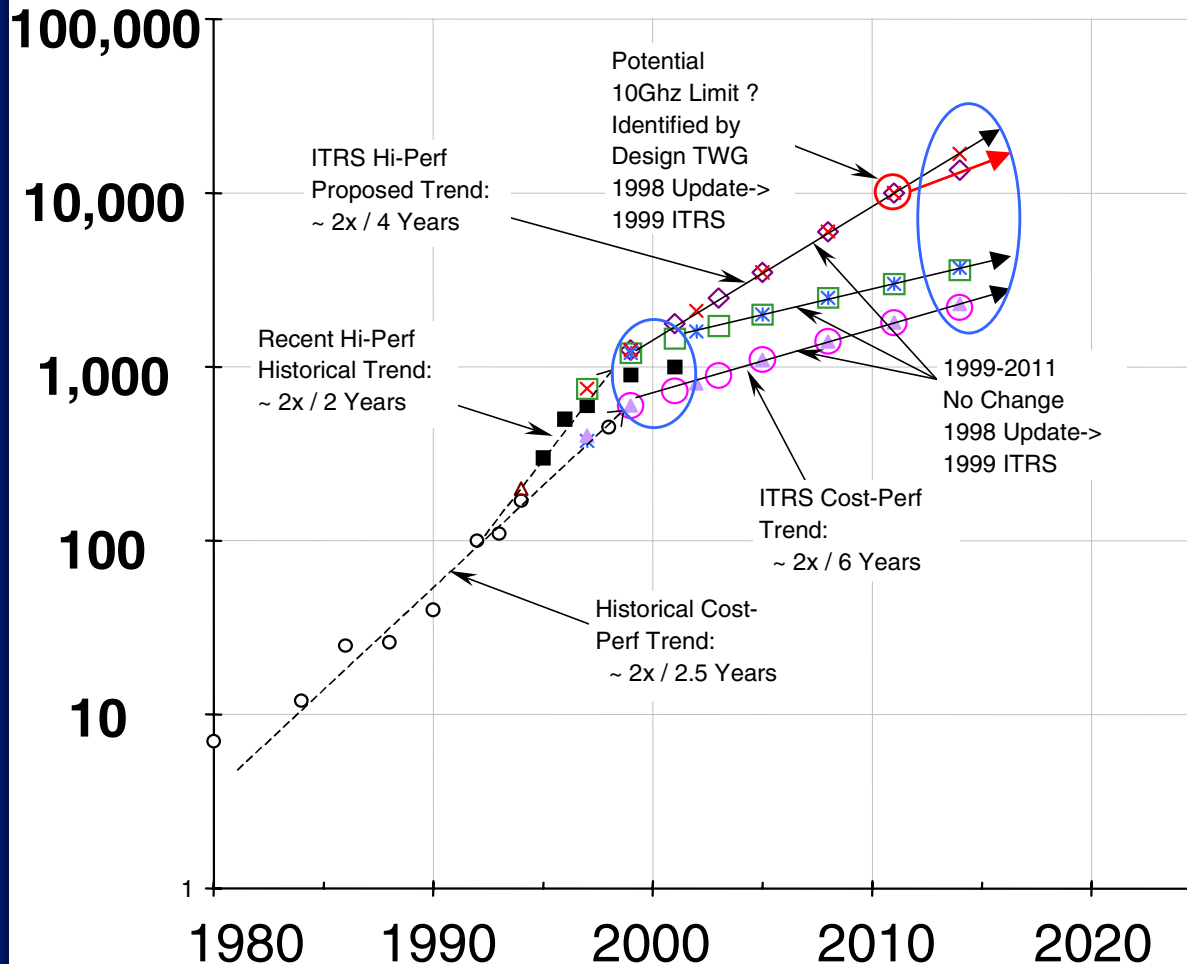


Logic and DRAM, wireless, SOC

ITRS High Level IC Timing

Chip Frequency: Logic - 1999 ITRS

Chip Frequency



■ U.S. MPU: high perf.	H D T
○ U.S. MPU: cost perf.	i a r
△ Toshiba	s t e
Source: S'TECH CAG	t a n
	d
	r / s
	i c
	a
	l

- ◇ ITRS 1999: on-chip local clock (high perf.)
- ITRS 1999: on-chip, across chip clock (high perf.)
- ITRS 1999: on-chip, across chip clock (cost perf.)
- × 1998 Update: on-chip local clock, (high perf.)
- × 1998 Update: on-chip, across chip clock (high perf.)
- ▲ 1998 Update: on-chip, across chip clock (cost perf.)

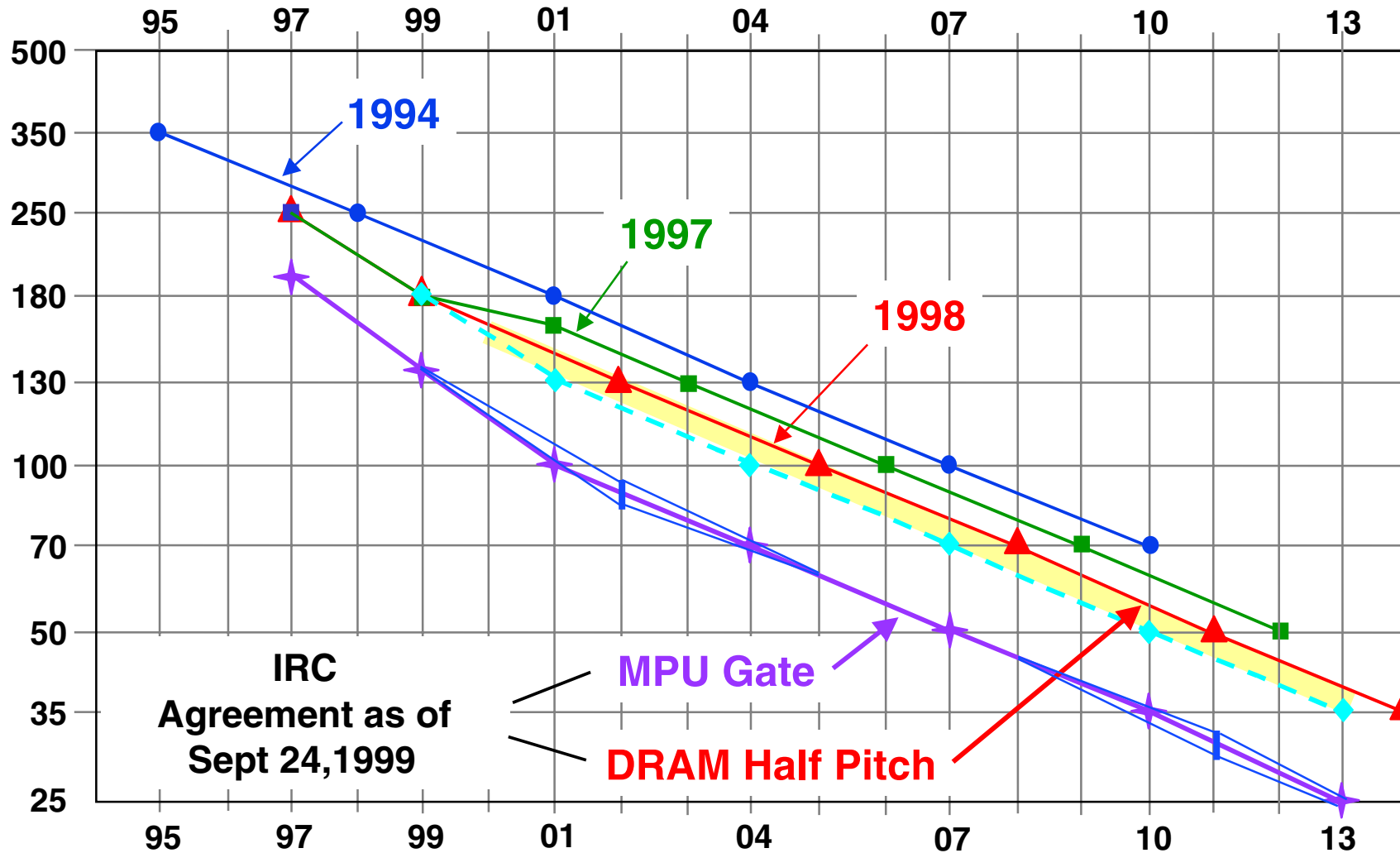
MHZ



ITRS Roadmap Node Timing

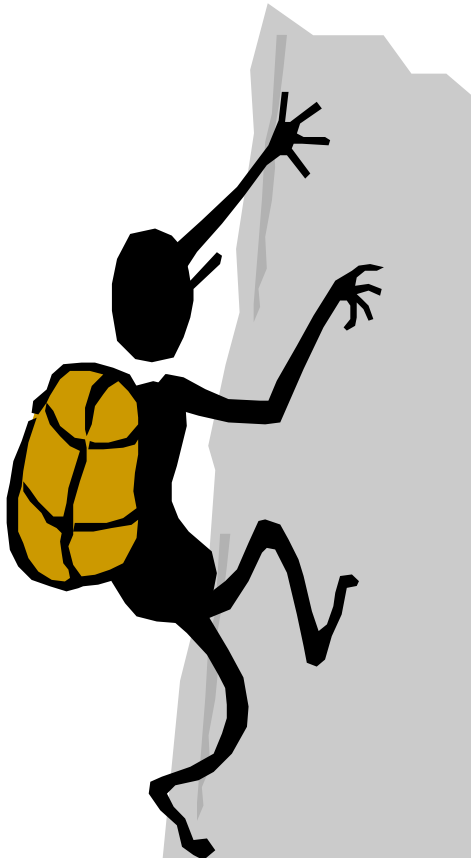
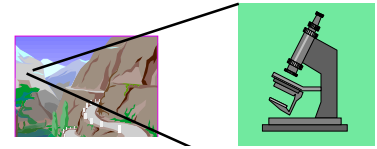
(from Litho TWG Summary)

Minimum Feature Size (nm)

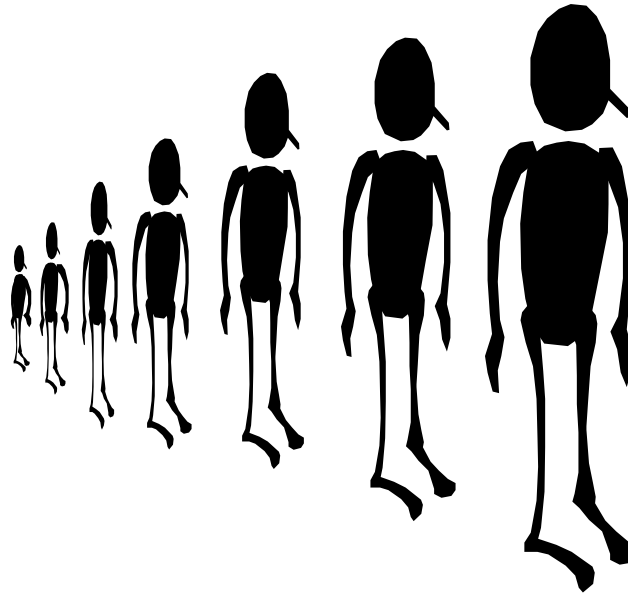


AGENDA

- ITRS Overview
- Metrology Roadmap Overview



OFF-Line



In - Line



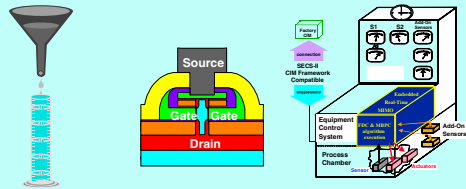
In-Situ

No Single Business Model for New Metrology?

Driver

New Metrology

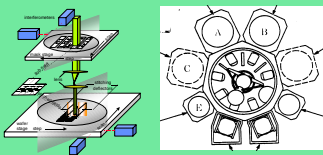
New Materials, Structures, & Process Timing



High/Low k, beyond CMOS, USJ

Optical & Electrical Metrology for High k, USJ, and low k

New Process Tool Timing



Litho λ , cluster, wafer size

157 nm Ellipsometry Sensors & Clustered Metrology

IC Node and Capability Timing



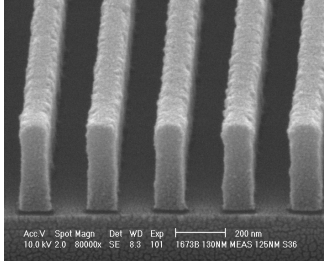
Logic and DRAM, wireless, SOC

High Frequency testing of low k

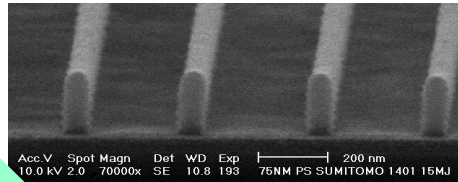
Microscopy is a critical need



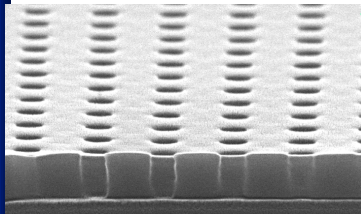
Dense Lines 130nm



Semi Dense = 75nm

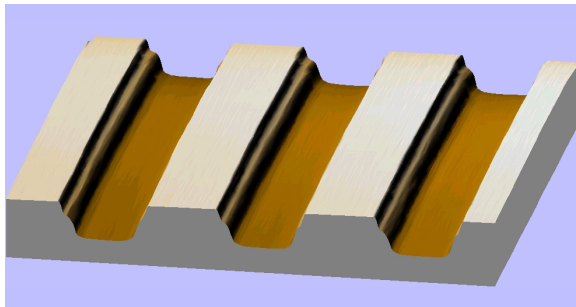


130nm Contacts

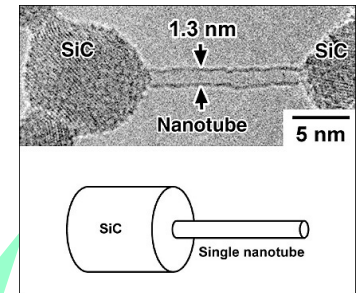


*smaller features
higher aspect ratios
new mask technology*

Masks

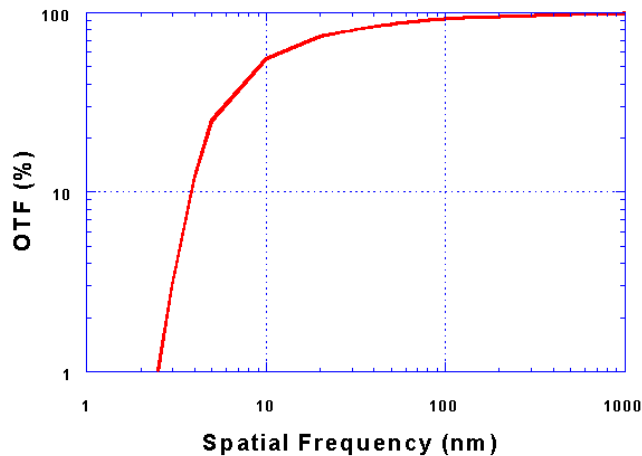


New devices



SEM Depth of Focus Issue

$$\text{DoF} = \frac{\text{(resolution)}}{\text{(convergence angle)}}$$

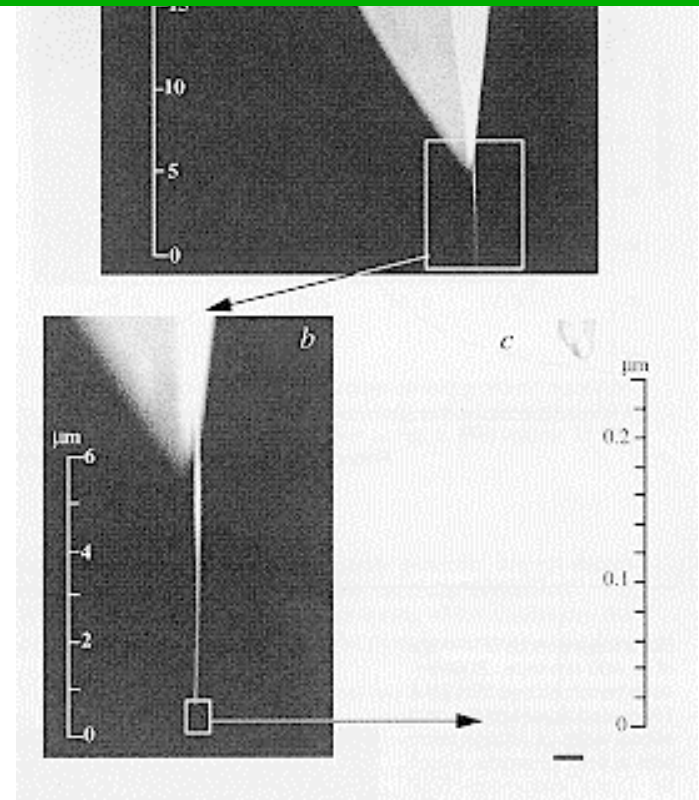


Today DoF ~ **0.4 micron**
2 nm/0.005 rads = **400 nm**

Tomorrow DoF ~ **0.02 micron**
1 nm/0.050 rads = **20 nm**

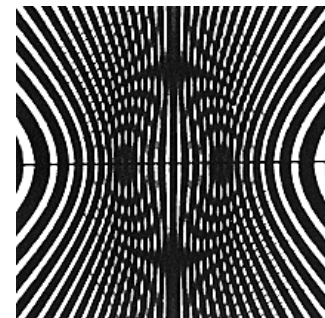
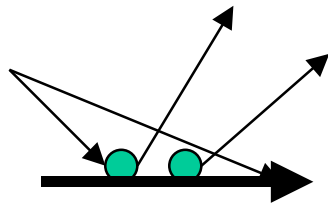
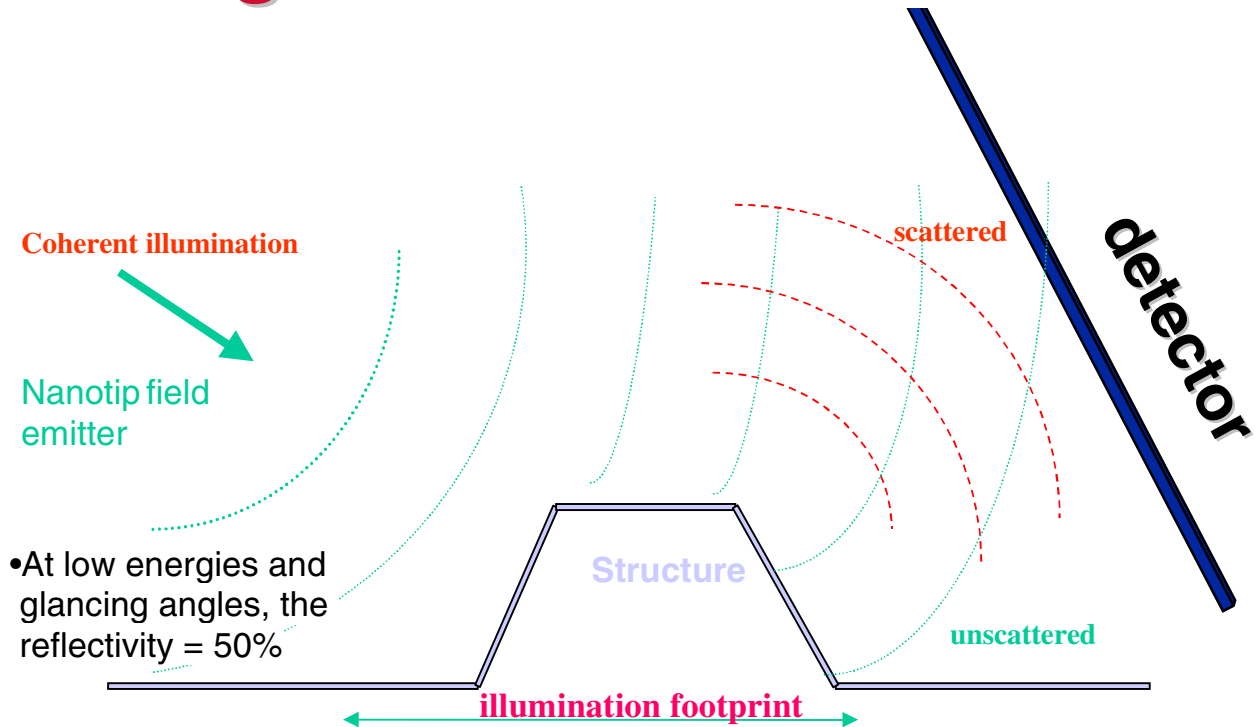
SPM Probe Tip Issue

High Aspect Ratios
sub 100 nm trench and via widths



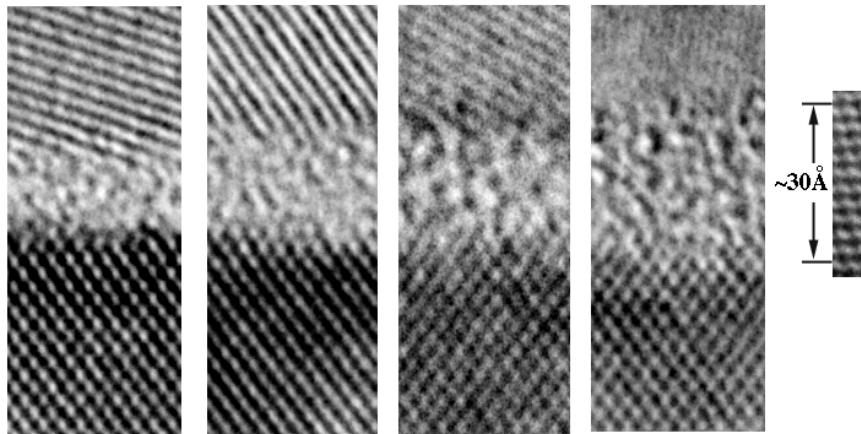
Dai, et al.,
Nature **384**, 147 (1996)

Electron Holography : a Long Term Potential Solution

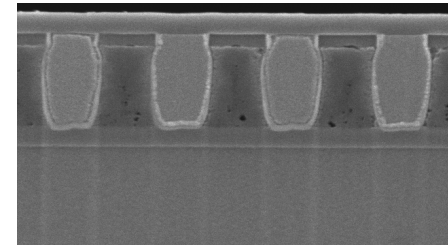


David Joy, Univ. of TN

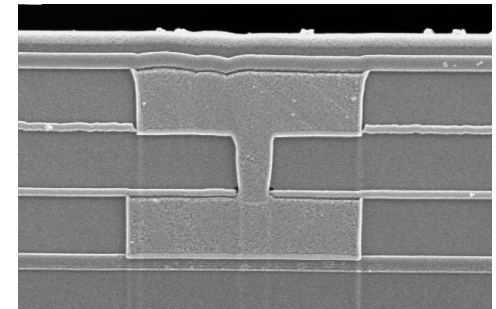
Interface Control



HRTEM	$14.2 \pm 1.7 \text{ \AA}$	$17.1 \pm 2.0 \text{ \AA}$	$18.6 \pm 1.7 \text{ \AA}$	$26.2 \pm 2.2 \text{ \AA}$
C-V	14 Å	17 Å	20 Å	29 Å



Barrier Layer / Cu



**Low k / barrier
etch stop / low k**

The Metrology Precision Roadblock

Year of First Product Shipment Technology Generation	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2003 100 nm	Driver
DRAM 1/2 Pitch	180	165	150	130	120	110	100	D½
Logic Isolated Lines	140	120	100	85	80	70	65	M Gate

Microscopy and Lithography

Microscopy resolution (nm) for P/T=0.1	1.4	1.2	1.0	0.85	0.8	0.7	0.65	MPU
Wafer Gate CD Control*	13	12	10	8.5	8	7	6.3	MPU
Wafer CD Tool Precision* P/T=.2 Isolated Lines**	2.6	2.4	2.0	1.8	1.6	1.4	1.3	MPU
Mask Area Metrology Tool Precision P/T=.2	4.8	4.2	3.4	2.8	2.6	2.4	2.2	MPU




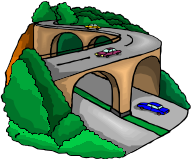
Front End Processes

Logic Dielectric Thick Precision 1σ (nm) ^B	0.0025	0.0024	0.0021	0.0017	0.0016	0.0013	0.0012	MPU Gate
2D Dopant Profile Spatial Resolution (nm)	3	3	3	2	2	2	1.5	MPU Gate

Interconnect

Barrier layer Thick (nm)	23	19	16	13	11	7	3	MPU
process range ($\pm 3\sigma$)	20%	20%	20%	20%	20%	20%	20%	
Precision 1σ (nm)	0.08	0.06	0.05	0.04	0.035	0.02	0.01	

AGENDA

- ITRS Overview
- Metrology Roadmap Overview 
- Lithography Metrology & New Structures from PIDS 
- Front End Processes Metrology 
- Interconnect Metrology 
- Integrated Metrology
- Materials & Contamination Characterization
- The Future

First Year of IC Production

1999

2002

2005

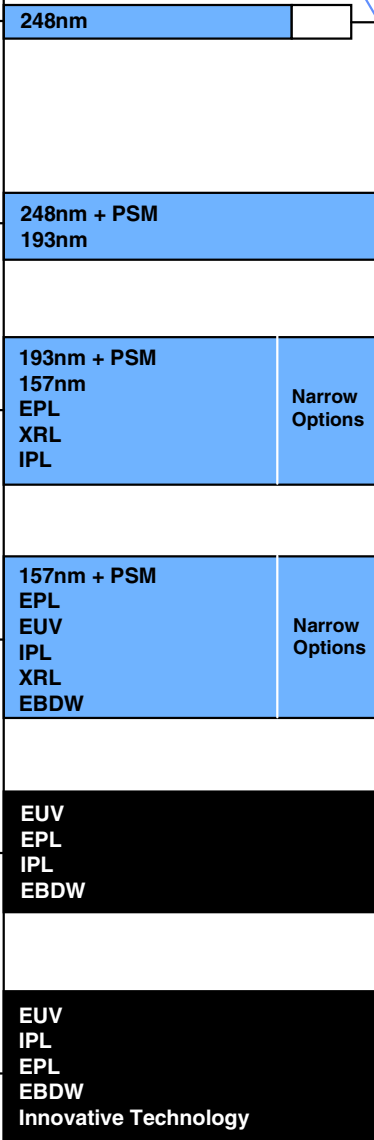
2008

2011

2014

Technology Options at Technology Nodes (DRAM Half Pitch, nm)

180
130
100
70
50
35



DRAM Half Pitch (Dense Lines)

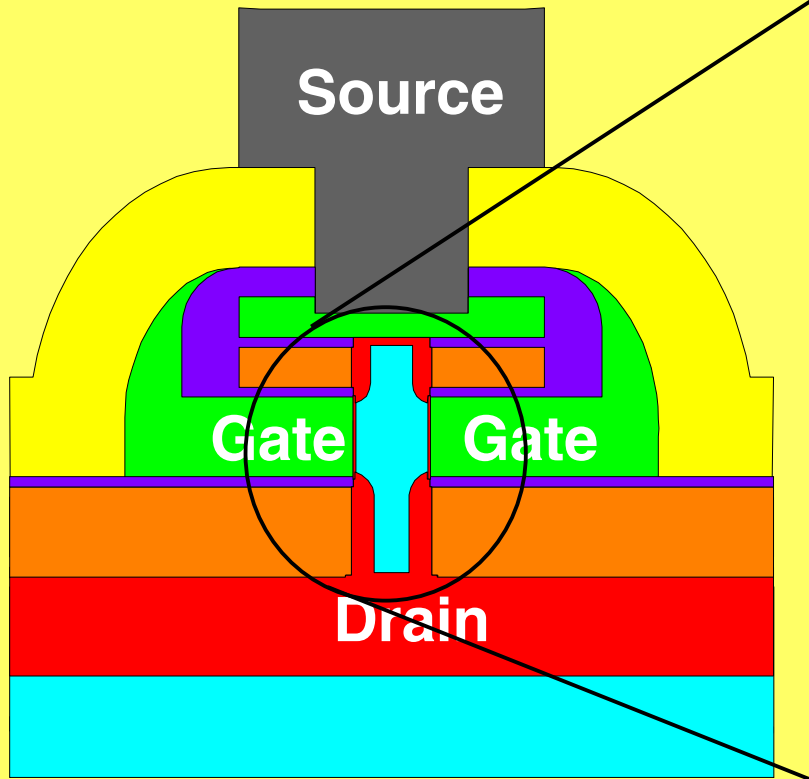
Research Required
 Development Underway
 Qualification/Pre-Production

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the technology solution.

Note: Production level exposure tools should be available one year before first IC shipment.



Lithography Metrology



**Vertical
Transistor**
**CD is a Film
Thickness**

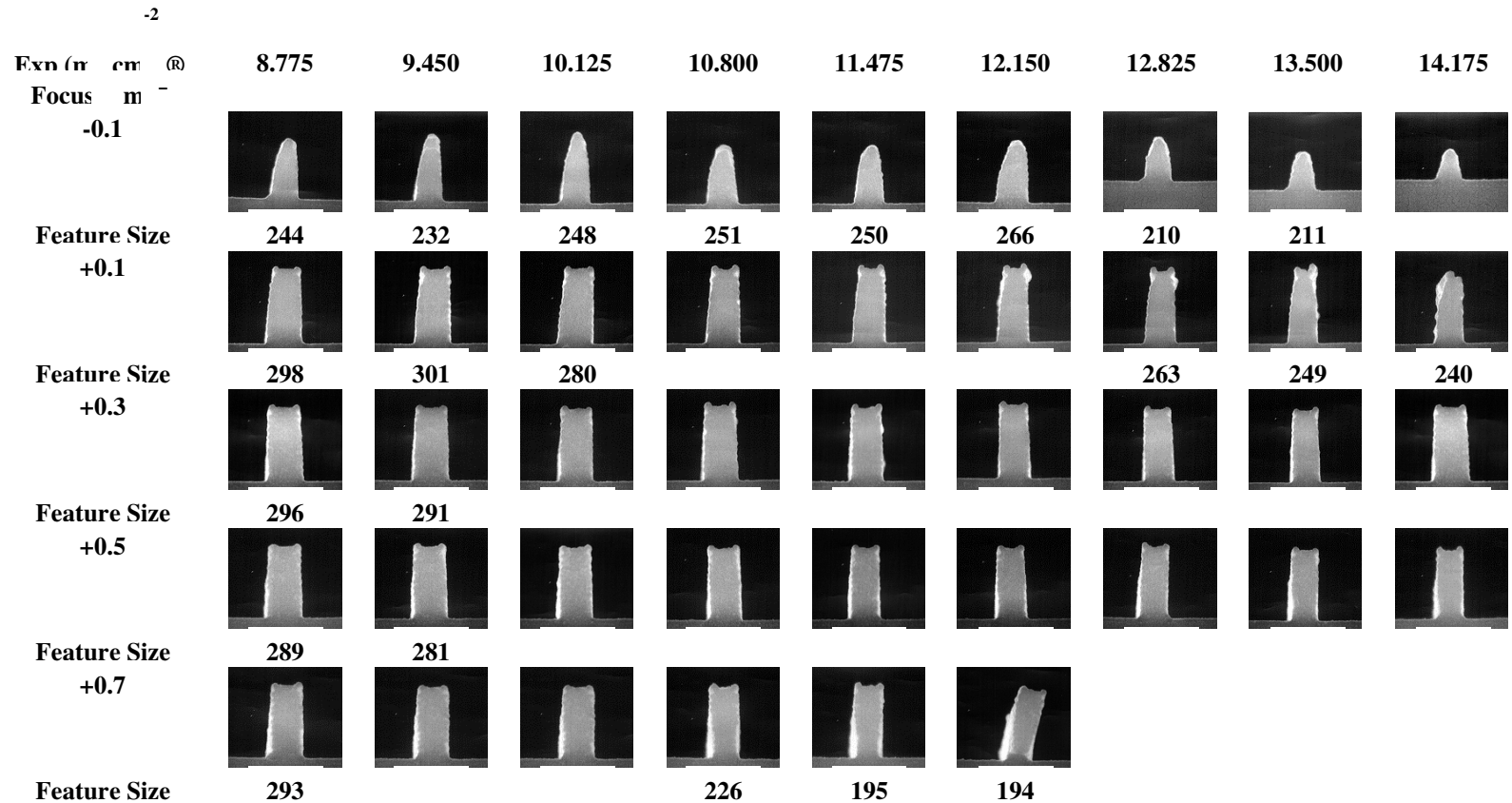
Rafi Kleiman

Focus / Exposure Matrix

A routine setup metrology requirement

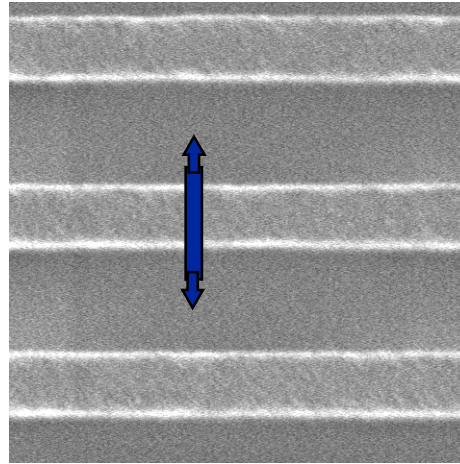
Nominal Feature
225nm Isolated

250 nm isolated lines



Lithography Metrology

Improve CD-SEM thru 100 nm node



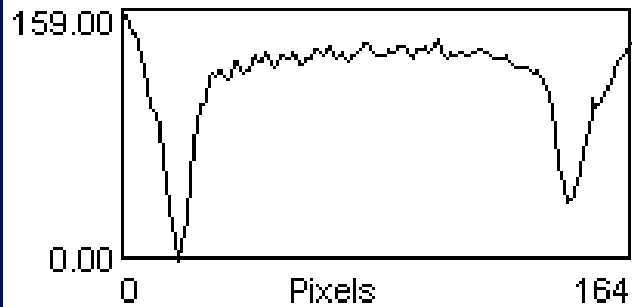
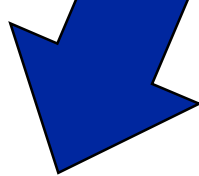
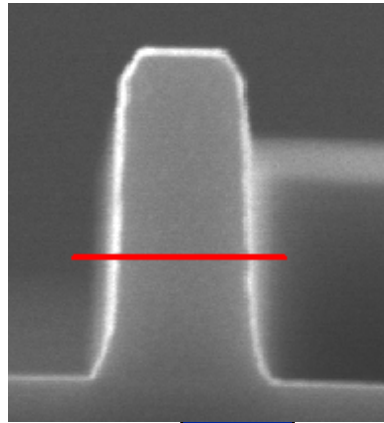
**top down
CD-SEM**

2D / 3D Information

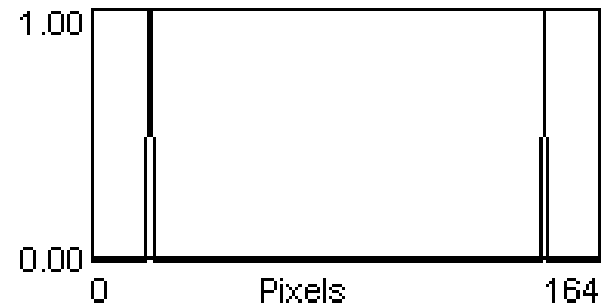
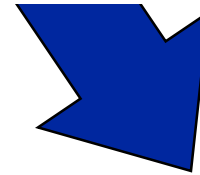
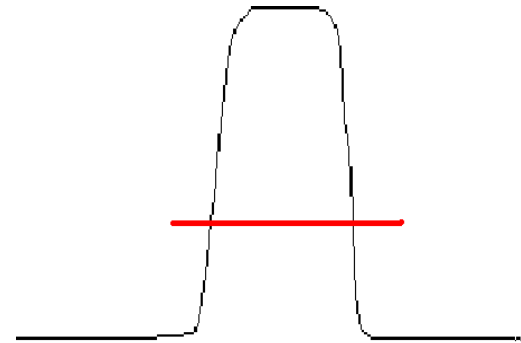
NEED: Determine CD from Fundamental Model

Intensity Profiles From SNP / SEM

SEM



SNP



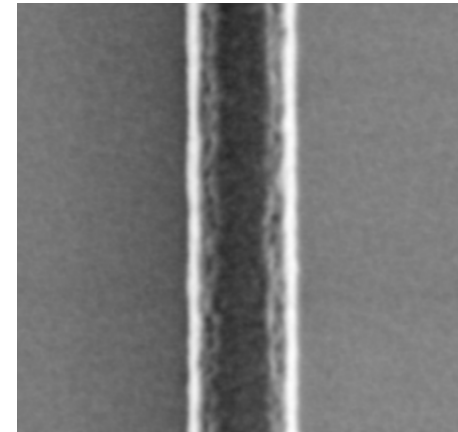
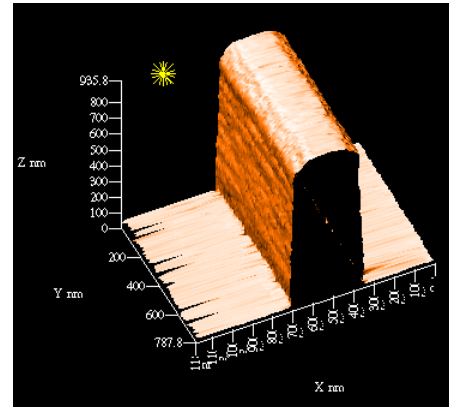
Thanks to Joe Griffith

Microscopy Issues:

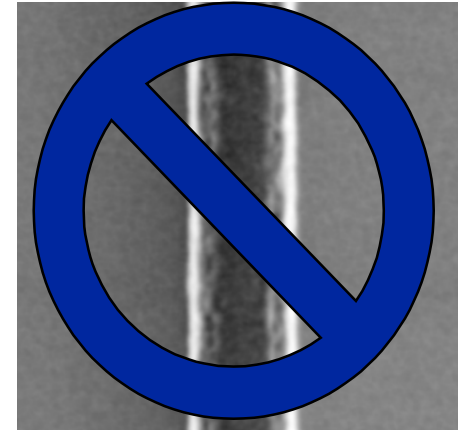
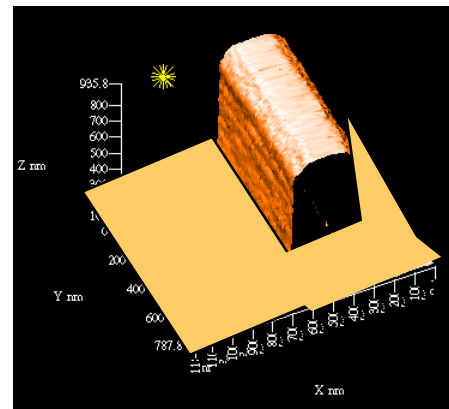
CD and Detection require
new microscopy

- SEM with resolution required for sub 100 nm has **poor Depth of Focus**
- 3D Information Required
- Improved throughput required

SEM

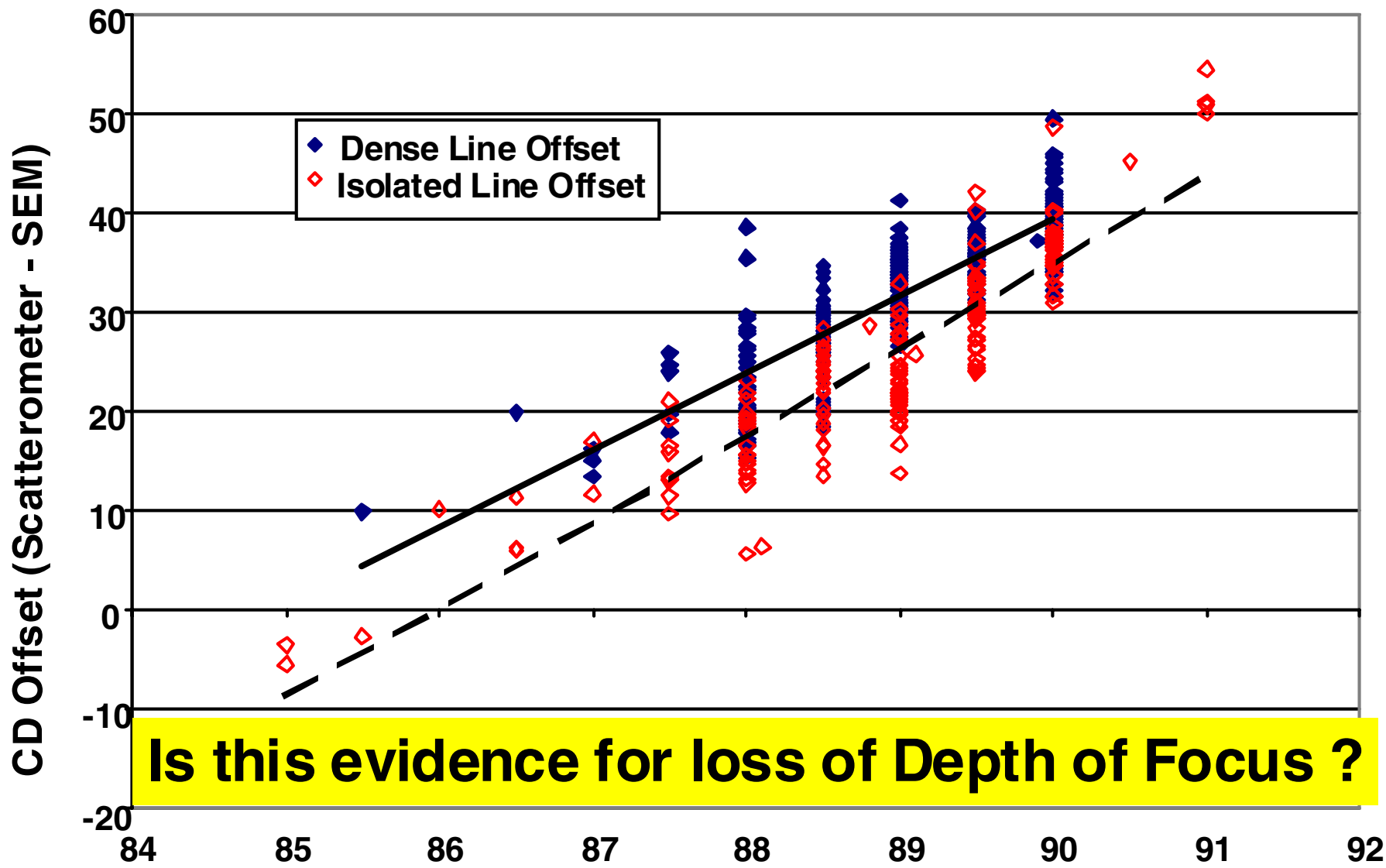


Today : Depth of focus > 1 micron







**With Future Resolution:
Depth of focus << 1 micron**

Offset from CD-SEM by Angle

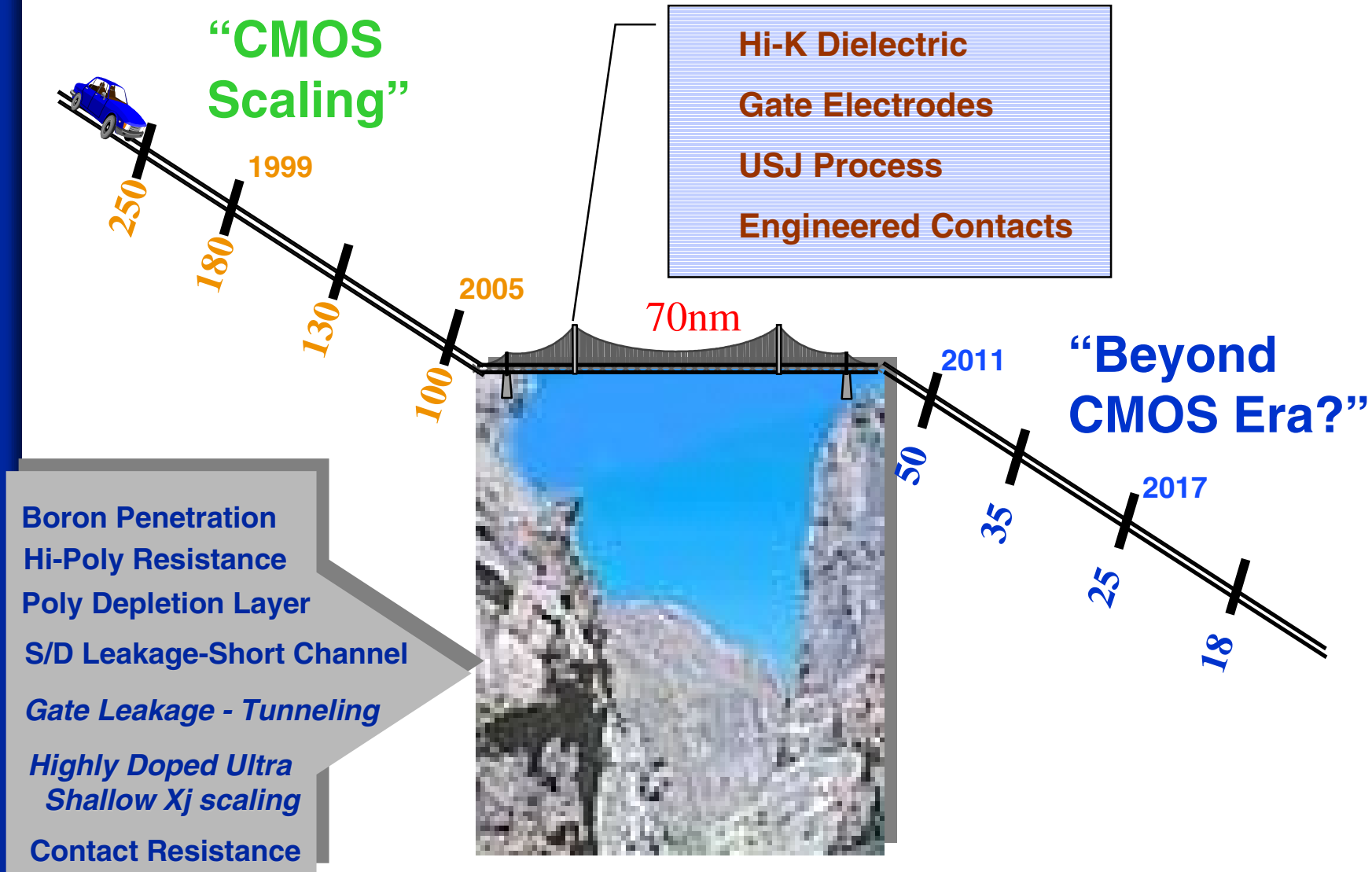


Is this evidence for loss of Depth of Focus ?

AGENDA

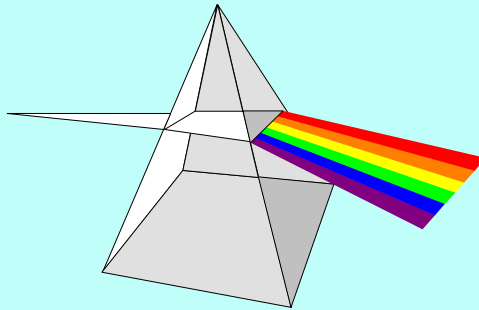
- ITRS Overview
- Metrology Roadmap Overview 
- Lithography Metrology 
- Front End Processes Metrology & New Structures from PIDS 
- Interconnect Metrology 
- Integrated Metrology
- Materials & Contamination Characterization
- The Future

Key FEP CMOS Scaling Challenges



Impact of New FEP Materials

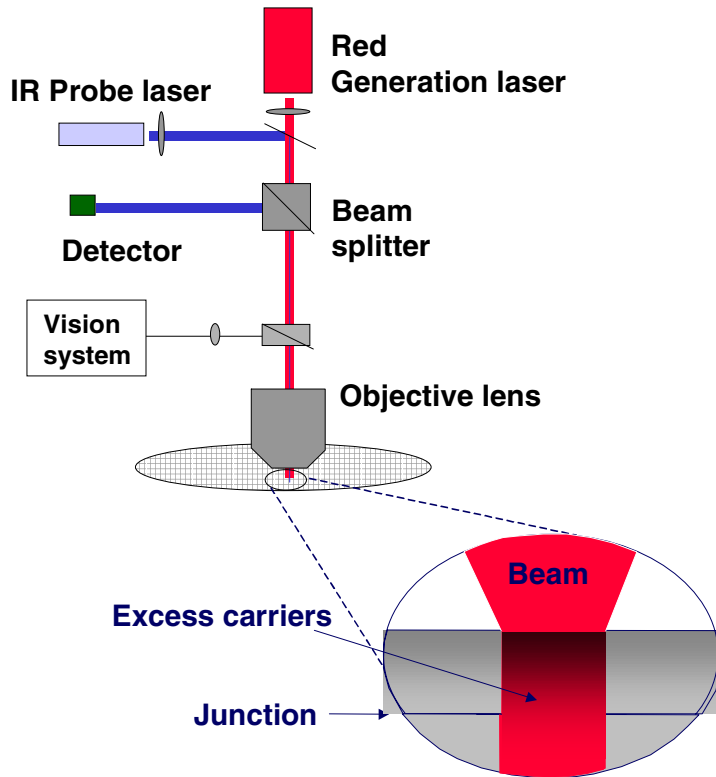
Issue:
**Control of Oxynitride, Silicon dioxide/Silicon nitride stacks
and high k with oxynitride interfacial layers**



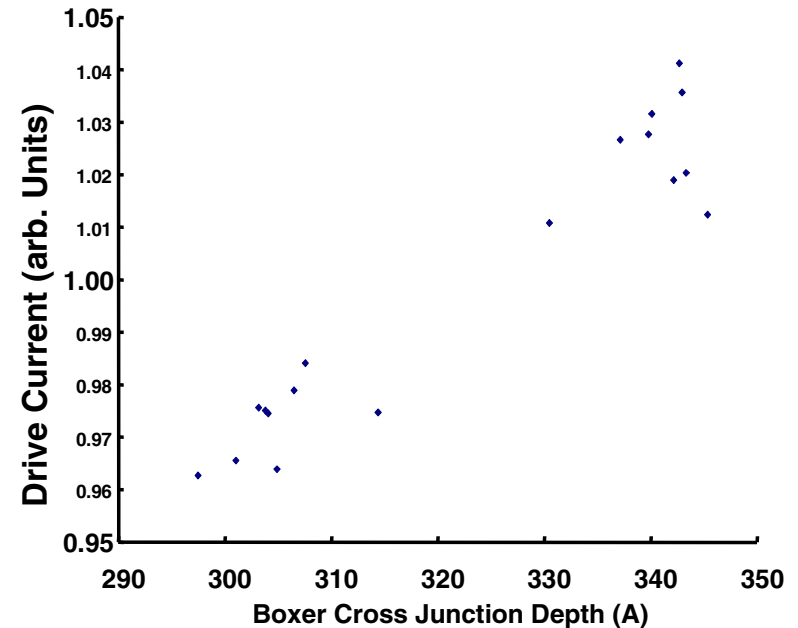
Should Future In-Line Ellipsometers include IR or VUV

Junction Depth Measurement in the FAB

Carrier Illumination



Correlation to drive current (0.18 μm NMOS)



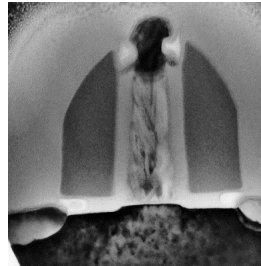
AMD and Boxer-Cross

Example of new technology from a Startup : Boxer-Cross

Transistor Evolution ?

Device
Structure
Size

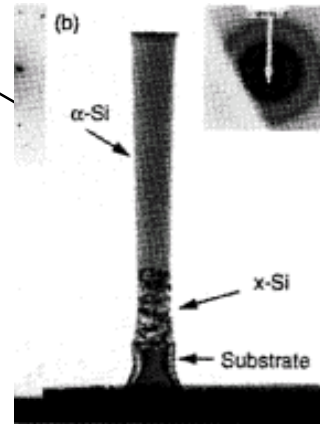
Planar
CMOS



Sub 50nm ?

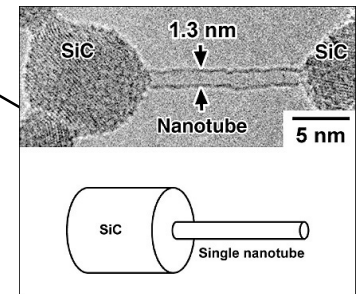
0 - 7 years.

Non-Planar
CMOS



7 - 12 years

New Switch
Structure



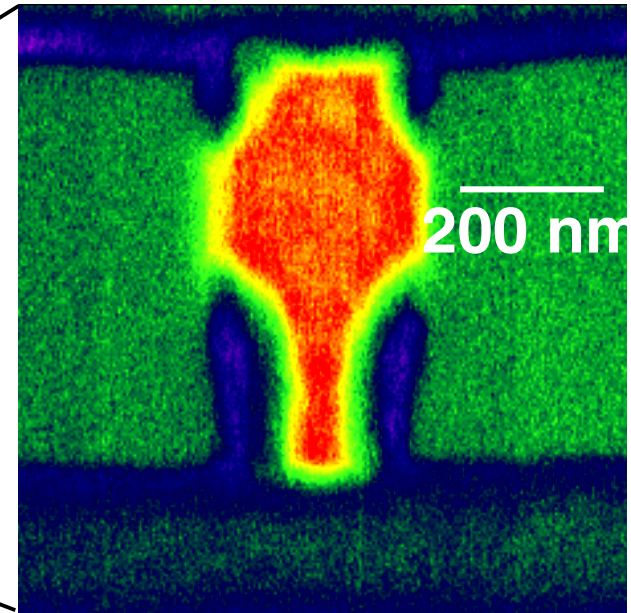
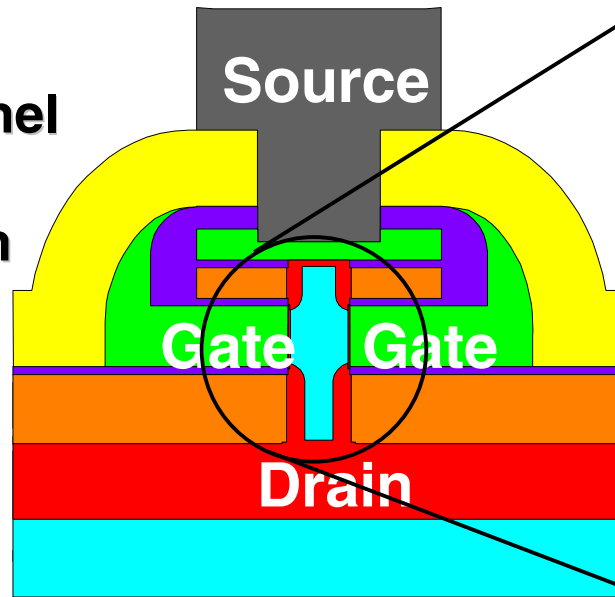
12 + Years.

TIME →

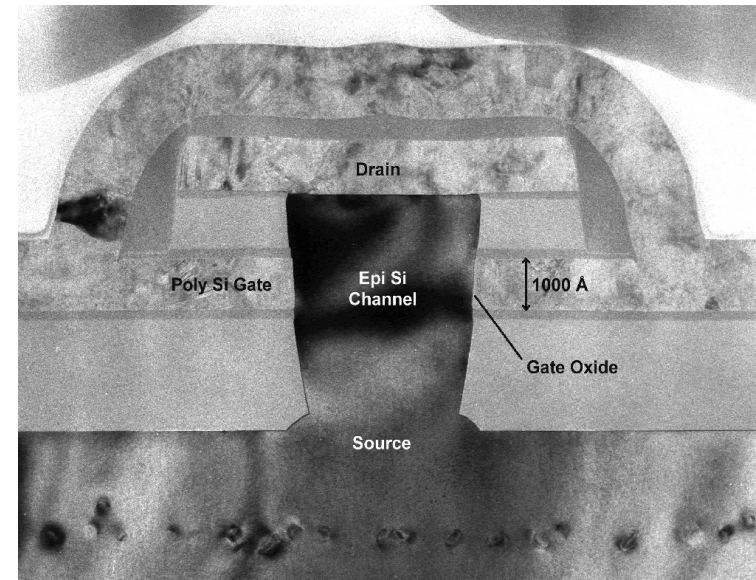
Transistor and Capacitor Metrology

New Transistor Designs vs Metrology

- Vertical, dual channel Transistor sub 100nm



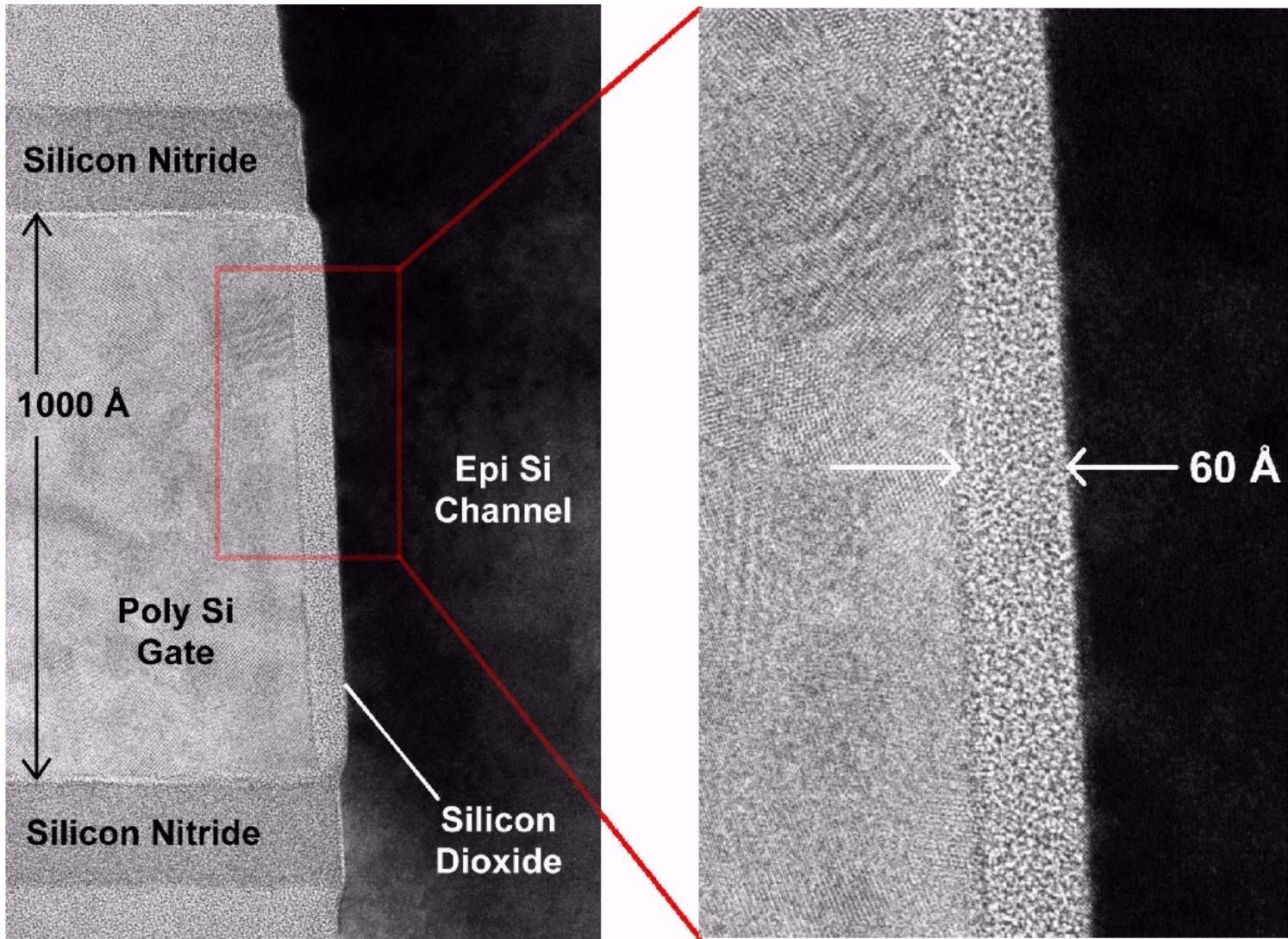
- CD done by film thickness
- Doping in LDD by diffusion



Rafi Kleiman (Lucent)

Transistor and Capacitor Metrology

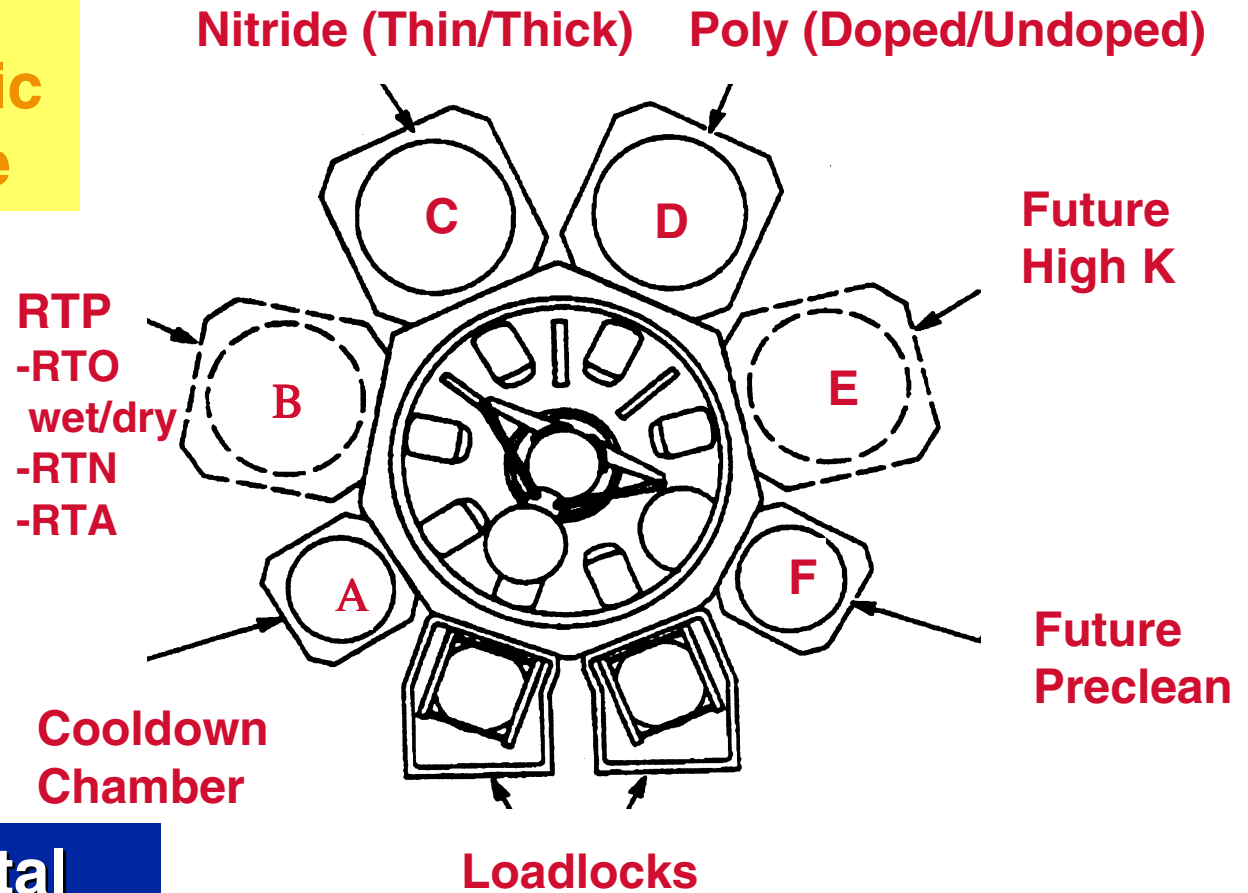
Vertical Transistor : Gate Dielectric is vertical



Front End Process Metrology





In-Situ Needs vs Integrated Metrology Trend

Clustered
gate dielectric
& electrode

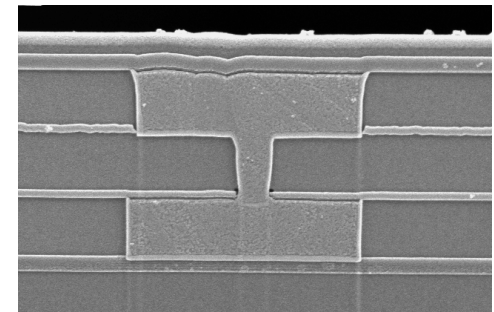
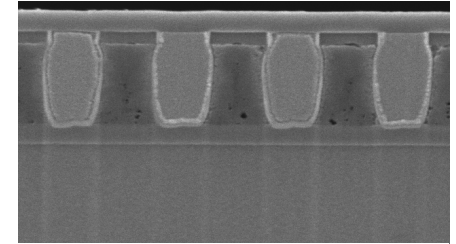
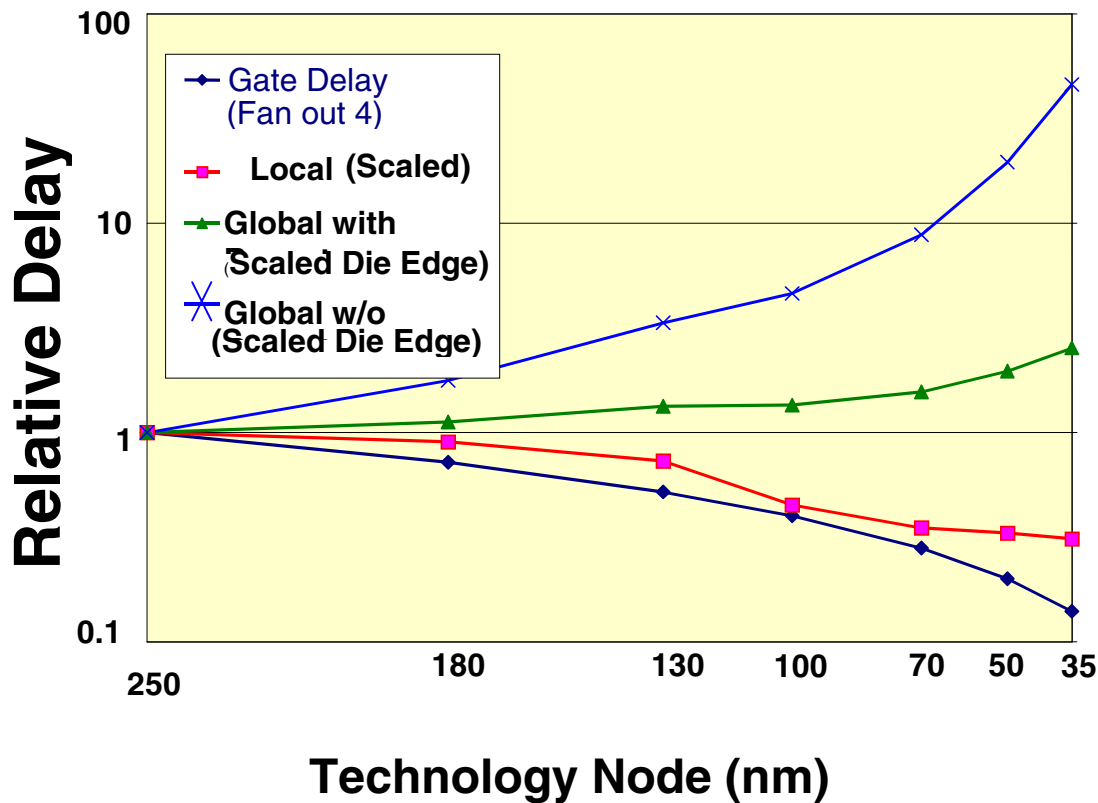


e.g., Metal
Gate forces in-
situ metrology
for dielectric

AGENDA

- ITRS Overview
- Metrology Roadmap Overview 
- Lithography Metrology 
- Front End Processes Metrology 
- **Interconnect Metrology** 
- Integrated Metrology
- Materials & Contamination Characterization
- The Future

Interconnect Challenges due to Clock Frequency: How long will Copper / low k work?

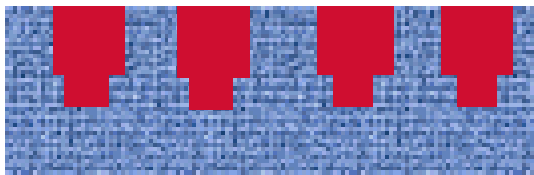


Low k / barrier
etch stop / low k

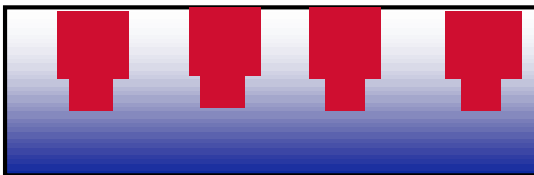
Impact on Metrology

Thickness Measurement
New Optical Models
for each low κ stack

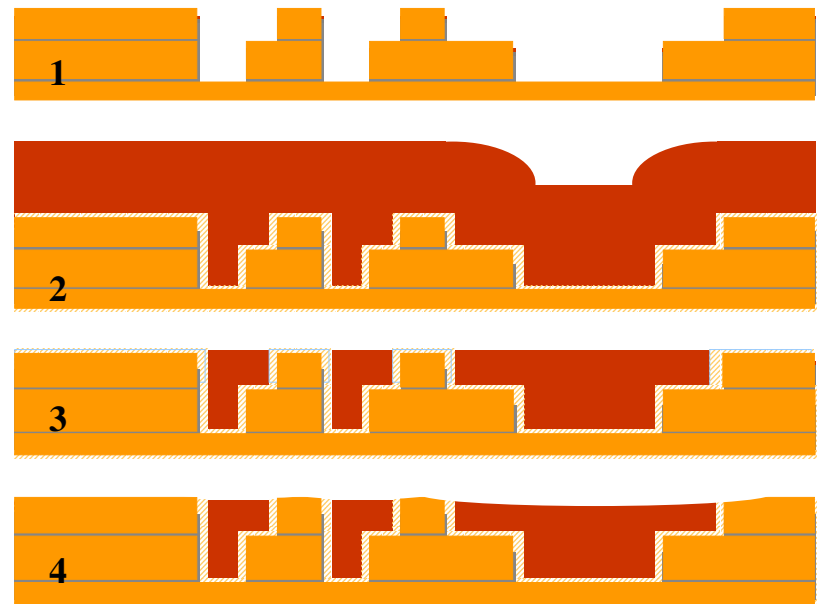
CMP Control
R&D for each new
low κ stack



Low κ Porosity



Gradient in % Porosity



Metal Film Thickness and CMP Control

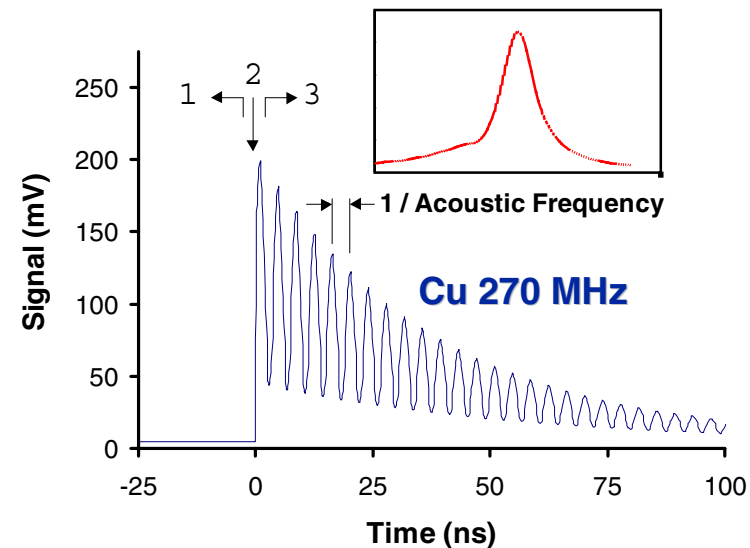
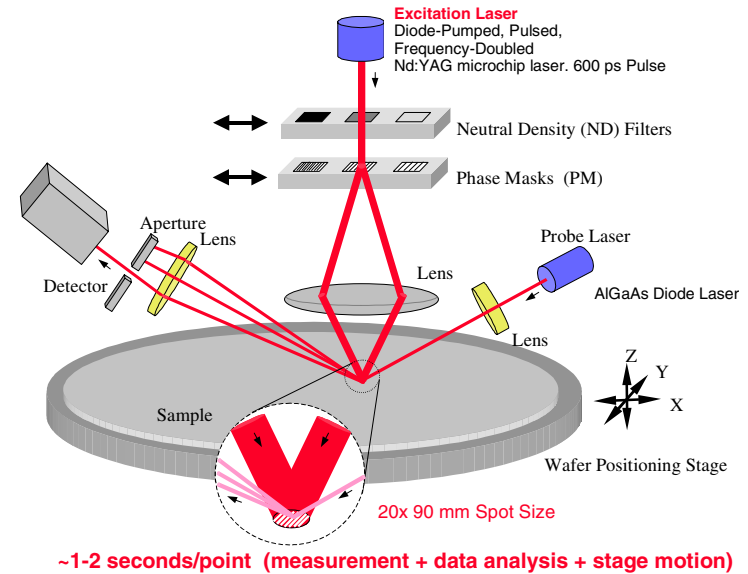
3 methods

- ISTS

- Picosecond Ultrasonics

- X-ray Reflectivity

- Near Future :
Patterned Wafer Capability
through better modeling



Depth of Focus Requirements for Litho

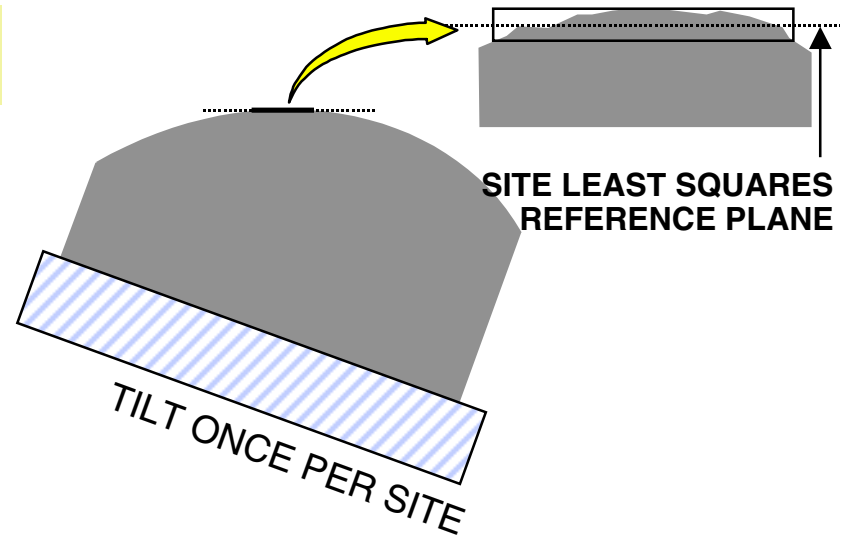
CMP Metrology tool should measure what litho tool “sees”

Full Field Steppers

SEMI STD

Site Frontside
least-sQuared
site reference

Range =
SFQR
Deviation =
SFQD

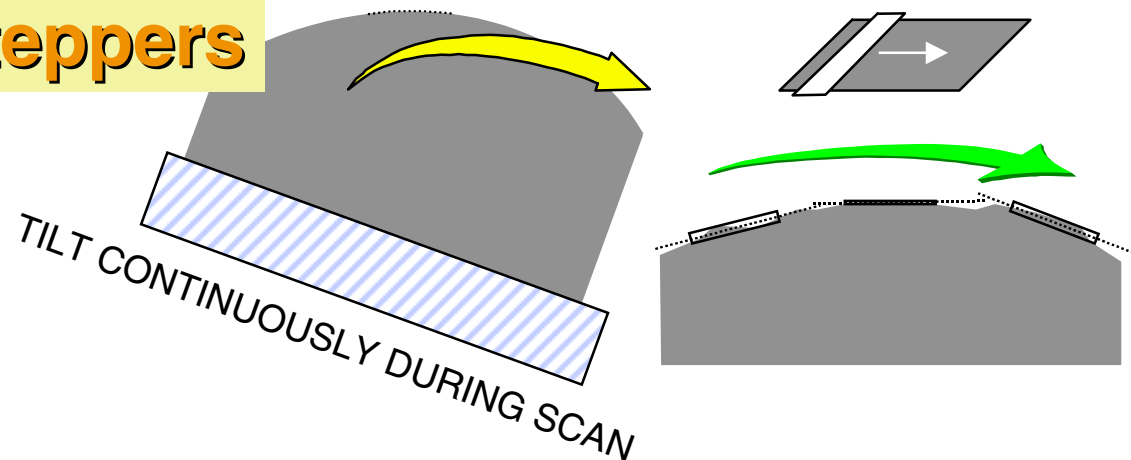


Scanning Steppers





SEMI STD

Site Frontside
Scanning*
site reference

Range = SFSR
Deviation = SFSD



AGENDA

- ITRS Overview
- Metrology Roadmap Overview 
- Lithography Metrology 
- Front End Processes Metrology 
- Interconnect Metrology 
- **Integrated Metrology**
- **Materials & Contamination Characterization**
- **The Future**

SENSOR based Integrated Metrology

Comments on :

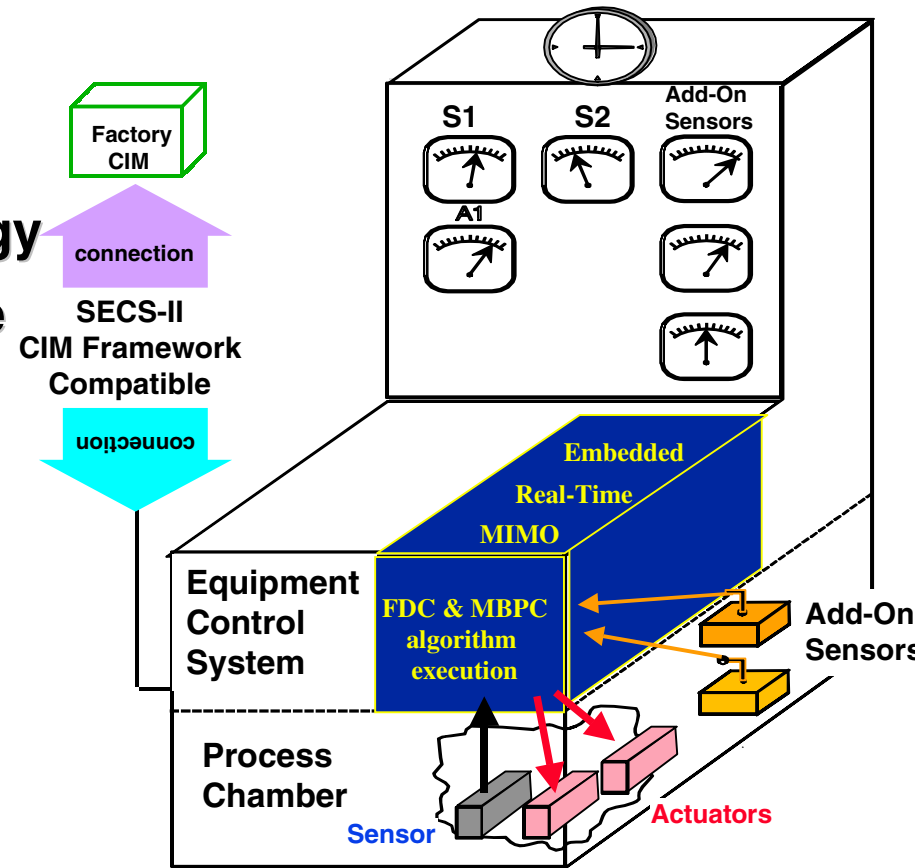
Advanced Process Control - Advanced Equipment Control

➤ AEC/APC GOAL :

model based predictive control
based on process and metrology
models using in-situ and in-line
measurements

➤ Momentum Shift ?

➤ Now suppliers advocate
Integrated Metrology



AGENDA

- ITRS Overview

- Metrology Roadmap Overview



- Lithography Metrology



- Front End Processes Metrology



- Interconnect Metrology



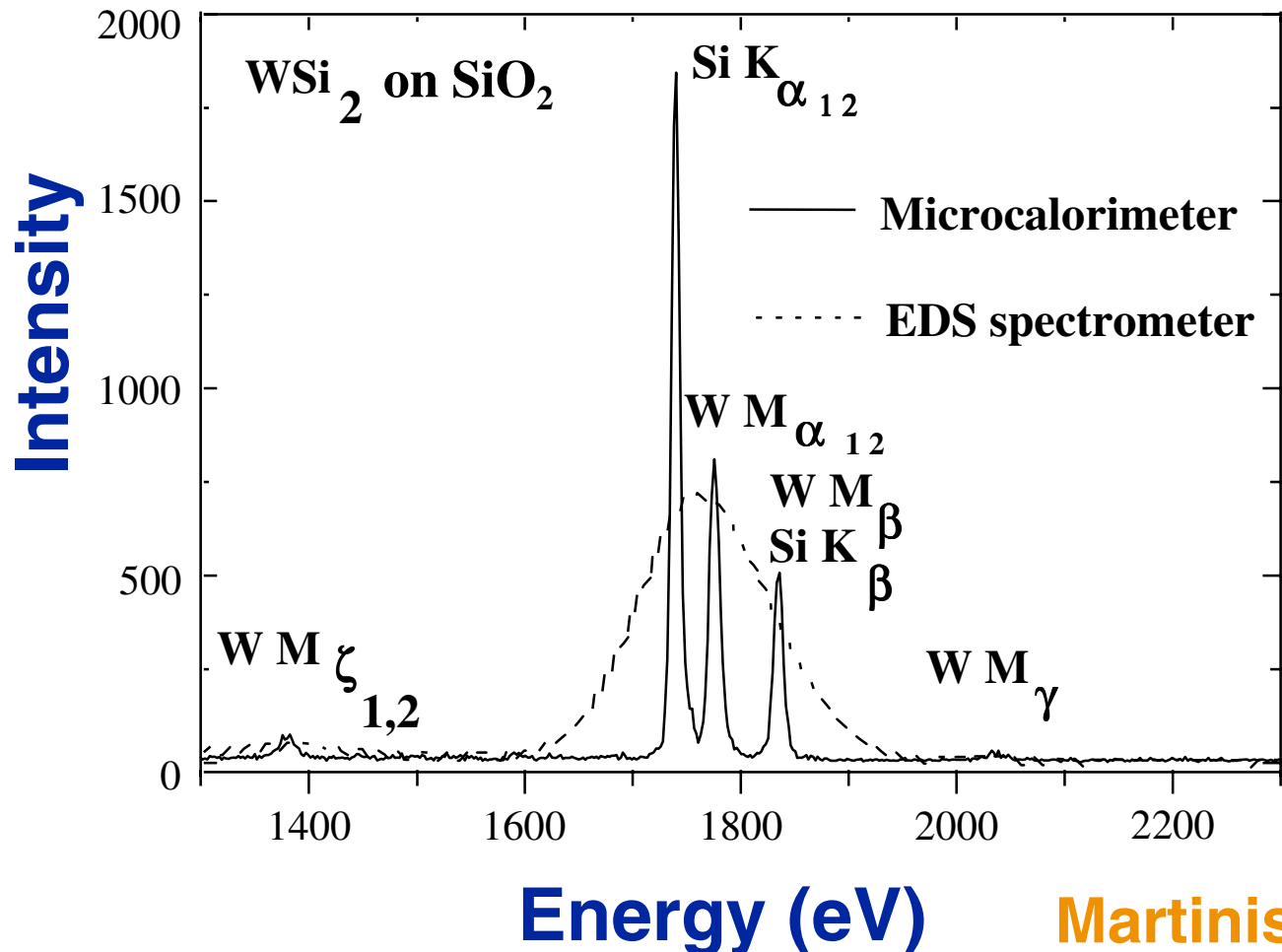
- Integrated Metrology

- **Materials & Contamination Characterization**

- The Future

New Microcalorimeter X-ray detector

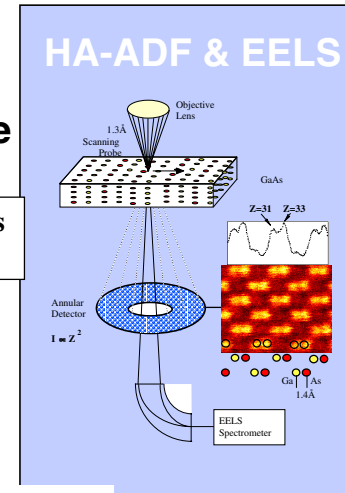
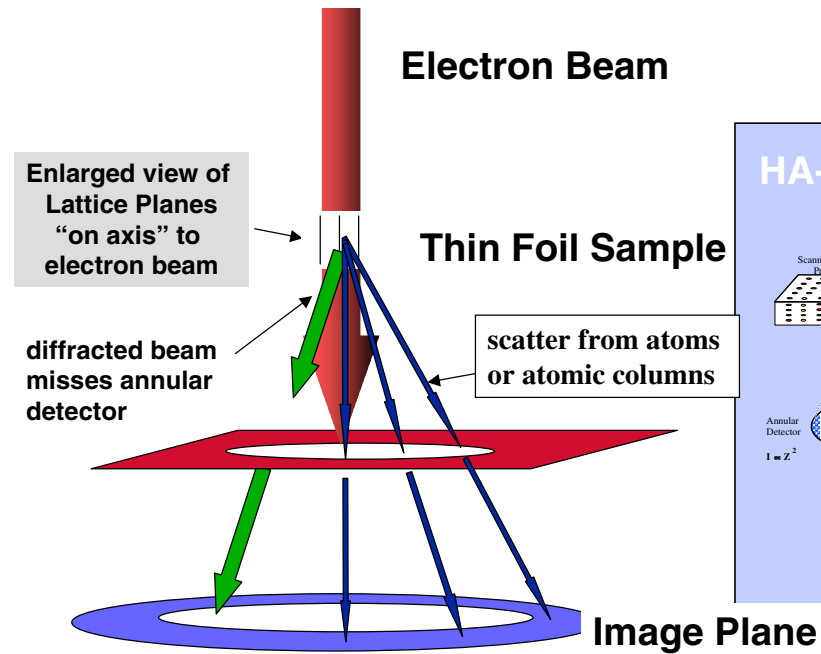
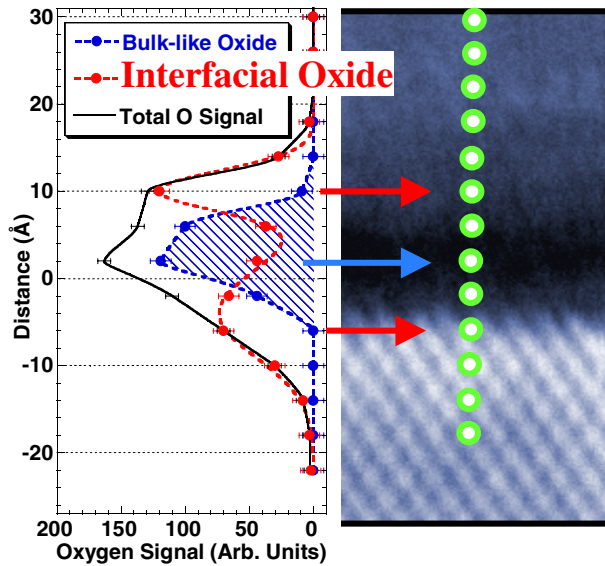
Industry needs accelerated commercialization



Martinis, Woolman
et al. NIST

Electron Energy Loss & HA-ADF STEM Interfacial State changes in O and Si K edge

High Angle - Annular Dark Field STEM

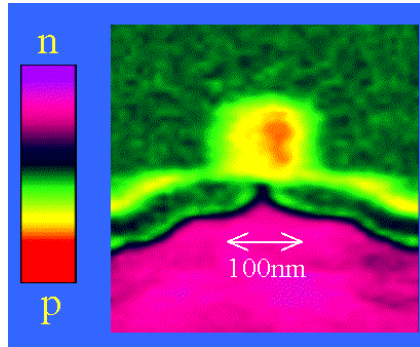


Dave Muller - Lucent
in G. Temp et al, IEDM 98, p615

2D Dopant Profiling

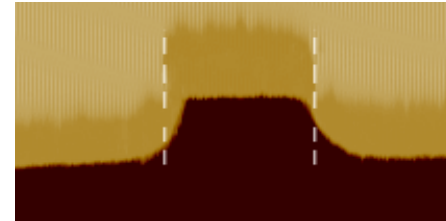
Requires Improved Spatial Resolution

SCM

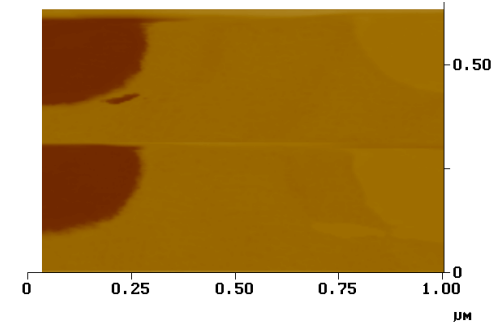


R. Kleiman - Lucent

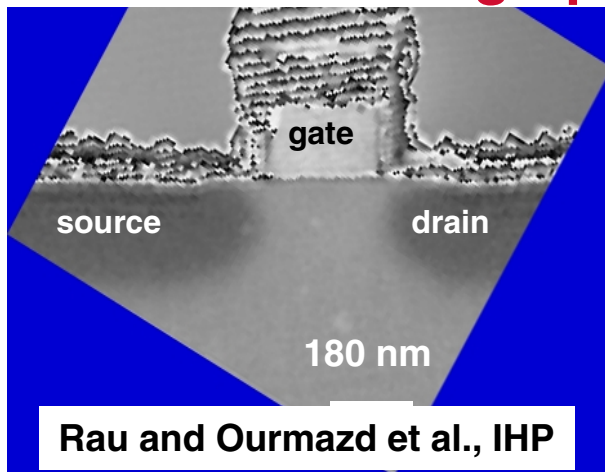
SSRM



Nanopotentiometry

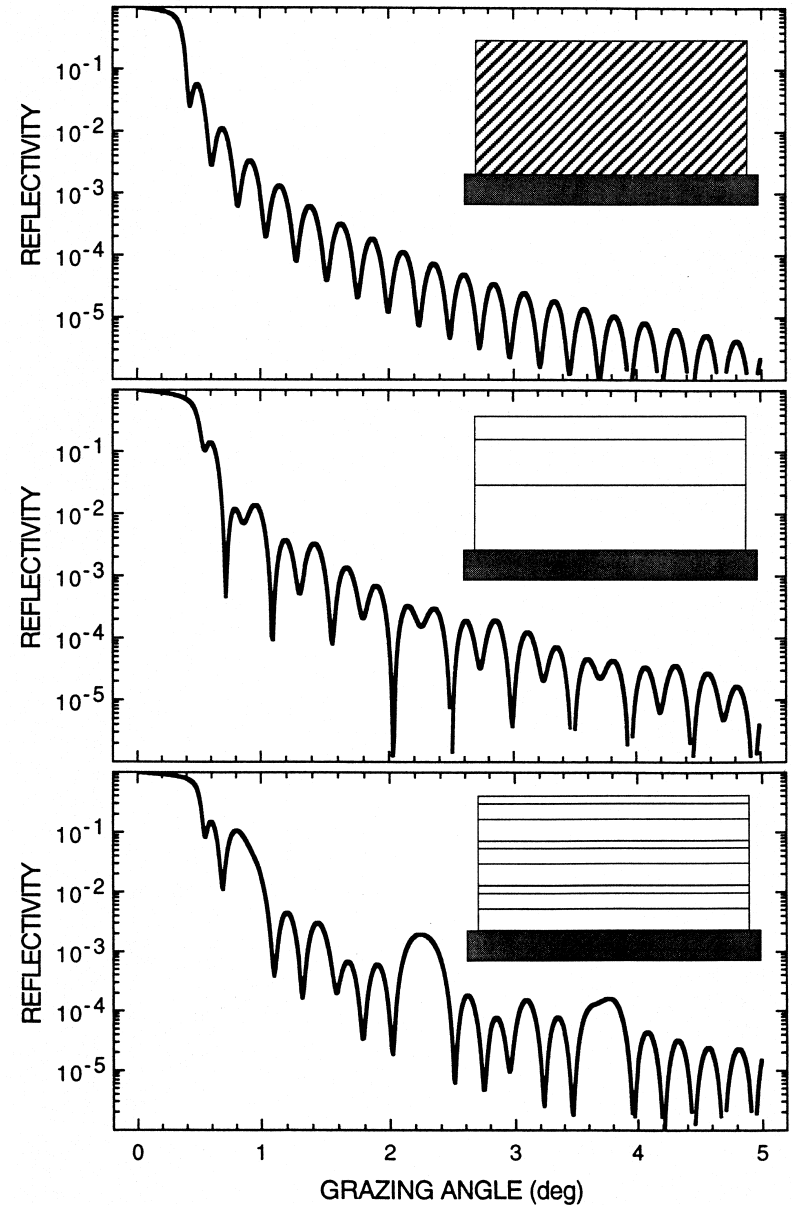
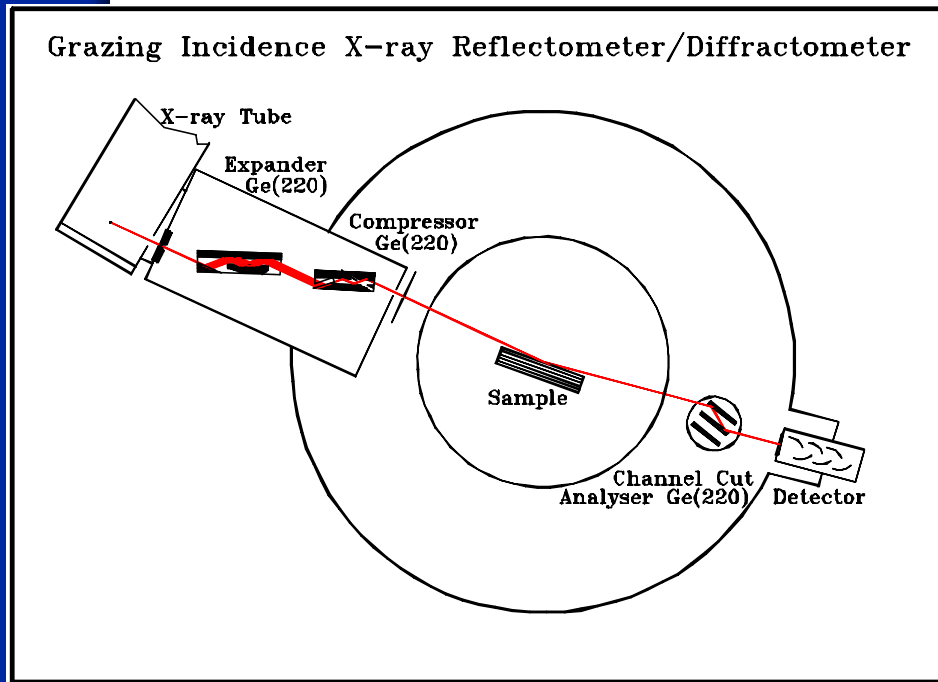


TEM Electron Holography







IMEC - W. Vandervorst

GI-XRR at NIST - R. Deslattes, et al



AGENDA

- ITRS Overview
- Metrology Roadmap Overview 
- Lithography Metrology 
- Front End Processes Metrology 
- Interconnect Metrology 
- Integrated Metrology
- Materials & Contamination Characterization
- The Future

Metrology Funding Types

~10%

Innovation Driven

- Entrepreneurial
- **High Market Risk**
- Longer Dev. Time
- Can precede requirement
- “Classic funding”
- **Self Risk Mitigation**

~30%

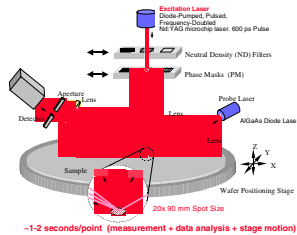
Application Driven

- Equipment Supplier “Customer” Driven
- **Medium Market Risk**
- Shorter Dev. Time
- Specific Process requirement
- Joint funding with Process tool supplier
- **Co-Risk Mitigation**

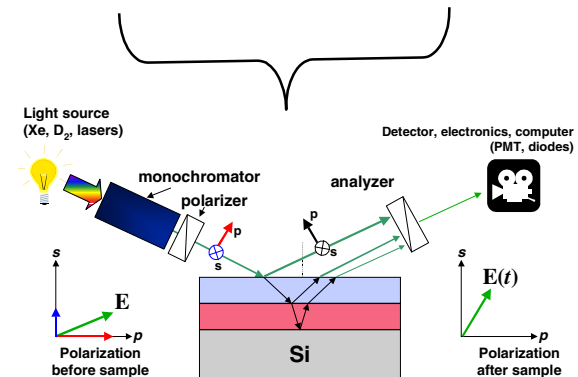
~ 60%

Market Driven

- ex post facto IC “Customer” Driven
- **Low Market Risk**
- Market Window
- Specific Process requirement
- Possible Joint funding with IC Manufacturer
- **Self Risk Mitigation**



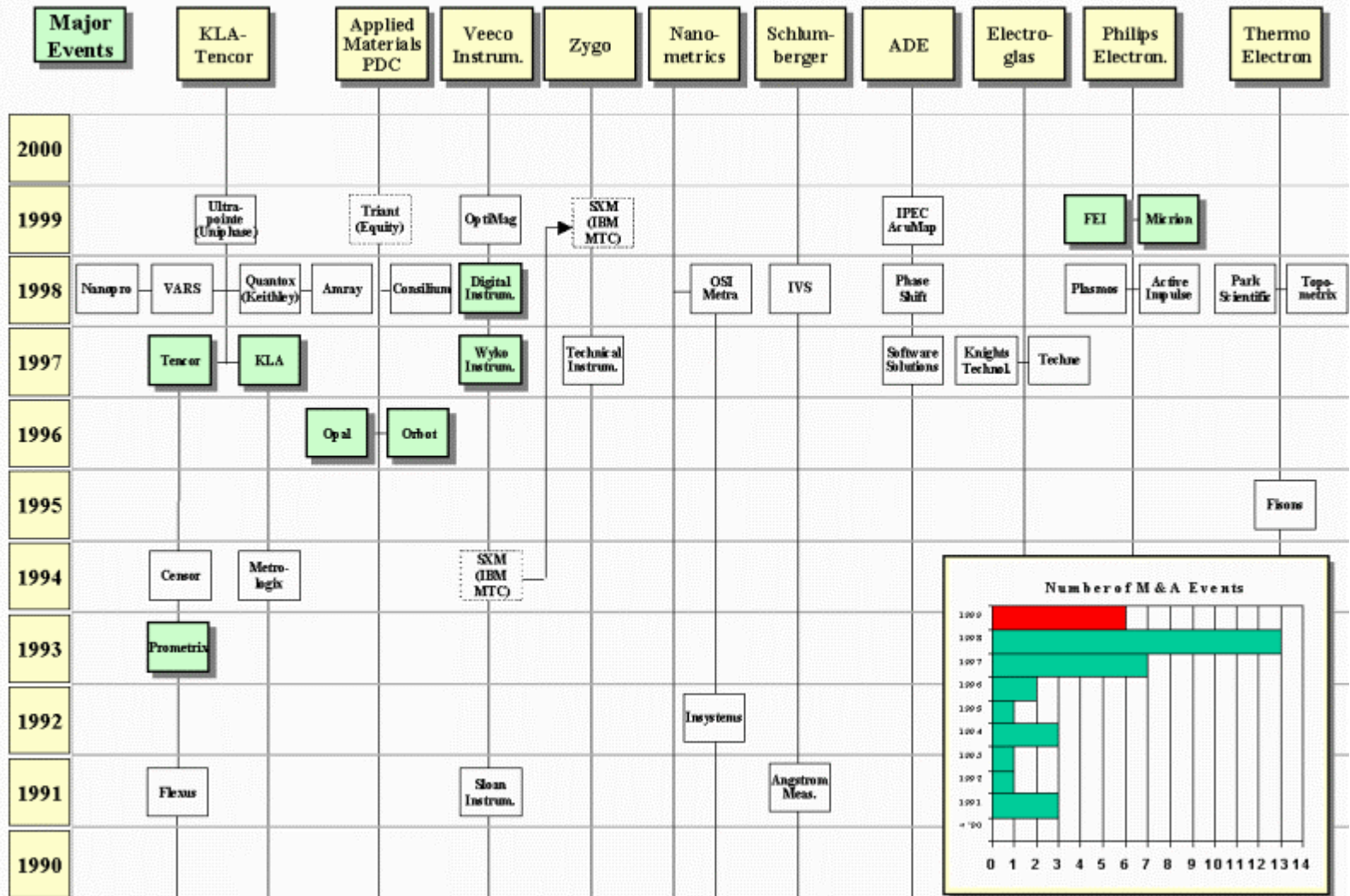
**Barrier/Metal Thickness
ISTS
&
Picosecond acoustics**



157 nm ellipsometry

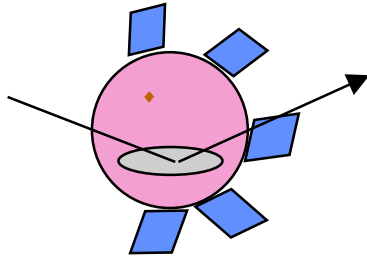
Will Market Risks allow for innovation?

◆ Metrology M&A's Have Slowed in 1999

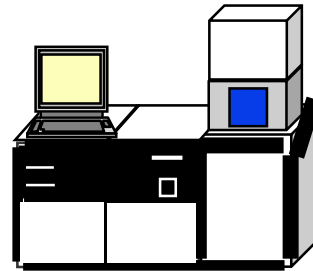


Dave Perloff - Veeco

IN-SITU



IN-LINE



OFF-LINE / AT-LINE



2000 Metrology Roadmap

Europe

**Alec Reader (Philips)
Wilfried Vandervorst (IMEC)**

Japan

Fumio Mizuno (Hitachi)

Taiwan

**Henry Ma (EPISIL)
George Yen (ProMOS)**

US

**Bob Scace (NIST)
Alain Diebold (SEMATECH)**

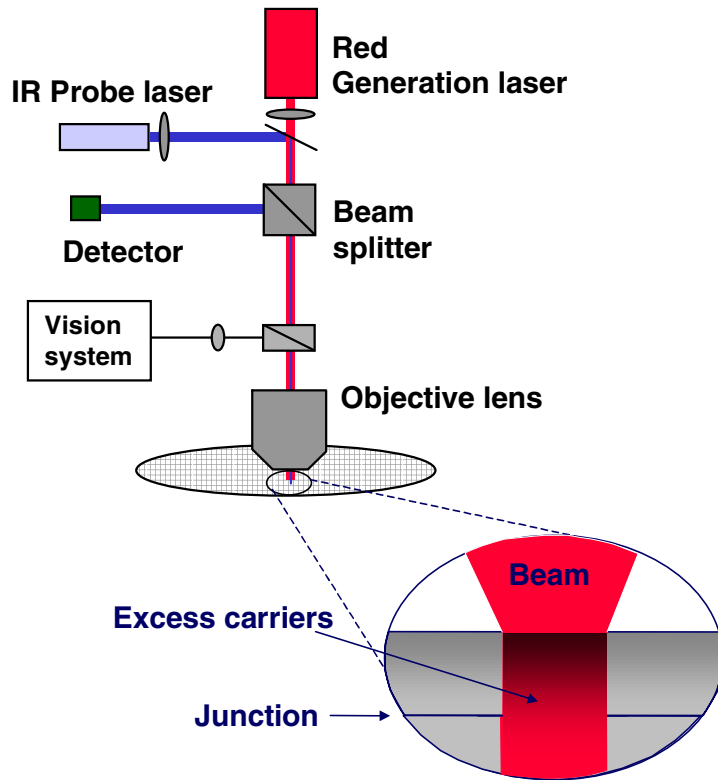
Acknowledgements

- **Will Chism, Jesse Canterbury, Lizz Judge**
- **Curt Richter and countless others at NIST**
- **US Metrology TWG**
- **Metrology and Analytical Lab Managers Councils**
- **ISMT Litho images - Dan Holladay**
- **Images of Litho tools - John Canning and Chris Van Peski - International SeMaTech**
- **FEP overhead - Mike Jackson, Howard Huff, Ed Strickland, Rinn Cleavelin**

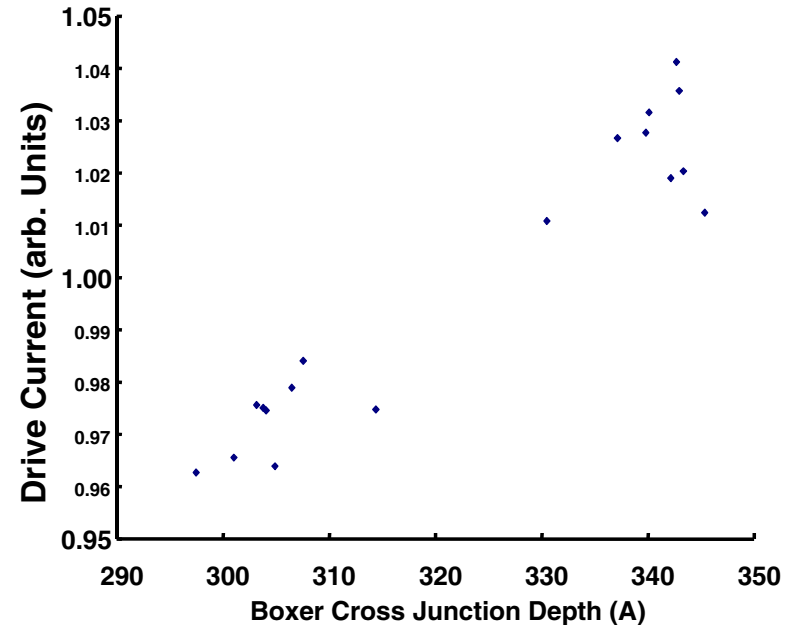


Junction Depth Measurement in the FAB

Carrier Illumination



Correlation to drive current (0.18 μm NMOS)



AMD and Boxer-Cross

Example of new technology from a Startup : Boxer-Cross