Testing and analysis for multiple PID mechanisms and stresses

Peter Hacke, NREL

PVQAT – TG3: Humidity Temperature Voltage

- Crystalline Silicon PID
  - Shunting: PID-s
  - Delamination: PID-d
- Thin film PID
  - Test method consideration
  - TCO corrosion
- Combined-stress cycle for better characterization of PID and other degradation mechanisms

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62804-1 PHOTOVOLTAIC (PV) MODULES – TEST METHODS FOR THE DETECTION OF POTENTIAL-INDUCED DEGRADATION Part 1: Crystalline Silicon

Procedures to test and evaluate the durability of crystalline silicon photovoltaic (PV) modules to the effects of short-term high-voltage stress including potential-induced degradation (PID)

PID-shunting (PID-s) & Polarization

Test methods

a) Testing in damp heat using an environmental chamber

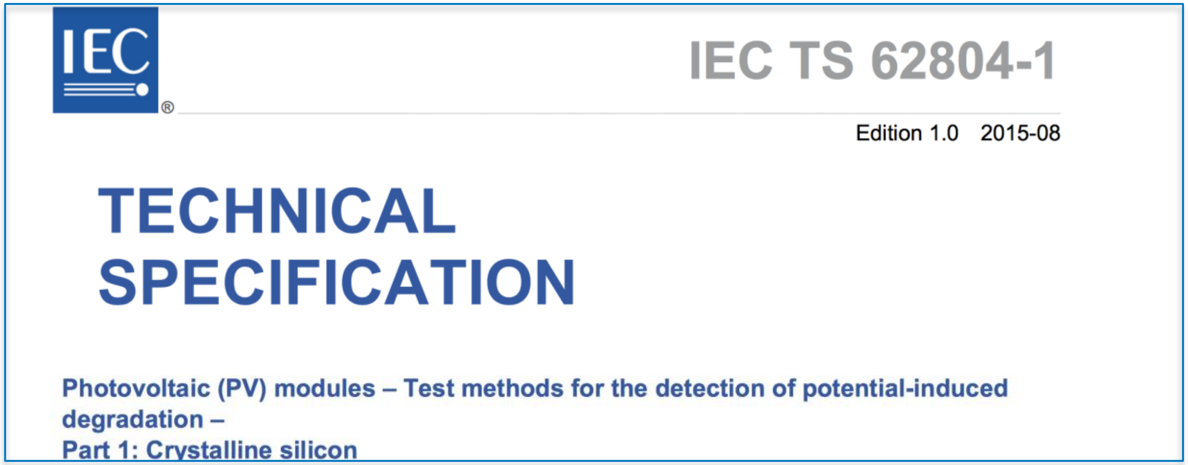
severities represent the minimal stress levels for detection of PID

- **60°C / 85% RH / + & – V_{sys} 96 h**
- **65°C and 85°C for further acceleration**

b) Testing in dry using Al foil

severities represent the minimal stress levels for detection of PID

- **25°C / <60% RH / + & – V_{sys} 168 h**
- **50°C and 60°C for further acceleration**



IEC TS 62804-1

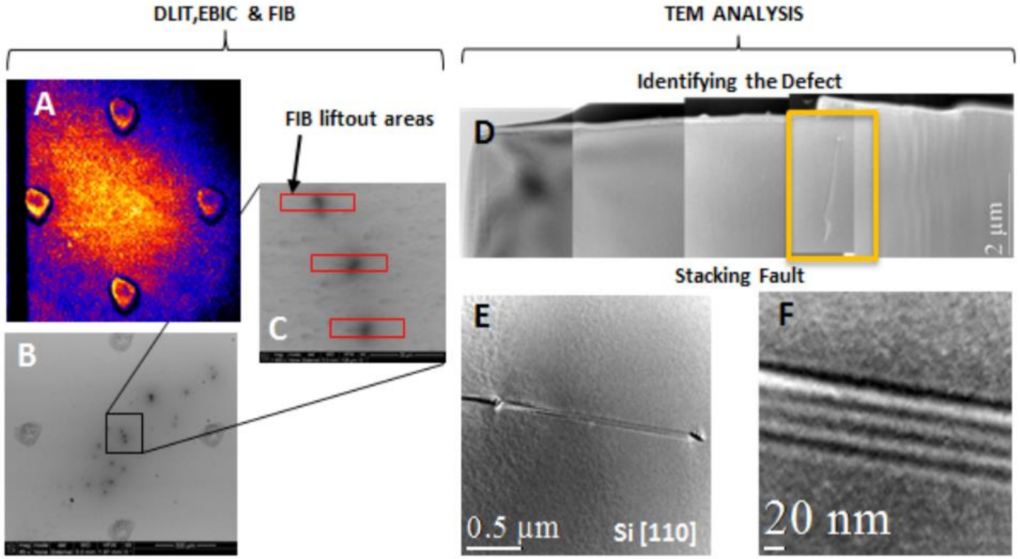
Edition 1.0 2015-08

TECHNICAL SPECIFICATION

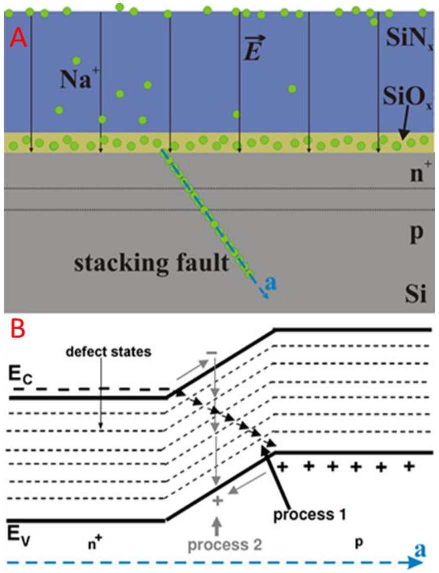
Photovoltaic (PV) modules – Test methods for the detection of potential-induced degradation –
Part 1: Crystalline silicon

Potential-induced degradation: PID-shunting, Polarization

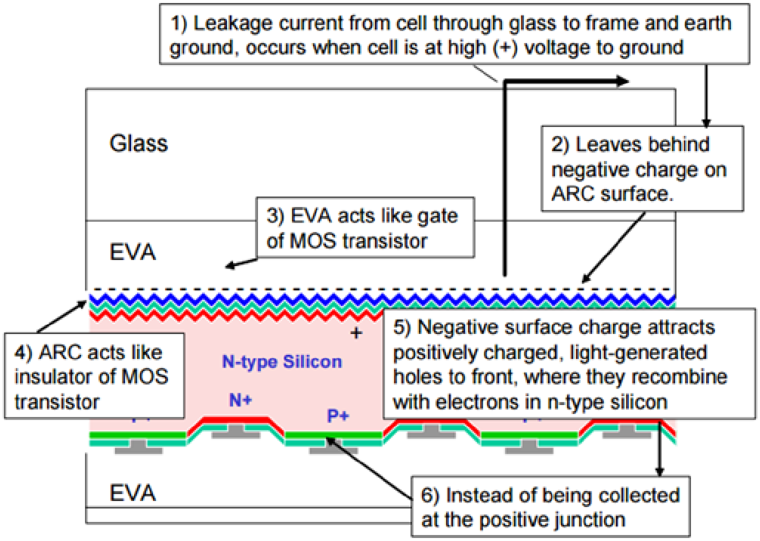
PID-shunting Na^+ drift + diffusion through stacking faults



Harvey, Mosely, Hacke, Norman, Johnston (NREL)



Naumann, Lausch, Hähnel, Breitenstein, Hagendorf, FrCSP



1) Leakage current from cell through glass to frame and earth ground, occurs when cell is at high (+) voltage to ground

2) Leaves behind negative charge on ARC surface.

3) EVA acts like gate of MOS transistor

4) ARC acts like insulator of MOS transistor

5) Negative surface charge attracts positively charged, light-generated holes to front, where they recombine with electrons in n-type silicon

6) Instead of being collected at the positive junction

PID-polarization

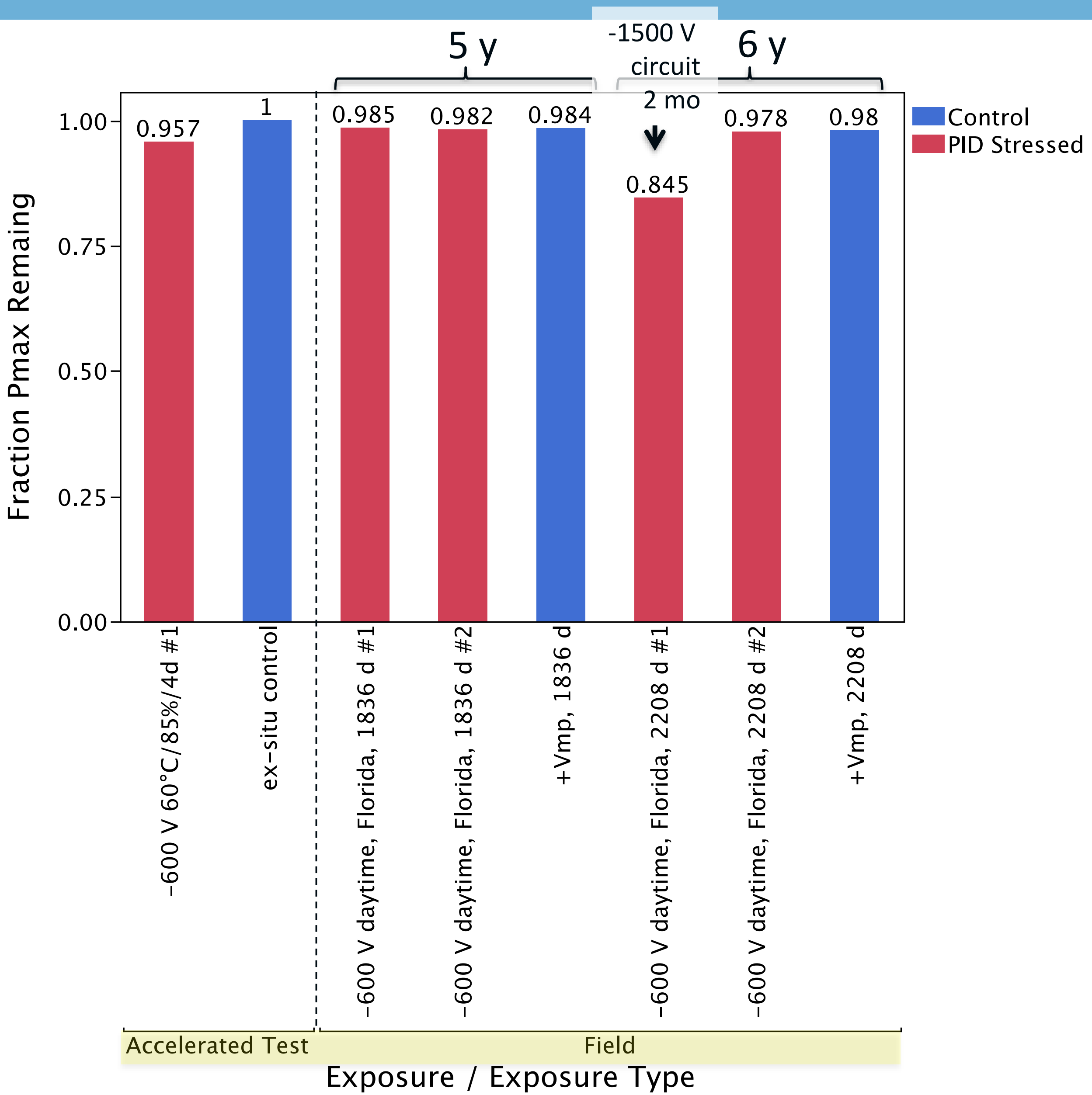
Charges in the passivation layer (SiN$_x$, SiO$_2$, Al$_2$O$_3$) attract minority carrier

60°C/95%RH/96h/-Vsys test versus 5 & 6 years in the field

- **C-Si modules** exposed to -600 V/ 60°C/85%RH/96 h (4 d) degraded 4.3 %.
- Fielded replicas in Florida (-600 V variable, daytime) show no degradation in 1836 d (5 y).
  - Degradation in 2208 d (6 y).

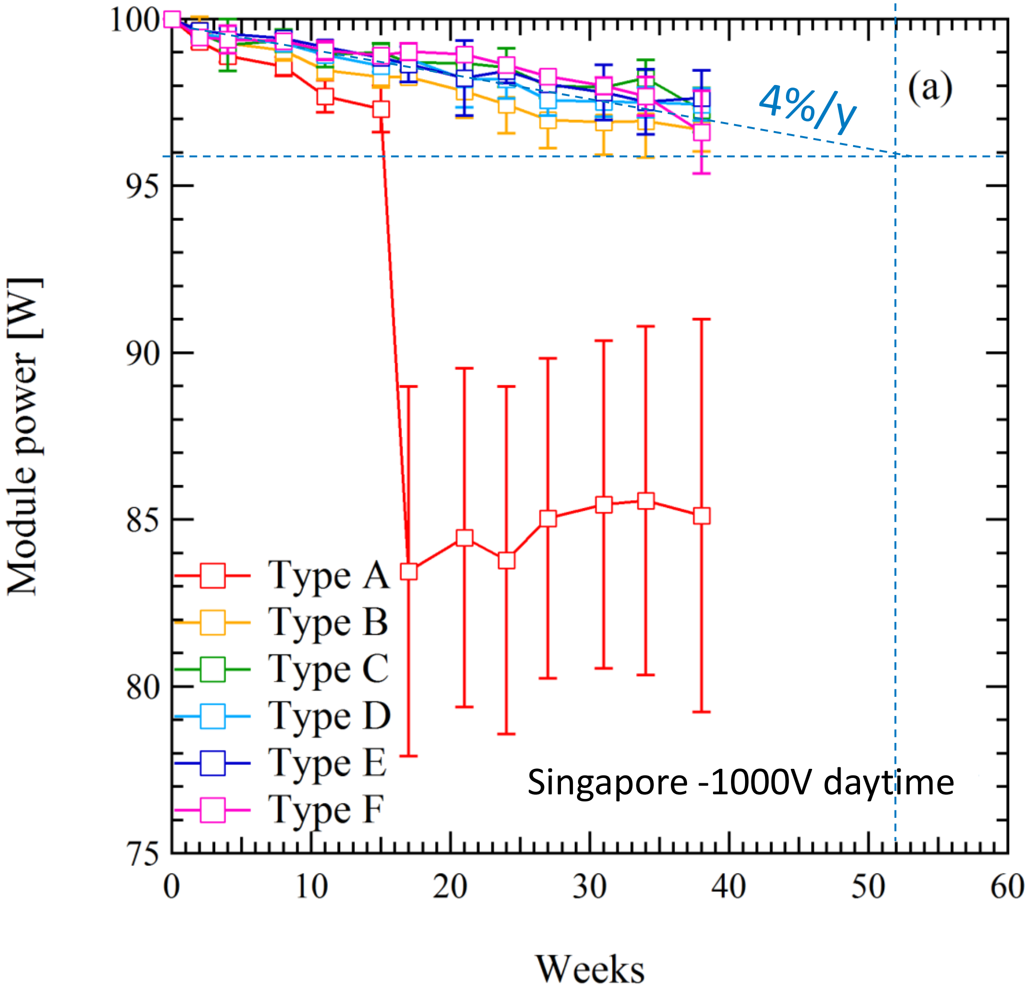
60°C/95%RH/96h/-Vsys level OK to qualify conventional c-Si modules for natural environment in the continental USA.

85°C/95%RH/96h/-Vsys level In IEC 61215 ed 3 draft (4x more stressful)



More at: Hacke NREL/CP-5J00-70264

Control of PID-shunting: 6 levels of PID susceptibility



Type A passed no PID test

Failed in field

Type B passed 85/85/96 –1000 V

Type C –F passed increasingly higher stress levels: No PID-S

Good control of PID

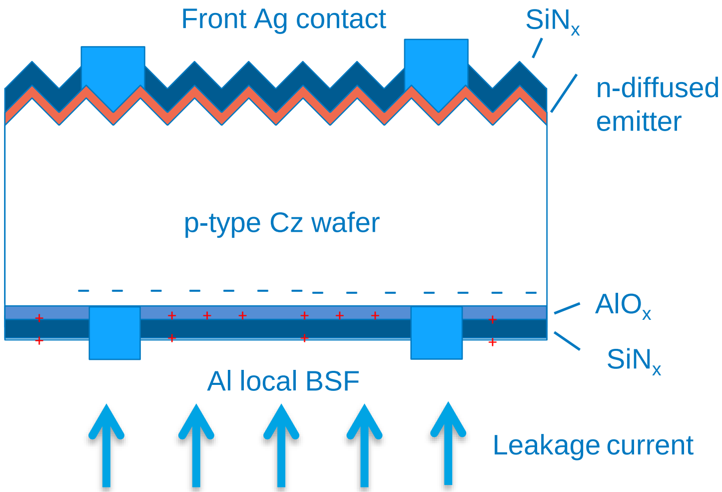
Degrading 4%/y in first year by something else

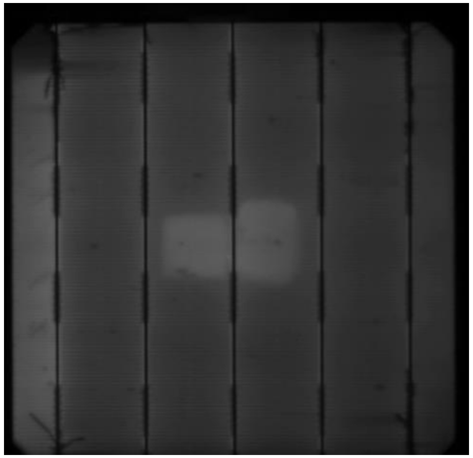
Y. Chen et al. Trina/SERIS/NREL collaboration

Consideration for PERC cells & other c-Si designs

PERC: Passivated Emitter Rear Contact

- Front junction same as conventional cells
- Polarization on rear (case of glass substrate module)
  - (–) bias to cells
  - (+) charge accumulates in rear passivating dielectric
  - Minority carrier electrons in p-base attracted to (+) rear and recombine
- Exposure to light quickly dissipates the charge: complete recovery < 5 h
- For this and other reasons, a better PID test **must** include the factor of light



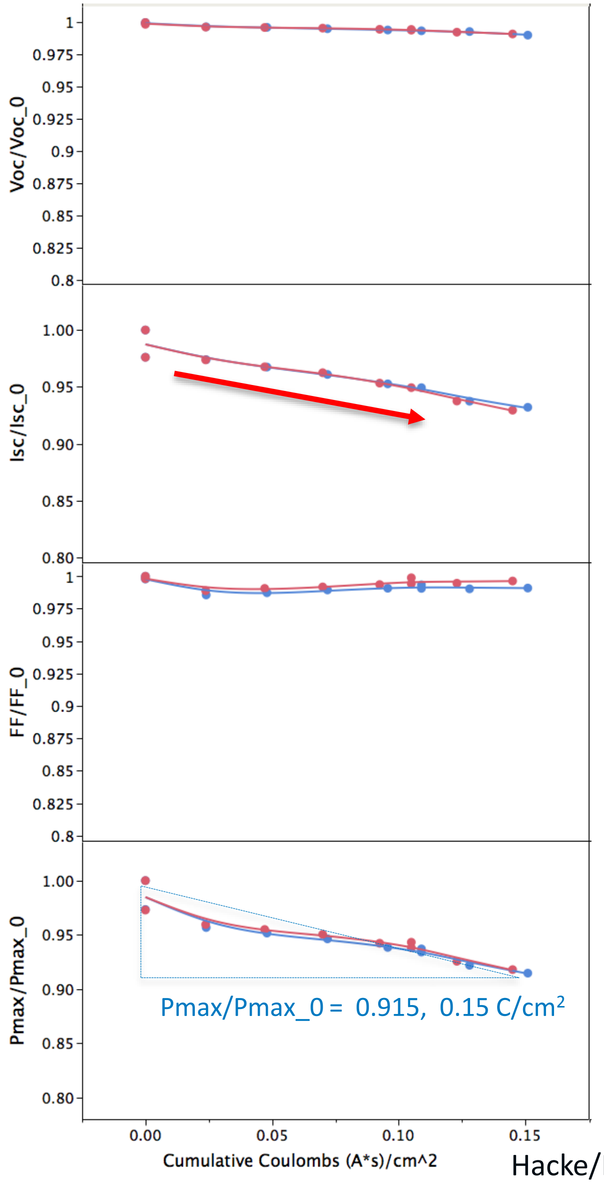


Electroluminescence: PERC Cell after PID stress on rear, after localized illumination

NREL/SERIS to be published

Consideration for electrochemical corrosion (+) to cell, UV/ionization damage

60°C/ 85% RH +1000 V

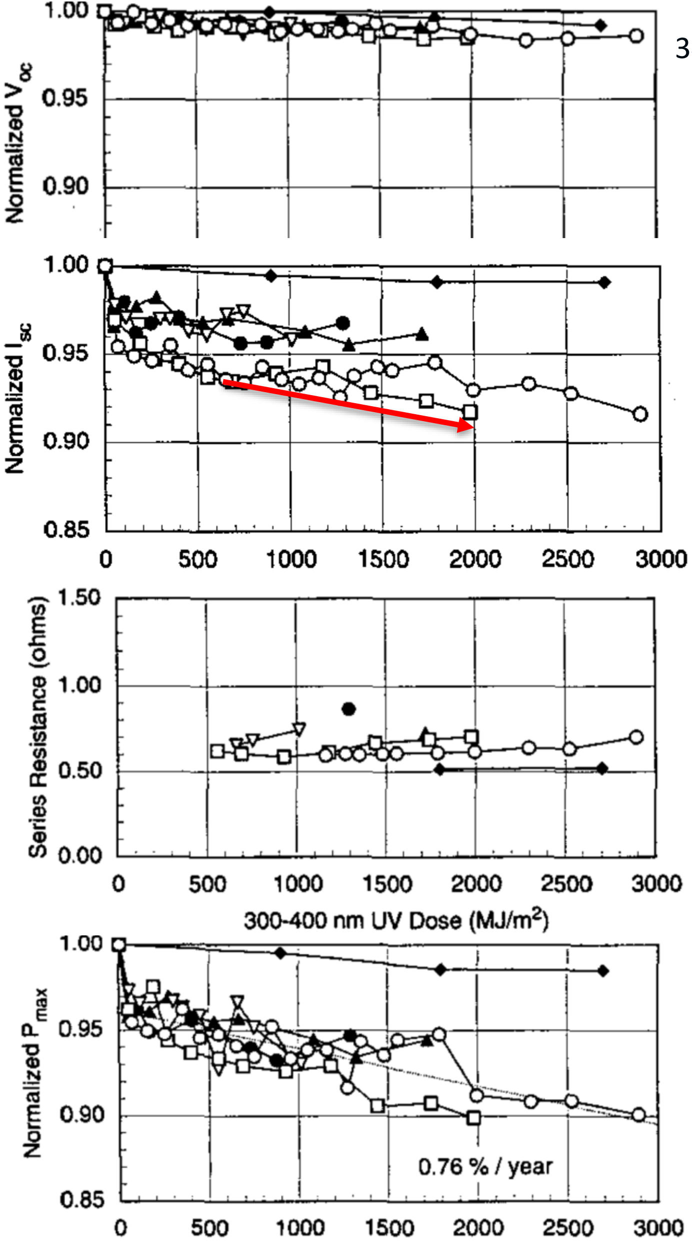


Pmax/Pmax_0 = 0.915, 0.15 C/cm^2

Hacke, Kempe (NREL) Han (SunPower)

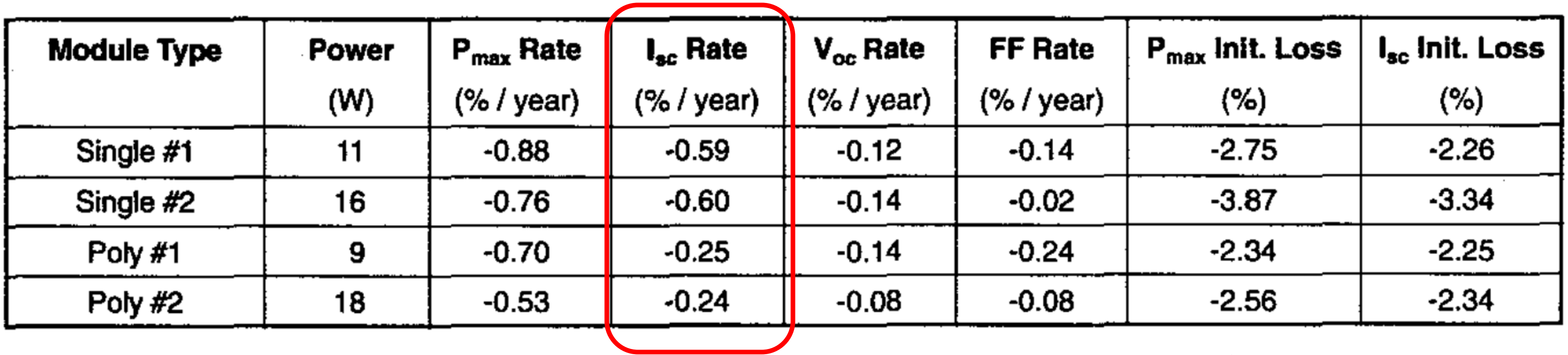
Hacke/Kempe/Han

340 – nm UVA



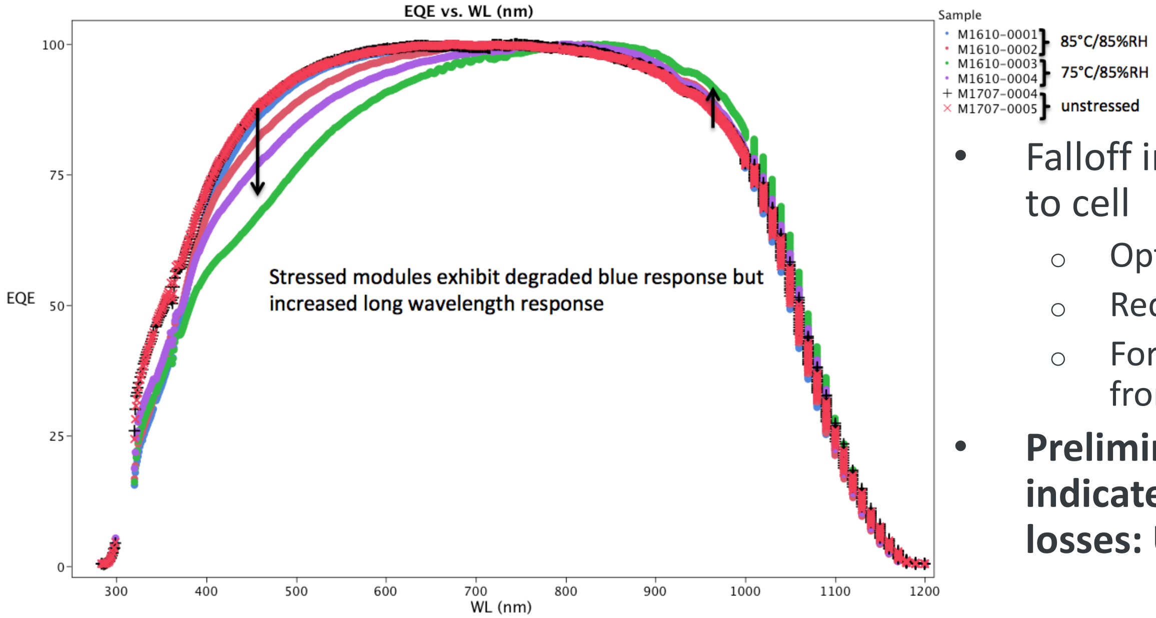
Osterwald, Anderberg,, Rummel, Ottoson 2002

Consideration for electrochemical corrosion (+) to cell, UV/ionization damage



Module Type	Power (W)	P_{max} Rate (% / year)	I_{sc} Rate (% / year)	V_{oc} Rate (% / year)	FF Rate (% / year)	P_{max} Init. Loss (%)	I_{sc} Init. Loss (%)
Single #1	11	-0.88	-0.59	-0.12	-0.14	-2.75	-2.26
Single #2	16	-0.76	-0.60	-0.14	-0.02	-3.87	-3.34
Poly #1	9	-0.70	-0.25	-0.14	-0.24	-2.34	-2.25
Poly #2	18	-0.53	-0.24	-0.08	-0.08	-2.56	-2.34

Osterwald 2002



- Falloff in short-circuit current in cells with $+V_{sys}$ to cell
  - Optical losses
  - Reduction in surface passivation
  - Formation of non-photoconverting dead layer at front of cell
- **Preliminary PC-1D modeling of QE curves indicate effect is not explainable by just optical losses: UV, $+V_{sys}$ bias leading to I_{sc} loss**

Hacke, Kempe (NREL)
Han (SunPower)

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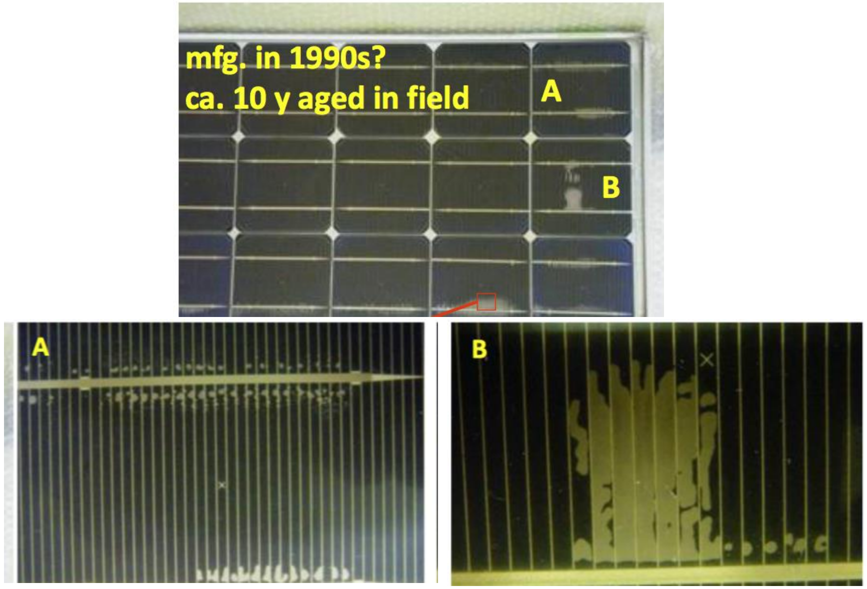
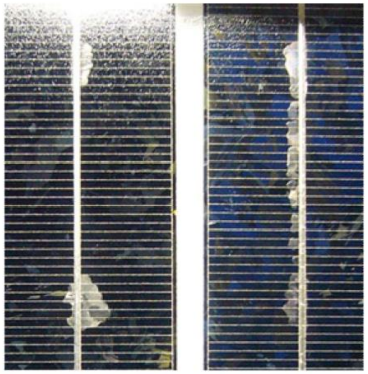
PID-delamination: photocatalyzed, electrocatalyzed

AIST (Matsuda, 2012) finding **TiO_2** catalyzing reactions leading to delamination





3 UV: -20/75°C 125 Cycles (250 h)

(Module) Temperature Cycling Protocol

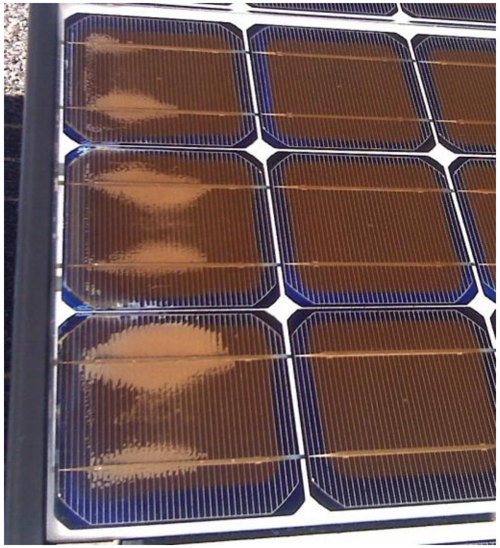
75°C, 0 / 3 UV
1 h

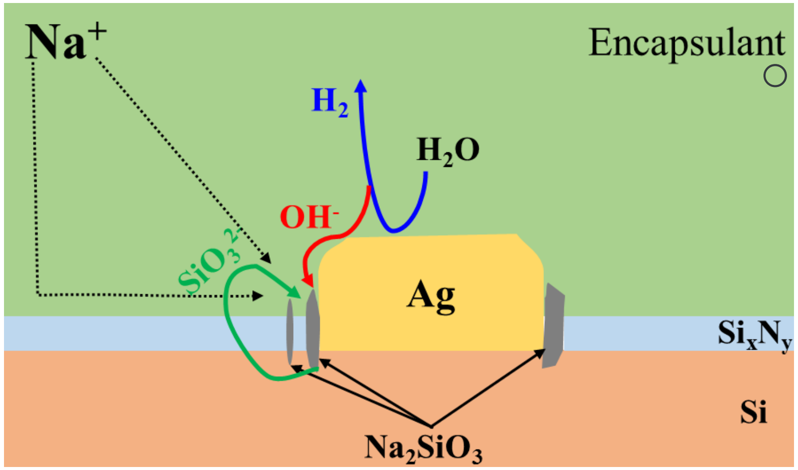
-20°C, 0 UV
1 h

3 UV: -20/75°C 75 Cycles (150 h) -> Delamination
0 UV: -20/75°C 75 Cycles (150 h) -> No Delamination

“R&D of Characterization Technology of Solar Cells（FY2006-FY2009）Final Report “, NEDO 2010.
Via T. Tanahashi PVQAT TG 3

PID-delamination: photocatalyzed, electrocatalyzed





Catalysis at Ag suspected with system voltage bias & ion drift

- Under negative bias, water is reduced
  - $2H_2O+2e^- \rightarrow H_2(g)+2OH^-$
- Under positive bias, water is oxidized
  - $2H_2O-4e^- \rightarrow O_2(g)+4H^+$

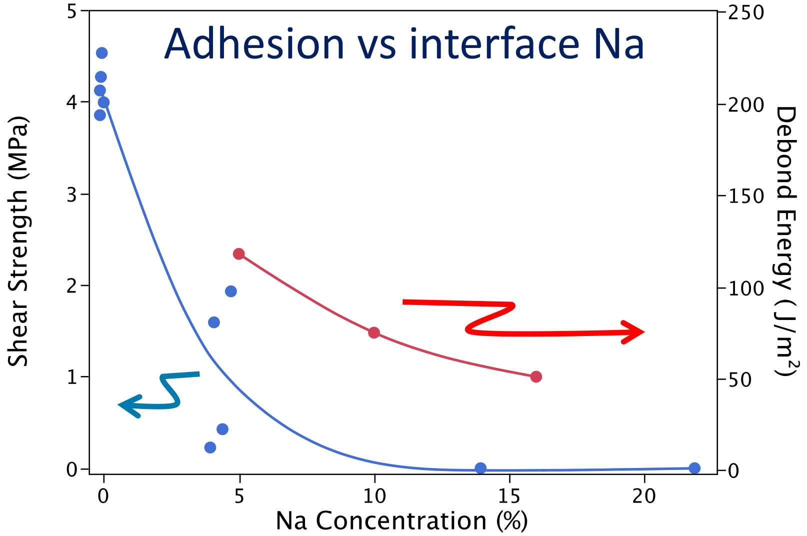
Li, Chen, Hacke, Kempe (2016 PVRW)

Excessive current transfer associated with the delamination

Results of DH + PID sequential stress test on four commercial modules
Factors that we believe contribute to this delamination are:

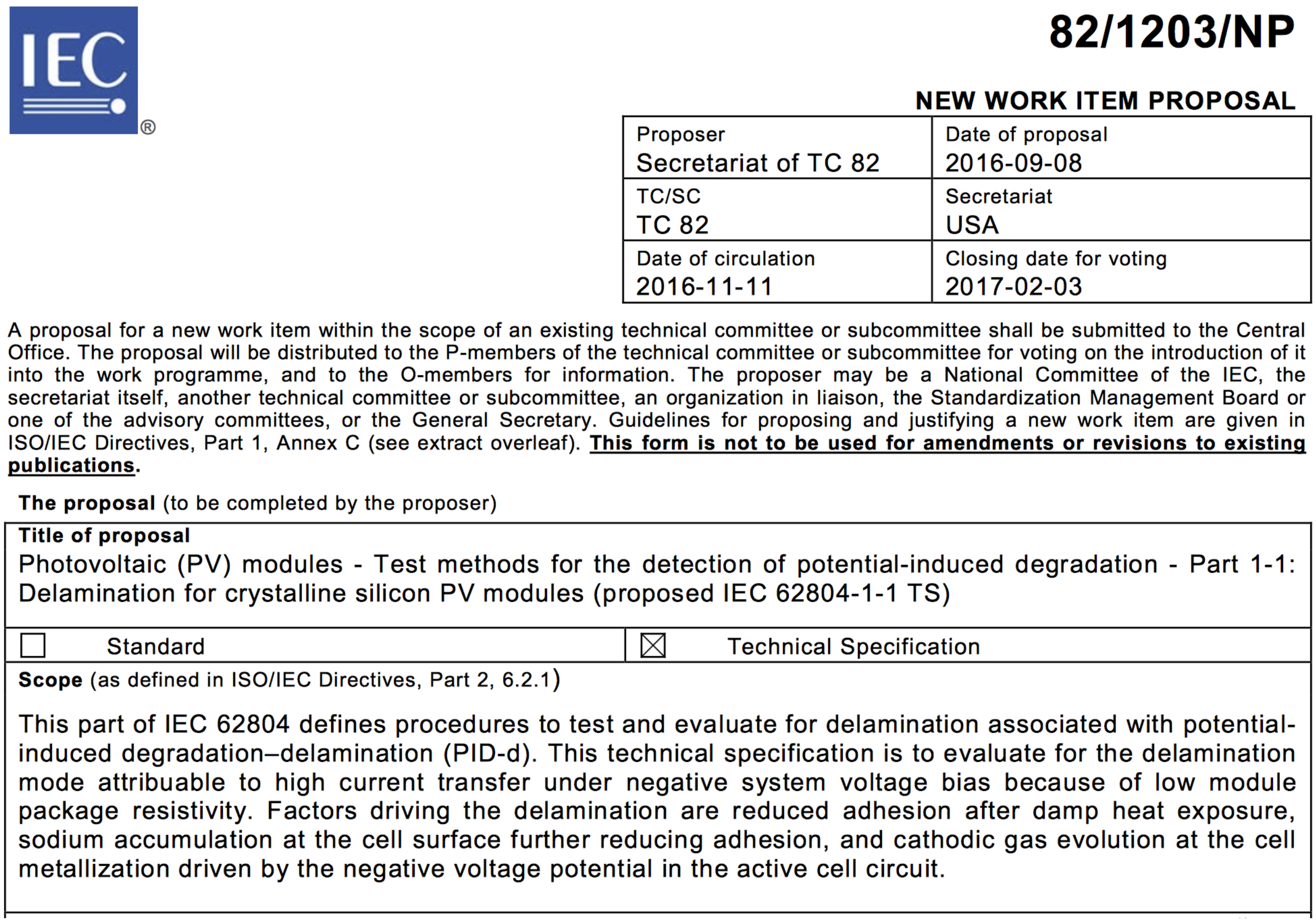
1) **Damp heat**
2) **Na migration to the cell**
3) **Products such as H_2 and O_2 or OH ions**

Module #	Current (nA/cm^2) (-1,000 V) 85°C/85% RH equilibrated	Delamination
1	4.9	No
2	1.8	No
3	36	Yes
4	0.071	No



Dhere (2001)
Bosco, Kempe, Hacke (2016)

PID-delamination tech spec - CD stage



IEC®

82/1203/NP

NEW WORK ITEM PROPOSAL

Proposer Secretariat of TC 82	Date of proposal 2016-09-08
TC/SC TC 82	Secretariat USA
Date of circulation 2016-11-11	Closing date for voting 2017-02-03

A proposal for a new work item within the scope of an existing technical committee or subcommittee shall be submitted to the Central Office. The proposal will be distributed to the P-members of the technical committee or subcommittee for voting on the introduction of it into the work programme, and to the O-members for information. The proposer may be a National Committee of the IEC, the secretariat itself, another technical committee or subcommittee, an organization in liaison, the Standardization Management Board or one of the advisory committees, or the General Secretary. Guidelines for proposing and justifying a new work item are given in ISO/IEC Directives, Part 1, Annex C (see extract overleaf). **This form is not to be used for amendments or revisions to existing publications**.

The proposal (to be completed by the proposer)

Title of proposal
Photovoltaic (PV) modules - Test methods for the detection of potential-induced degradation - Part 1-1: Delamination for crystalline silicon PV modules (proposed IEC 62804-1-1 TS)

☐ Standard ☒ Technical Specification

Scope (as defined in ISO/IEC Directives, Part 2, 6.2.1)

This part of IEC 62804 defines procedures to test and evaluate for delamination associated with potential-induced degradation–delamination (PID-d). This technical specification is to evaluate for the delamination mode attribuable to high current transfer under negative system voltage bias because of low module package resistivity. Factors driving the delamination are reduced adhesion after damp heat exposure, sodium accumulation at the cell surface further reducing adhesion, and cathodic gas evolution at the cell metallization driven by the negative voltage potential in the active cell circuit.

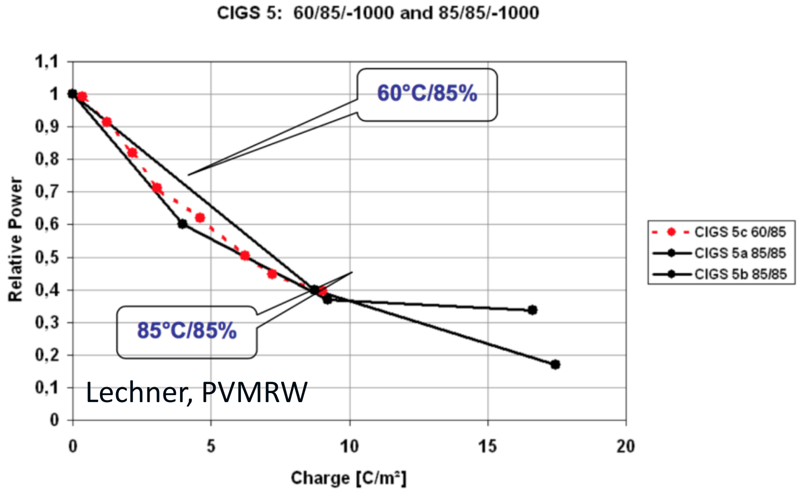
Approval				
P-Members Voting	**P-Members Approving**	**Approval %**	**Criteria**	**Result**
29	29	100	>50%	APPROVED

Focus is on the electrochemical, but understanding of optical processes required

- Crystalline Silicon PID
    - Shunting: PID-s
    - Delamination: PID-d
- Thin film PID
    - Test method consideration
    - TCO corrosion
- Combined-stress cycle for better characterization of PID and other degradation mechanisms

PID Thin film - Power loss

Concept that coulomb of transfer in the chamber does the same damage as a coulomb transferred in the field (per Lechner-ZSW, Weber, PI-Berlin, Hacke NREL).



Lechner, PVMRW

- Confirmed by NREL for two CdTe module types **with outdoor data** to be published
- Does not work with moisture ingress, or if there is significant PID recovery

- **Match of PID with transferred charge**

$$t_F = C_{F\_chamber} / (C/t)_{field}$$

$(C/t)_{field}$. : Coulombs transferred/unit time in field

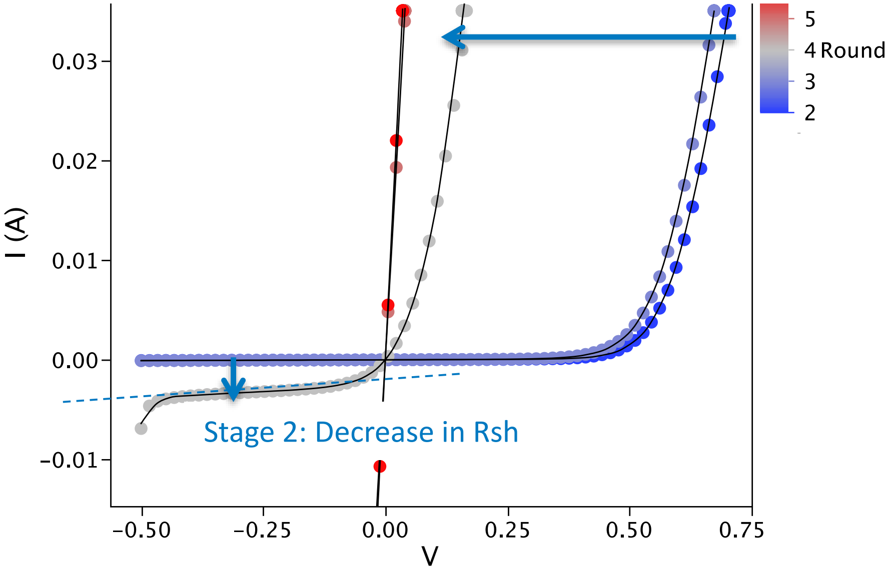
$C_{F\_chamber}$: Coulomb corresponding to the chosen failure criterion

t_F :projected time for the equivalent coulomb transfer in the field corresponding to the failure level in the chamber.

Data: 1000 h (42 d) in 85°C 85% RH chamber stress test x (46 days field/day chamber) = 5.3 y of coulomb transfer in field.

- 96 h 85/85 corresponds to *less than* ½ y in the field)
- Acceleration varies widely depending on mounting insulation: factor or 50
- Necessitates looking at *AF* on case by case basis

PID degradation mechanism in CIGS, (-) bias on cells


Stage 1: decrease in ionized carrier concentration, reducing built-in potential V, increasing saturation current

Stage 2: Decrease in Rsh

Round/stage	Rs (ohm·cm²)	Rsh(ohm·cm²)	Jo (A/cm²)	N_A/N_{Ao}
2	0.657	3164	7.59E-08	1.00
3	0.869	2290	1.61E-07	0.23
4	0.511	187	0.00656	1.28E-05

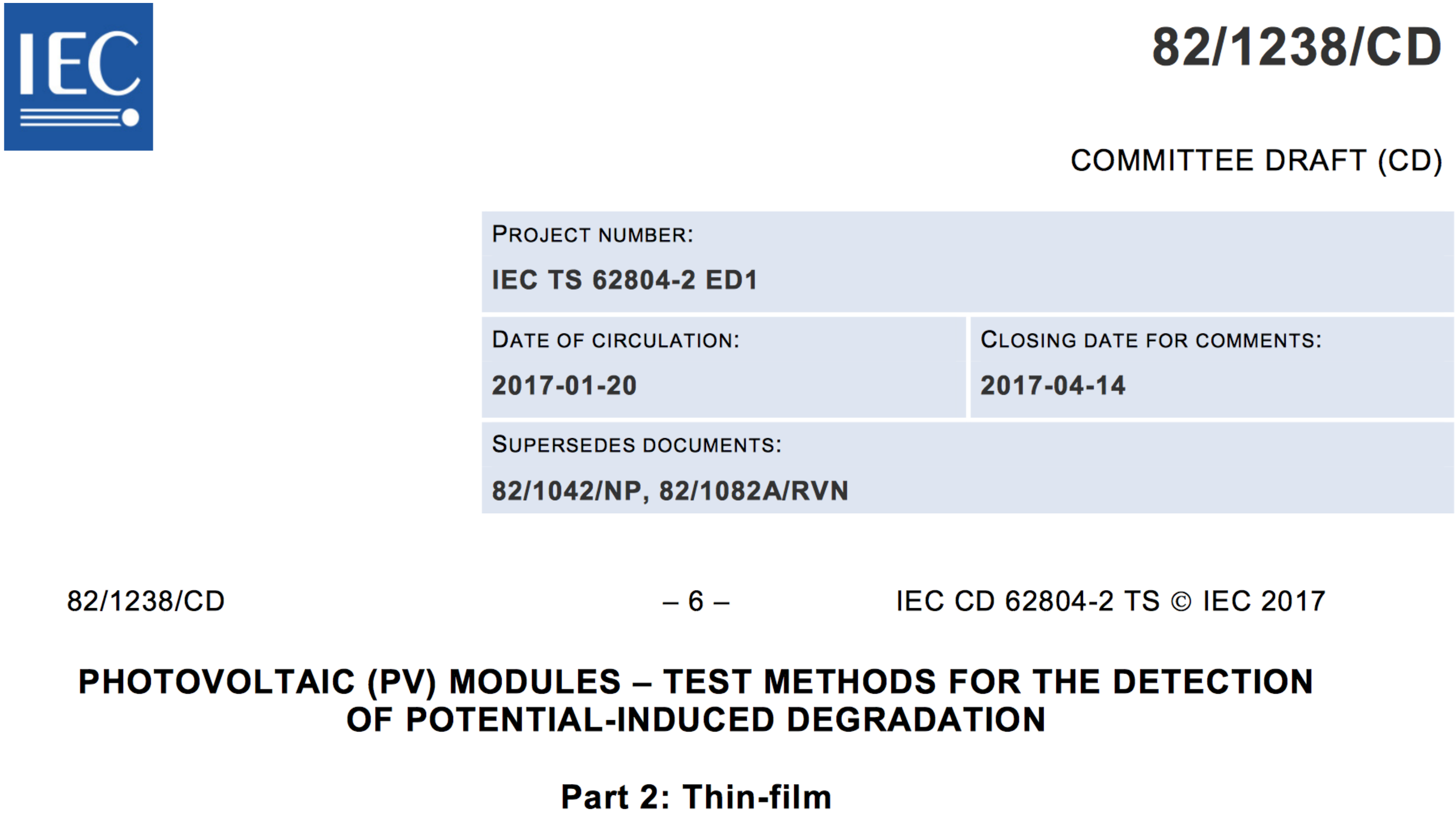
- Good fit of degradation assuming increase in saturation current
- Suspicion is variation may be due to change in ionized acceptor concentration in CIGS (C-V measurements)

$$I_S = qAn_i^2 \cdot \left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right)$$

Saturation current

Alonso-Garcia, Hacke, Mansfield, Reppins

PID test method for thin film modules



82/1238/CD

COMMITTEE DRAFT (CD)

PROJECT NUMBER:
IEC TS 62804-2 ED1

DATE OF CIRCULATION: **2017-01-20**	CLOSING DATE FOR COMMENTS: **2017-04-14**

SUPERSEDES DOCUMENTS:
82/1042/NP, 82/1082A/RVN

82/1238/CD – 6 – IEC CD 62804-2 TS © IEC 2017

PHOTOVOLTAIC (PV) MODULES – TEST METHODS FOR THE DETECTION OF POTENTIAL-INDUCED DEGRADATION

Part 2: Thin-film

PVQAT – TG3: Humidity Temperature Voltage

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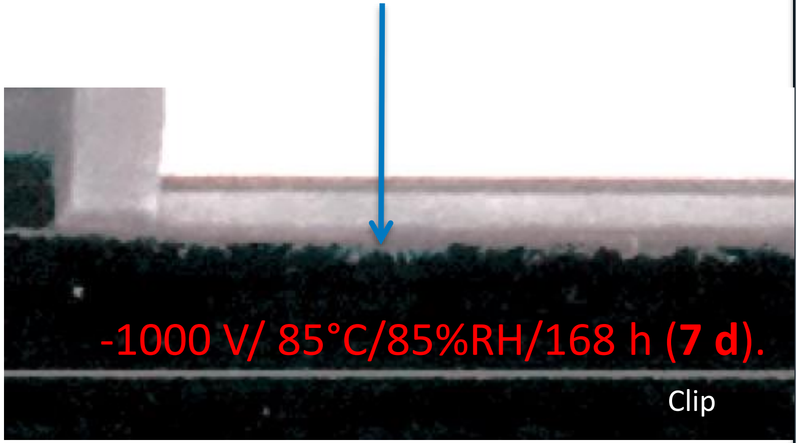
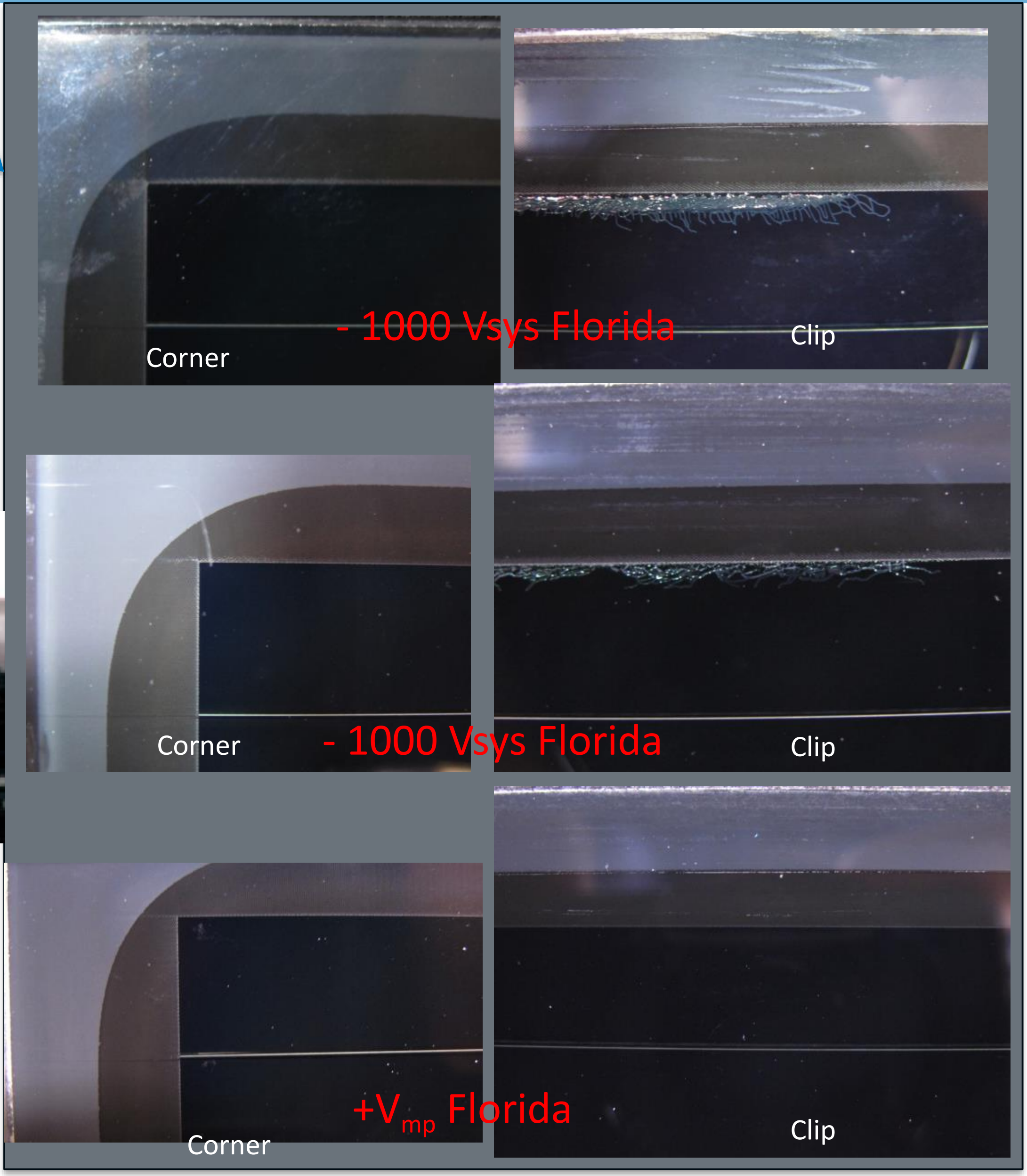
- Thin film PID
    - Test method consideration
    - TCO corrosion
- Combined-stress cycle for better characterization of PID and other degradation mechanisms

85°C/85%RH/168 h/-Vsys test versus 1.1 y in the field

- **PID stress (Na migration) + moisture ingress →TCO corrosion**
- **TF 1 modules** Both show degradation at edge clamps



- **7-14 days in chamber = 1.1 y in the field For corrosion damage equivalence**
- **Future standardized test method required**



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Shortcomings of current PID tests

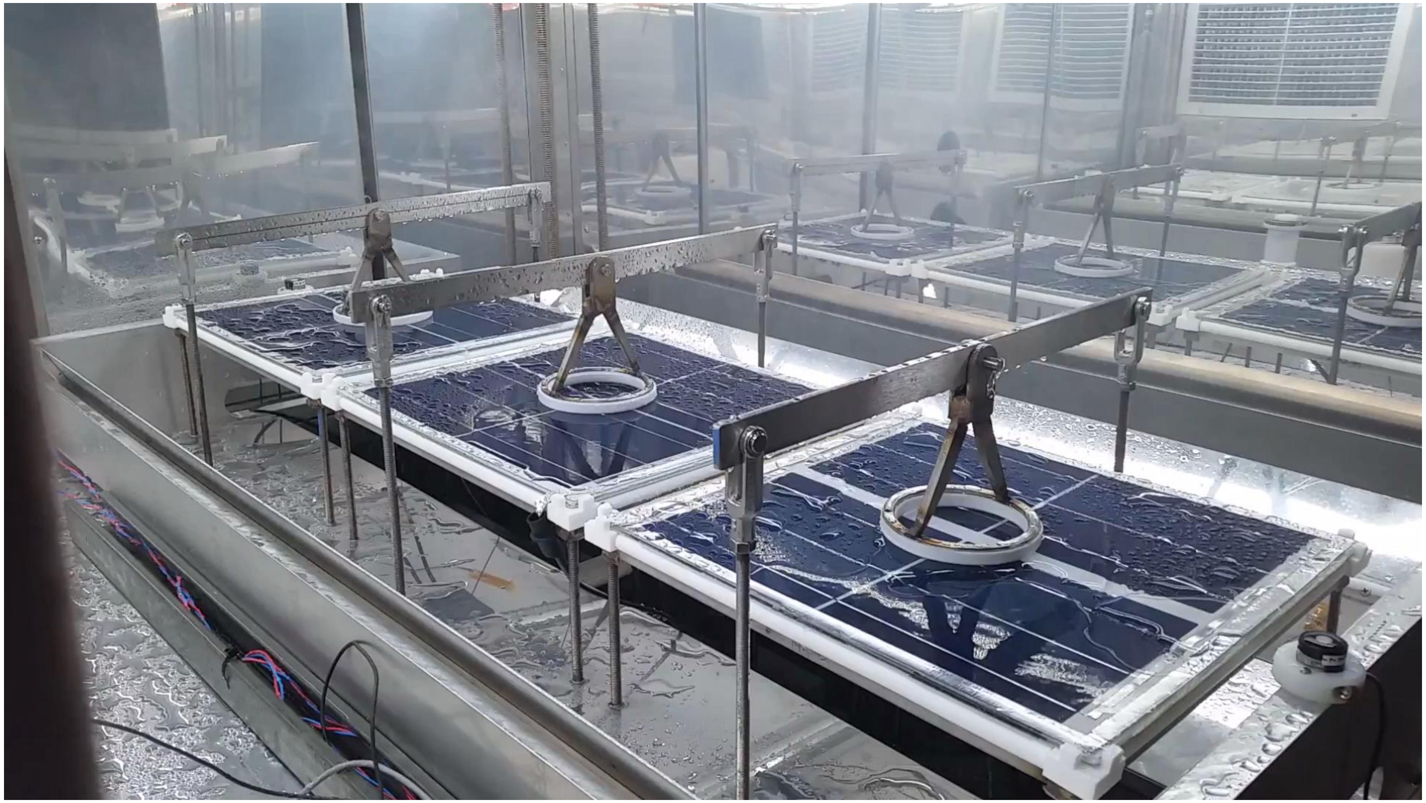
- Tests done in the dark
- No representation of rain on insulating mounts
- No representation of stress state that can damage edge seals
- No tests for recovery

Many roads lead to:

Combined stress testing: applying V_{sys} bias with light

Factors applied cyclically

Xe Light (with partial shading)
Temperature
Humidity (uncondensed)
Rain
System voltage
Mechanical stress



Rain and damp heat stage

- 40°C Rain (pulsed), 40°C chamber, >95% RH (dark)

Pressure bars (pulsed, simulation of wind (or snow load). Pressure scaled for mini modules through modeling and simulation)

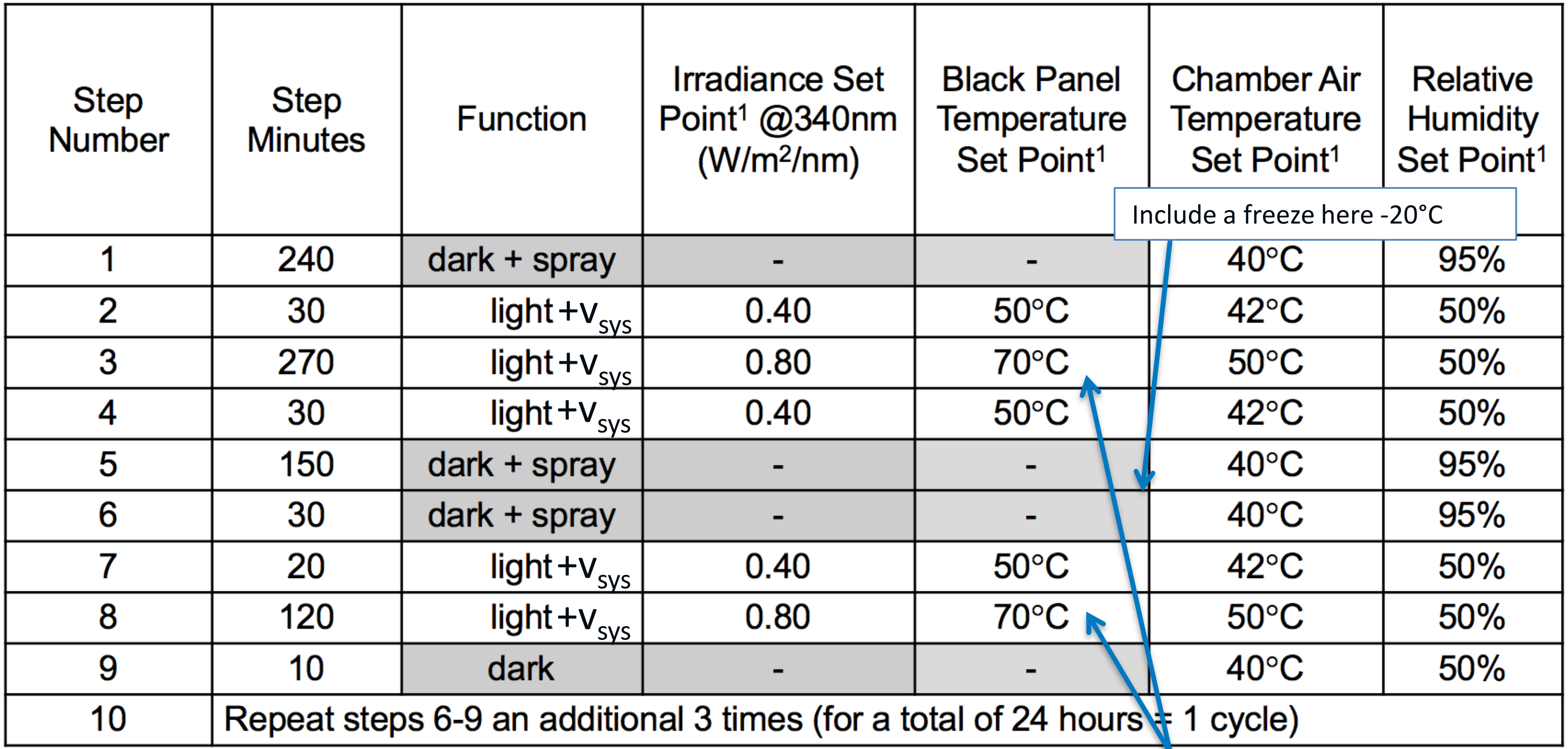
System voltage bias to cell circuit, module frame grounded
Followed cyclically by periods of irradiance, dry heat

DuraMAT
Durable Module Materials Consortium

- Hacke, Miller, Spataru, Kempe, Schelhas, Moffitt, King

- DuPont/AIST/Mitsui Chemical/FrISE

Basis of initial C-AST trials: ASTM D7869



Step Number	Step Minutes	Function	Irradiance Set Point^1 @340nm (W/m^2/nm)	Black Panel Temperature Set Point^1	Chamber Air Temperature Set Point^1	Relative Humidity Set Point^1
1	240	dark + spray	-	-	40°C	95%
2	30	light $+V_{sys}$	0.40	50°C	42°C	50%
3	270	light $+V_{sys}$	0.80	70°C	50°C	50%
4	30	light $+V_{sys}$	0.40	50°C	42°C	50%
5	150	dark + spray	-	-	40°C	95%
6	30	dark + spray	-	-	40°C	95%
7	20	light $+V_{sys}$	0.40	50°C	42°C	50%
8	120	light $+V_{sys}$	0.80	70°C	50°C	50%
9	10	dark	-	-	40°C	50%
10	Repeat steps 6-9 an additional 3 times (for a total of 24 hours = 1 cycle)					

Include a freeze here -20°C

Move to higher temperature 90°C

Courtesy Al Zielnik – Atlas-Ametek

Mechanical loading – simulate snow load, wind load

- Longer dark/spray cycles to achieve moisture uptake levels (saturation)
- Multiple irradiance levels to simulate diurnal outdoor conditions; High level increases acceleration
- No light/spray together it doesn't typically rain in max sunshine conditions
- Interspersed light/dark sub-cycles to simulate thermal shock effects occurring in natural exposures

Other degradation mechanisms we can examine with C-AST

Backsheet cracking → UV, cyclic oxidative/hydrolytic stress, CTE stress, EVA acidity

PID → System voltage, rain/humidity/condensation, temperature, light, soiling (light required to get an accurate picture of sensitivity)

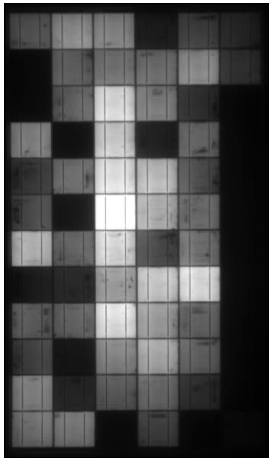
Grid finger corrosion – delamination → System voltage, humidity, temperature, light, soiling

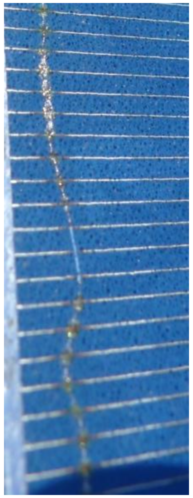
Light and elevated Temperature induced degradation → Light, elevated temperature, current

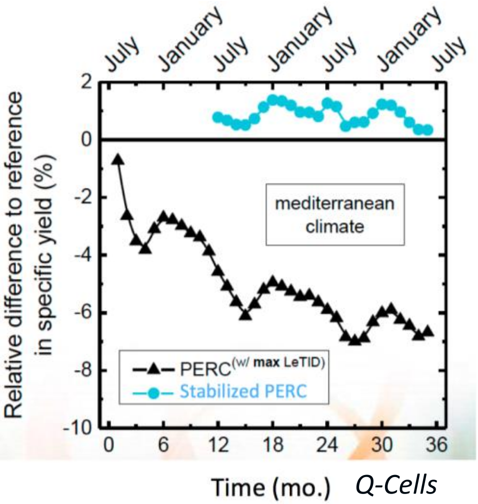
Snail trails→ delamination → Mech. load, UV, electric field, moisture, impurities

Edge seal failure→ Mech. load, CTE stress, UV, moisture, impurities

Delamination→ CTE stress, UV, moisture, impurities, system voltage







Q-Cells

Issues not well clarified in existing standardized testing

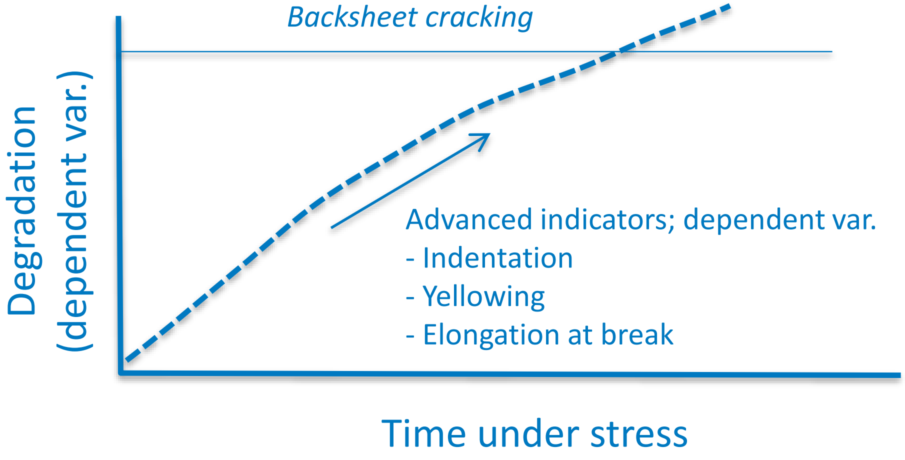
Application of rate equations

Generalized polymeric rate of degradation

$$R_D \sim I^x \cdot (b + m \cdot TOW) \cdot T_f^{\frac{T - T_0}{10}}$$

*Fischer *et. al*, Kempe PVMRW

T_f=1.41±0.23 Acceleration per 10°C increase.
X=0.64±0.2 Irradiance acceleration exponent.
m=-0.0015±0.12 Time of Wetness (TOW) factor.
b=1.071±0.0026



Advanced indicators; dependent var.
- Indentation
- Yellowing
- Elongation at break

System voltage: exponential model

$$\frac{d(P_{\max}/P_{\max\_0})}{dt} = A_0 \cdot f(V) \cdot e^{\frac{-E_a}{kT}} \cdot e^{\mathrm{RH\%} \cdot B}$$

UV(on cell efficiency)

$$N_{NP} = N_T - N_{P0}(-\sigma_{UV}(\lambda)\phi_B t_{UV})$$

N_{NP} non-passivating bonds due to damage,
t_{UV} under UV light
$\sigma_{UV}(\lambda)$ is the capture cross section for a photon, ϕ, flux
N_T is the total number of bonds, and N_{PO} is the initial number of non-passivated bonds

Summary

- Crystalline Silicon PID
  - Shunting: PID-s, 60°C/85% 96 h clarifies >5 y in Continental USA, need light to better simulate PID in the field (PERC cells,etc)
  - Delamination: PID-d: driven by photocatalytic and electrocatalytic processes, Na migration, moisture ingress
- Thin film PID
  - Test method consideration: takes more than 1000 h 85°C/85% to evaluate 5 y Florida, depends on design.
    - Evaluation of coulomb transfer field/chamber to determine acceleration
  - TCO corrosion: 7-14 days in chamber = 1.1 y in the field for corrosion damage equivalence, standard for this yet to be started
- Combined-stress cycle for better characterization of PID and other degradation mechanisms

Thank you !

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