

# Silicon Wafers for the Mesoscopic Era

**Howard R. Huff**

**512-356-3334 (ph) / 512-356-7640 (fax)**

**[howard.huff@sematech.org](mailto:howard.huff@sematech.org)**

# Agenda

## ➤ Introduction

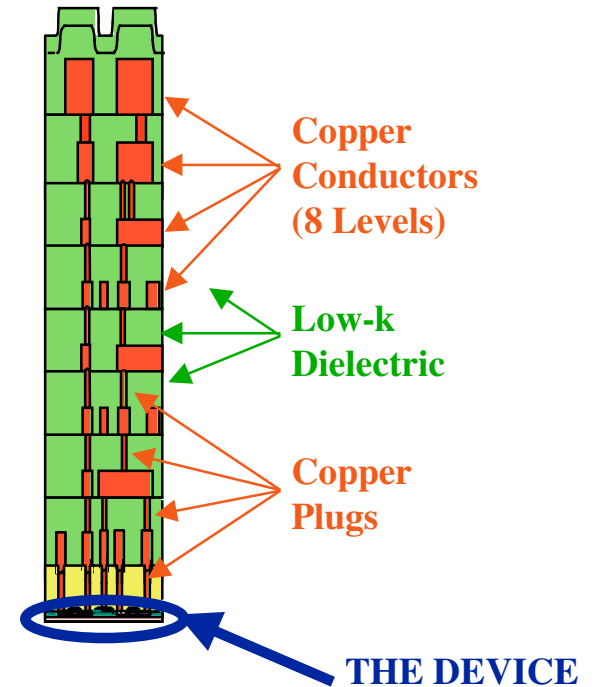
## ➤ International Technology Roadmap for Semiconductors

## ➤ Silicon

- Surface
  - Metals
  - Particles
  - COPs
  - Microroughness
  - Flatness
- Bulk
  - Oxygen / Gettering Centers
  - Resistivity
- Epitaxy
- Large Diameter Wafers
- SOI

## ➤ Summary

### 100 nm High End Microprocessor



**1% of the thickness with  
60% of the issues**

# Pervasiveness of Microelectronics Revolution

- **Learning curve (Haggerty)**
  - Market elasticity (1960's ...)
- **Device scaling (Moore)**
  - Moore's Law #1
    - Number transistors per chip quadruples every 3 years (1965)
  - Moore's Law #2
    - Fabricator economic constraints may reduce return on capital investment (1995)
  - Moore's Law #3
    - Computing advances ensures further advances as computers are main tools by which new computers designed (2000) \*
- **Int'l Technology Roadmap for Semiconductors (ITRS)**
  - Focus to **realize the roadmap** to ensure Moore's law
  - Expansion of economy (GWP) - market elasticity (2000's) - accommodates IC CAGR

# Integrated Circuit Scaling Trends (Historical)

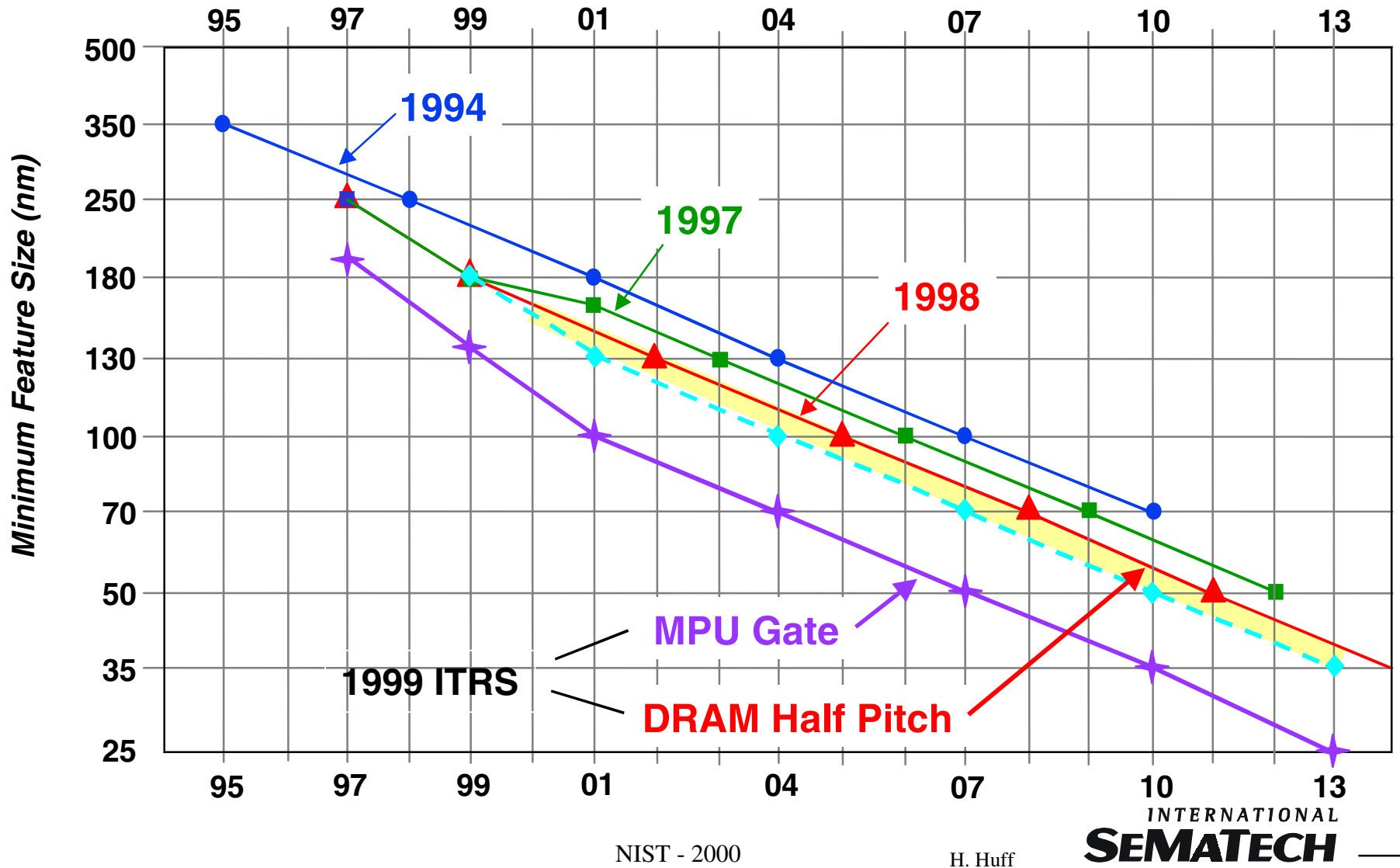
## ➤ **4K DRAM (1974)**

- SiO<sub>2</sub> thickness  $\approx$  75-100 nm
- Gate (channel) length  $\approx$  7500 nm

## ➤ **High-performance MPU (1999) (ITRS - 180 nm node)**

- SiO<sub>2</sub> equivalent oxide thickness  $\approx$  1.9 - 2.5 nm
- Gate (channel) length  $\approx$  130 nm

# SIA Roadmap Acceleration Analysis (from Litho TWG Summary)



# Scaling Methodology

| DIMENSION              | $\lambda$            | $\kappa$     |
|------------------------|----------------------|--------------|
| Potential              | $\kappa$             | $\kappa$     |
| Impurity Concentration | $\kappa / \lambda^2$ | $1 / \kappa$ |
| Electric Field         | $\kappa / \lambda$   | 1            |
| COX                    | $\lambda$            | $\kappa$     |
| Current                | $\kappa^2 / \lambda$ | $\kappa$     |
| Power                  | $\kappa^3 / \lambda$ | $\kappa^2$   |
| Power x Delay          | $\lambda^2 / \kappa$ | $\kappa$     |

$\kappa$ = voltage scaling ( $\approx 0.7X$ )

$\lambda$ =linear dimension scaling ( $\approx 0.7X$ )

# Integrated Circuit Scaling Trends (Current)

## ➤ Gate Stack

- **Scaling** SiO<sub>2</sub> - direct-tunneling leakage current  $\approx$  NMOSFET  $I_{\text{off}}$
- Intrinsic SiO<sub>2</sub> performance may be more limited by fundamental material properties in sub-2 nm gate oxides than by metals/COPS
- $T_{\text{EOT}} = (3.9/\text{K}) (T_{\text{PHYS}})$ ;  $I_{\text{DSAT}} = (w/2l) (3.9\text{K}_0\text{A}) (T_{\text{EOT}})^{-1} \mu (V_{\text{G}} - V_{\text{T}})^2$

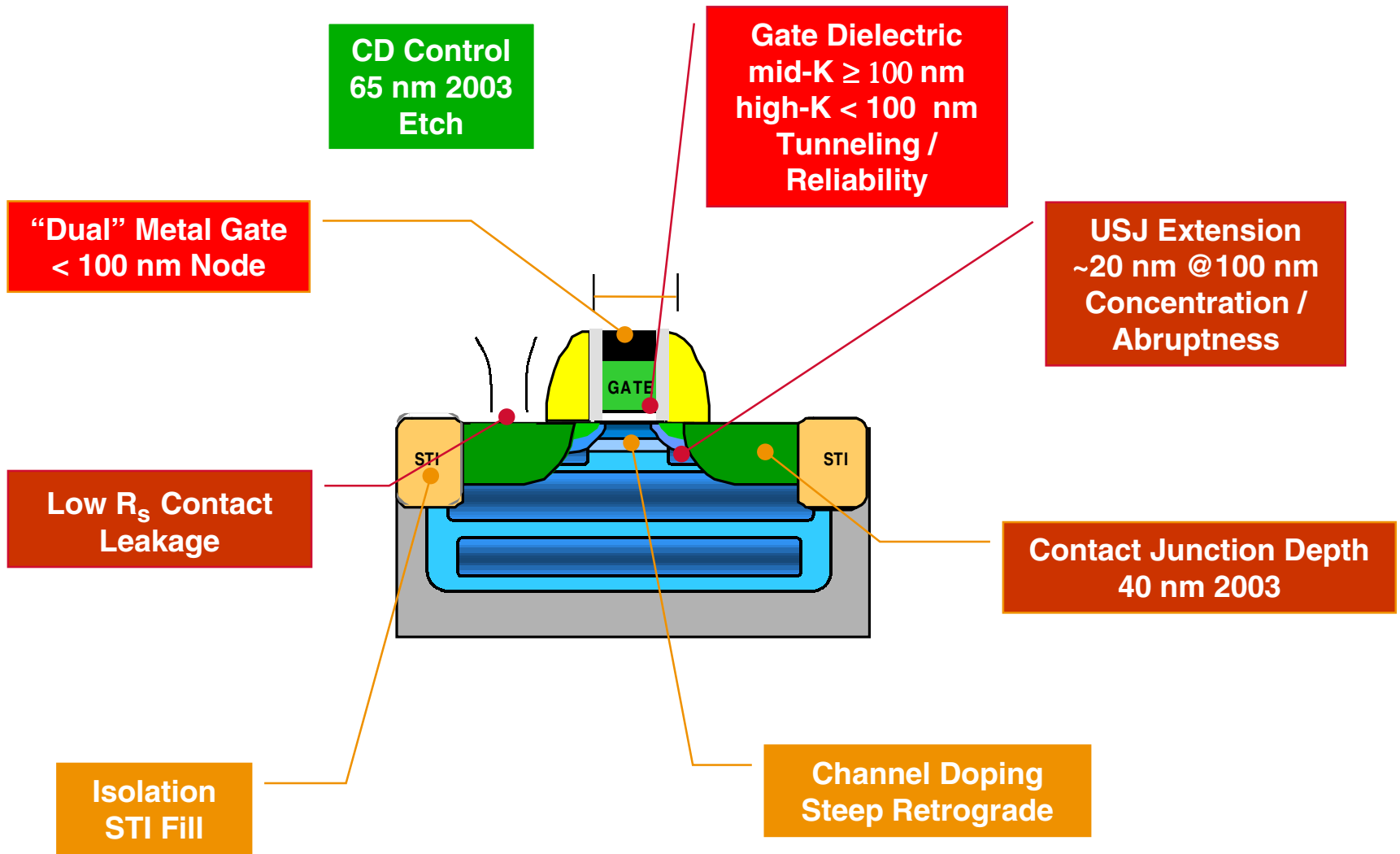
## ➤ Channel doping

- Increased capacitive coupling of gate electrode to channel (by reducing  $T_{\text{EOT}}$ ) accommodated with increased channel doping, ensuring further **scaling** due to increased channel barrier - improved isolation - between source and drain
- Statistical fluctuations in number / distribution of dopant atoms

## ➤ Source / drain doping

- **Scaling** requires increasingly shallow junction, increased doping

# Critical Transistor Related Issues





# Selected Highlights of ITRS - 2000

| YEAR                 | 1999 | 2002  | 2005 | 2008 | 2011  | 2014  |
|----------------------|------|-------|------|------|-------|-------|
| TECHNOLOGY NODE (nm) | 180  | 130   | 100  | 70   | 50    | 35    |
| DRAM 1/2 pitch (nm)  | 180  | 130   | 100  | 70   | 50    | 35    |
| MPU Gate Length (nm) | 140  | 85-90 | 65   | 45   | 30-32 | 20-22 |

## **CIRCUIT CHARACTERISTICS (HIGH-PERFORMANCE MICROPROCESSOR)**

|   |       |               |       |       |       |        |
|---|-------|---------------|-------|-------|-------|--------|
| Functions per chip<br>( M transistors)        | 110   | > 220 , < 441 | 882   | 2,494 | 7,053 | 19,949 |
| Chip size at ramp (mm <sup>2</sup> )          | 450   | > 450 , < 567 | 622   | 713   | 817   | 937    |
| Logic Transistors/cm <sup>2</sup> at ramp (M) | 24    | > 49 , < 78   | 142   | 350   | 863   | 2,130  |
| Clock Frequency, across-chip<br>(MHz)         | 1,200 | 1,600         | 2,000 | 2,500 | 3,000 | 3,600  |
| Maximum chip power with<br>heatsink (W)       | 90    | 130           | 160   | 170   | 174   | 183    |

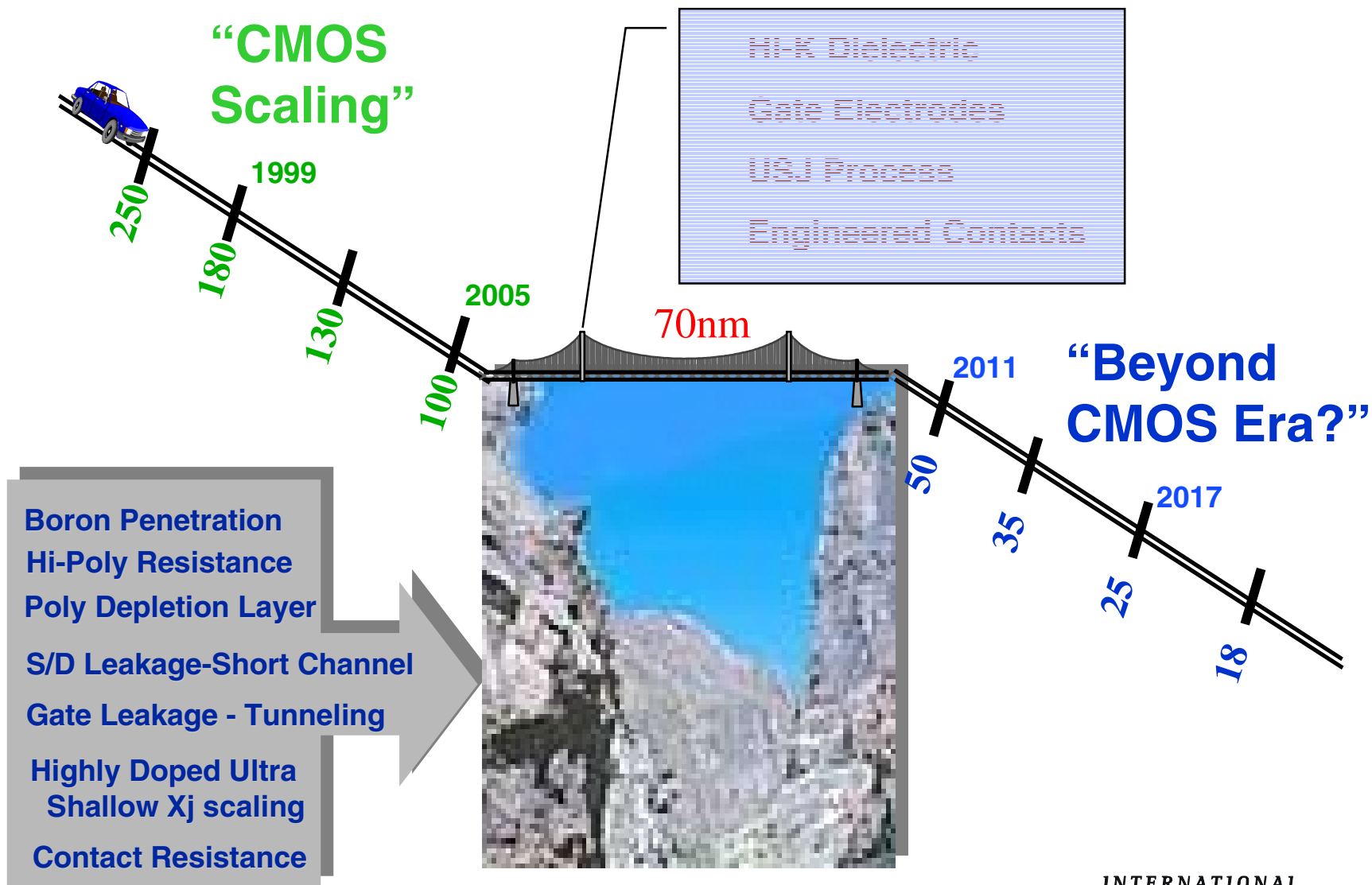
## **DEVICE CHARACTERISTICS (HIGH-PERFORMANCE MICROPROCESSOR)**

|  |           |           |           |           |           |           |
|--|-----------|-----------|-----------|-----------|-----------|-----------|
| Power Supply Voltage V <sub>DD</sub> (V)                     | 1.8 - 1.5 | 1.5 - 1.2 | 1.2 - 0.9 | 0.9 - 0.6 | 0.6 - 0.5 | 0.6 - 0.3 |
| Maximum I <sub>OFF</sub> @ 25C (minimum L<br>device) (nA/μm) | 5         | 10        | 20        | 40        | 80        | 160       |
| Nominal I <sub>ON</sub> @ 25C (μA/μm)<br>(NMOS / PMOS)       | 750 / 350 | 750 / 350 | 750 / 350 | 750 / 350 | 750 / 350 | 750 / 350 |

## **MOSFET DIMENSIONS**

|   |           |           |           |           |           |           |
|---|-----------|-----------|-----------|-----------|-----------|-----------|
| T <sub>EOT</sub> (nm)                         | 2.5 - 1.9 | 1.9 - 1.5 | 1.5 - 1.0 | 1.2 - 0.8 | 0.8 - 0.6 | 0.6 - 0.5 |
| Source / drain contact, X <sub>J</sub> (nm)   | 145 - 75  | 90 - 45   | 70 - 35   | 55 - 30   | 40 - 20   | 35 - 15   |
| Source / drain extension, X <sub>J</sub> (nm) | 70 - 42   | 43 - 25   | 33 - 20   | 26 - 16   | 19 - 11   | 13 - 8    |

# Key Front-End of Line CMOS Scaling Challenges



NIST - 2000

H. Huff

INTERNATIONAL  
**SEMATECH**

# Introduction - Summary (I)

- **IC scaling will continue for next 15 years utilizing silicon (and silicon-germanium)**
- **Silicon and silicon-germanium have been / will continue to be vehicle for mainstream CMOS structures / applications far beyond next 15 years**
  - Silicon-based materials utilized for applications not requiring state-of-the-art design rules structures throughout 21st century
  - Significant CoO opportunities in wafer specifications
- **Inability and inadvisability of predicting which materials and technologies will extend digital switching beyond 10 nm and become market successes**
  - Enunciated in 1948 (Bob Wallace) upon invention of point-contact transistor (1947) and re-iterated in 2000 (Robert Lucky)

# **Introduction - Summary (II)**

## **Materials and Technologies Not Discussed**

- **SiC**
- **Fullerenes**
- **Carbon nanotubes**
- **Single-electron devices**
- **Self-assembled structures**
- **Optical computers**
- **Quantum computers**
- **DNA computers**

# Agenda

## ➤ Introduction

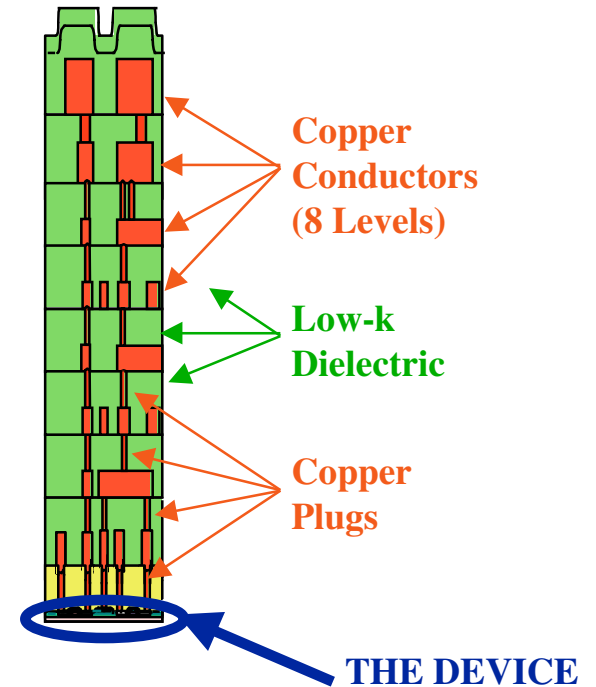
## ➤ International Technology Roadmap for Semiconductors

## ➤ Silicon

- Surface
  - Metals
  - Particles
  - COPs
  - Microroughness
  - Flatness
- Bulk
  - Oxygen / Gettering Centers
  - Resistivity
- Epitaxy
- Large Diameter Wafers
- SOI

## ➤ Summary

### 100 nm High End Microprocessor

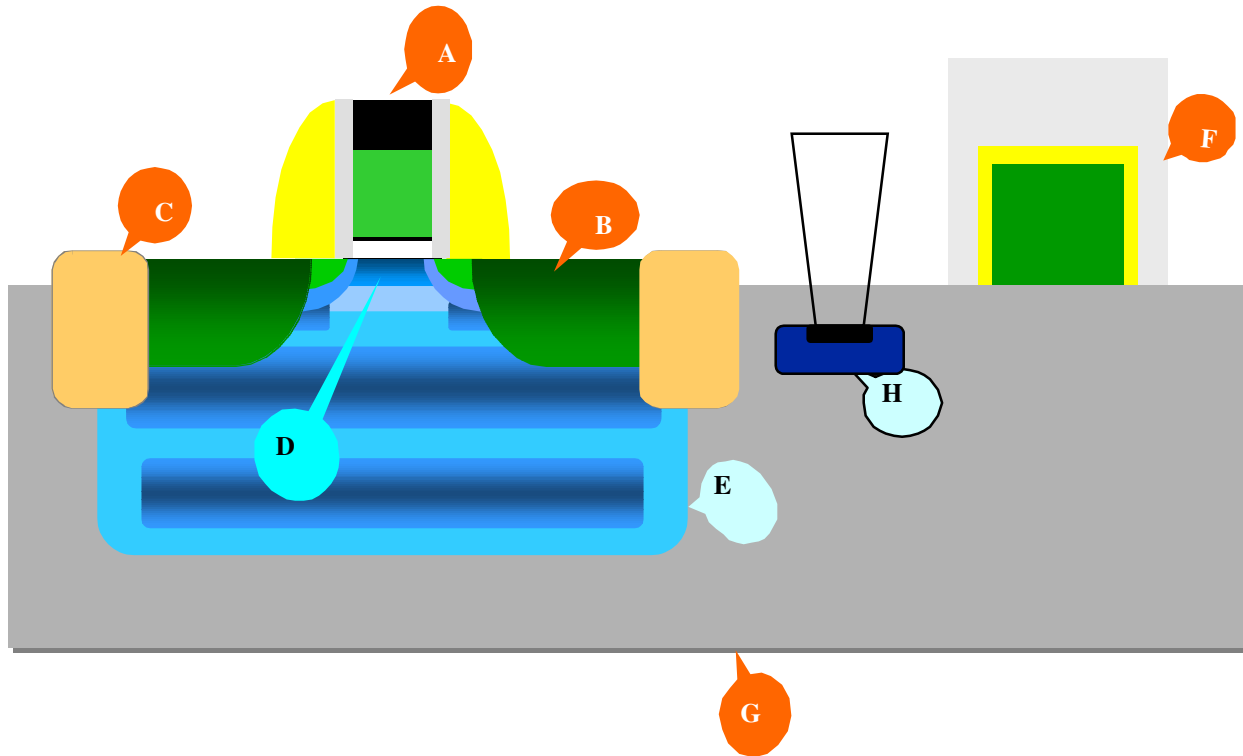


**1% of the thickness with  
60% of the issues**

## Concise summary of key technology characteristics

- **Targets for equipment / material / software suppliers**
- **Targets for researchers**
- **Common reference for semiconductor industry**

# Front-End Processes Roadmap Scope



**A: Gate Stack    B: Source/Drain - Extension**  
**C: Isolation    D: Channel**  
**E: Wells    F: Capacitor Stack/Trench**  
**G: Starting Material    H: Contacts**

# Starting Materials Parameters

- **Particles / COPs**
- **Critical metals**
- **Flatness**
- **Oxygen**
- **Carrier lifetime**
- **Oxidation stacking faults**
- **Epitaxy**
- **SOI**



# ITRS - Starting Materials

- **Paradigm shift occurred during '90's**
  - Increased emphasis toward scientific understanding of physico-chemical properties and selective application of design of experiment methodologies
- **Model-based** experiments and simulation procedures became *de rigeur* in IC industry
- **Technology advancement based on scientific principles rather than experience per se**
- **Necessary to balance “best wafer possible” against CoO opportunity of not driving silicon requirements to detection limit but to some less stringent value consistent with achieving high IC yield**

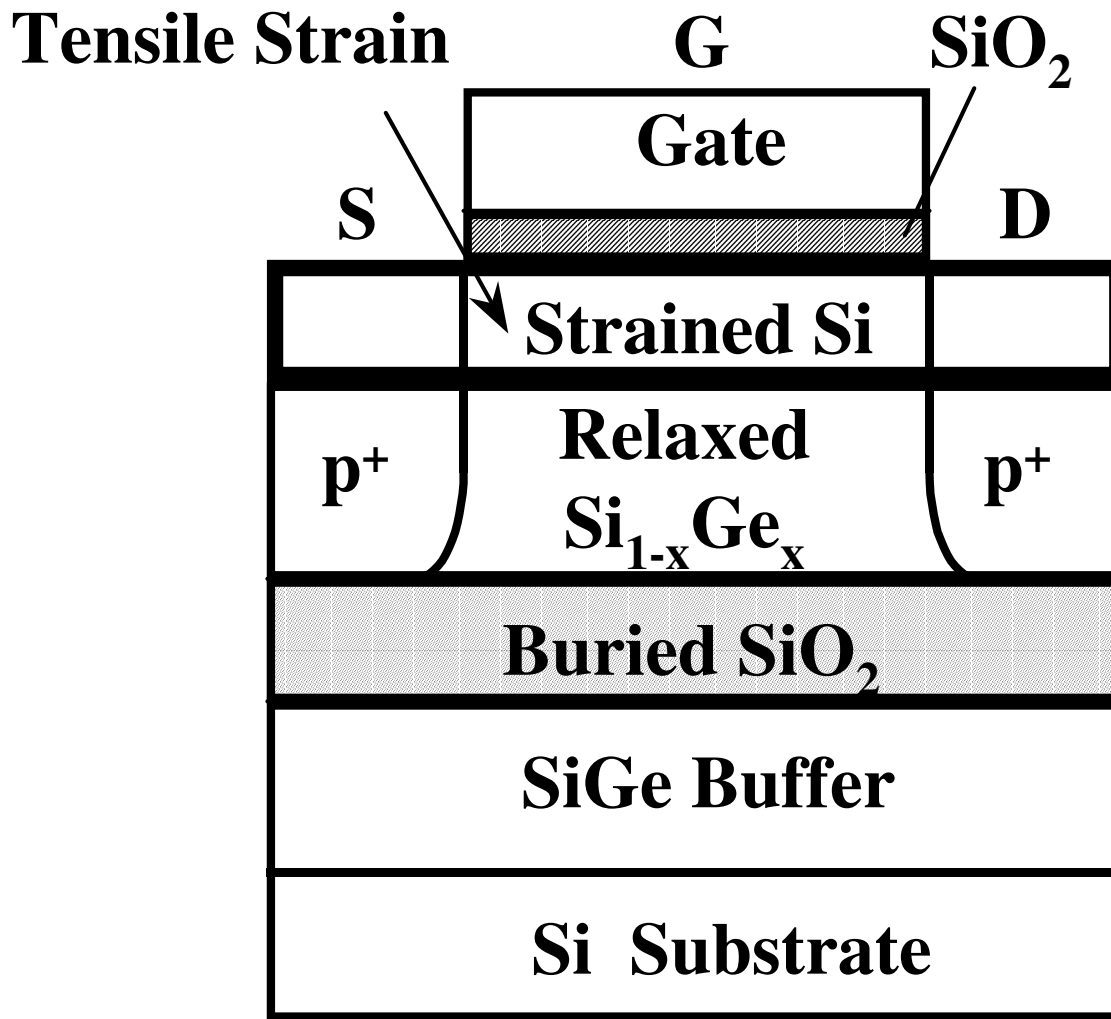
# ITRS - Starting Materials: *Strategy*

- **Modular approach of core set of general characteristics applicable for as-received wafers by IC manufacturers**
- **Parameter values generally derived from **model-based** analysis based on CDs, bits or transistors per chip, wafer size, etc.**
  - Empirical **models** employed as appropriate
  - Values only as reliable as underlying **models**
  - Anecdotal opinions minimized
- **Understanding underlying **models** of IC performance-characteristic relationships may be more critical than specific numerical values**

# Silicon Wafer Specification Historical Trends

- If you can **measure it in silicon**, spec it (1970's)
- Decreasing design rules and vertical dimensions along with increasing die size **drove improvements in silicon** materials (1990's)
- Innovative transistor heterostructure configurations — natural evolution of multi-zone wafer design concept — will further **de-couple starting silicon wafer** from active transistor structure, offering significant cost-of-ownership (CoO) opportunities in relevant wafer specifications (2000's)
- Continued evolution towards 3-D device integration

# Strained-Si PMOSFET on SiGe-on-Insulator



# Materials Science Issues (I)

- **New materials being introduced into multi-zone device structures at unprecedented rate**
  - Low-K interlevel dielectric
  - Copper metallization
  - High-K gate dielectric
  - Metal-gate electrodes
  - Silicon-germanium channel and contacts
- **Alternate gate dielectric materials required to reduce excessive power levels (leakage current) in scaling  $\text{SiO}_2$**
- **Selection of high-K gate dielectric, gate electrode and related gate stack processing, in conjunction with ultra-shallow / highly doped junctions and contacts, must be compatible with **process integration** requirements**

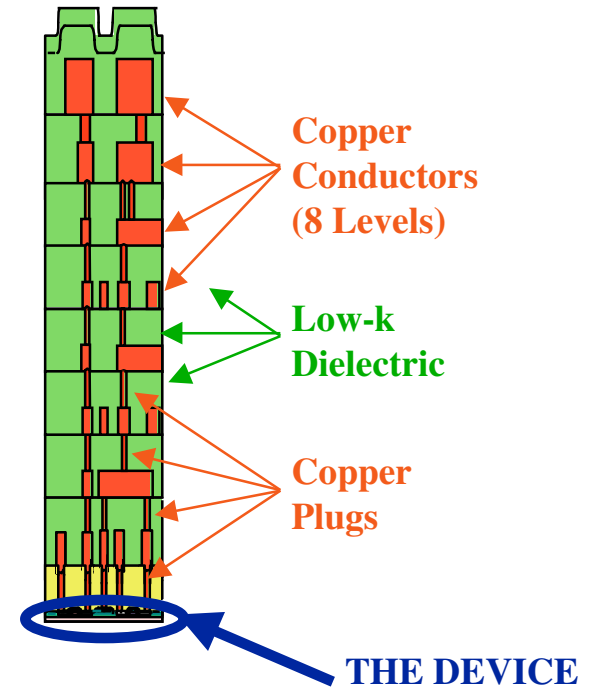
# Materials Science Issues (II)

- **Maintaining Moore's law requires cognizance of CoO for engineered, multi-zone wafers, new gate stack materials and introduction of 300 mm wafers**
- **Silicon wafers must be effectively modeled to guide ITRS specification trends**
- **Is silicon wafer a commodity?**
  - Should wafer specifications reflect commodity nature
  - 300 mm wafers driven to historical silicon percent levels of raw goods cost (<10%) to ensure requisite wafer fab CoO

# Agenda

- Introduction
- International Technology Roadmap for Semiconductors
- Silicon
  - Surface
    - Metals
    - Particles
    - COPs
    - Microroughness
    - Flatness
  - Bulk
    - Oxygen / Gettering Centers
    - Resistivity
  - Epitaxy
  - Large Diameter Wafers
  - SOI
- Summary

100 nm High End Microprocessor



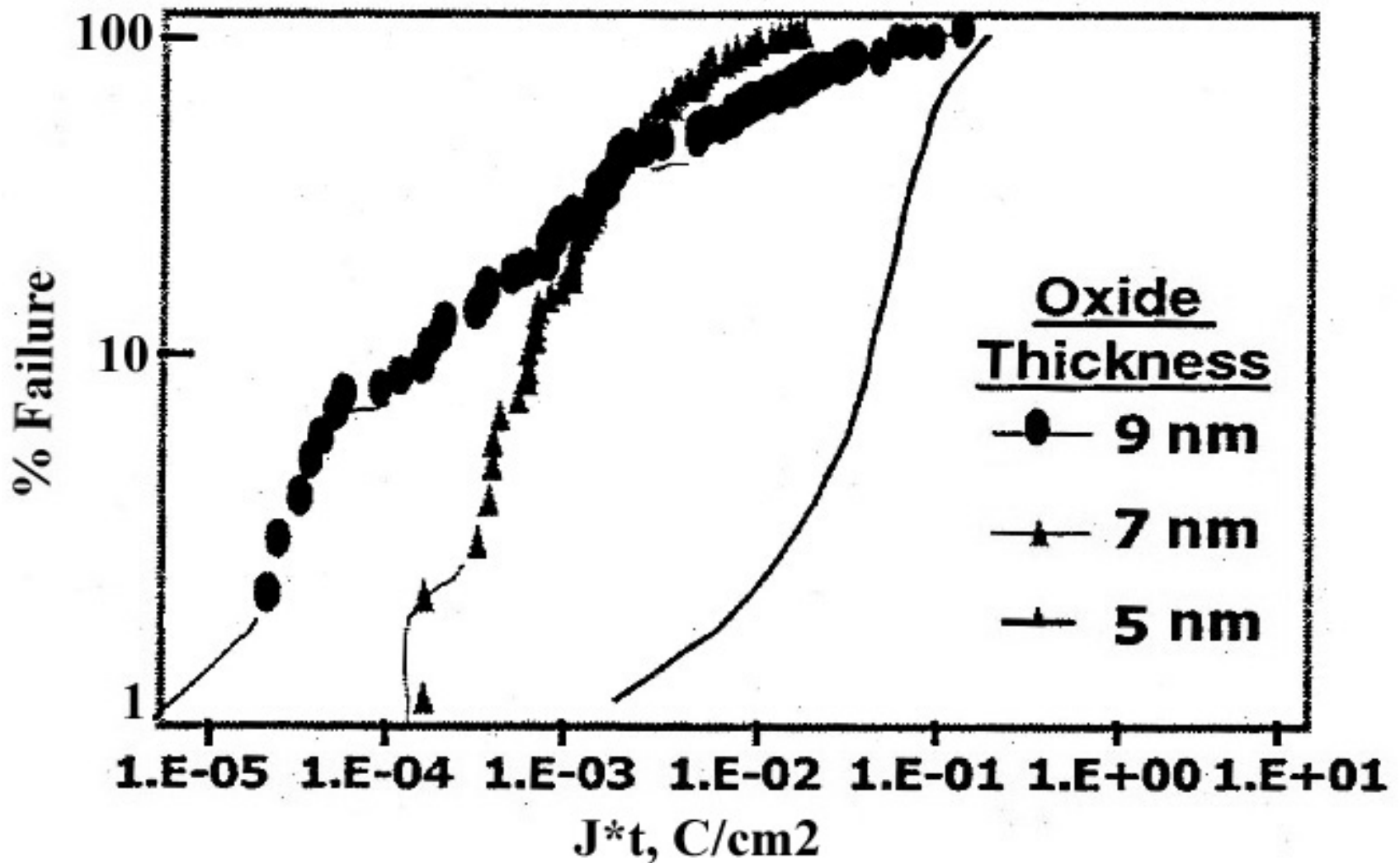
1% of the thickness with  
60% of the issues

# **Silicon:** *Surface Metals*

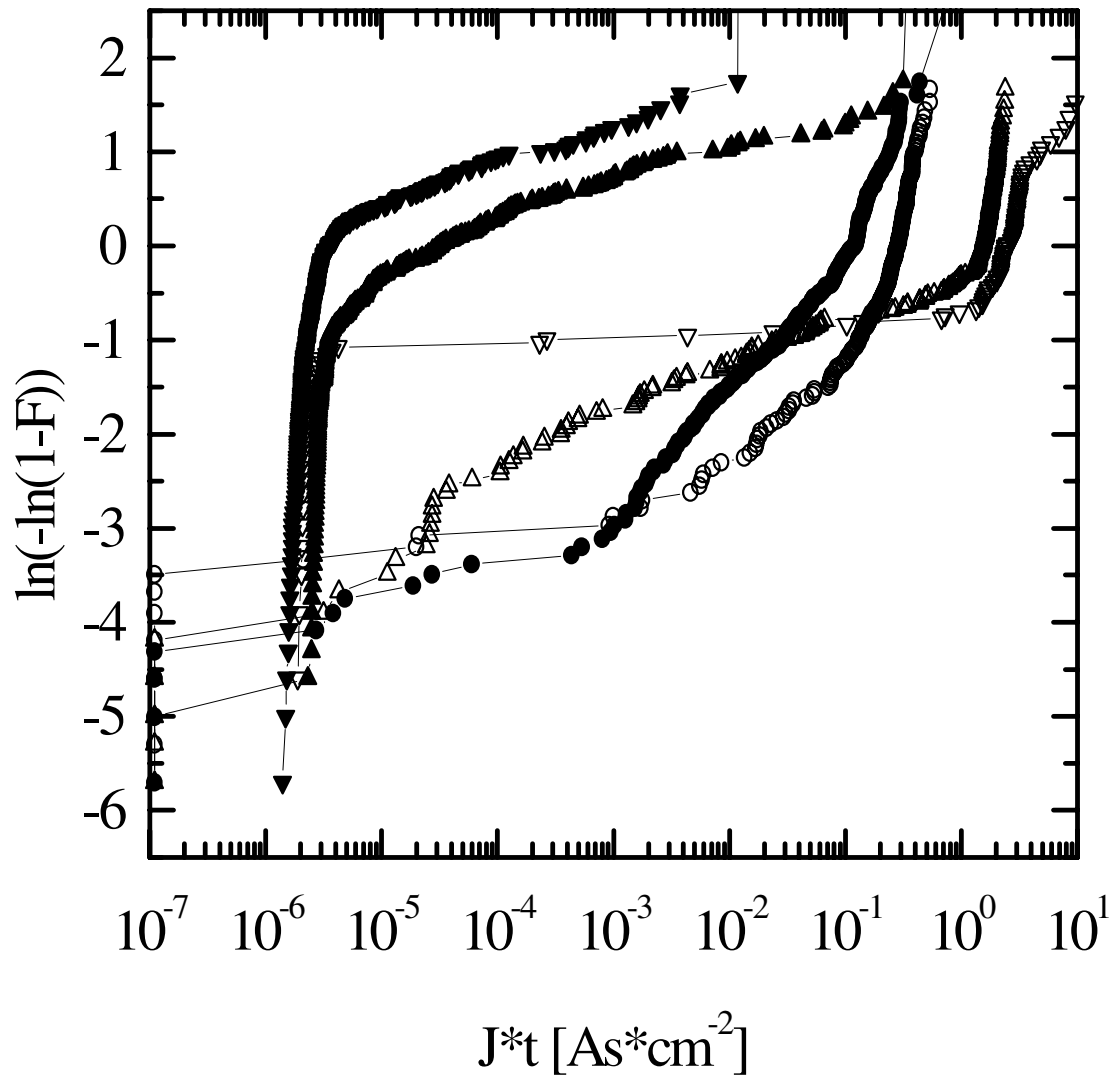
- **Recent experiments on 5–10 nm oxides indicate reduced influence of metals (i.e.,  $10^{11}$  Ni/cm<sup>2</sup>) and higher on  $Q_{BD}$**
- **Cleaning efficiencies > 95% for critical metals (i.e., Fe)**
  - Incoming metal specification  $\approx 10^{11}$ /cm<sup>2</sup> may operationally result in  $< 10^{10}$ /cm<sup>2</sup> after cleaning
- ***CoO OPPORTUNITY:***
  - Viability of driving initial metals  $< 10^{10}$ /cm<sup>2</sup> may be inappropriate from CoO perspective, even though most silicon suppliers can currently meet upper  $10^9$ /cm<sup>2</sup> specification for most metals



# Silicon: *Surface Metals*



# Silicon: *Surface Metals*



- ▽— no cont., 17nm
- △— no cont., 7.5nm
- no cont., 5nm
- ▼— Ni  $5 \times 10^{12}$  at/cm<sup>2</sup>, 17nm
- ▲— Ni  $5 \times 10^{12}$  at/cm<sup>2</sup>, 7.5nm
- Ni  $5 \times 10^{12}$  at/cm<sup>2</sup>, 5nm

# **Silicon:** *Surface Metals*

- **Metallics may require re-assessment**
  - Active p-n junction length in IC increasing due to increased number of transistors per chip
  - Potential onset of gate dielectric materials with K significantly greater than SiO<sub>2</sub> beyond 100 nm technology node may require different pre- and post-gate surface preparation cleans

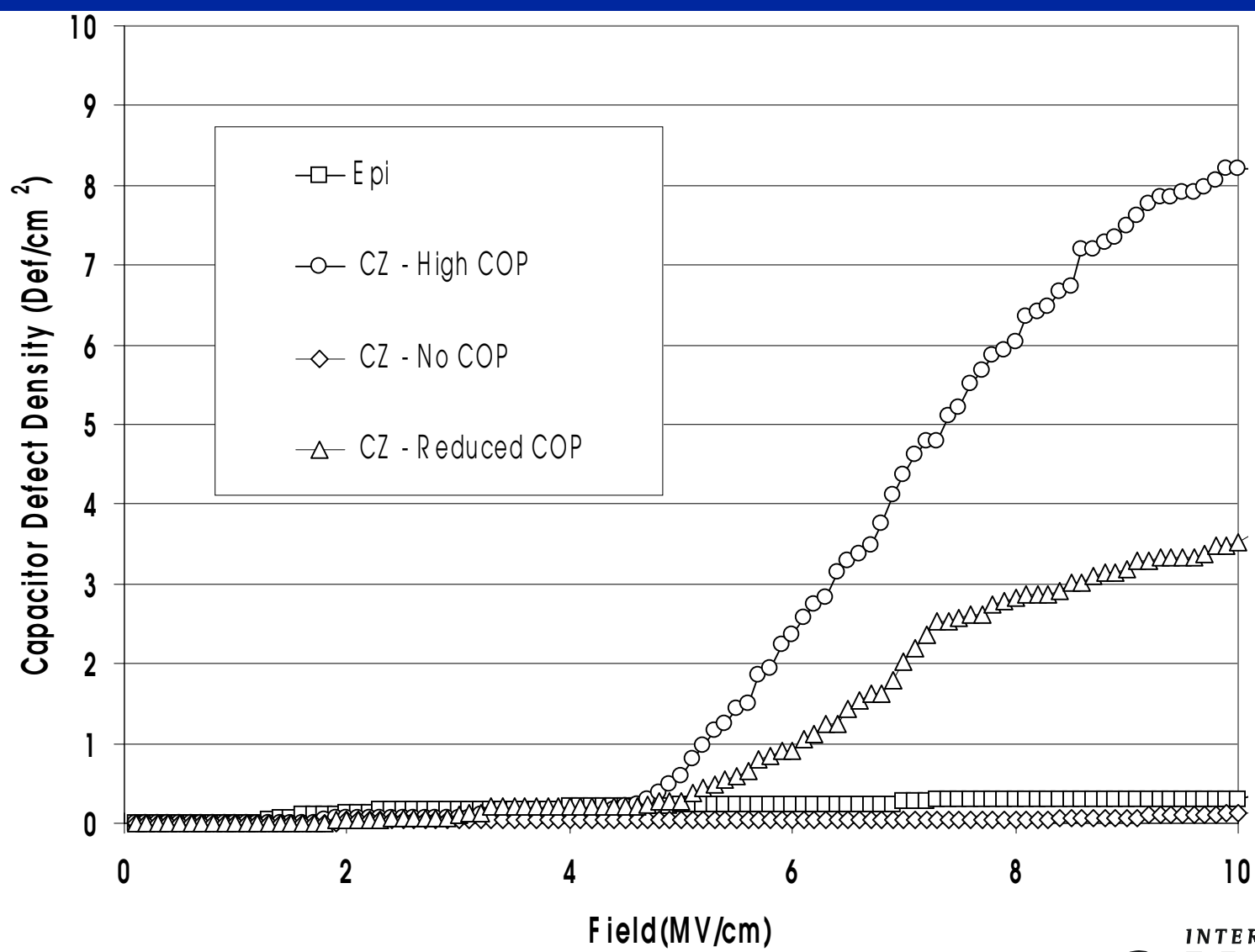
# **Silicon:** *Surface Particles*

- **Critical particle size modeled in '97/'99 @ 33-50% CD**
- **Silicon suppliers note wafers supplied for 180 nm technology generation apparently function quite well with particles comparable to or as large as CD**
  - Do not confuse what can be shipped (tolerable to IC house) with what needed to ensure optimal IC performance and yield
- ***CoO OPPORTUNITY:***
  - Taking particle size = 90 nm (50% CD at 180 nm node) through 130 nm node may not be as detrimental as previously envisioned due to improved particle distribution (reduced  $\sigma$  and  $\langle x \rangle$ )
  - Specification of particle density required at given technology generation in terms of equivalent, smaller number of particles at larger design rule (inverse square power law) useful from CoO and metrology requirements

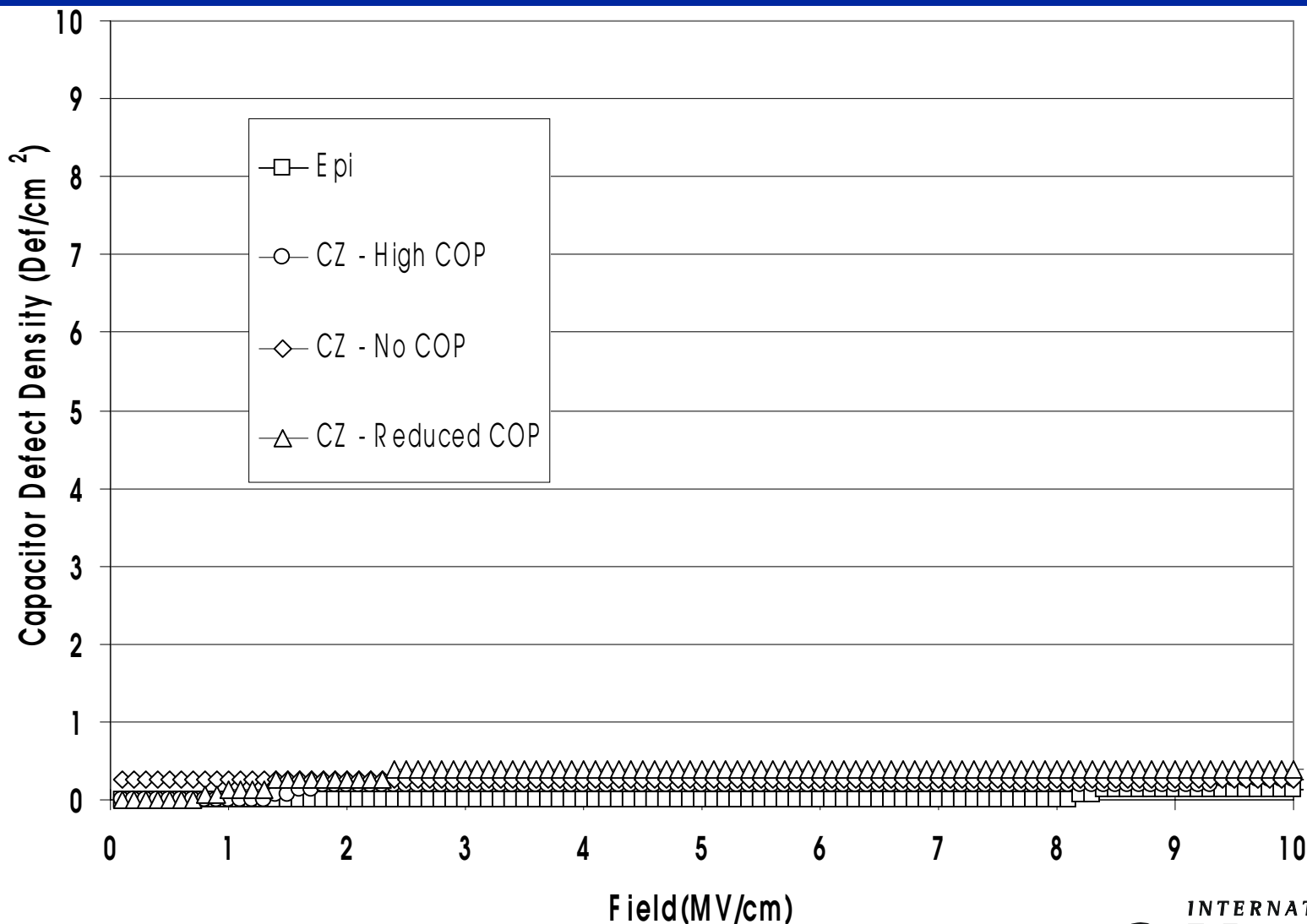
# **Silicon:** *Surface COPS*

- Influence of COPS (and related flow-pattern defects) on GOI becomes negligible (CZ) as  $T_{ox} \Rightarrow \approx 5 \text{ nm}$
- Gate dielectric fabrication typically performed after prior thermal processes, which typically annihilate near-surface COPS
- ***CoO OPPORTUNITY:***
  - Efficacy of utilizing highly “perfect” CZ material - while a scientific achievement - must be re-assessed for polished wafers
  - Epitaxial layers  $> \approx 100 \text{ nm}$  covers up COPS and heavily-doped substrate wafers, furthermore, exhibit essentially no COPS

# Silicon: Surface COPS - Capacitor Defect Density for Varying COPS levels -20 nm Oxide



# Silicon: Surface COPS - Capacitor Defect Density for Varying COPs levels - 5 nm Oxide



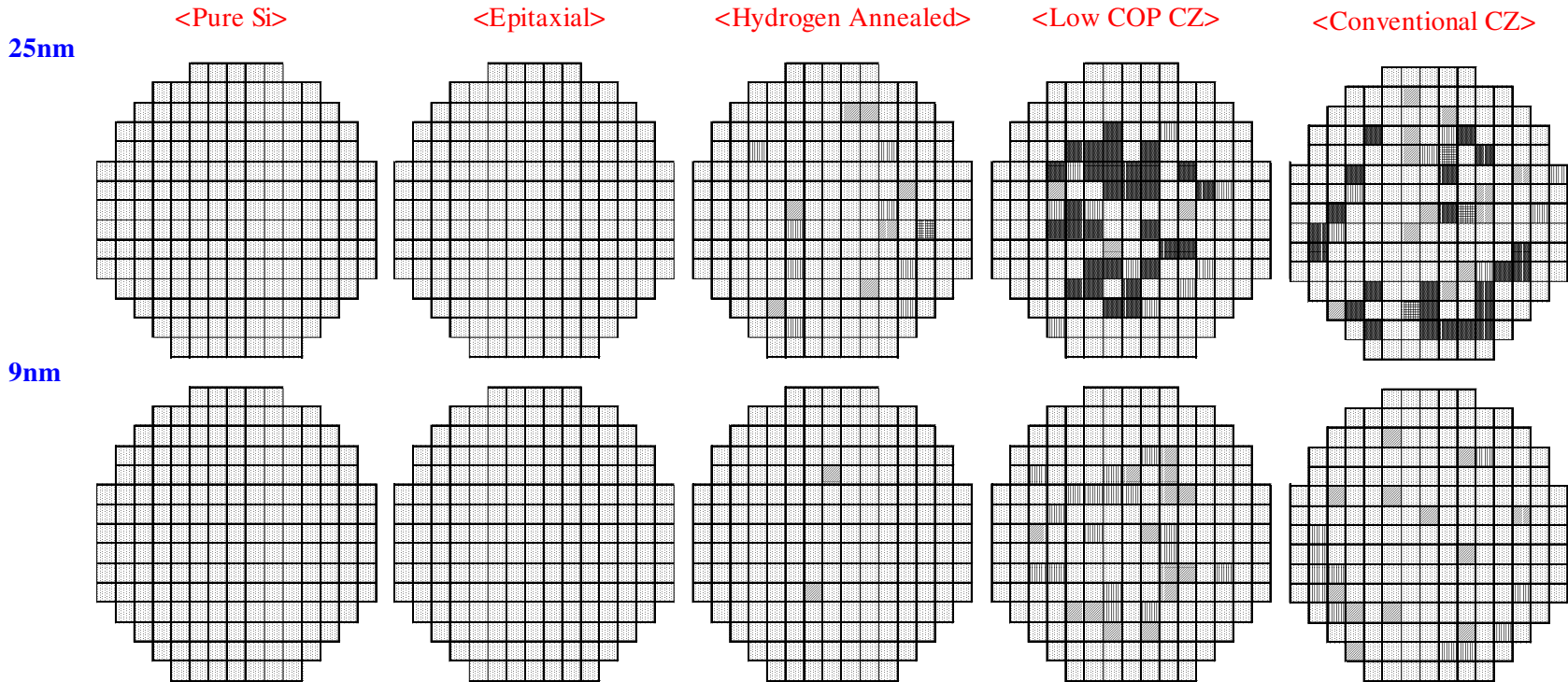
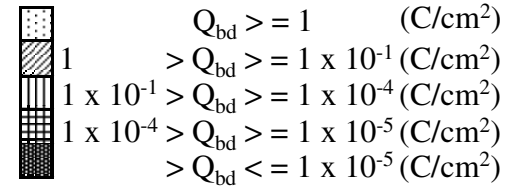
# Silicon: Surface COPs - TDDDB Measurements

After CMOS Simulation

850-900, Pyro oxidation  $T_{ox}=9\text{ nm}, 25\text{ nm}$

Poly-Si gate electrode  $4\text{ nm}^2$

Final Stress Current  $1 \times 10^{-3}\text{ A/cm}^2$





# **Silicon:** *Surface Microroughness*

- Fabrication of 1.0 - 1.3 nm “SiO<sub>2</sub>” gate dielectric with  $R_{\text{RMS}} \approx 0.15 \text{ nm} \pm 0.02 \text{ nm}$  achieved on epitaxial silicon (initial  $R_{\text{RMS}} \approx 0.07 \text{ nm}$ ) via modified NH<sub>4</sub>OH + H<sub>2</sub>O<sub>2</sub> wet clean
- Utilization of UV-Cl<sub>2</sub> clean reduced  $R_{\text{RMS}}$  to  $\approx 0.1 \pm 0.01 \text{ nm}$  (epi wafers), with significant improvements in both  $Q_{\text{BD}}$  and increased (effective) tunneling barrier height
  - Oxide thicknesses  $\approx 1.3 - 4.0 \text{ nm}$  exhibited similar  $R_{\text{RMS}}$  using UV-Cl<sub>2</sub>
  - Both roughening and smoothing can occur as independent mechanisms under some oxidation conditions
  - Influence of cumulative thermal processing on  $R_{\text{RMS}}$  during IC fabrication requires cognizance
- ***CoO OPPORTUNITY:***
  - Viability of driving initial surface  $R_{\text{RMS}} < 0.1 \text{ nm}$ , readily achieved today, may not be justified

# Silicon: *Surface Flatness*

- **SFSR metric typically results in flatness value  $\approx$  one technology node smaller than SFQR metric (same field size)**
  - Greater topographic accommodation of scanners than steppers
  - Scanners, rather than steppers, used at most critical process levels
- **Wafer flatness continues to be perturbation to lens aberrations / related lithography tool components**
  - DOF ranges from  $0.7 \mu\text{m} \Rightarrow 0.6 \mu\text{m} \Rightarrow 0.5 \mu\text{m}$  across Roadmap
  - Relentless pursuit of resolution enhancement technologies
  - Development of vertical transistor structures without (eventual) limitations of optical lithography also in progress
- **Flatness metric  $\approx$  CD (dense lines, DRAM 1/2 pitch, ITRS)**
- ***CoO OPPORTUNITY:***
  - Expand earlier SEMI epitaxial specification with  $\text{SFQR} > \text{CD}$
  - Pragmatic solution:  $\text{SFQR} \approx 30\%$  greater than CD

# Agenda

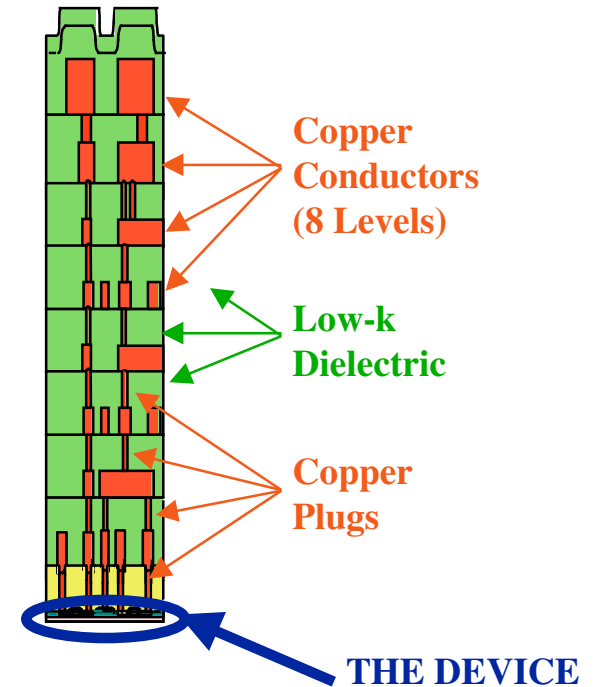
- Introduction
- International Technology Roadmap for Semiconductors

## ➤ Silicon

- Surface
  - Metals
  - Particles
  - COPs
  - Microroughness
  - Flatness
- Bulk
  - Oxygen / Gettering Centers
  - Resistivity
- Epitaxy
- Large Diameter Wafers
- SOI

## ➤ Summary

100 nm High End Microprocessor



1% of the thickness with  
60% of the issues

# Silicon: *Gettering - Motivation*

Gettering of Metal Impurity  
during IC Manufacturing  
Process

**EG (Extrinsic Gettering)**  
Poly-Si Deposition,  
Back Side Damage, *etc.*

**IG (Intrinsic Gettering)**  
Oxygen related defects

**300 mm** CZ Silicon Wafers  
( Next Generation Advanced Wafers)

**Both Sides Polished**

**Oxygen precipitation behavior may be more  
important in 300 mm wafers**

# **Silicon:** *Bulk Oxygen and Bulk Microdefect Density Centers*

- IG in polished wafer still required to remove deleterious metals inadvertently introduced during IC processing
- $\pm 2$  ppma  $O_i$  variation ( $O_i$  range  $\approx 18 - 31$  ppma) may be sufficient to ensure bulk defect control/homogeneous IG
- Adequate wafer strength and resistance to warpage, along with denuded-zone width control, also required
- ***CoO OPPORTUNITY:***
  - Although methodologies developed wherein IG independent of  $O_i$  — essentially dependent on local vacancy concentration in thermally treated wafer — utilization of  $p^+$ ,  $p^{++}$  epitaxial substrates offers effective gettering system via Fermi effect

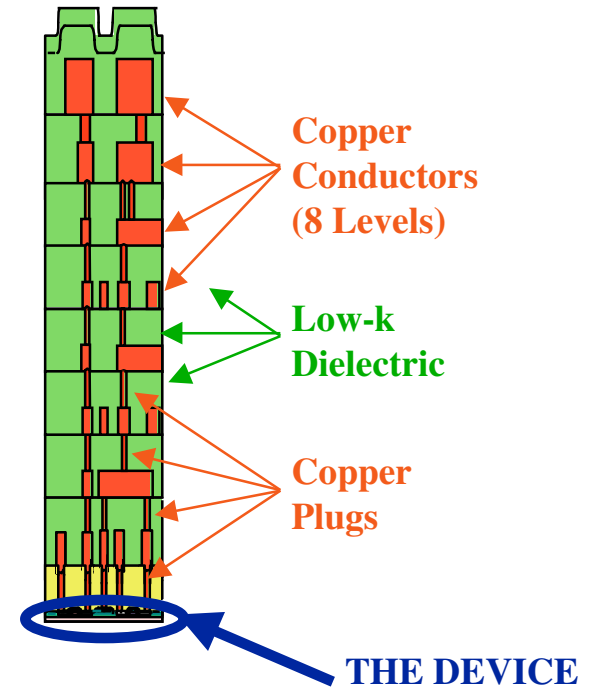
# Silicon: *Bulk Resistivity*

- **Utilization of multiple-well structures fabricated by ion implantation de-couples transistor from original silicon material characteristics**
  - Transistor exhibits less sensitivity to initial substrate resistivity, tolerance and uniformity for both CZ and epitaxial wafers
- **Nominal substrate doping for epitaxial wafers  $\approx 5 - 10$  mohm-cm to ensure latch-up control**
  - Utilization of shallow trench isolation (STI) rendering classical concerns for latch-up, such as  $n^+ - p^+$  spacing (admittedly becoming smaller) moot
- ***CoO OPPORTUNITY:***
  - Substrate resistivity ranges  $> \approx 20\%$  may not be inappropriate

# Agenda

- Introduction
- International Technology Roadmap for Semiconductors
- Silicon
  - Surface
    - Metals
    - Particles
    - COPs
    - Microroughness
    - Flatness
  - Bulk
    - Oxygen / Gettering Centers
    - Resistivity
  - Epitaxy
  - Large Diameter Wafers
  - SOI
- Summary

100 nm High End Microprocessor



1% of the thickness with  
60% of the issues

# Silicon: *Epitaxy*

## ➤ Reduction of epitaxial-to-polished wafer cost ratio for 300 mm diameter wafers favors

- Continued utilization for logic applications
- Consideration for memory applications
  - Conventionally manufactured on lower cost CZ wafers

## ➤ *CoO Opportunity:*

- Development of highly “perfect” CZ material - while a significant scientific achievement - may require consideration of its viability for future generations of ICs, especially as substrates for epitaxial wafers
- Efficacy of utilizing highly “perfect” CZ material for polished wafers must also be re-assessed



# **Future Materials Directions:**

## *Large Diameter Wafers*

- **Conversion to 300 mm wafers began slowly in 1999 with peak conversion anticipated  $\approx$  2002 - 2003**
- **ITRS projections of wafer diameter beyond 300 mm suggests 450 mm may be next appropriate size (2014)**
  - Economic issues may become overwhelming for 450 mm
  - Technology barriers show-up after rising costs have gone beyond bounds of economic sense\*
- **Acceleration of technology generations and related economic factors may cause introduction of 450 mm wafers to occur later than projected**
- **Paradigm shift in preparation of cost-effective silicon substrates required**

# Fab Issues / Opportunities

- **Fab yield**
- **Scaling**
- **Larger diameter wafer**
- *Overall equipment effectiveness (OEE)*

# **Future Materials Directions:** *Silicon-on-Insulator*

- **SOI does not extend device scaling trend compared to conventional silicon materials\***
- **SOI offers benefits for certain applications compared to conventional silicon materials at given technology node**
- **SOI is entering IC mainstream as material system along with polished and epitaxial wafers, albeit dependent on the application**

\* K. Mistry et al., VLSI Technology Symposium, p. 204-205, 2000

# Materials Science Issues (II)

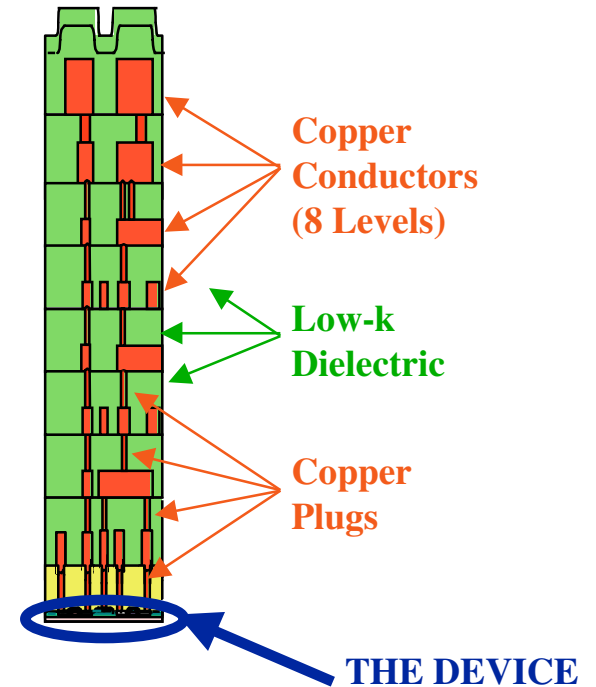
- **Maintaining Moore's law requires cognizance of CoO for engineered, multi-zone wafers, new gate stack materials and introduction of 300 mm wafers**
- **Silicon wafers must be effectively modeled to guide ITRS specification trends**
- **Is silicon wafer a commodity?**
  - Should wafer specifications reflect commodity nature
  - 300 mm wafers driven to historical silicon percent levels of raw goods cost (<10%) to ensure requisite wafer fab CoO

# Agenda

- Introduction
- International Technology Roadmap for Semiconductors
- Silicon
  - Surface
    - Metals
    - Particles
    - COPs
    - Microroughness
    - Flatness
  - Bulk
    - Oxygen / Gettering Centers
    - Resistivity
  - Epitaxy
  - Large Diameter Wafers
  - SOI

## ➤ Summary

100 nm High End Microprocessor

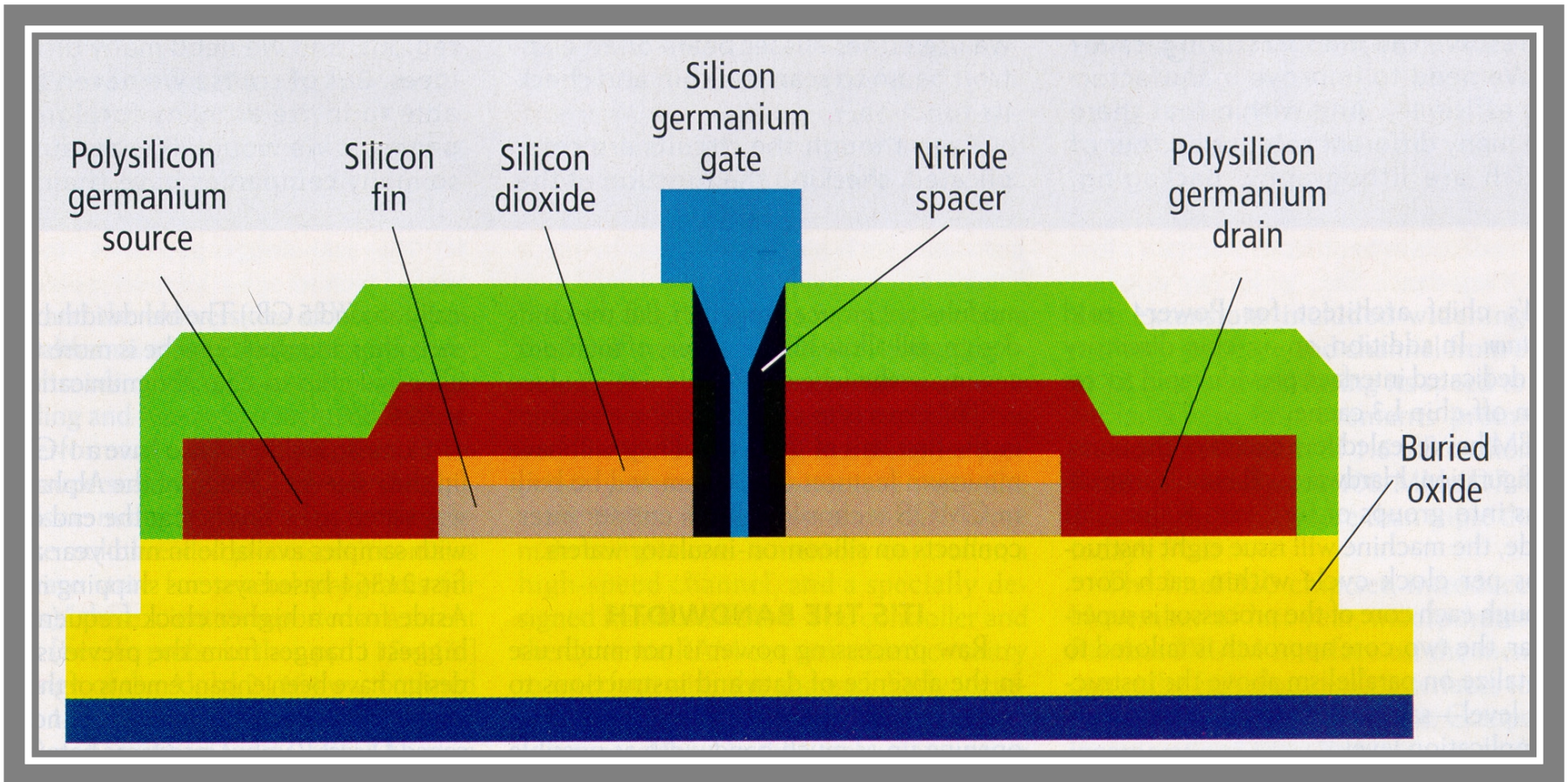


**1% of the thickness with  
60% of the issues**

# Summary - Device Structures

- **Perhaps the greatest revolution in silicon CMOS technology now in progress**
  - Transistor gate materials
  - Interconnect materials
  - 300 mm (and larger?) diameter wafers
- **Scaling beyond 100 nm node may bring new gate insulators, electrode materials, process flows, and possibly, new basic device(s)**
  - Vertical transistor
  - Ballistic transistor
  - FinFET
- **Possible pathway to ultimate MISFET postulated**

# Sub 50-nm FinFET:PMOS - (U. Calif., Berkeley)



X. Huang et al., IEDM 67-70 (1999)

NIST - 2000

H. Huff

INTERNATIONAL  
**SEMATECH**

# Potential Solutions / Challenges

## ➤ Materials Selection

- Anticipate no winnowing of polished, epitaxial and SOI wafer approaches **ALTHOUGH**, eventually, SOI may dominate

## ➤ CoO - Wafer Diameter

- Expand interaction with Super Silicon Initiative and maintain coordination amongst Silicon Suppliers and IC houses

## ➤ Model-Based Parameter Specifications

- Rigorous solution requires silicon supplier's distribution and IC yield distribution for specific material property / defect
  - Standards will provide pathway to ameliorate issues

## ➤ Statistical Specifications

- Purchasing wafers based on in-line Silicon Suppliers data, rather than shipment lots data, may require different Silicon Supplier / IC house relationship



# Yield - Defect Density Model

$$\text{Yield}_{\text{DRAM}} = \exp [- D_i R_i T A (\text{CD})^2 ] = 99\%$$

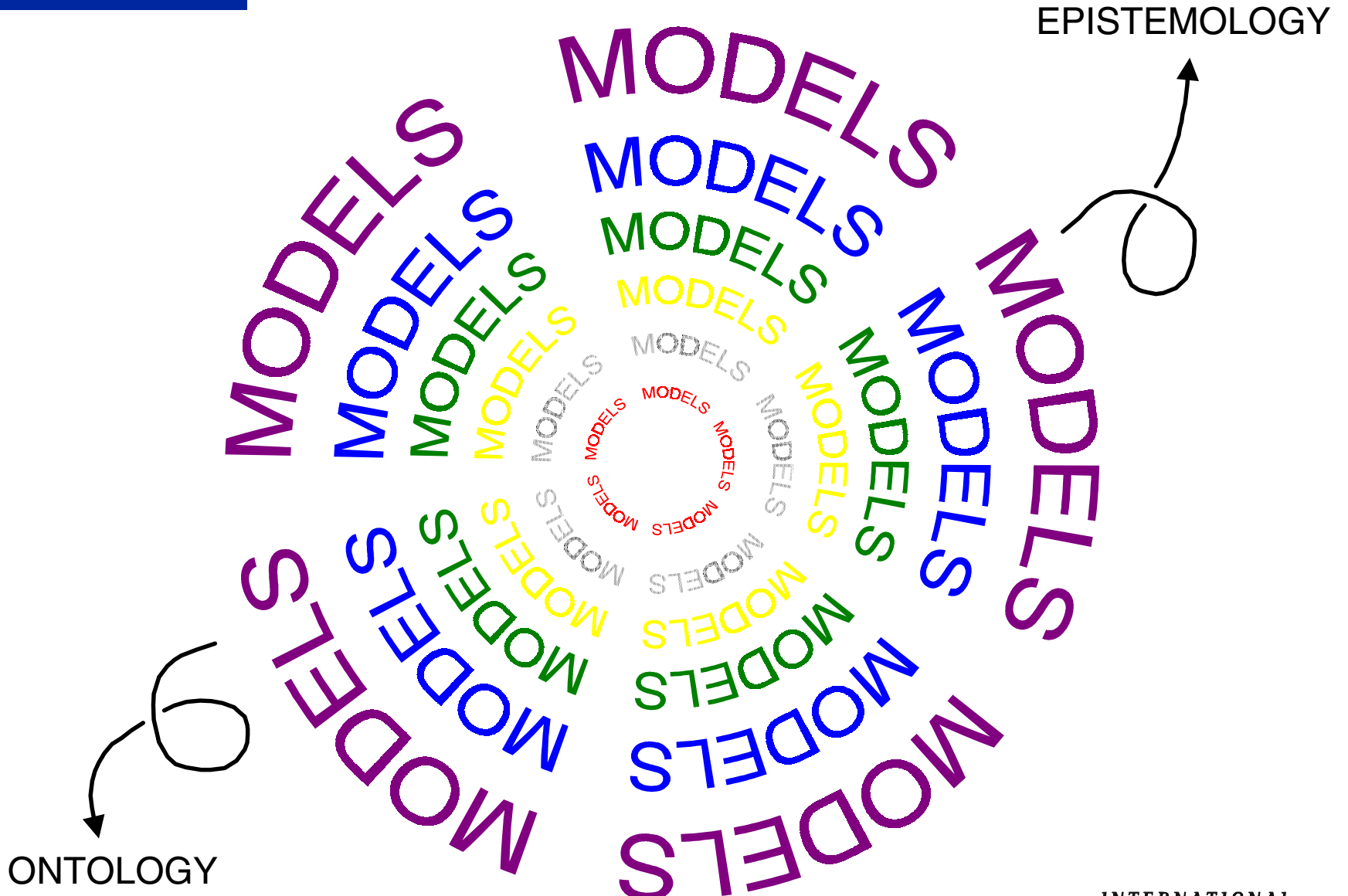
$$\text{Yield}_{\text{MPU}}^* = \exp [- D_i R_i T \beta \delta (\text{CD})^2 ] = 99\%$$

\* Applied to those cases where “A” not known; however, particles, metals, etc. are taken equal to DRAM value

# Summary - Implications for Silicon Specifications

- MOS transistor scaling continues to be critical factor improving IC density and performance
- Smaller dimensions associated with transistor scaling offers opportunity for detailed re-examination of role and usefulness of silicon wafer specifications
- Lesser numbers of various contaminants and defects not necessarily required to ensure improved IC performance, yield and reliability
- In spite of 35 years of IC fabrication, current **models** do not sufficiently establish real requirements for parameter uniformity or effects of parameter variability on IC properties
- Detailed understanding of silicon issues in relation to IC design and process technologies remains significant scientific opportunity with far-reaching CoO implications
- Development of such **models**, in conjunction with statistical specifications, essential to enhance utility of future Roadmaps

# Models



ONTOLOGY

EPISTEMOLOGY

# Acknowledgements

- **M. Alles**
- **W.M. Bullis**
- **G. Celler**
- **R.K. Goodall**
- **D. Gupta**
- **H. Hovel**
- **1999 ITRS Starting Materials team**
- **W. Lin**
- **D. McCormack**
- **T. Messina**
- **P. Tobias**
- **M. Walden**

# Dedication

**This presentation is dedicated to Dr. P.K. Vasudev**