The "Ultimate" CMOS Device: A 2003 Perspective

(Implications for Front-End Characterization and Metrology)

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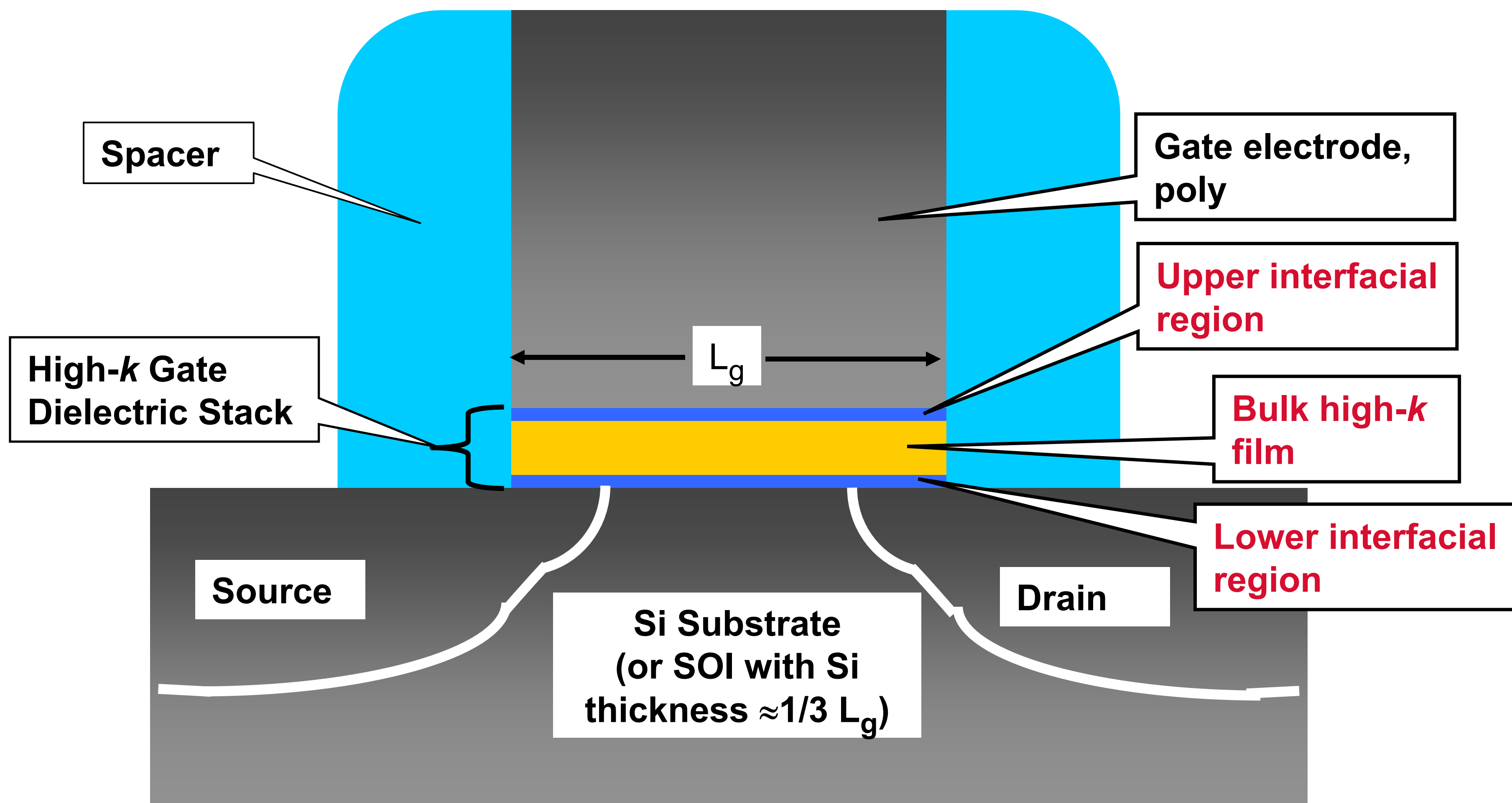
Agenda

- Introduction
  - MOSFET scaling drivers
- Front-end approaches and solutions
- Non-classical CMOS structures
- Summary / Trends
- Acknowledgements

Simplified Cross-Section of MOSFET Transistor Structure



Modified from P.M. Zeitzoff, R.W. Murto and H.R. Huff, Solid State Technology, July 2002

Integrated Circuit Historical Scaling Trends

- **4K DRAM (1974)**
  - SiO_2 thickness ≈ 75-100 nm
  - Channel physical length (L_g) ≈ 7500 nm
  - Junction depth ≈ several μm
    - Power supply = 5 V
- **High-performance MPU (2003) - ITRS: 100 nm technology generation**
  - SiO_2 equivalent oxide thickness (EOT) ≈ 1.1 - 1.6 nm
  - Channel physical length (L_g) ≈ 45 nm
  - Extension junction depth ≈ 25 nm
    - Power supply = 1 V

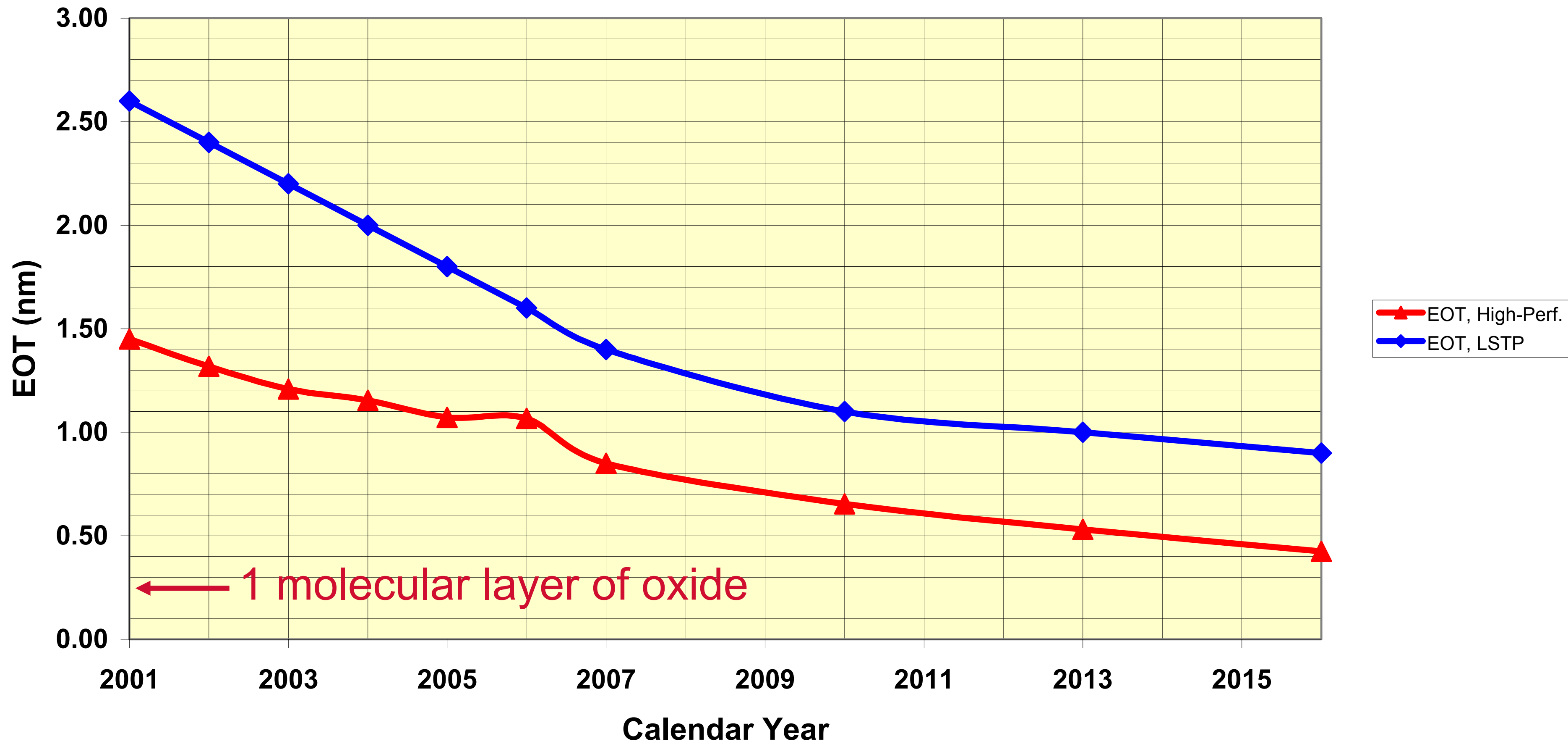
Pervasiveness of Microelectronics Revolution

- **Learning curve (Haggerty)**
  - **Market elasticity (1960's …)**
- **Moore & device scaling (Dennard –1968 -1T/1C DRAM cell)**
  - **Moore's Law**
    - **Number of transistors per chip doubles every year (1965)**
      - **Technology: Feature reduction**
      - **Design: Reduction in number of transistors per memory cell from 6 (SRAM) to 1.5 (DRAM)**
    - **Number of transistors per chip doubles every two years (1975)**
      - **Technology: Feature reduction**
      - **Design: No more reduction in transistors per memory cell possible. Benefits derived only from improvements in layout**
- **Industrial concern in mid '90s as regards fab economic constraints might reduce return on capital investment**
- **Int'l Technology Roadmap for Semiconductors (ITRS)**
  - **Focus to ensure Moore's law by realizing the roadmap**
  - **Expansion of economy (GWP) - market elasticity (2000's) - accommodates IC CAGR**

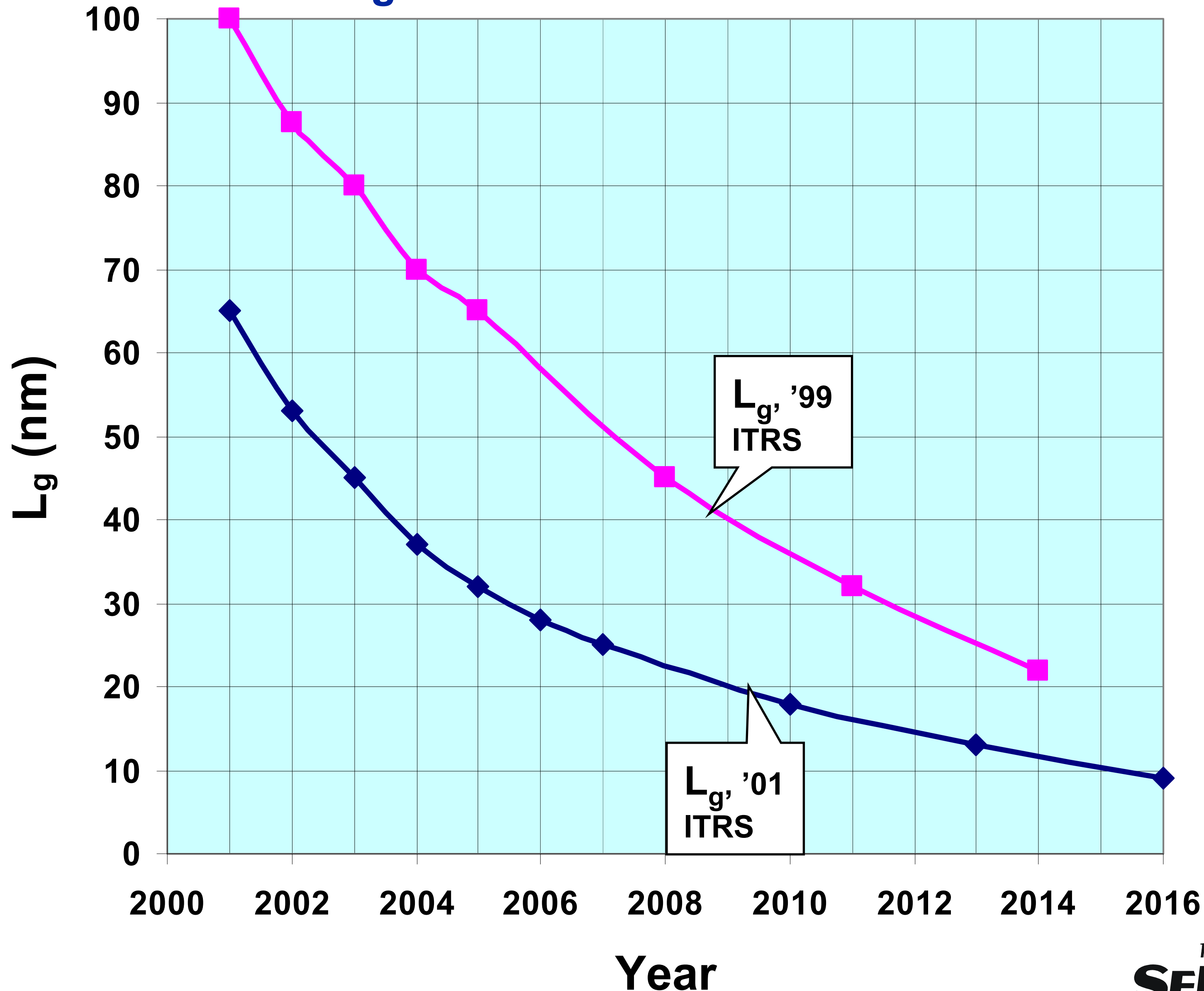
Introduction

- **Moore's law and scaling – lower cost per function**
  - Lower power dissipation per function
  - Increased speed (intrinsic transistor gate delay)
  - Increased transistor and function density
- **MOSFET scaling: processes/structures/tools**
  - Meet both increased I_{on} and low I_{off} (I_{leak}) metrics
  - Reduce I_{gate} for ≤ 1.5 nm gate dielectric
  - Fabrication / control for abrupt, shallow, low sheet resistance S/D extensions
  - Control short channel effects (SCE) ….
- **Potential solutions & approaches:**
  - Material and processes (front end): high-k gate dielectric, metal gate electrodes, elevated source / drain
  - Structural configurations: non-classical CMOS devices
    - Fully depleted, multi-gate SOI structures
    - Challenge of uniformity control in scaling body thickness and width in fully depleted SOI with decreasing L_g

2001 ITRS Projections of EOT for High-Performance Logic and Low Standby-Power



2001 vs. 1999 ITRS Projections of Physical Gate Length (L_g): High Performance Logic



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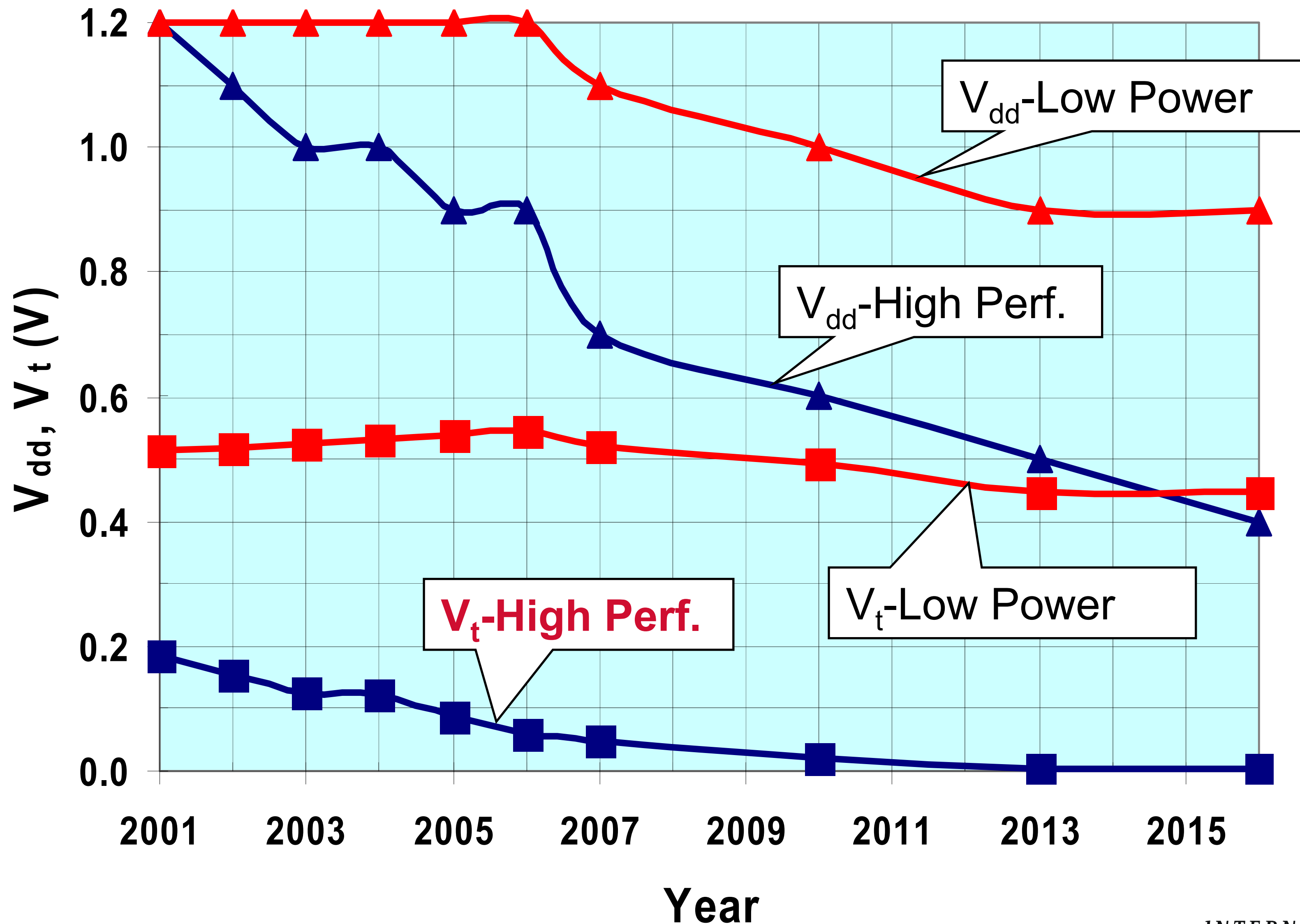
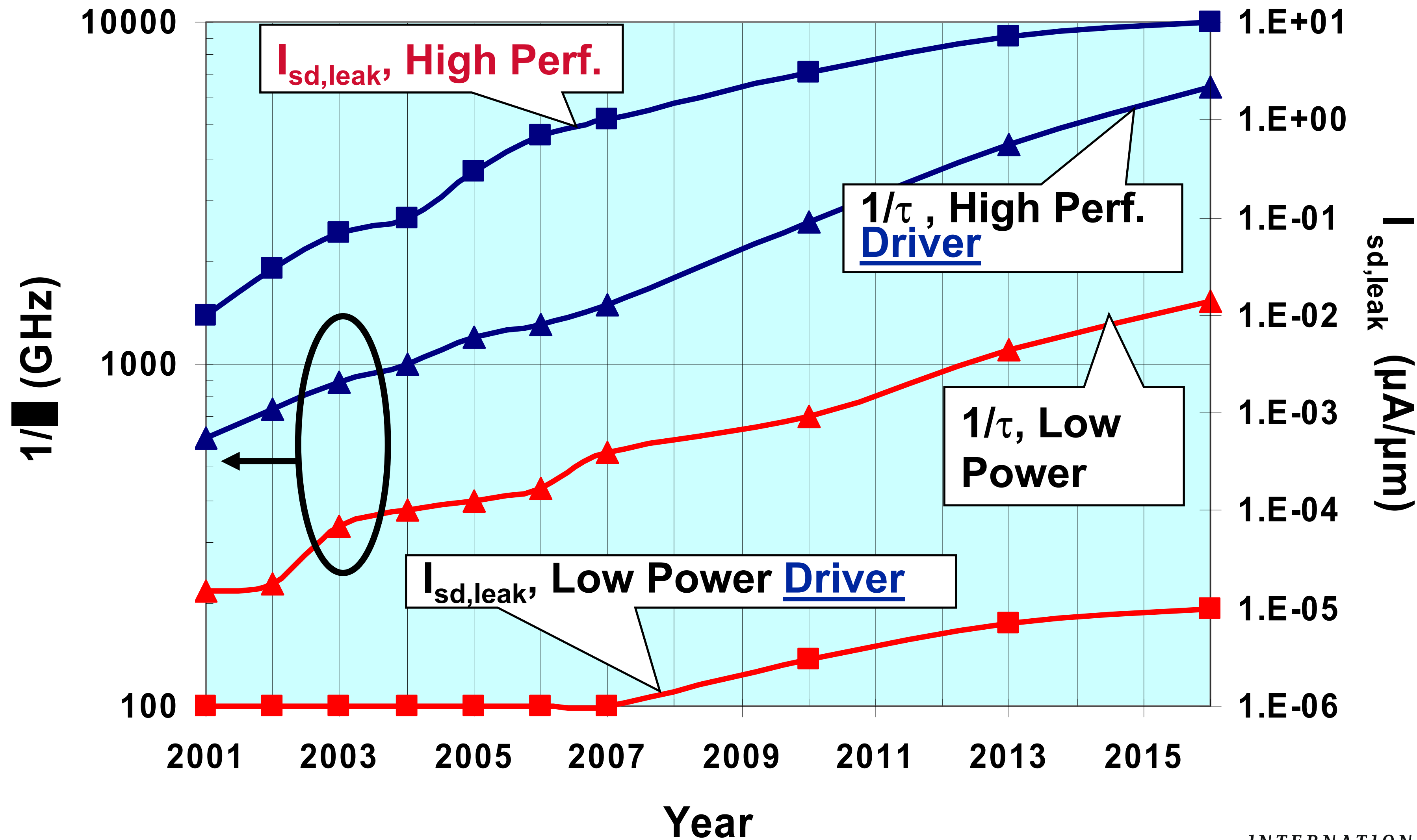
ITRS Projections of V_{dd} and V_t Scaling



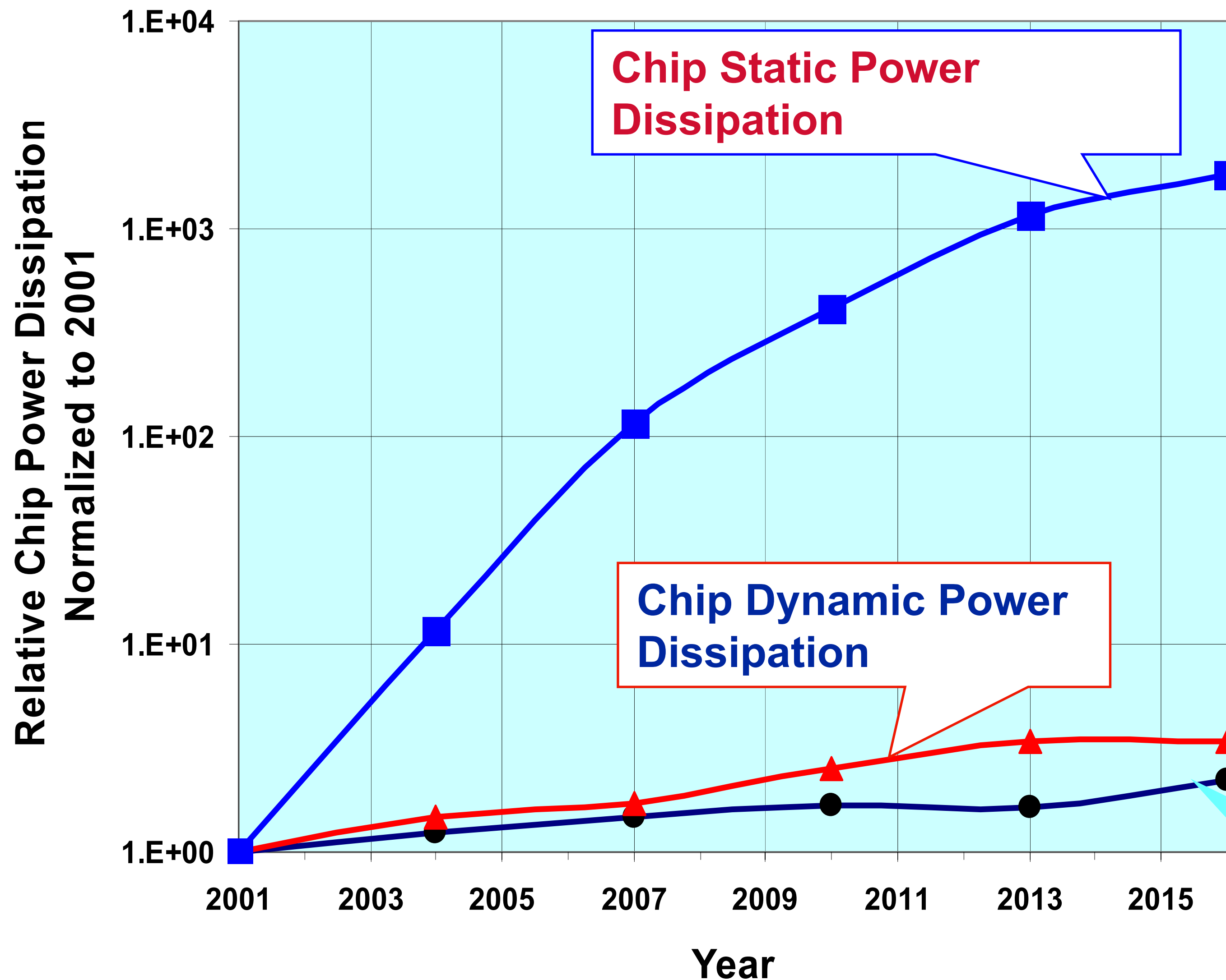
2001 ITRS Projected Scaling of $1/\tau$ and $I_{sd,leak}$ for High Performance & Low Standby Power (under revision)



I_{dsat} Trends

- I_{dsat} trending slightly above 1 mA/μm for nMOS and approaching > 0.5 mA/μm for pMOS
- Concurrently, intrinsic transistor gate delay has trended below sub 1 psec for nMOS and slightly below 1 psec for pMOS as $L_g \leq$ about 20 nm

Relative Chip Power Dissipation for High Performance MPU (Based on 2001 ITRS)



Assumptions:

- Only one type of (high I_{on}, high I_{leak}) transistor and no power reduction techniques
- Simple scaling
- **Unrealistic scenario**, only meant to clearly illustrate static power dissipation issues

Allowable Total Chip Power Dissipation

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Difficult Transistor Scaling Issues

- Previously discussed scaling results involve high-level, idealized MOSFET physics
  - Assumption: highly scaled MOSFETs with required characteristics can be successfully fabricated
- Lateral / vertical MOSFET dimensions (EOT, x_j's, spacer width, etc.) scaling down rapidly with L_g
- Increasing difficulty in meeting transistor requirements with scaling
  - High gate leakage
    - Direct tunneling increases rapidly as T_{ox} is reduced
  - Poly depletion in gate electrode $\Rightarrow$ increased effective T_{EOT}, reduced I_{on}
  - Quantum effect on near-surface charge additionally increases T_{EOT}
  - High $R_{series,s/d}$ $\Rightarrow$ reduces I_{on} in scaling source / drain extension and deep source / drain junctions

Advanced CMOS Scaling Options

Device Type	High-k	Metal Gate MG	Metal Gate DM	Strained Si SiGe	Strained Si Process	R S/D	SOI	Permutations
Scaled Bulk CMOS	X	X	X	X	X	X		47
Partially Depleted	X	X	X	X	X	X	Req'd	47
Fully Depleted	X	X		X	X	X	Req'd	31
Multi-Gate FET								
FinFET - 2 gates	X	X		X		X	Req'd	15
MuG-FET >2 gates	X	X		X		X	Req'd	15

Courtesy of Rinn Cleavelin and Rick Wise, Texas Instruments, Inc.

High-k Gate Dielectric Candidates (and Issues)

- Modest k (<10)
  - Al_2O_3
    - Negative charge, complicated defect structure
- Medium k (10-25)
  - Group IV Oxides - ZrO_2, HfO
  - Low crystallization temperature, unless “doped”
  - Group III Oxides - Y_2O_3, La_2O_3,…
    - Charge, epitaxial configurations
  - Silicates - (Zr, Hf, La, Y, ..) • SiO_4
    - Lower k if too diluted with SiO_2
  - Aluminates - (Zr, Hf, La, Y, ..) • Al_2O_3
    - Charge issue, complicated defect structure
- High k (≥ 25)
  - Ta_2O_5 , TiO_2
    - Low-barrier height

C. M. Osburn & H. R. Huff, Spring ECS Meeting, 2002, abst. #366

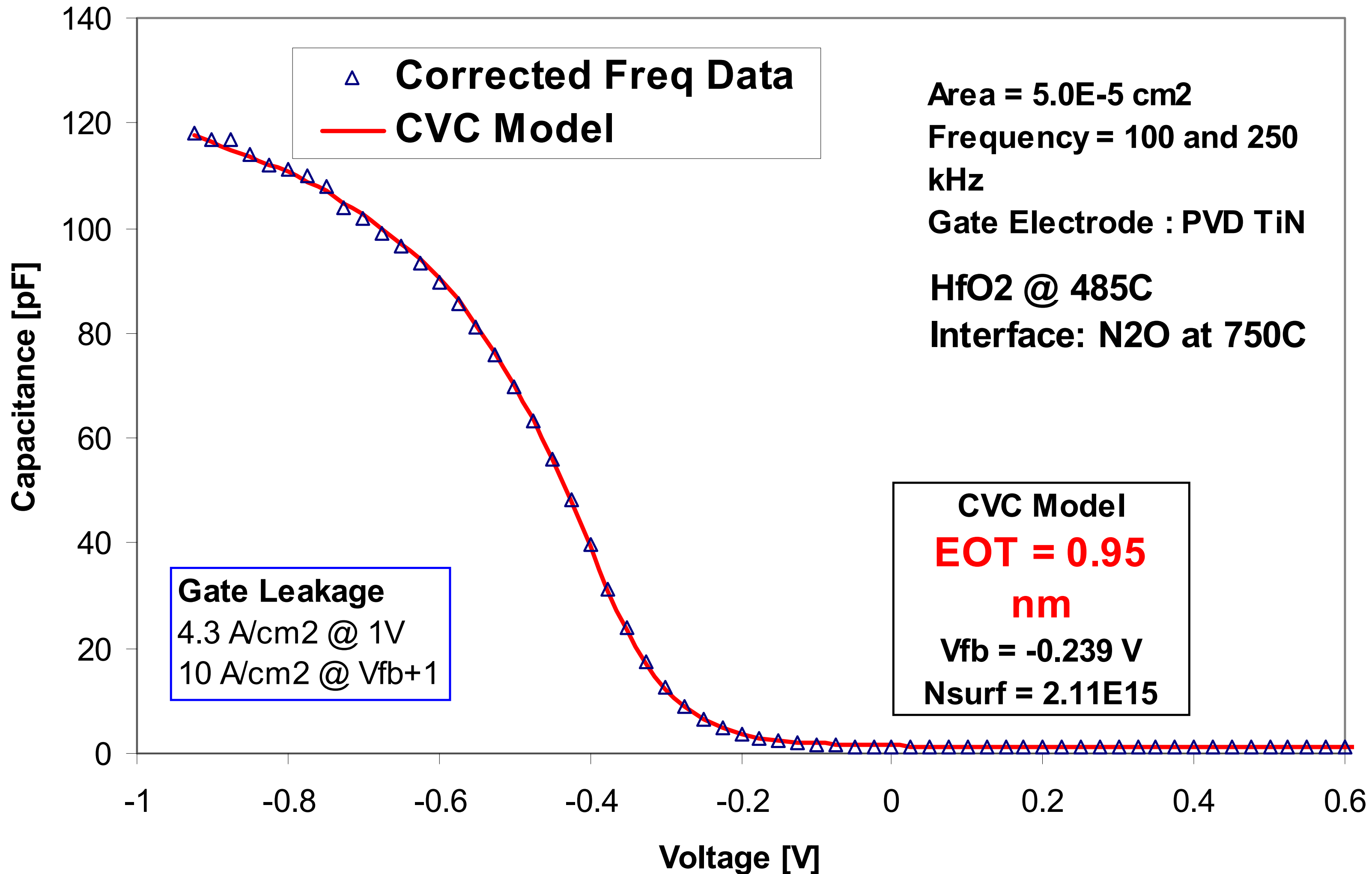
High-K Issues

- Process integration
  - Thermal stability of high-k material
    - Retain high-k performance with planar CMOS flow (S/D anneal temperature, ambient, oxygen partial pressure, etc.,)
      - "Replacement gate" flow useful to quickly assess materials
  - Thermal, chemical compatibility with polysilicon
    - Boron penetration
    - Metal electrode may be required
  - Interface with both Si substrate and gate electrode
    - Deposition / post process anneals modify interfacial SiO_2 layer, T_{EOT}
- Interface properties: D_{it}, N_t, Q_f, $\mu = \mu$(interfacial SiO_2)
- Leakage, reliability
- Short channel effects (SCE) $\Rightarrow$ fringing field effects
- New material: major challenge

Process - Structure - Property Relation

- Crystalline / polycrystalline
  - Phase structure
    - Epitaxial alignment to substrate
  - Stoichiometry
  - Bond coordination
  - Morphology
  - Interfacial microroughness
- Retention of amorphicity by doping
- Mixed oxide phase separation
- Spatial inhomogeneity / periodicity in energy gap(s)

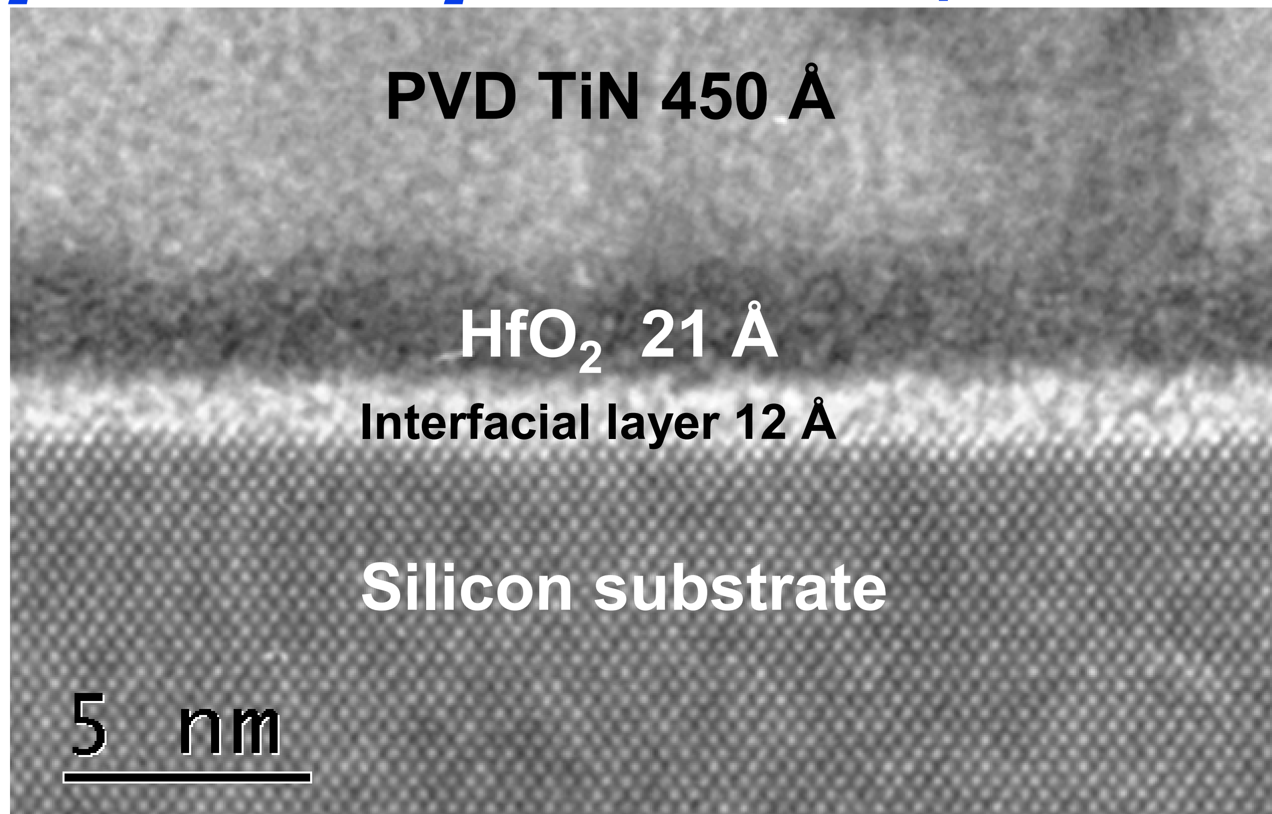
MOCVD HfO_2 CV Curve (EOT = 0.95 nm)



Avinash Agarwal et al., (Alternatives to SiO_2 as Gate Dielectrics for Future Si-Based Microelectronics, 2001 MRS Workshop Series (2001) (reprinted with permission of the MRS Society)

MOCVD HfO_2 TEM (EOT = 0.95 nm)

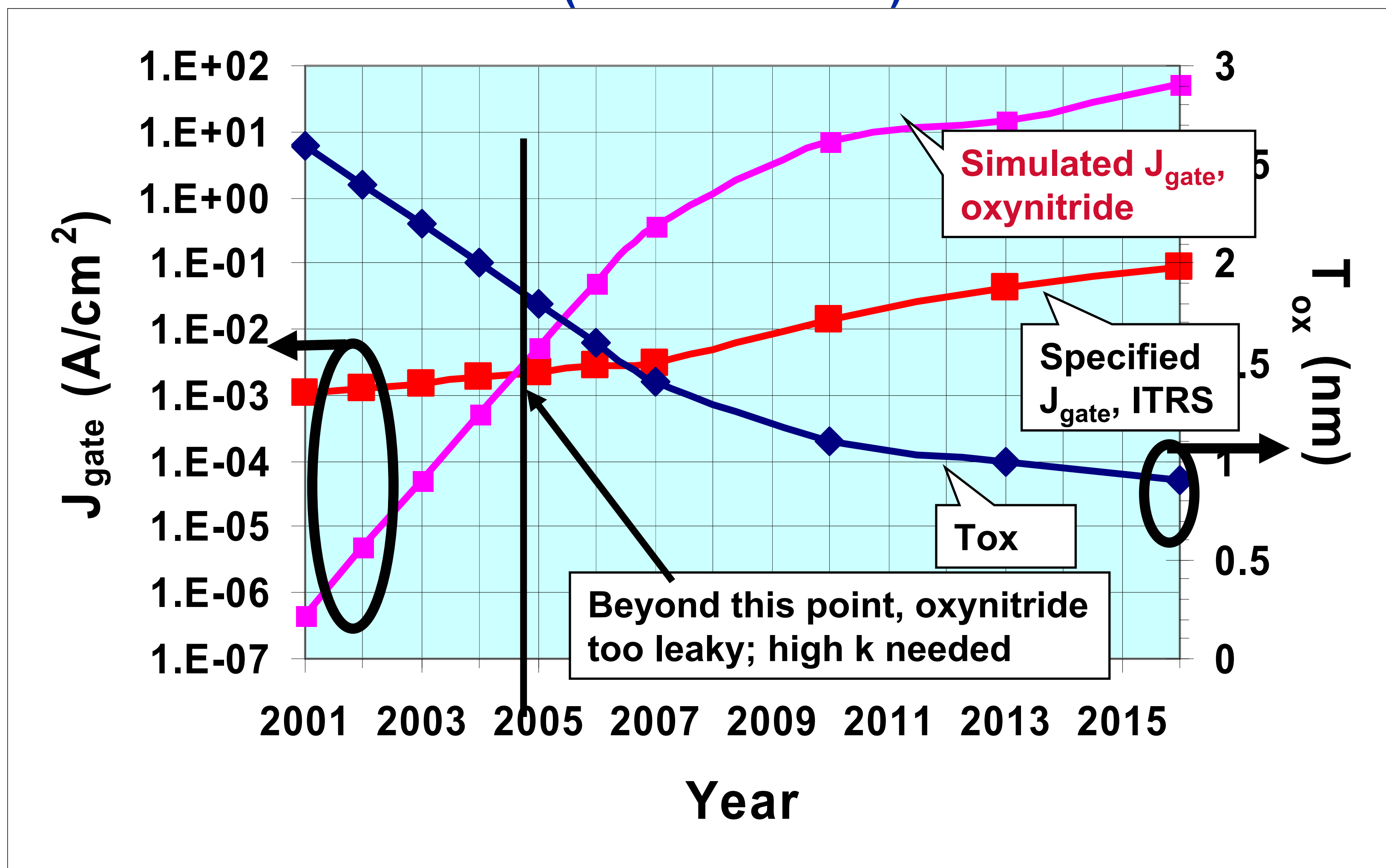
(HfO_2 on HF-last, N_2O-750°C Pre-Deposition Anneal)



- **Effective k for above dielectric stack ≈ 13.5**
- **k for interfacial layer may be significantly greater than SiO_2 indicating reaction or intermixing of HfO_2 film with interfacial SiO_2**
- **"High" surface roughness at HfO_2 / TiN interface may contribute to high J_g**

Avinash Agarwal et al., Alternatives to SiO_2 as Gate Dielectrics for Future Si-Based Microelectronics, 2001 MRS Workshop Series (2001) (reprinted with permission of the MRS Society)

2001 ITRS Projections Versus Simulations of Direct Tunneling Gate Leakage Current Density for Low Standby Power Logic (under revision)



Implementation of high-k driven by low standby power logic in 2005

Simulations by C. Osburn, NCSU and ITRS

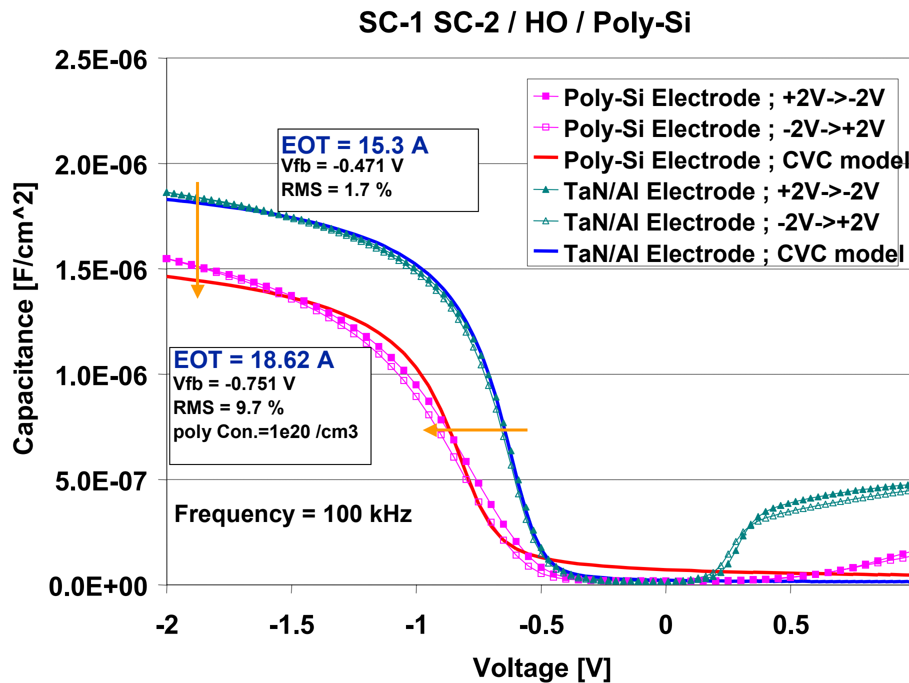
Polysilicon Limitations

- Polysilicon depletion
  - Increases effective "electrical" EOT $\Rightarrow$ reduces E_{ox} and hence inversion charge
  - As EOT is scaled $\Rightarrow$ poly doping must increase
    - Ge:Si facilitates increased B incorporation
- Boron penetration (PMOSFET) in thin oxides
  - Oxynitrides & reduction of $(DT)^{0.5}$ effective now
- Compatibility with high-k
- Gate resistance of thin gates (with silicide)

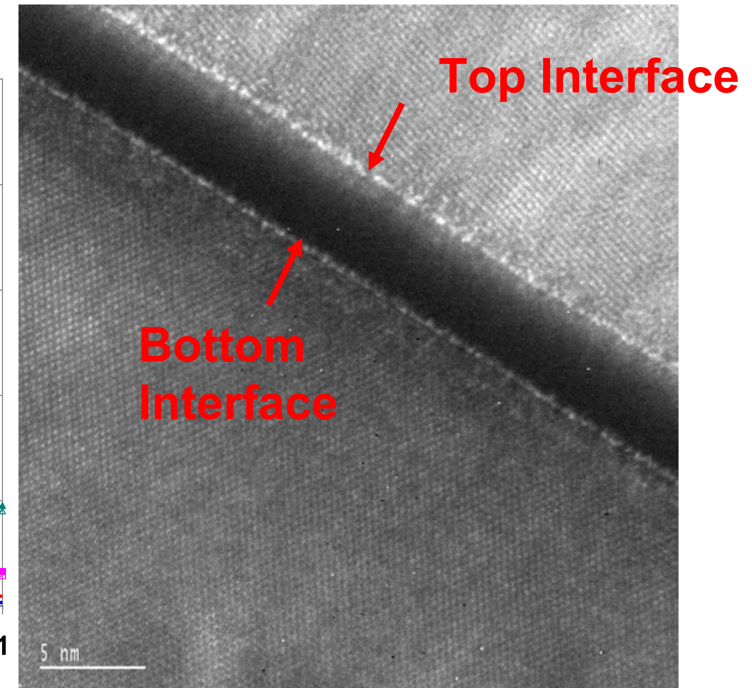
Metal Gate Electrodes

- Metal gate electrodes potential solution when poly "runs out of steam"
  - Implement <≈ 65 nm technology node (2007)
  - No depletion, very low resistance gate, no boron penetration, compatibility with high-k
- Issues
  - Different work functions for PMOS and NMOS
    ⇒ 2 different metals required
    - Process complexity, process integration
    - Utilize one metal: tune work function via N implant (i.e., Mo)
  - Plasma etching / damage of metal electrodes
  - Compatibility with spacer and sidewall profile
  - New materials: major challenge

ALD HfO_2 / Poly-Si vs. HfO_2 /TaN/Al



3 nm HfO_2/poly- Si transistor (Yudong Kim)



- EOT increase by poly-Si gate process comes from both top and bottom interfaces, former suppressed by metal electrode
- CV stretch-out becomes worse in HfO_2 / poly stacks, suggesting degraded interface quality after thermal cycle process

Source / Drain Extension Issues

- Increasingly abrupt, shallow, heavily doped profiles required for successively scaled technologies
  - Needed for optimal devices, especially to control SCE
  - Difficult $\rho_{s,ext}$-$x_{j,ext}$ tradeoffs, especially for PMOS (B) $\Rightarrow$ difficult to control $R_{S/D,series}$

Source / Drain Extension Potential Solutions

- Near-term
  - Ultra-low energy implants (< 1 KeV, B)
  - Rapid Thermal Processing (RTP) and spike anneal: reduces $(DT)^{0.5}$ and thermally enhanced diffusion
    - Role of residual Si_i during "slow" cool-down
  - Increase dose as much as possible $\Rightarrow$ reduced $R_{series,s/d}$
- Beyond 90 nm technology generation
  - Doped, selective epi
  - Co-implant
  - Laser thermal annealing, …

Potential Front-end Solutions for Power Dissipation Problems, High-Performance Logic

- Increasingly common approach to concurrently meet chip power, performance and density requirements to place multiple transistor types on chip ⇒ multi-V_t, T_{EOT}, L_g, X_j…
  - Utilize high-performance, high-leakage transistors only in critical paths - lower leakage transistors elsewhere
  - Improves flexibility for system-on-chip (SOC)
- Electrical or dynamically adjustable V_t devices (future possibility)
- Circuit and architectural techniques: pass gates, power down circuit blocks, etc.

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Device Metrics

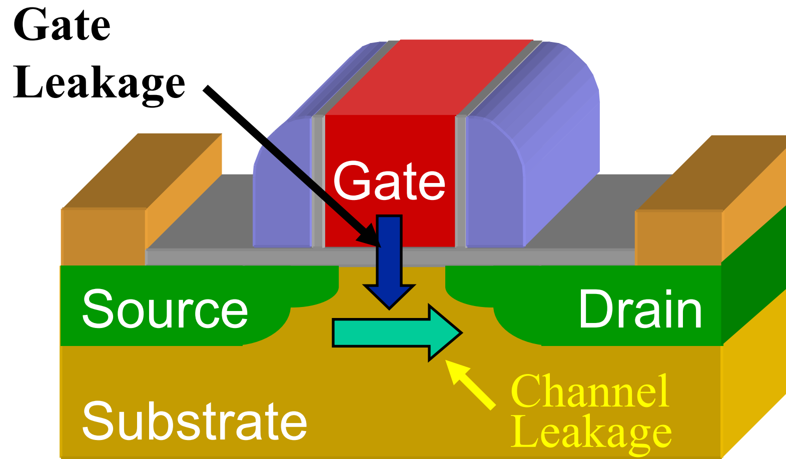
- **Power**
  - $P_{dynamic} = f_{clock} C_{load} V_{dd}^2$ and $P_{static} = N_{tr} W I_{leak} V_{dd}$
- **Intrinsic transistor gate delay (speed)**
  - $\tau = C_{load} V_{dd} / I_{DSAT}$
    - I_{dsat} (maximum saturated drain current)
      - $I_{dsat} = (W/2L_g)(3.9K_oA)(T_{EOT,INV})^{-1} \mu_{eff} (V_G - V_T)^2$ (long-channel, ideal)
      - W and L_g device width and physical gate length
      - $T_{EOT,INV}$ = equivalent oxide thickness in inversion
        - $T_{EOT} = (k_{high\ k} / k_{SiO2}) T_{phys}$
      - μ_{eff} = mobility, generally determined in long-channel device (g_m)
      - $V_G - V_T$ = gate overdrive, where V_G is voltage applied to gate ($V_G \Rightarrow V_{dd}$) and V_T is threshold voltage
- **Transconductance**
  - $g_m = (W/L_g)(3.9K_oA)(T_{EOT,INV})^{-1} \mu_{eff} V_{dd}$ (long-channel, ideal)
  - Sub-threshold swing $\Rightarrow$ Inverse slope of ln I_D versus V_G
- **Drain-induced-barrier-lowering (DIBL)**

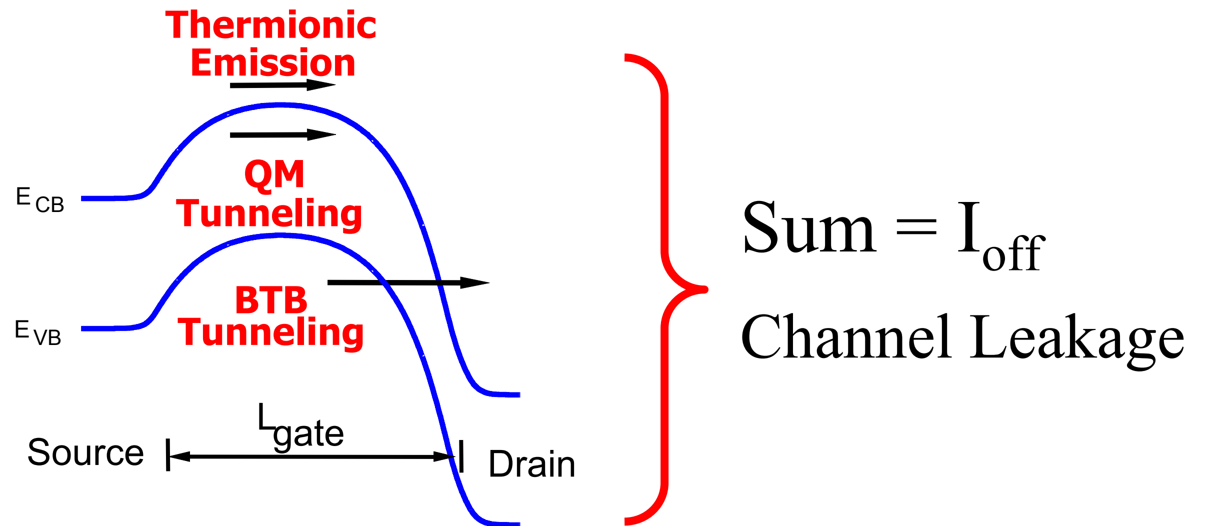
Limits of Scaling Planar, Bulk MOSFETs

- 65 nm technology generation (L_g = 25 nm, 2007) ⇒ beyond
  - Increased difficulty meeting device metrics with classical planar, bulk CMOS (even with material and process solutions: high k, metal electrodes, elevated source/drain ….)
    - Control of SCE
    - Impact of quantum effects
    - Dopant stochastic variations (number and spatial location in channel)
    - Need for enhanced mobility, $I_{d,sat}$
    - Impact of high substrate doping
    - Control of series source / drain resistance ($R_{series,s/d}$)
    - Other contributors

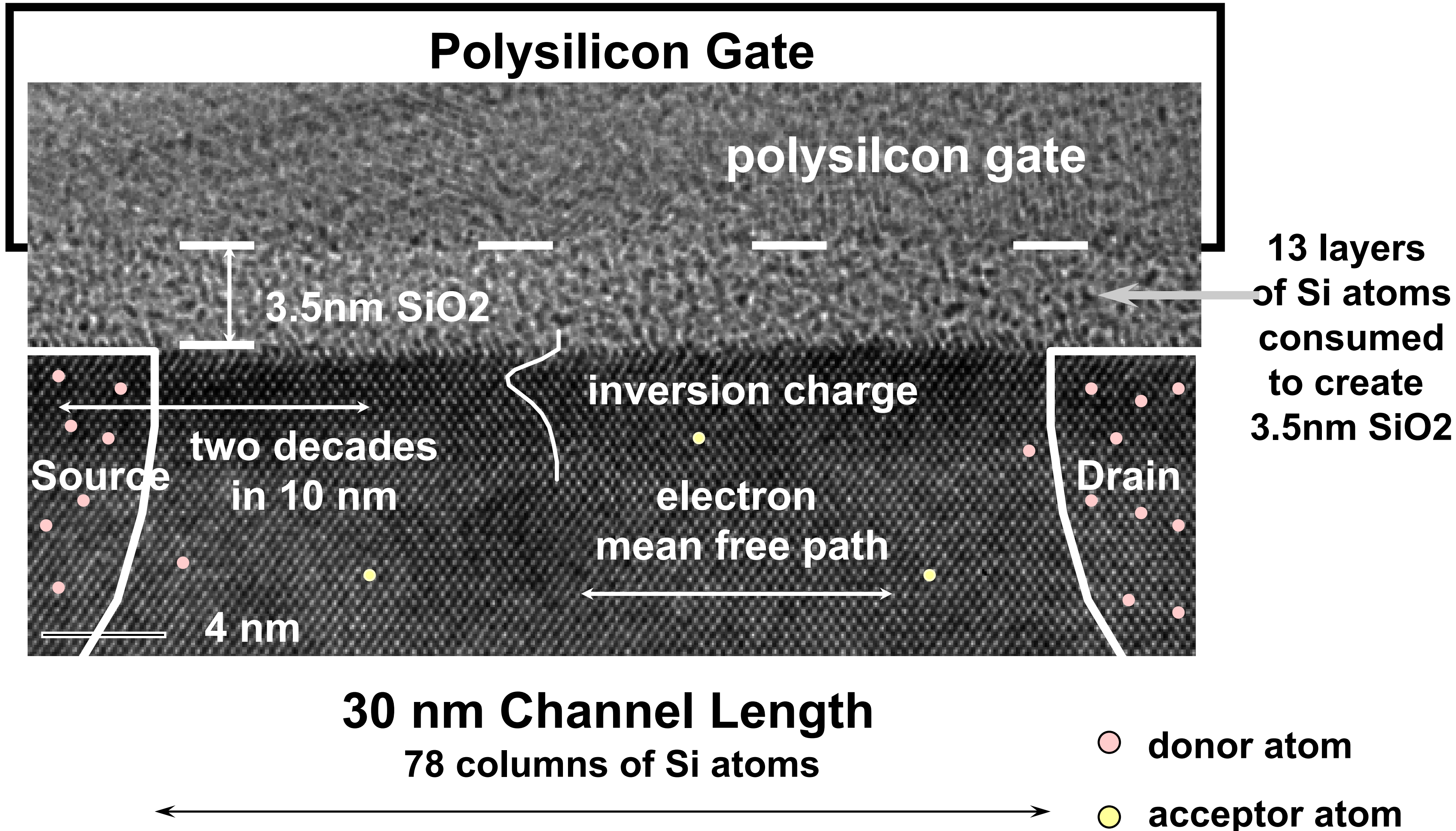
- Alternative structures (non-classical CMOS) may be required
  - Band engineered transistors ⇒ improved transport/mobility
  - Ultra thin body SOI
  - Multi- gate SOI - Including FinFET and Vertical FETs

Electrostatic Scaling - Channel Leakage (I_{off})



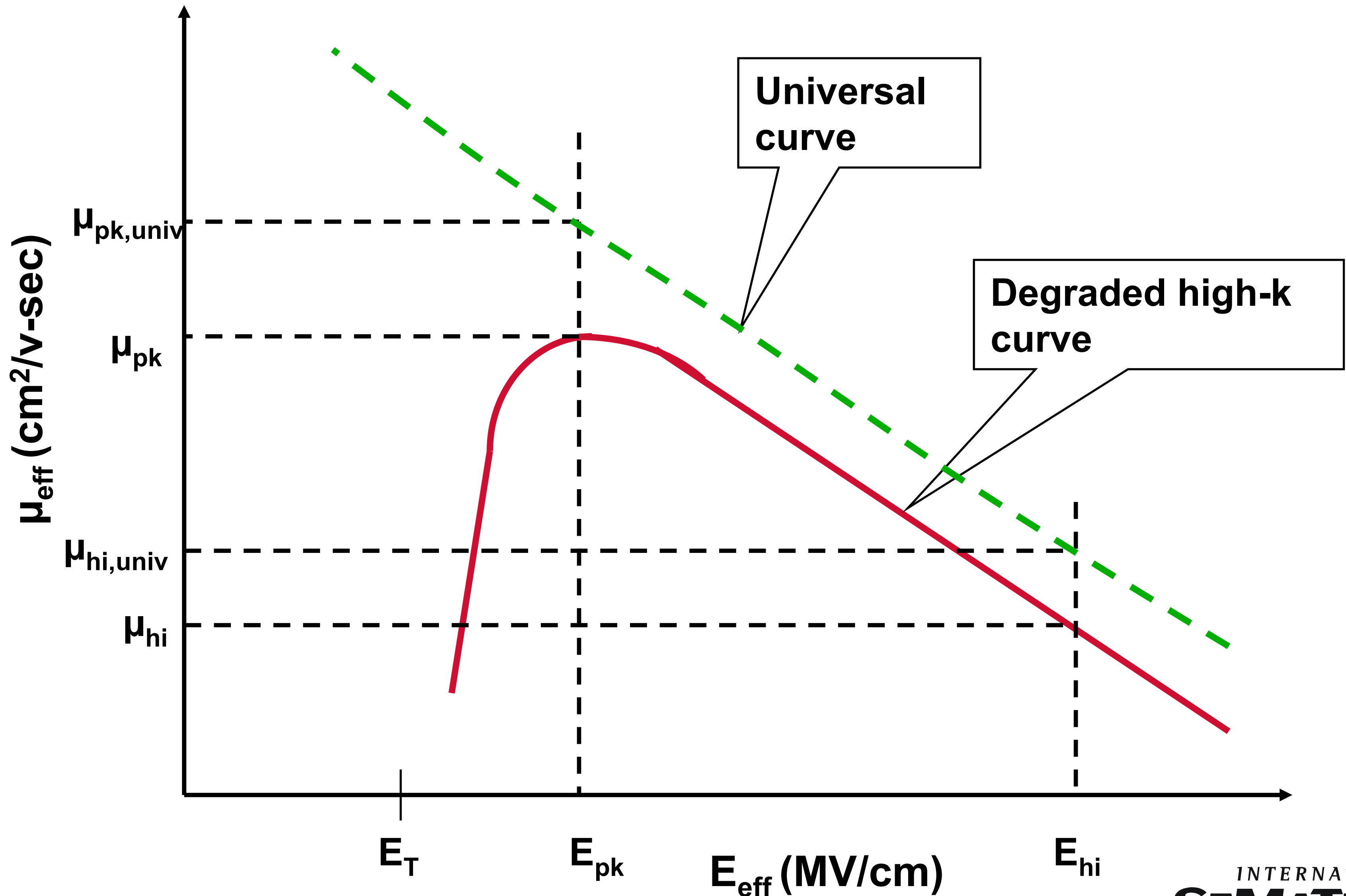


High Resolution TEM Showing 30 nm Channel Length



Courtesy of Yoshi Nishi / Dick Chapman

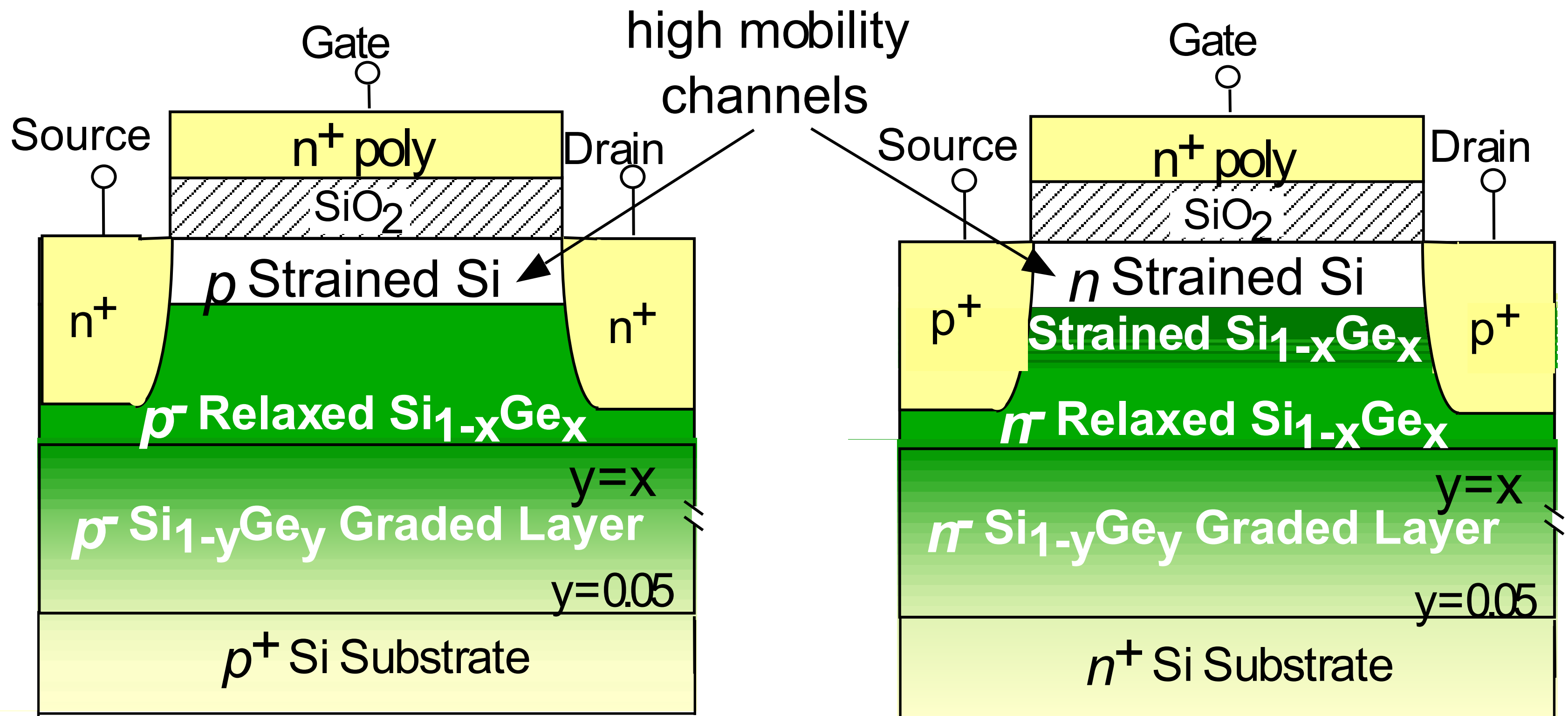
Representative Theoretical and Universal Mobility Curve



Mobility Considerations

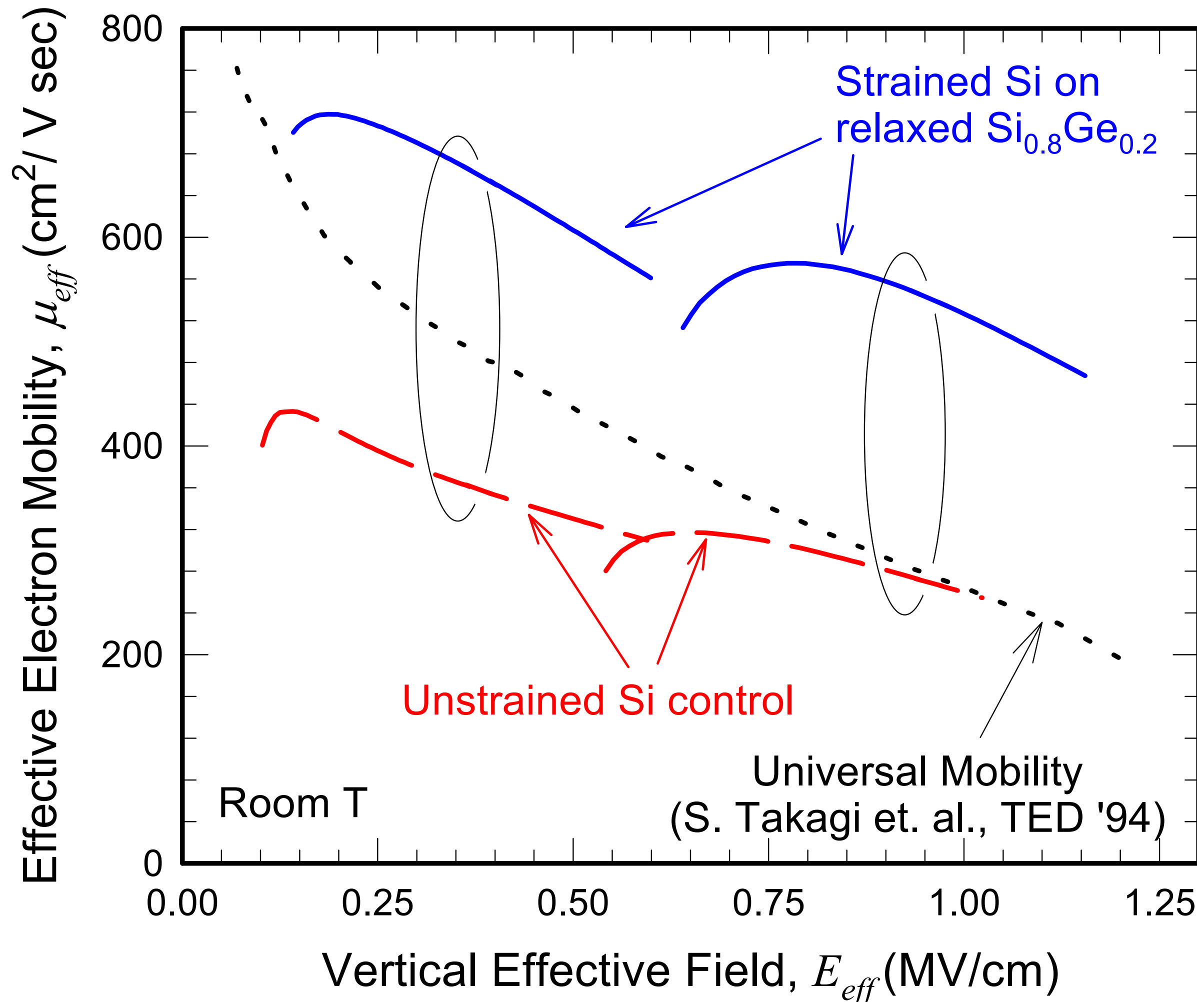
- Theoretical
  - Low electric field
    - Unscreened (by inversion layer free carriers) ionized dopant scattering centers in silicon
  - High electric field
    - Surface acoustic phonons
    - Surface microroughness
      - H x L (where *H* is height of surface undulation and *L* is undulation correlation length)
    - Remote scattering by high-k phonons (modulated by interfacial SiO_2)
- Experimental adders (not presently theoretically modeled)
  - Interfacial and high k bulk traps
  - Crystalline inclusions in amorphous high k gate dielectric
  - N, Al and other elemental (interface) scatterers
  - Remote scattering due to gate electrode
- Universal curve ignores scattering from ionized dopants

Band Engineered MOSFETs: Surface-channel Strained-Si MOSFET Structures



- \+ Increased effective mobility, increased I_{on}
- \- Difficult integration issues, manufacturability
- \- Compatibility with ultra-thin body SOI
- \- Cost

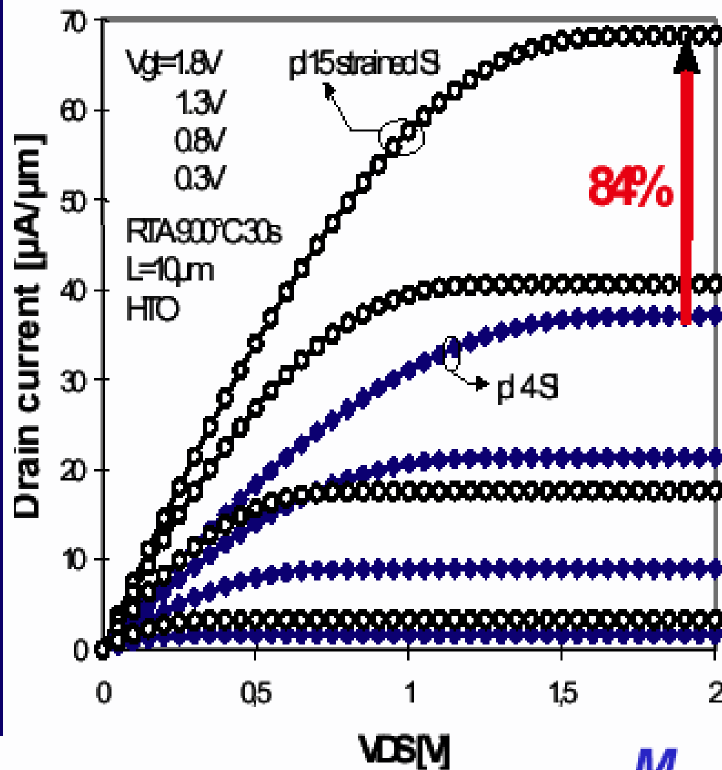
Electron Mobility Enhancement in Strained Si MOSFETs (Rim.et al.. IEDM 1998)

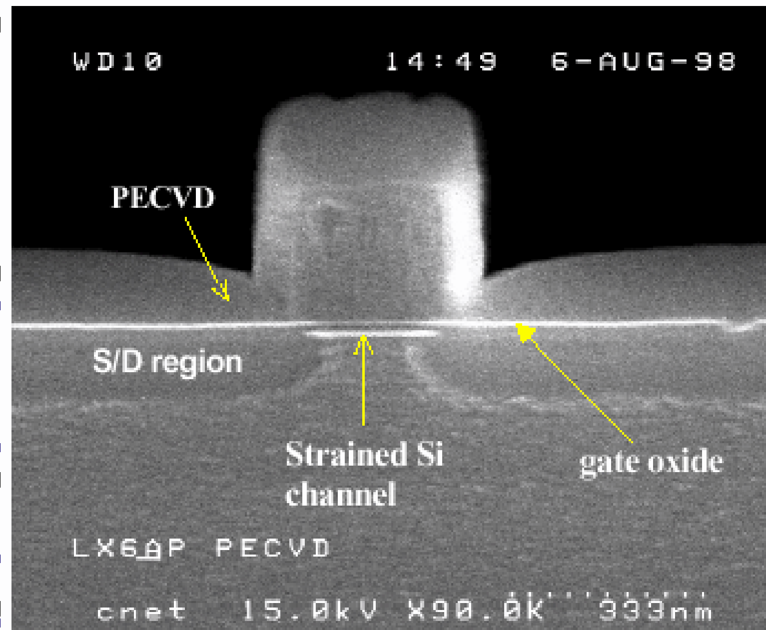


- Electron mobility enhancement of ~ 1.8X persists up to high E_{eff} (~ 1MV/cm)
- Strained-Si allows "moving off" universal mobility curve

Strained Si:Ge

HIGH MOBILITY DEVICES - STRAINED Si CHANNELS:



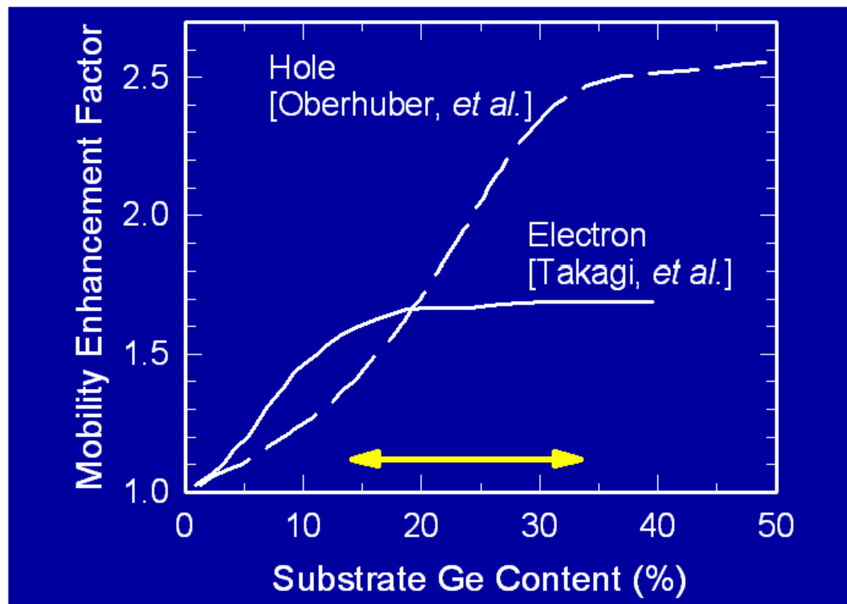


M. Jurczak et al., ESSDERC 1999

SEMICON Europa 2001 - Slide 26

Strained Si Device Structures

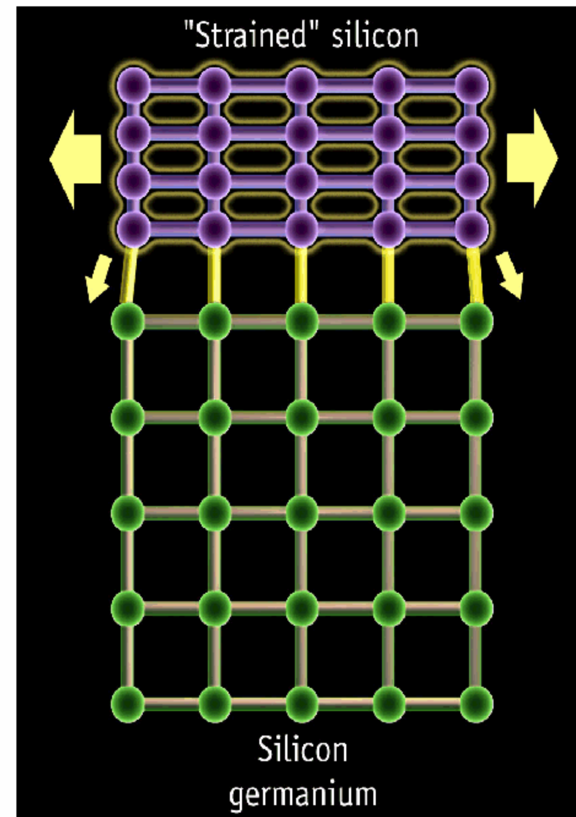
modified band structure of Si under biaxial tensile strain ==> enhanced mobility



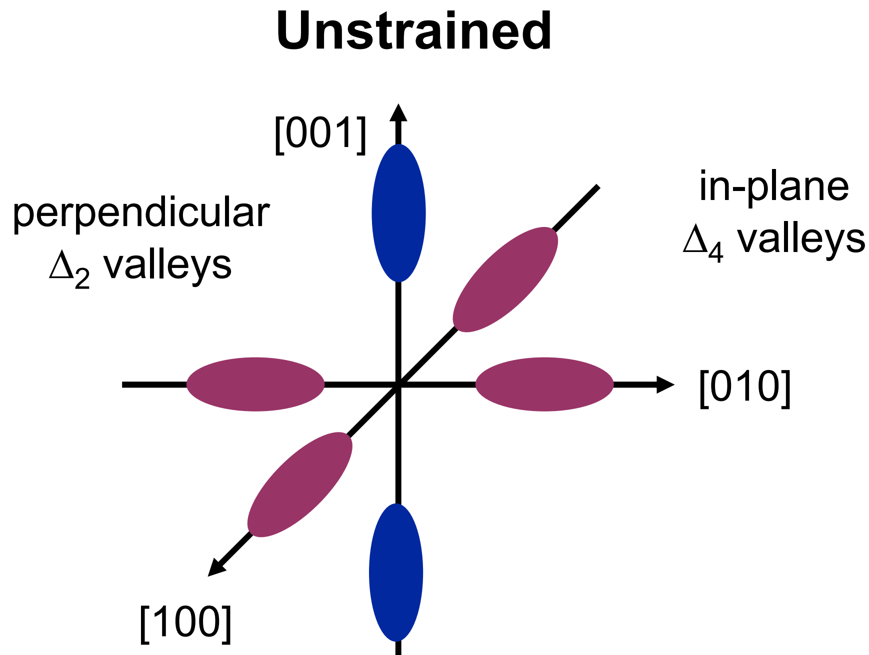
need relaxed $Si_{1-x}Ge_x$ with $0.15<x<0.35$

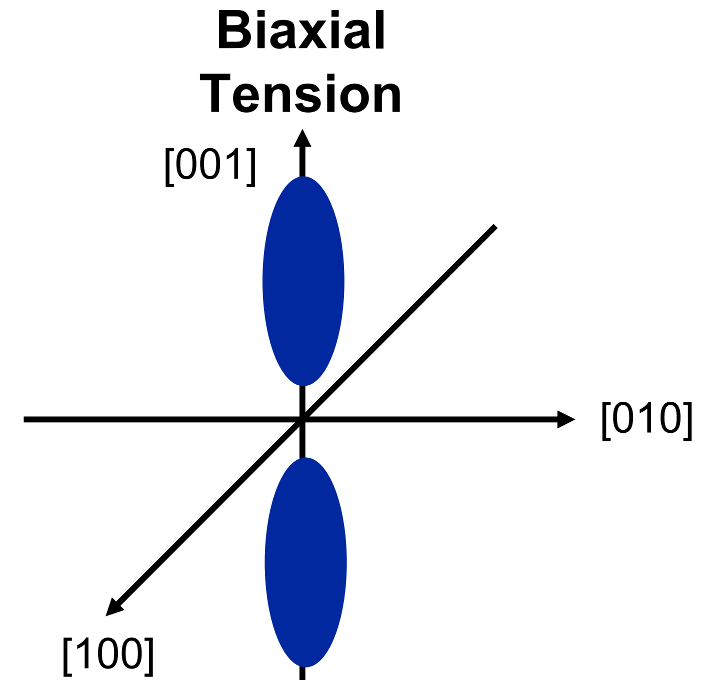
P.M. Mooney, et al., presented at the American Physical Society Meeting, Austin, TX, March 3-7, 2003

Strained Si on SiGe

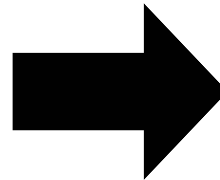


Electron Transport in εMOS™





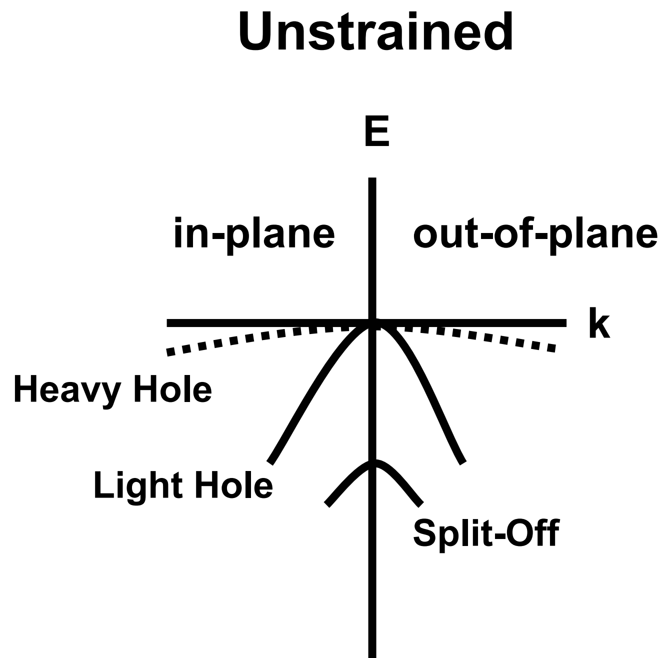
Tensile strain splits conduction band degeneracy

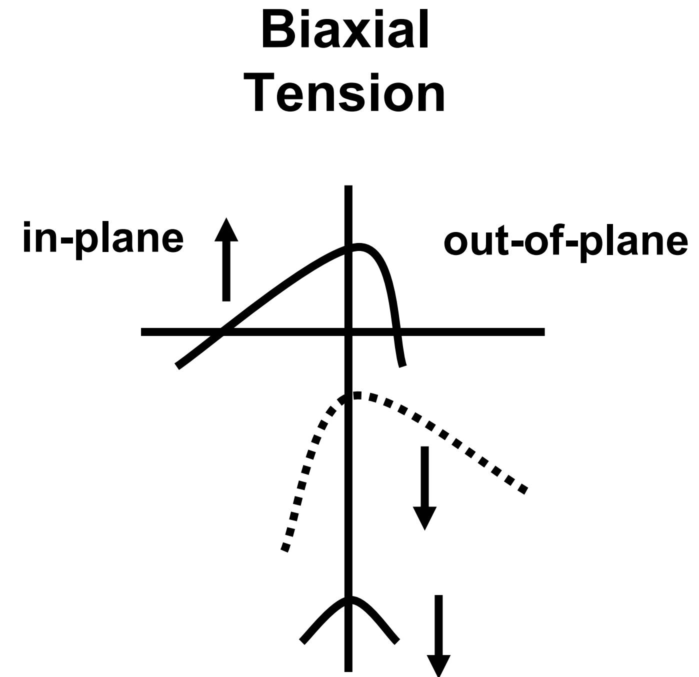


- **Reduced intervalley scattering**
- **Light in-plane effective mass**

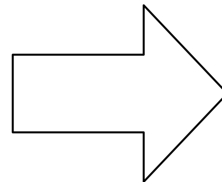
Courtesy of Matt Currie
AmberWave Systems Corp.

Hole Transport in εMOS™





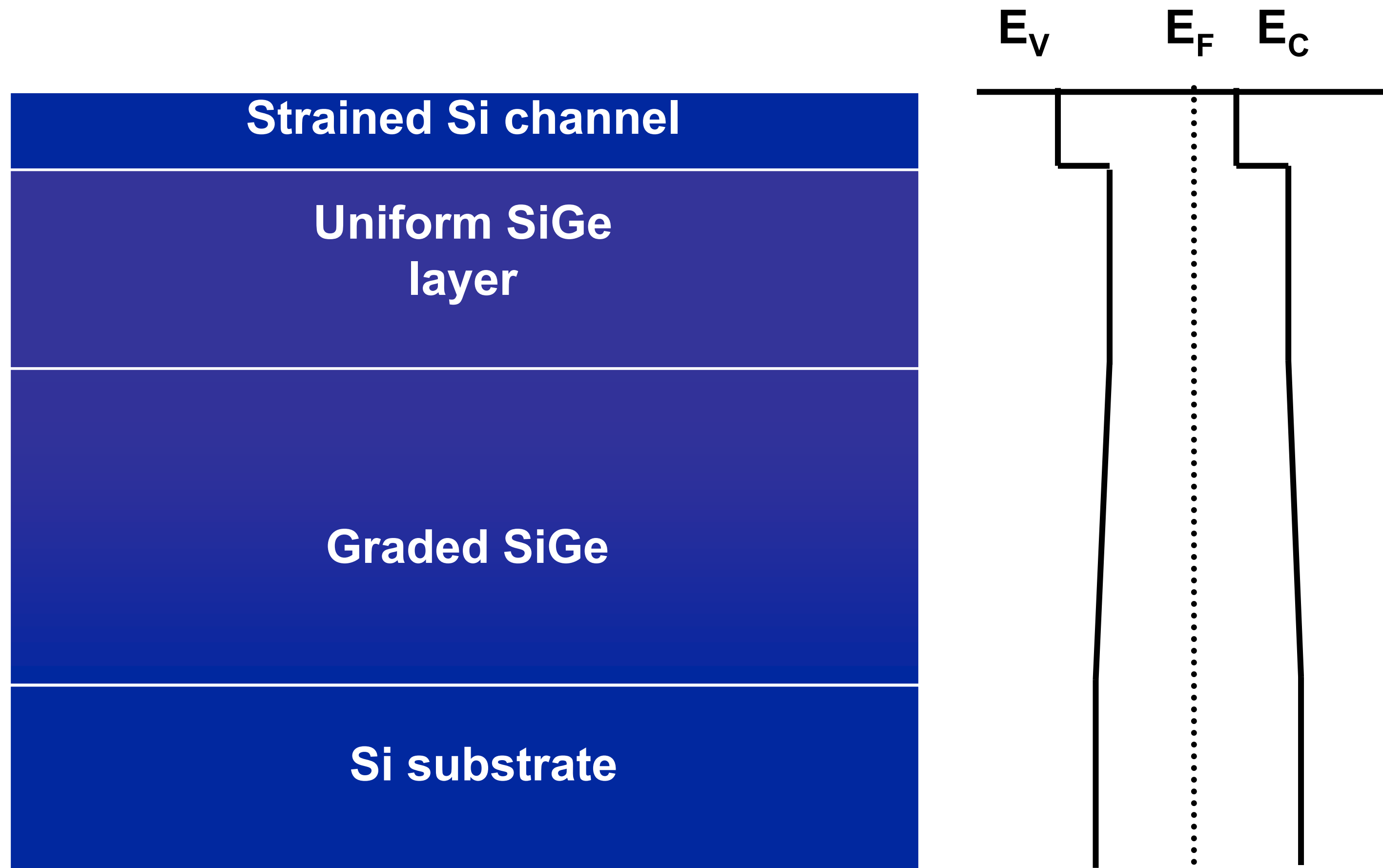
Tensile strain splits valence band degeneracy



- **Reduced intervalley scattering**
- **Light in-plane effective mass**

Courtesy of Matt Currie
AmberWave Systems Corp.

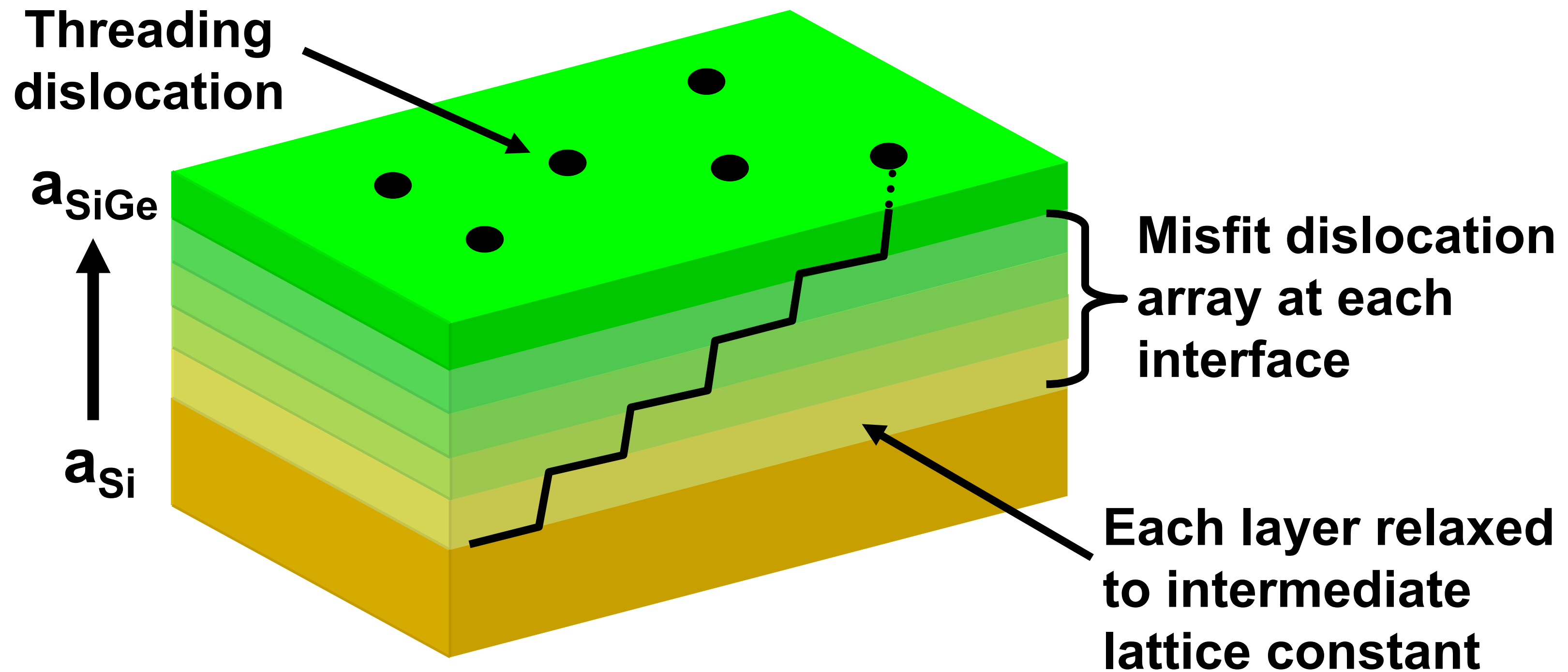
εMOS™ Electronic Structure



Type II Band Offset ⇨ V_t Shift

Courtesy of Matt Currie
AmberWave Systems Corp.

Defect Control: SiGe Virtual Substrates



- Constant low strain rate
  - minimize dislocation nucleation
- Relaxation via existing defects
  - low threading dislocation density

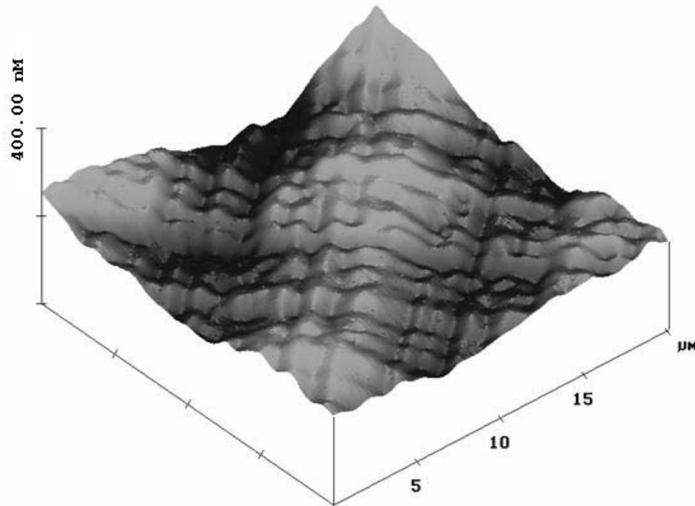
Courtesy of Matt Currie
AmberWave Systems Corp.

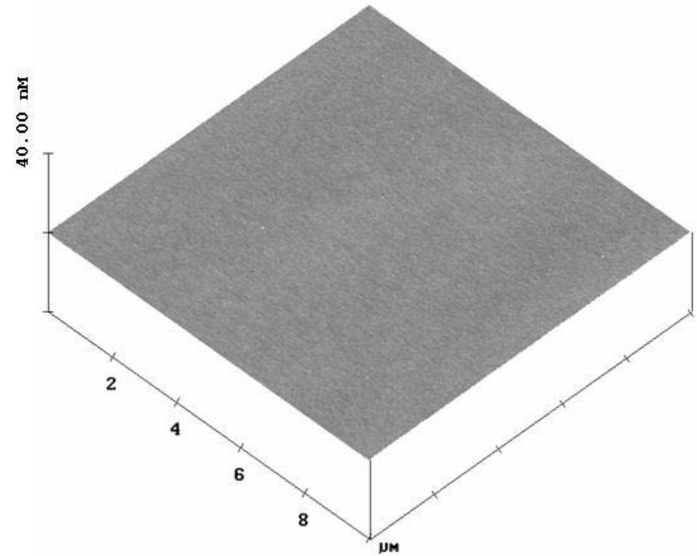
Systems Substrate Technology

- **Underlying misfit dislocation array affects local epitaxial growth rates**
- **"Crosshatch" surface roughness can be problematic for device manufacturability**
  - **Photolithography**
  - **Optical metrology**

Courtesy of Matt Currie
AmberWave Systems Corp.

Substrate Technology





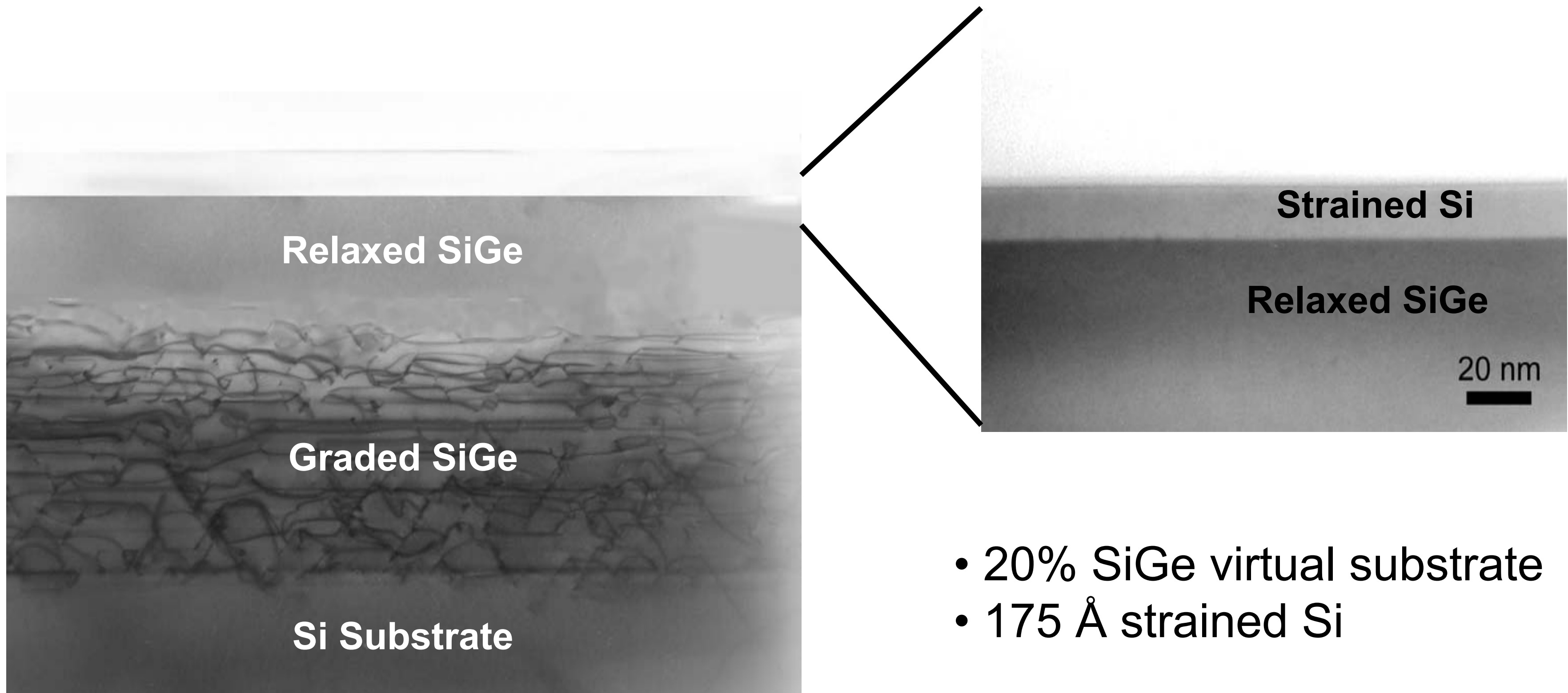
RMS Roughness before CMP : 50-100 Å

After CMP : <2 Å

Proprietary planarization & regrowth process is a key differentiator of AmberWave substrate technology

Courtesy of Matt Currie
AmberWave Systems Corp.

Strained Silicon: XTEM

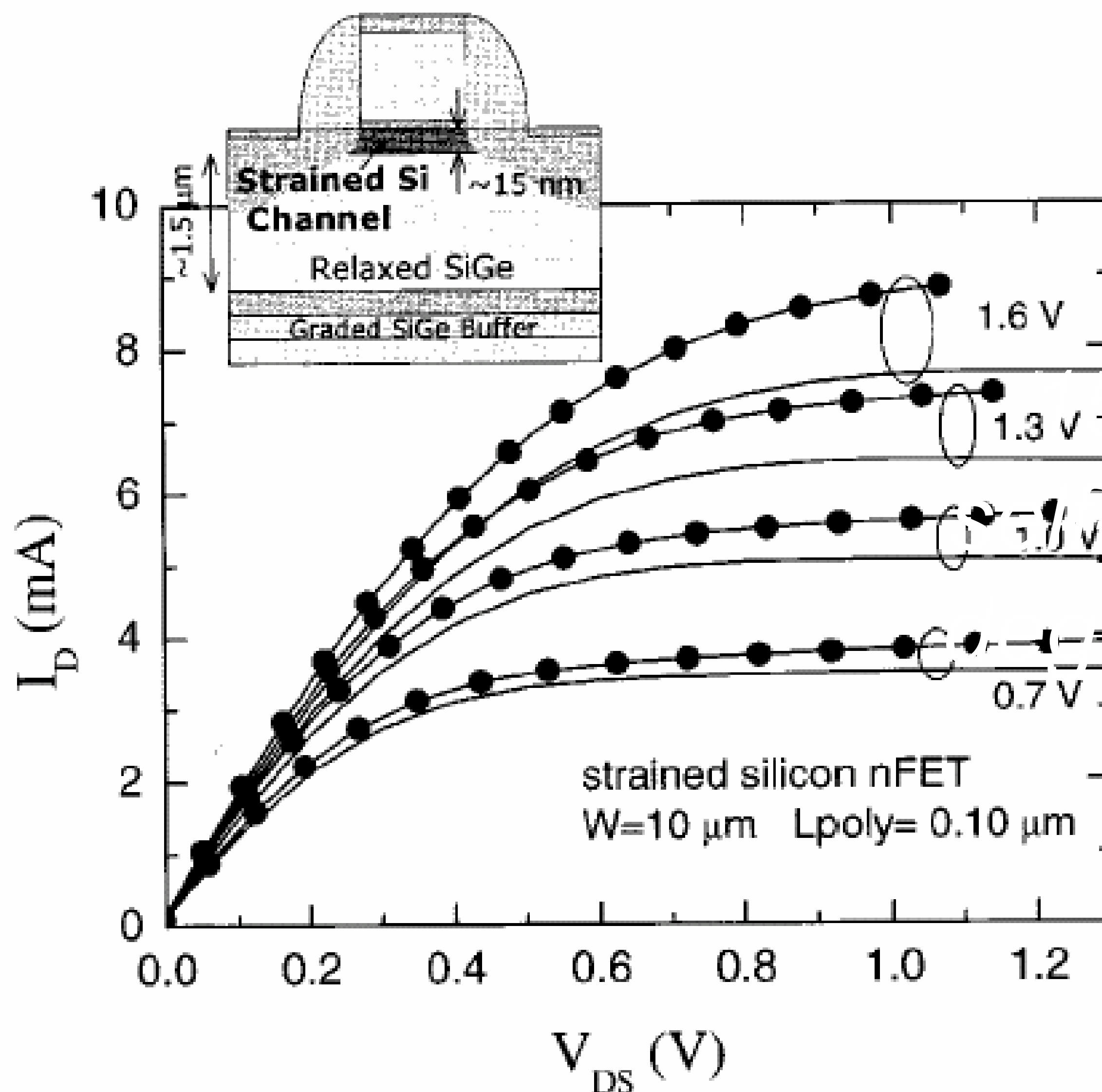


- 20% SiGe virtual substrate
- 175 Å strained Si

Well-controlled introduction of misfit dislocations results in a high quality relaxed SiGe substrate for strained Si

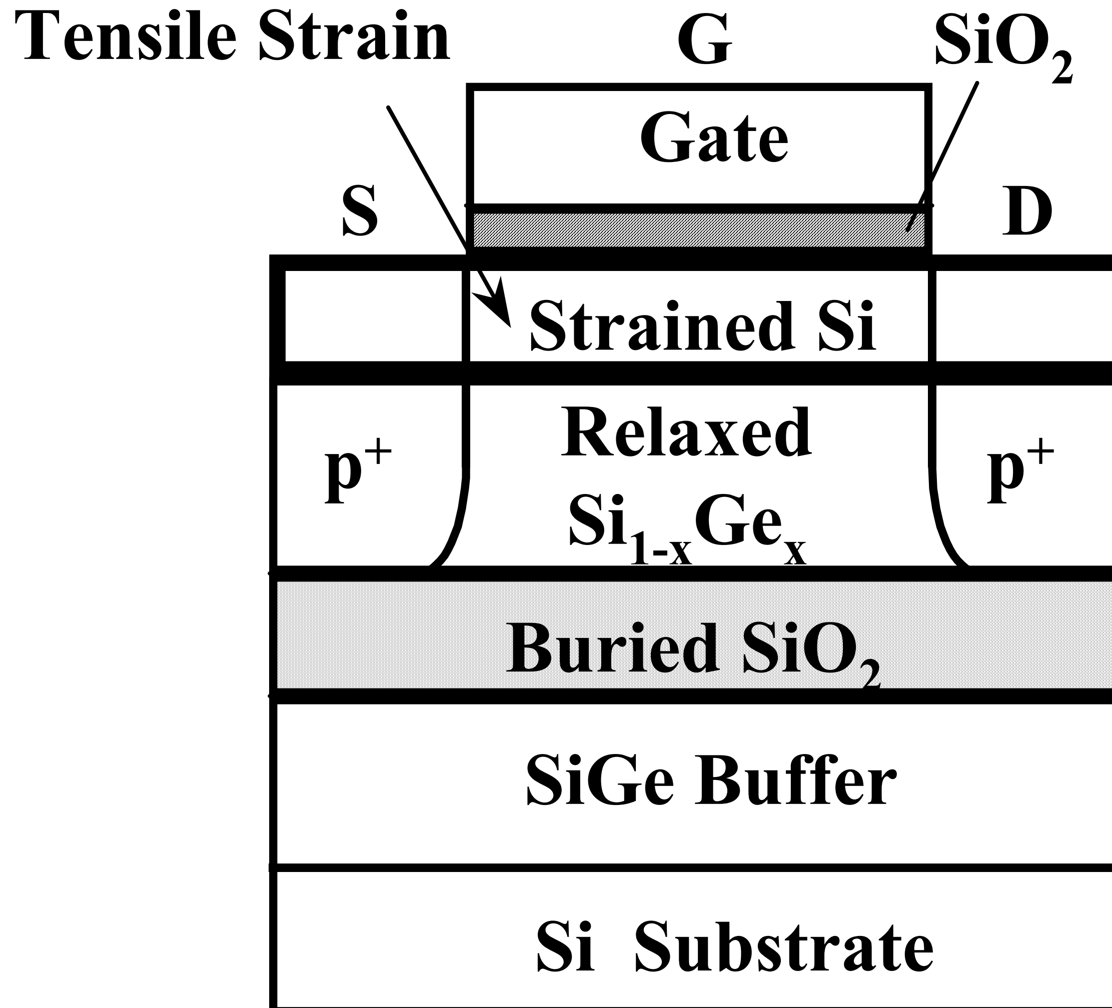
Courtesy of Matt Currie
AmberWave Systems Corp.

Drain Current versus Source-Drain Voltage



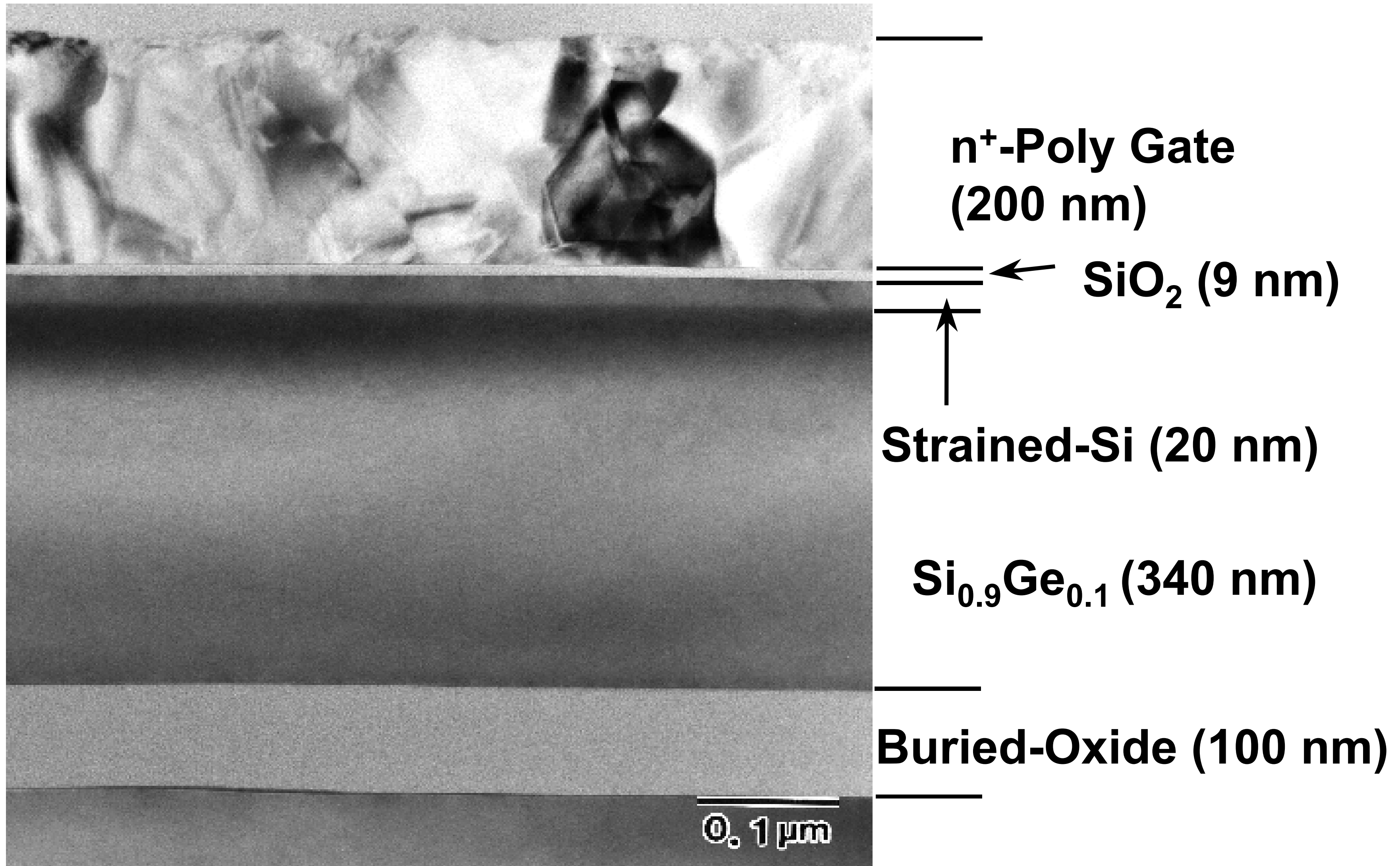
K.A. Jenkins and K. Rim, *Measurement of the Effect of Self-Heating in Strained-Silicon MOSFETs*, Electron Dev. Lett., **23,** 360-362 (2002) (© 2002, IEEE)

Strained-Si PMOSFET on SiGe-on-Insulator



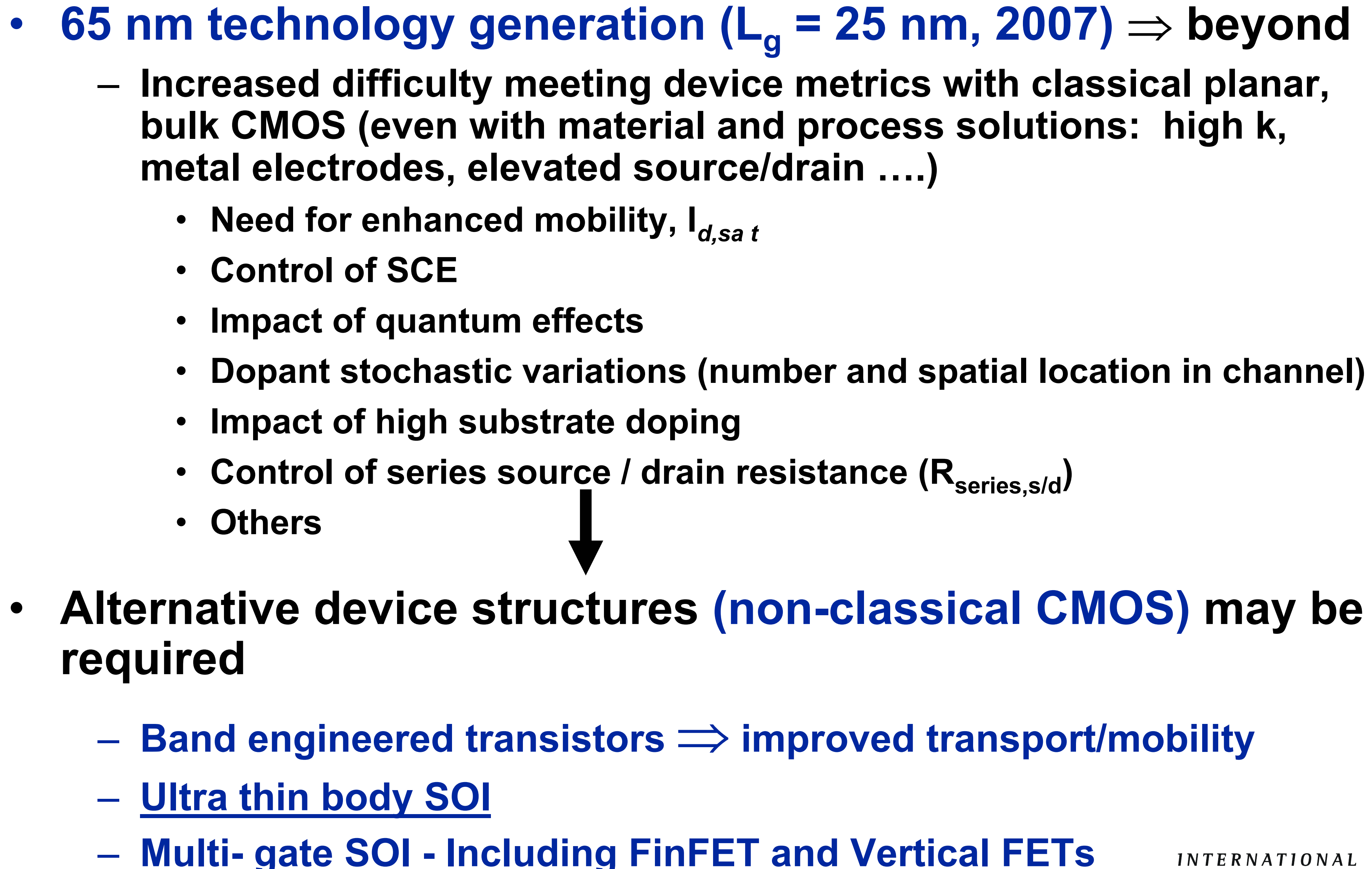
T. Mizuno et al., IEDM, 934-936 (© 1999, IEEE)

Strained-Si PMOSFET on SiGe-on-Insulator



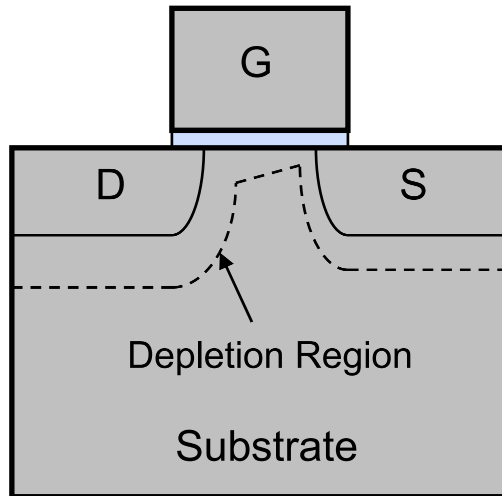
T. Mizuno et al., IEDM, 934-936 (© 1999, IEEE)

Limits of Scaling Planar, Bulk MOSFETs

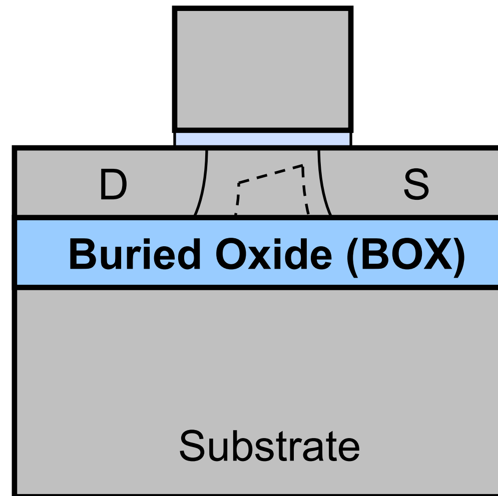


Transistor Structures

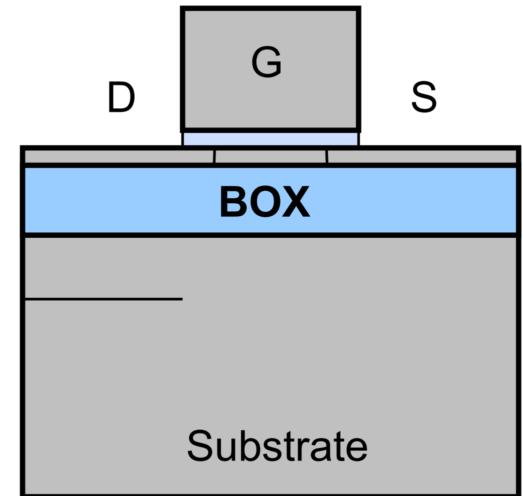
Planar Bulk



Partially Depleted SOI



Fully Depleted SOI



Planar Bulk

- \+ Wafer cost / availability
- \- SCE scaling difficult
- \- High doping effects and statistical variation
- \- Parasitic junction capacitance

Partially Depleted SOI

- \+ Lower junction cap
- \+ F.B. performance boost
- \- F.B. history effect
- \- SCE scaling difficult
- \- Wafer cost/availability

Fully Depleted SOI

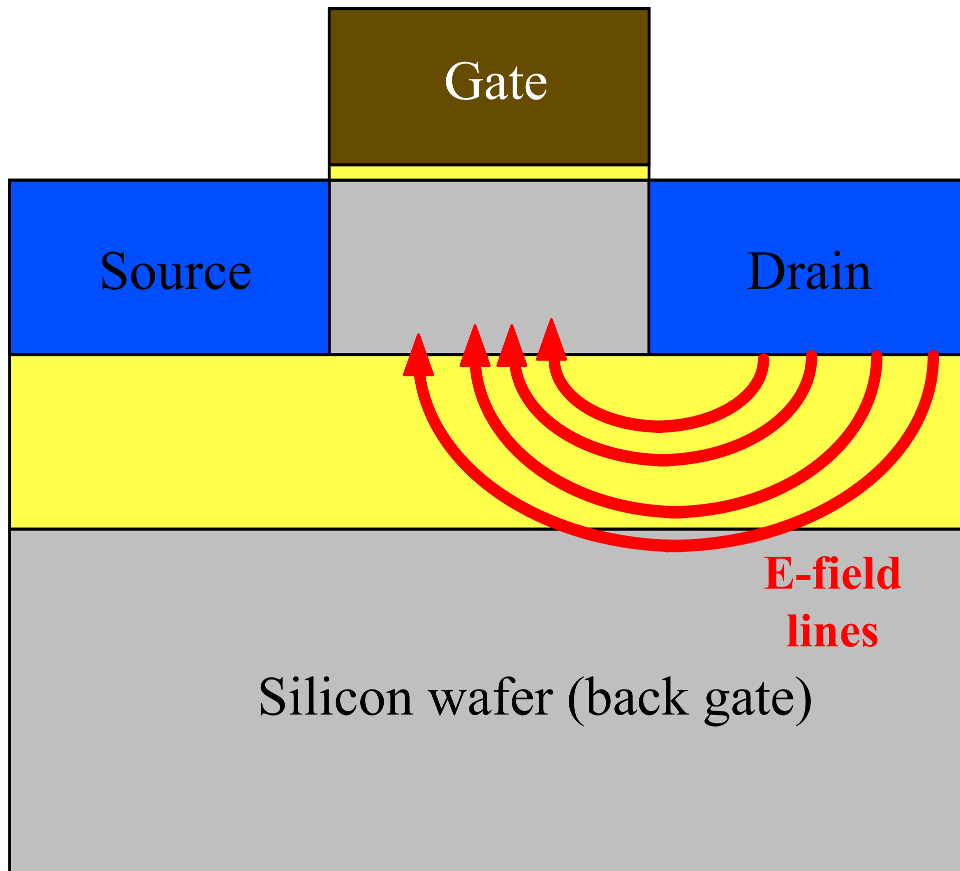
- \+ Lower junction cap
- \- SCE scaling difficult
- \- High $R_{series,s/d} \Rightarrow$ raised S/D
- \- Sensitivity to Si thickness (very thin)
- \- Wafer cost/availability

References:

1. P. Zeitzoff, J. Hutchby and H. Huff, Internat. Jour. High Speed Electronics & Systems
2. Mark Bohr, ECS Meeting PV **2001-2**, Spring, 2001

Short-channel MOSFET: DIBL

or: Drain-Induced Barrier Lowering

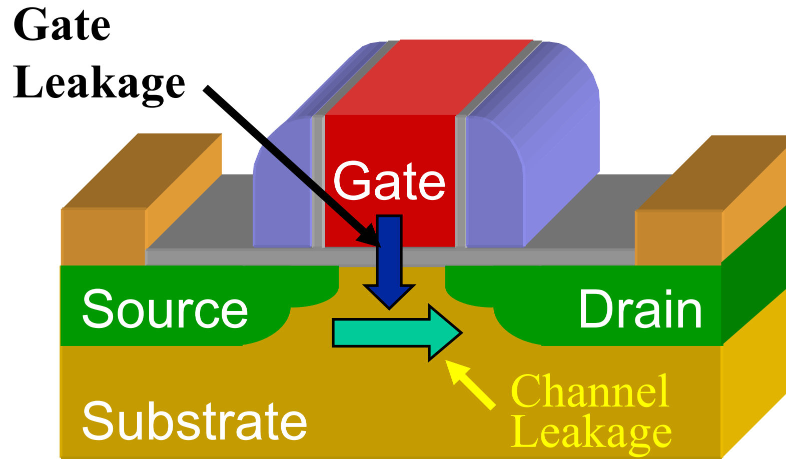


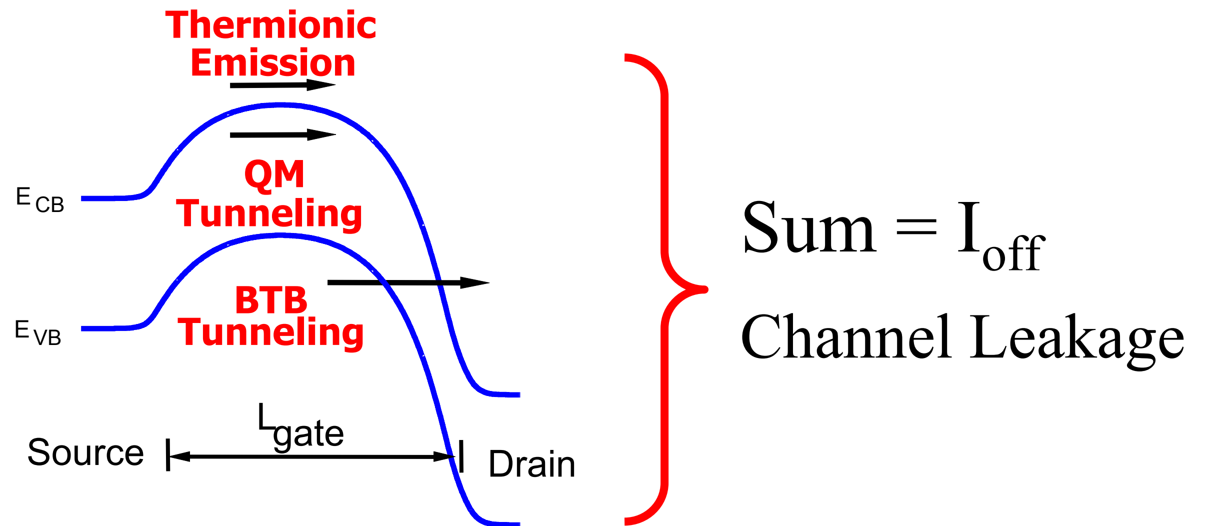
Electric field lines from drain encroach on channel region.

Any **increase of drain voltage decreases threshold voltage** (the "NPN" potential barrier between source and drain is lowered)

J-P Colinge, U.California., Davis

Electrostatic Scaling - Channel Leakage (I_{off})

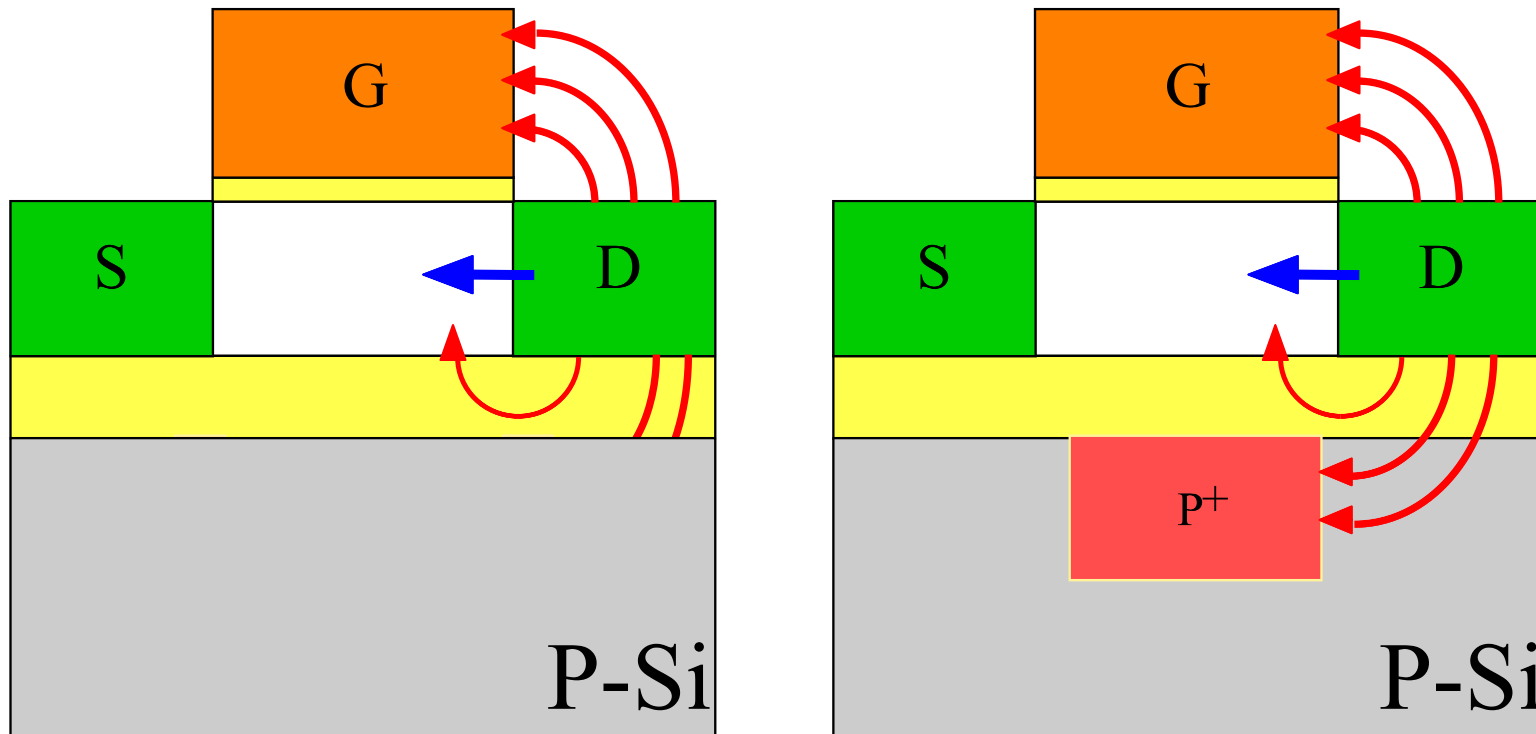




Sum = I_{off}

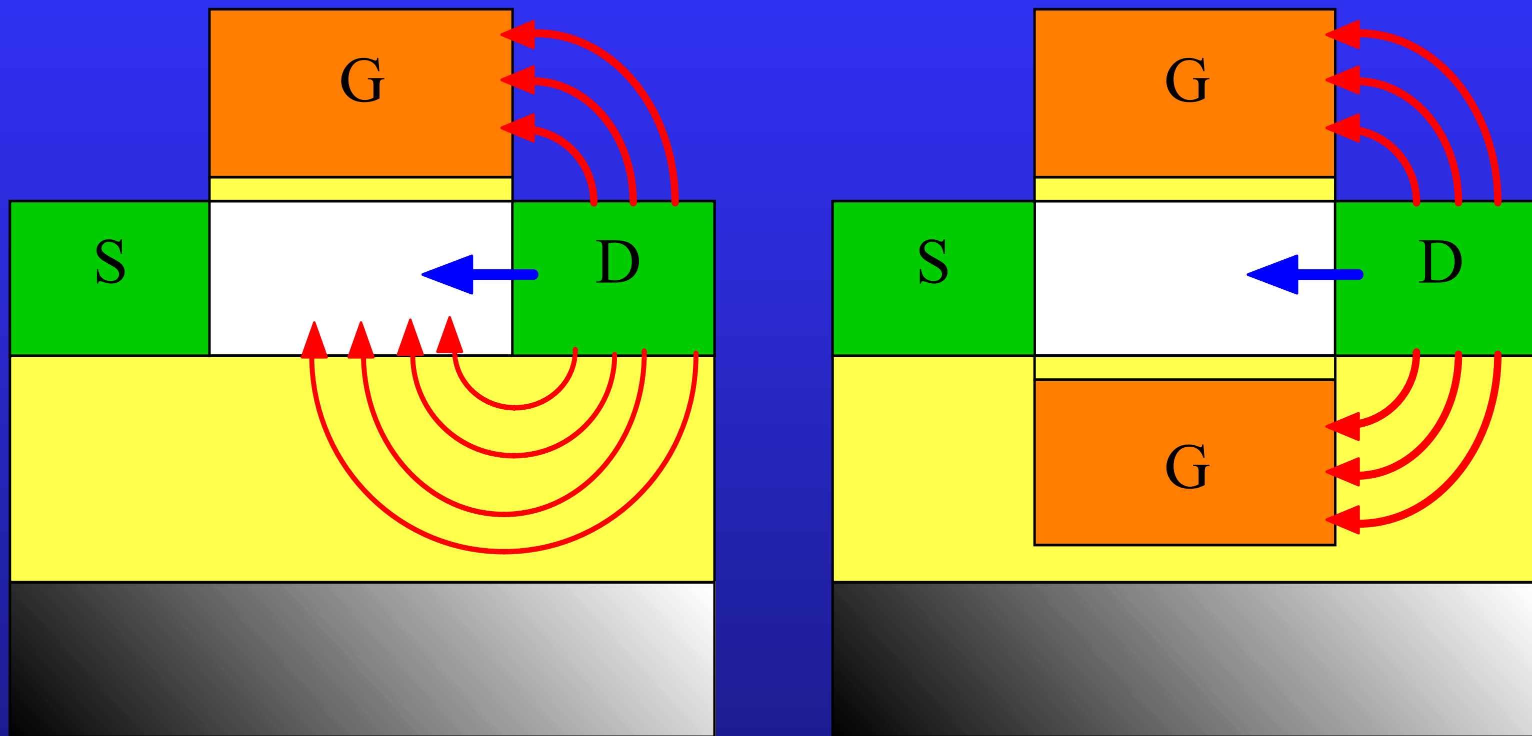
Channel Leakage

E-Field lines



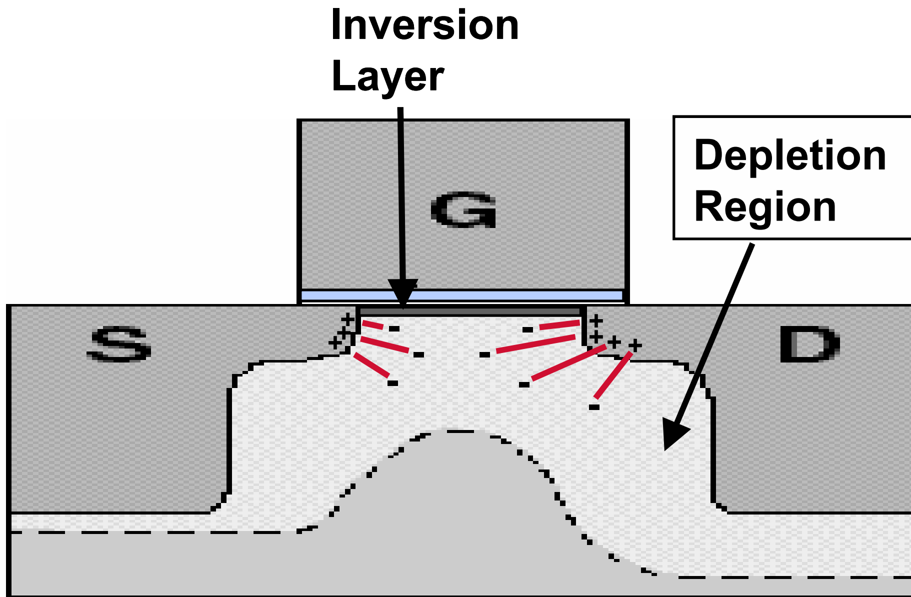
Ground-plane SOI MOSFETs

E-Field lines

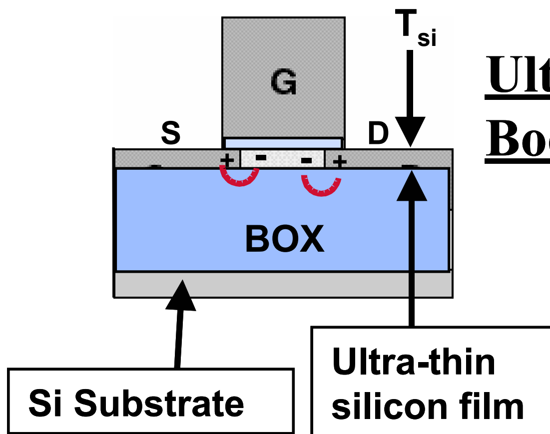


Regular SOI MOSFETDouble-gate MOSFE

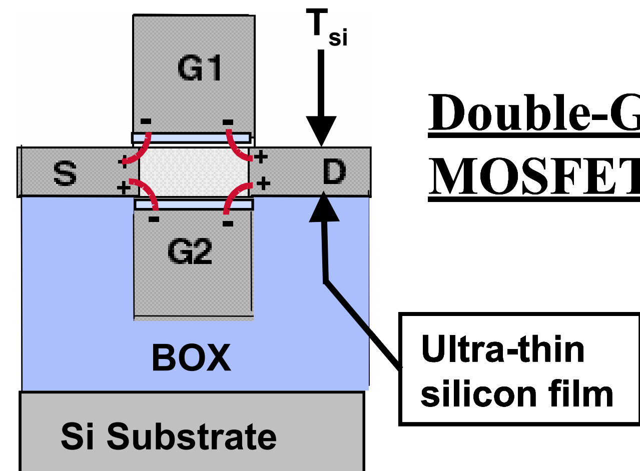
Schematic Cross Section of Planar Bulk, UTB SOI and DG SOI MOSFET



Bulk MOSFET



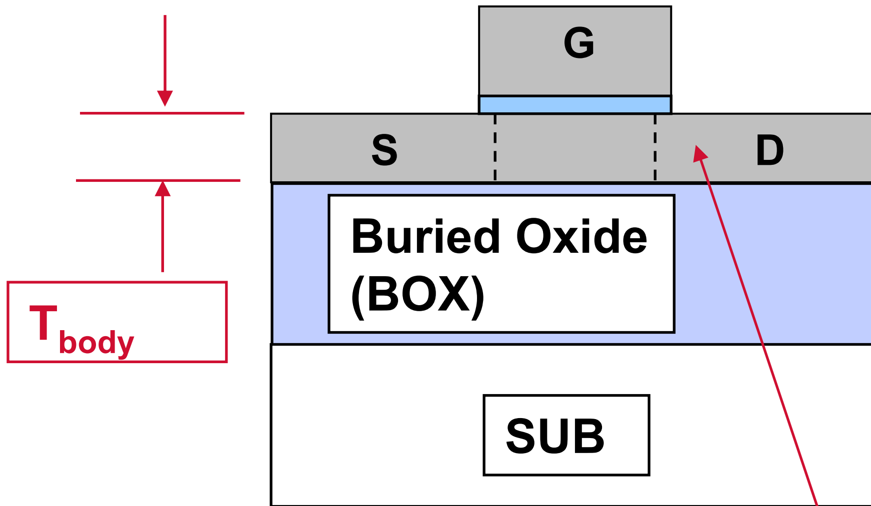
Ultra-Thin Body SOI



Double-Gate SOI MOSFET

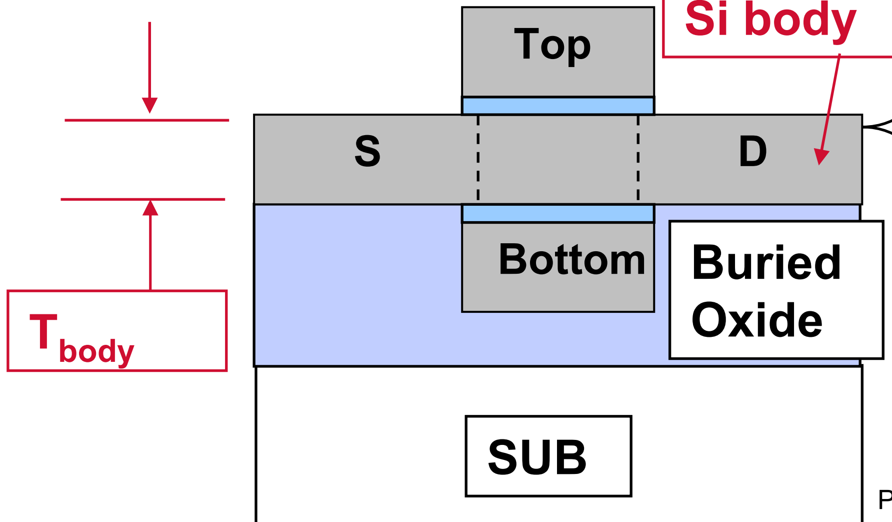
Ultra-Thin Body, Fully Depleted Single and Double-Gate Transistors: Pros and Deltas

Single Gate:



- \+ Lower junction capacitance
- \+ Reduced channel doping for metal gate electrode, fully depleted
- \- SCE scaling difficult
- \- Sensitivity to Si thickness
- \- Wafer cost/availability

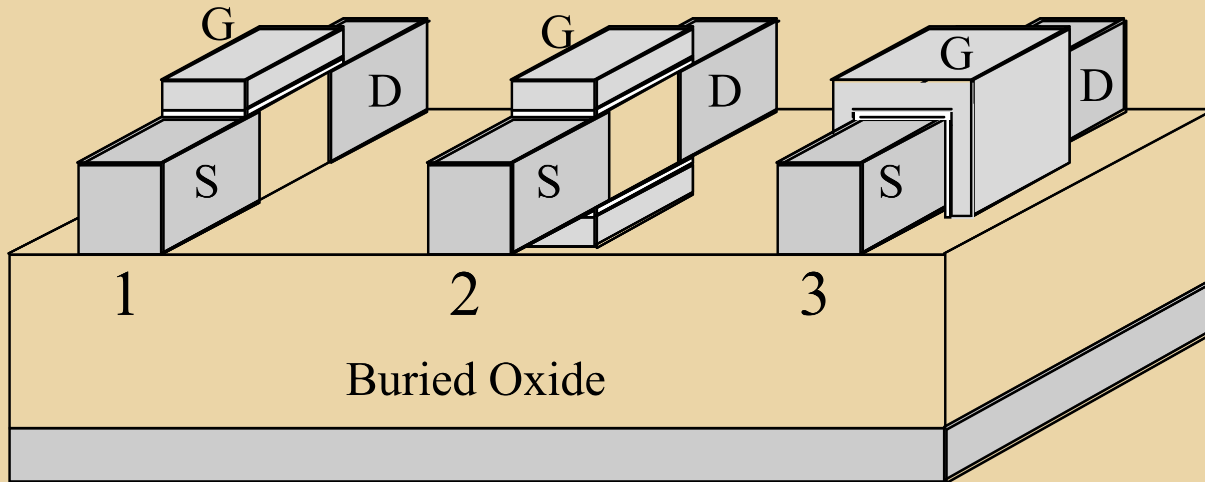
Double Gate SOI:



- \+ Enhanced scalability
- \+ Near ideal subthreshold slope, S
- \+ Reduced channel doping for metal gate electrode, fully depleted
- \+ Lower junction capacitance
- \+ ~2x drive current
- \- ~2x gate capacitance
- \- Complex process
- \- Wafer cost/availability
- \- Most advanced, optimal device structure, difficult to fabricate

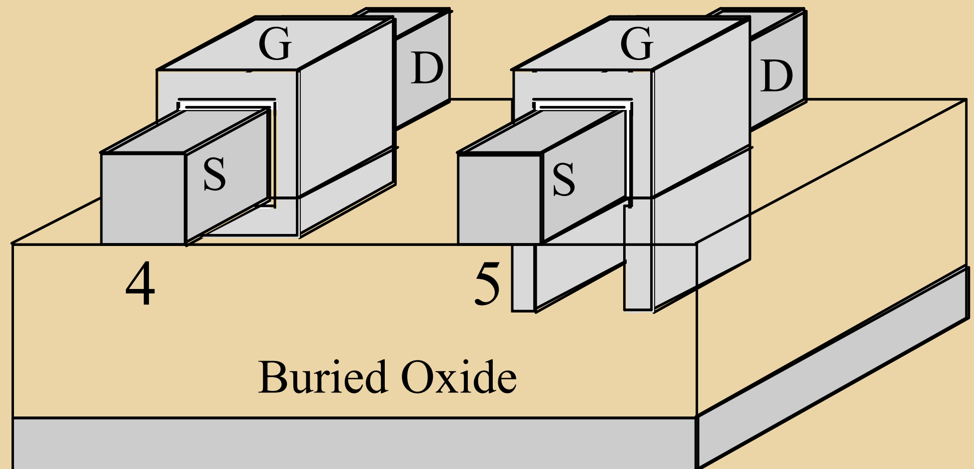
P. M. Zeitzoff, J. Hutchby and H.R. Huff
M. Bohr, ECS Meeting PV **2001-2**, Spring, '01

"Multiple Gates"

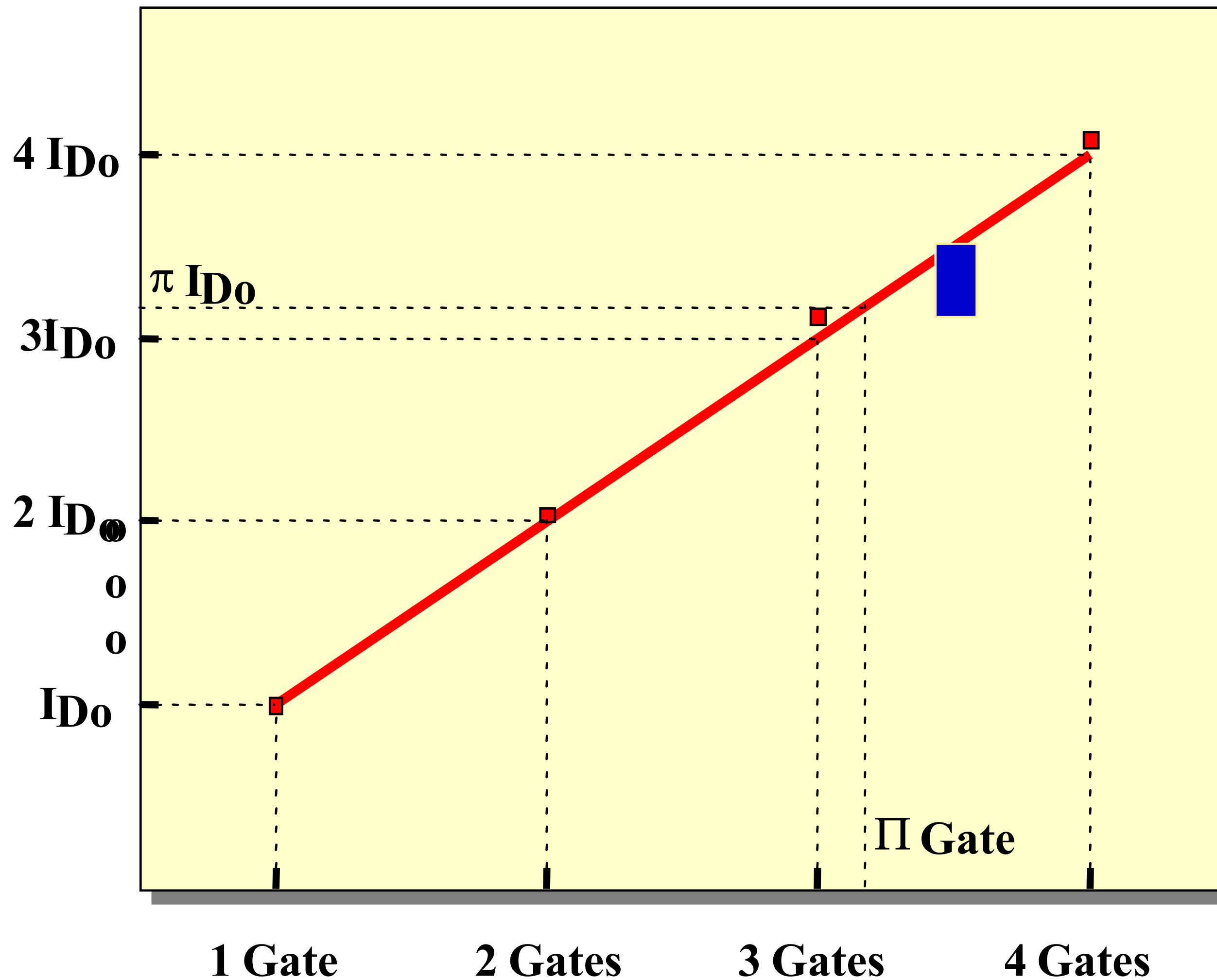


Current Drive

1: Single gate
2: Double gate
3: Triple gate
4: Quadruple gate (GAA)
5: Π gate

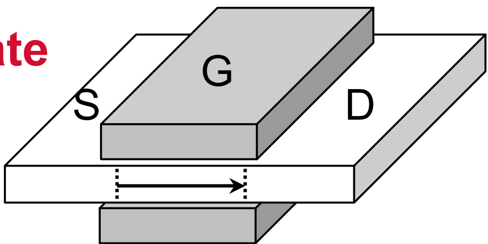


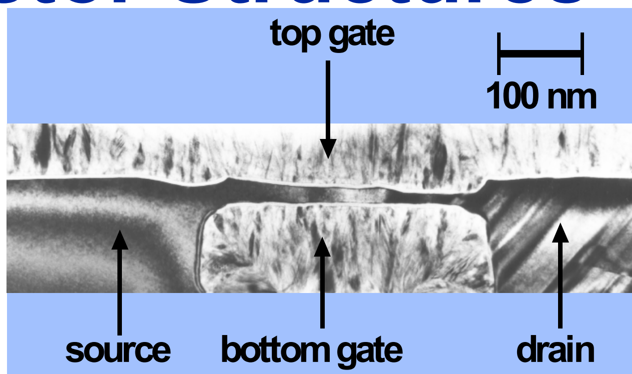
Simulation of Multiple-Gate SOI MOSFETs



Double-Gate Transistor Structures

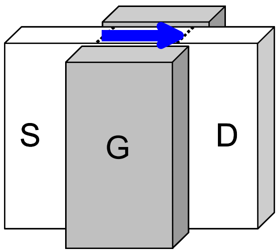
Double Gate SOI



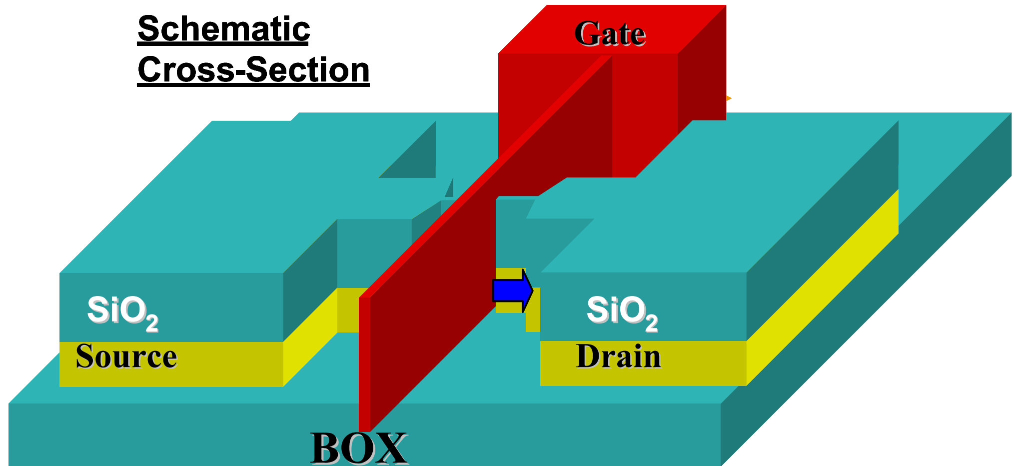


IBM '97

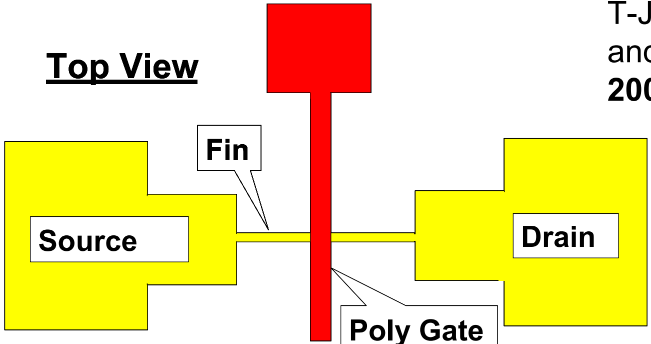
FinFET



Simplified view of FinFET (one type of double-gate MOSFET)

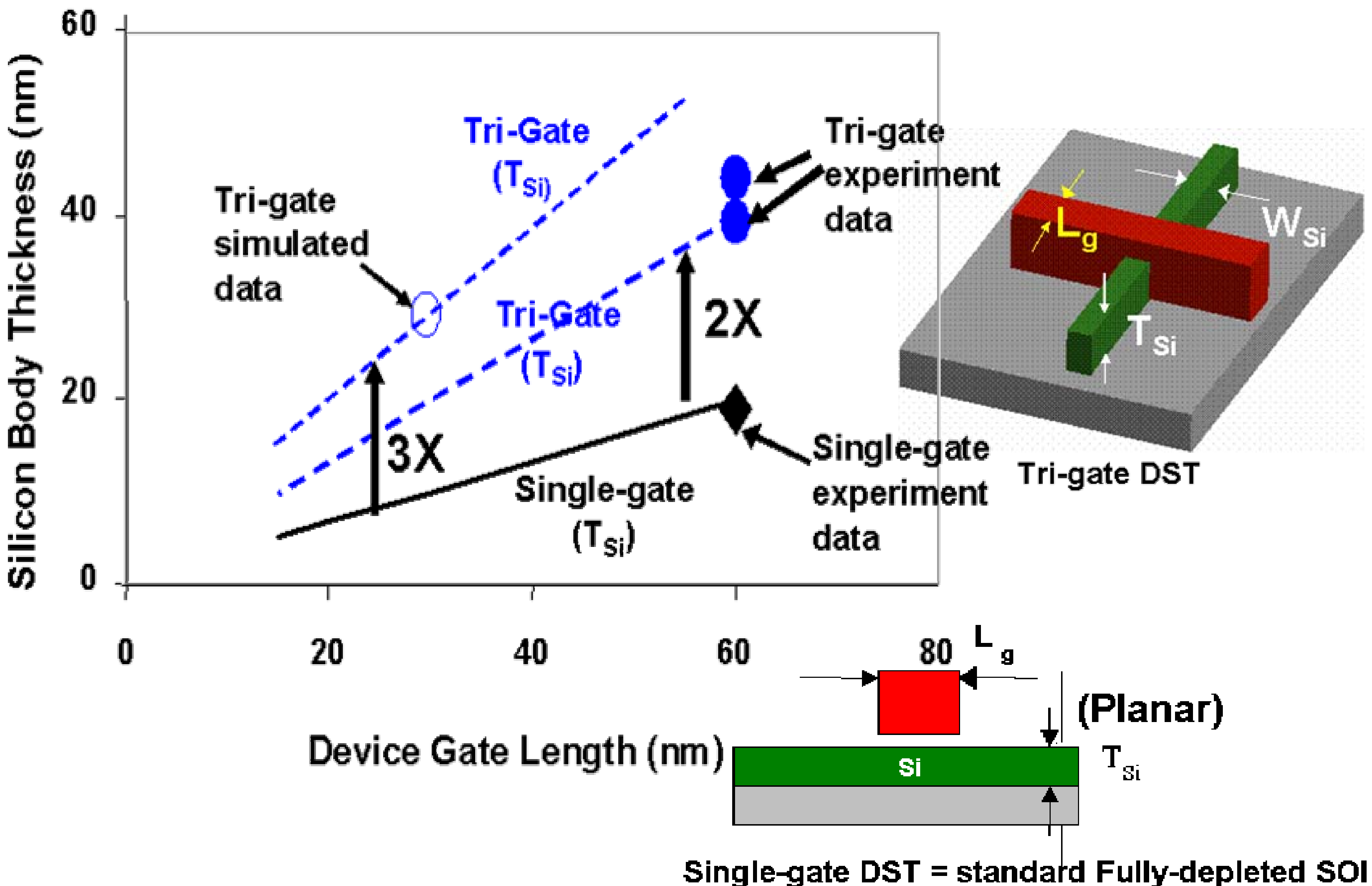


Key advantage: relatively conventional processing, largely compatible with current techniques



T-J. King and C. Hu, UC/Berkeley and Mark Bohr, ECS Meeting PV **2001-2**, Spring, 2001

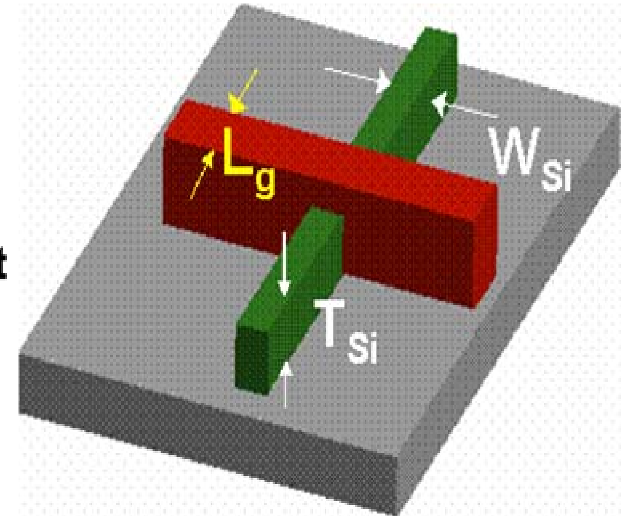
Tri-gate Relaxes T_{Si} Requirement of Single-gate



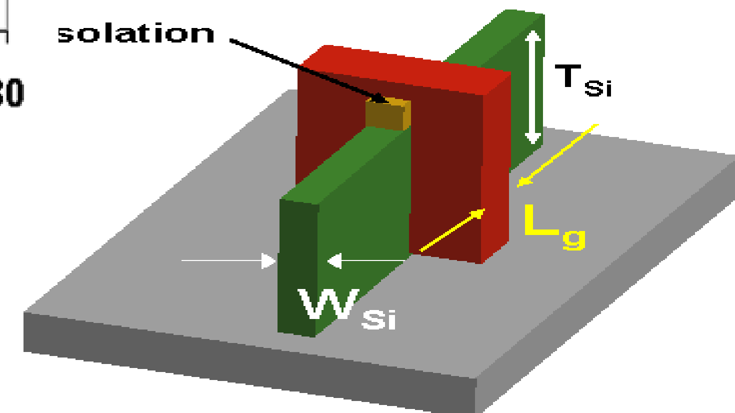
Courtesy of Robert Chau et al., ISSDM, 2002

Tri-gate Relaxes W_{Si} Requirement of Double-gate

Silicon Body Thickness (nm)
80
60
40
20
0
0
20
40
60
80
Device Gate Length (nm)
Tri-gate (W_{Si})
Double-gate (W_{Si})
1.5X
Tri-gate simulated data
Tri-gate experiment data



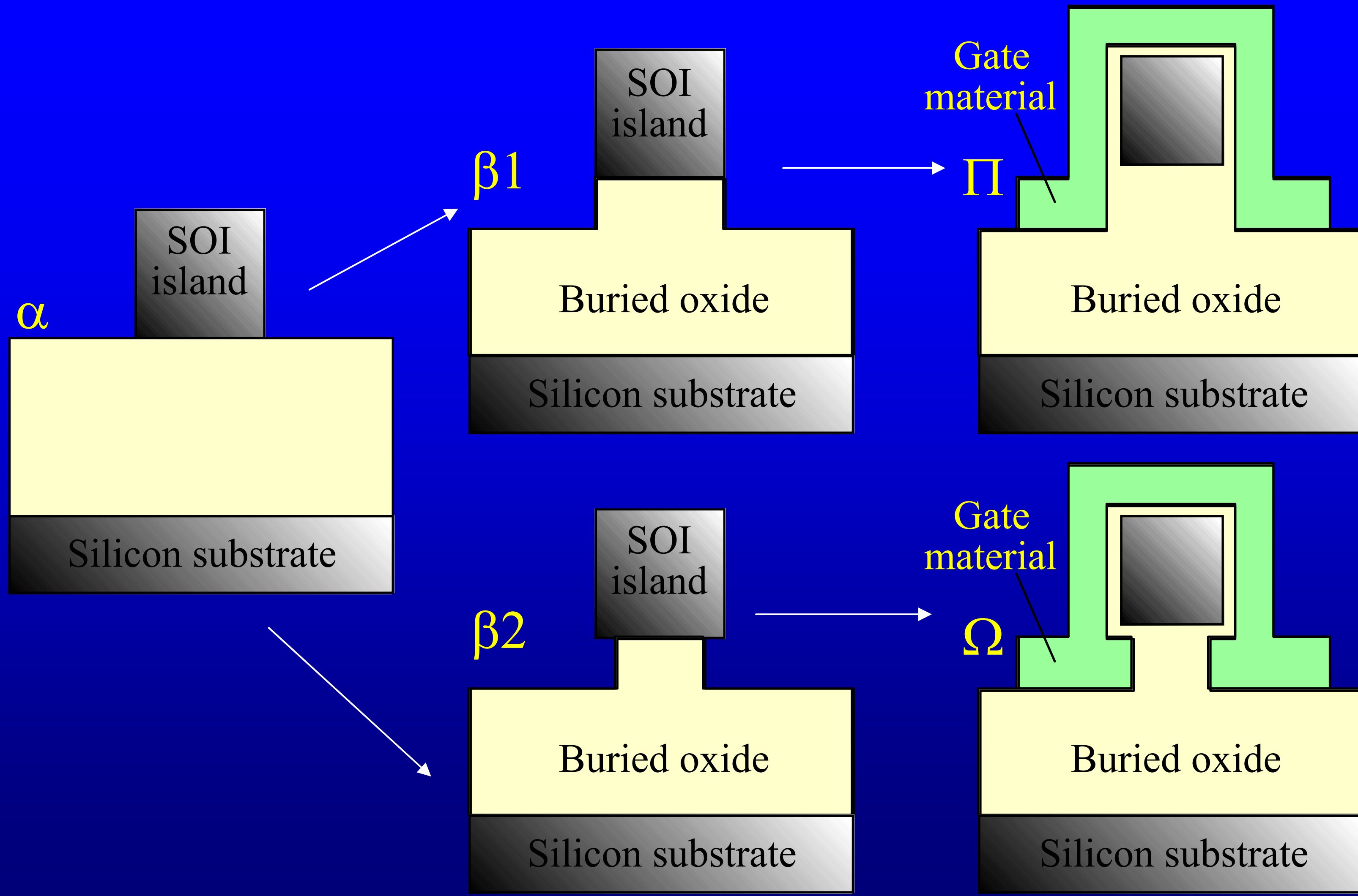
Tri-gate DST



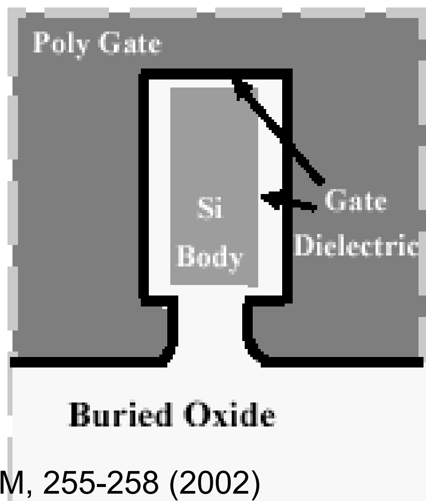
Double-gate (e.g. FINFET)

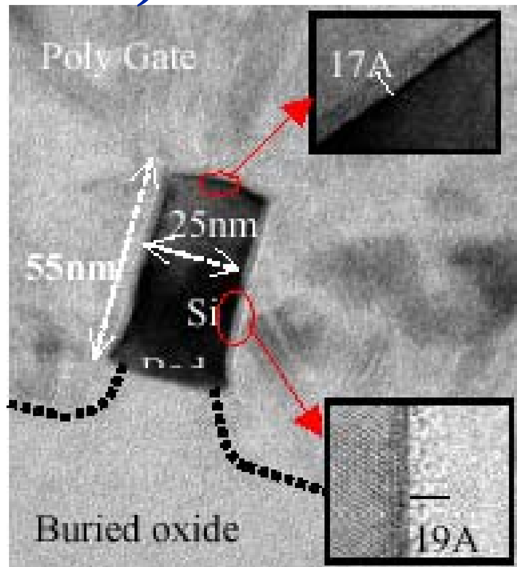
Courtesy of Robert Chau et al., ISSDM, 2002

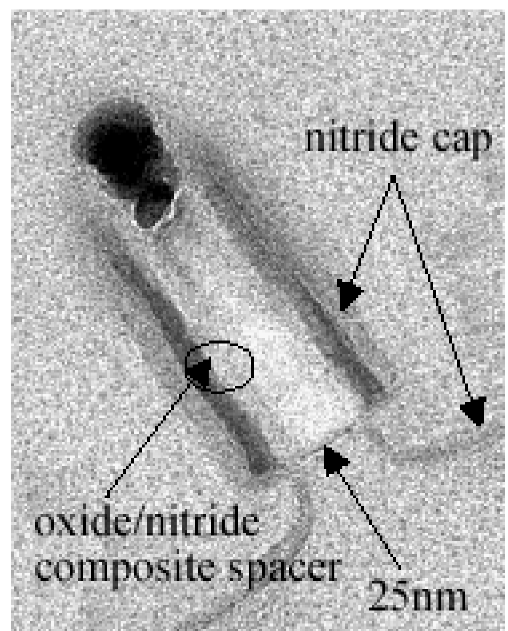
PI-Gate / OMEGA Gate Structure



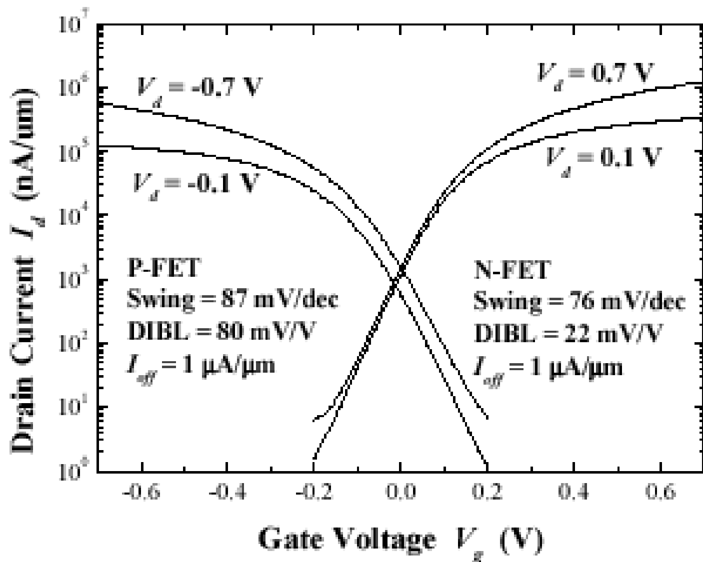
TSMC's Ω-gate (IEDM'02)







Fu-Liang Yang et al., IEDM, 255-258 (2002)
(© 2002, IEEE)



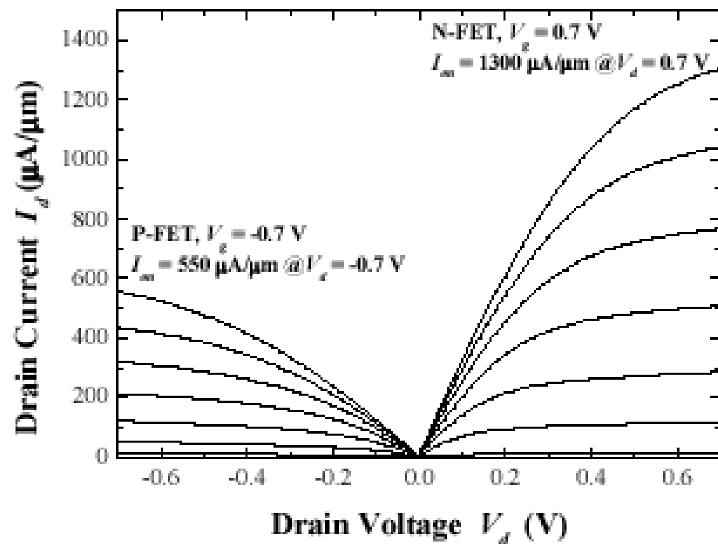
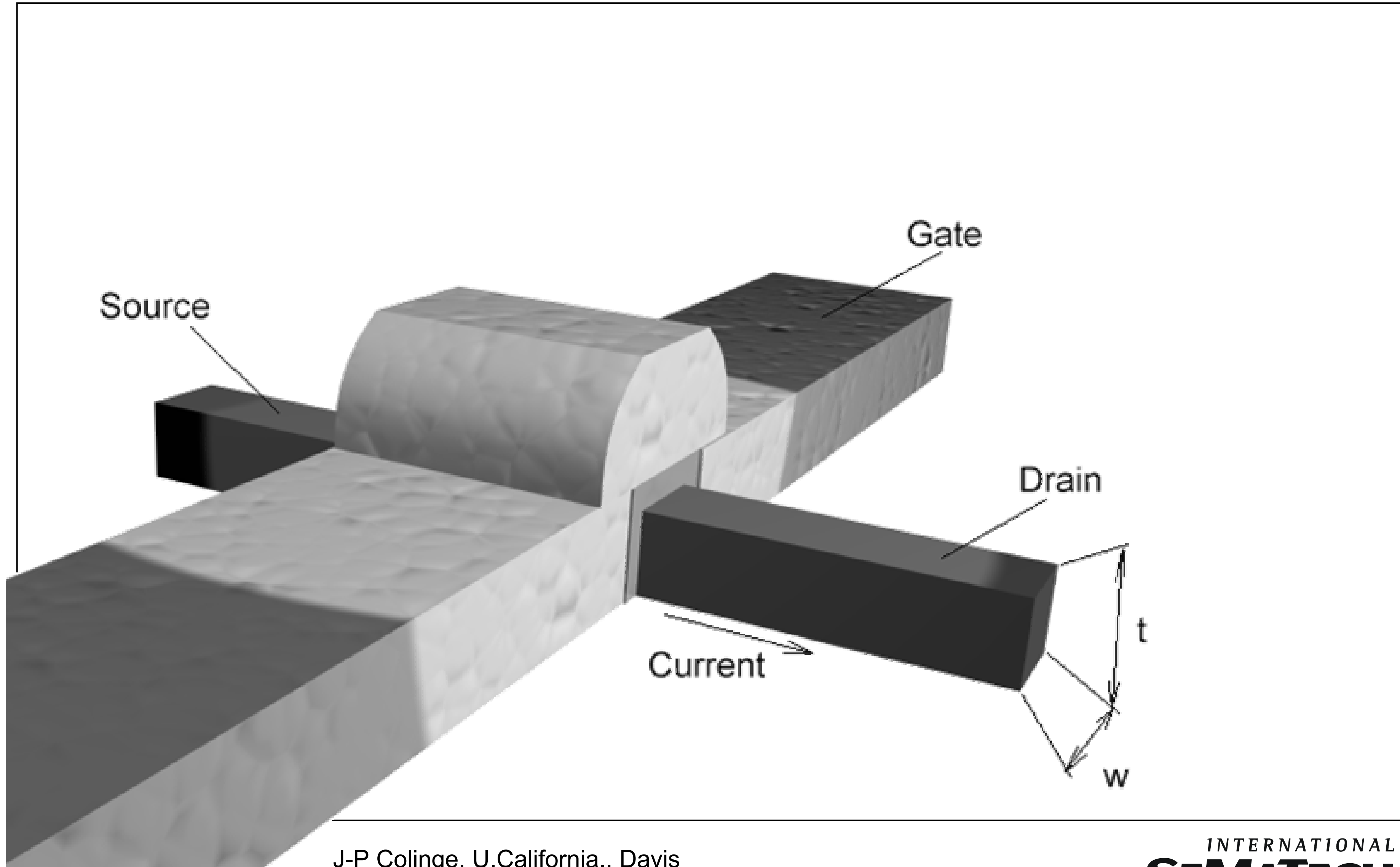
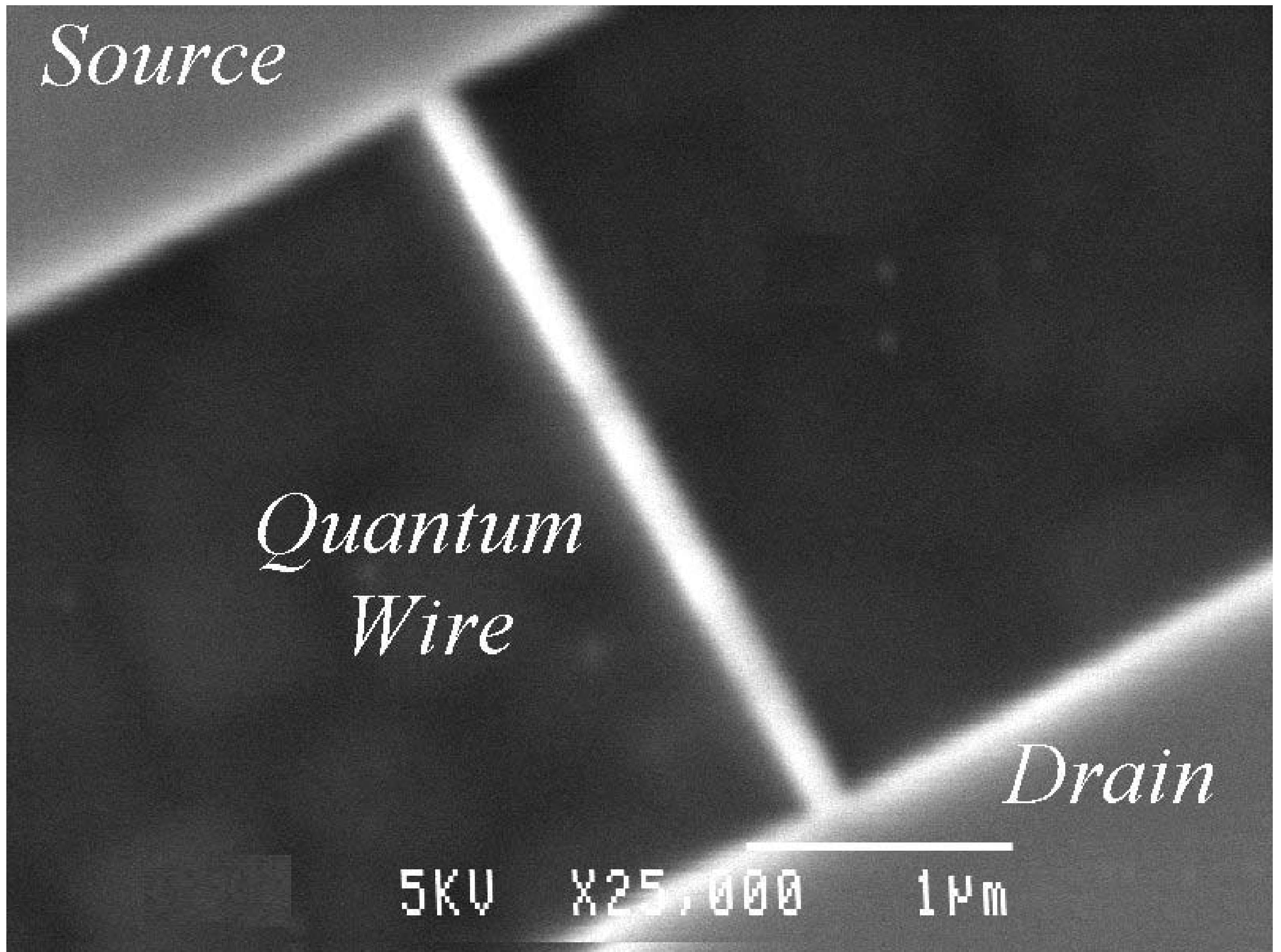


Figure 6. (a) I_d-V_g and (b) I_d-V_d characteristics of the 0.7 V version of the 25 nm L_g CMOS Ω-FETs. Channel width, W, is defined as H_{Si}.

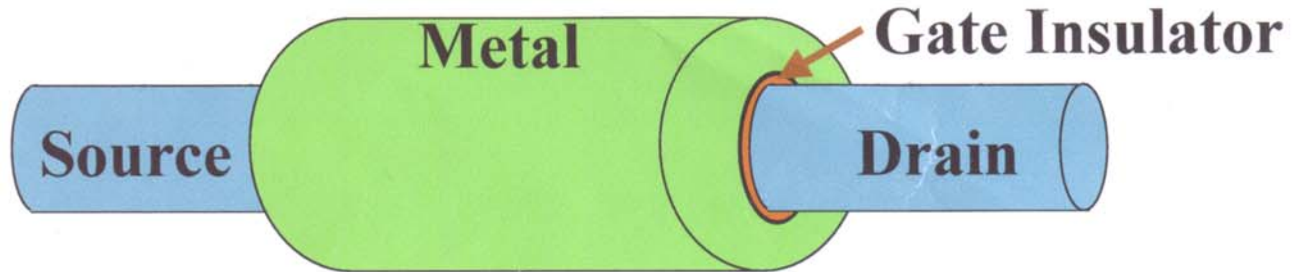
Quantum Wire MOSFET (UCL SOI Conf., 1995)



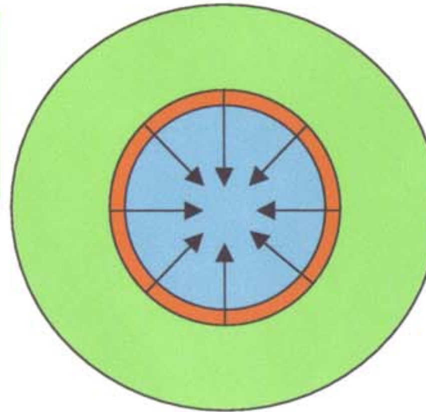
J-P Colinge, U.California., Davis


Source
Quantum
Wire
Drain
5KV X25,000 1μm

The Ideal MOS Transistor



Fully Surrounding Metal Electrode



Fully Enclosed, Depleted Semiconductor

High-K Gate Insulator

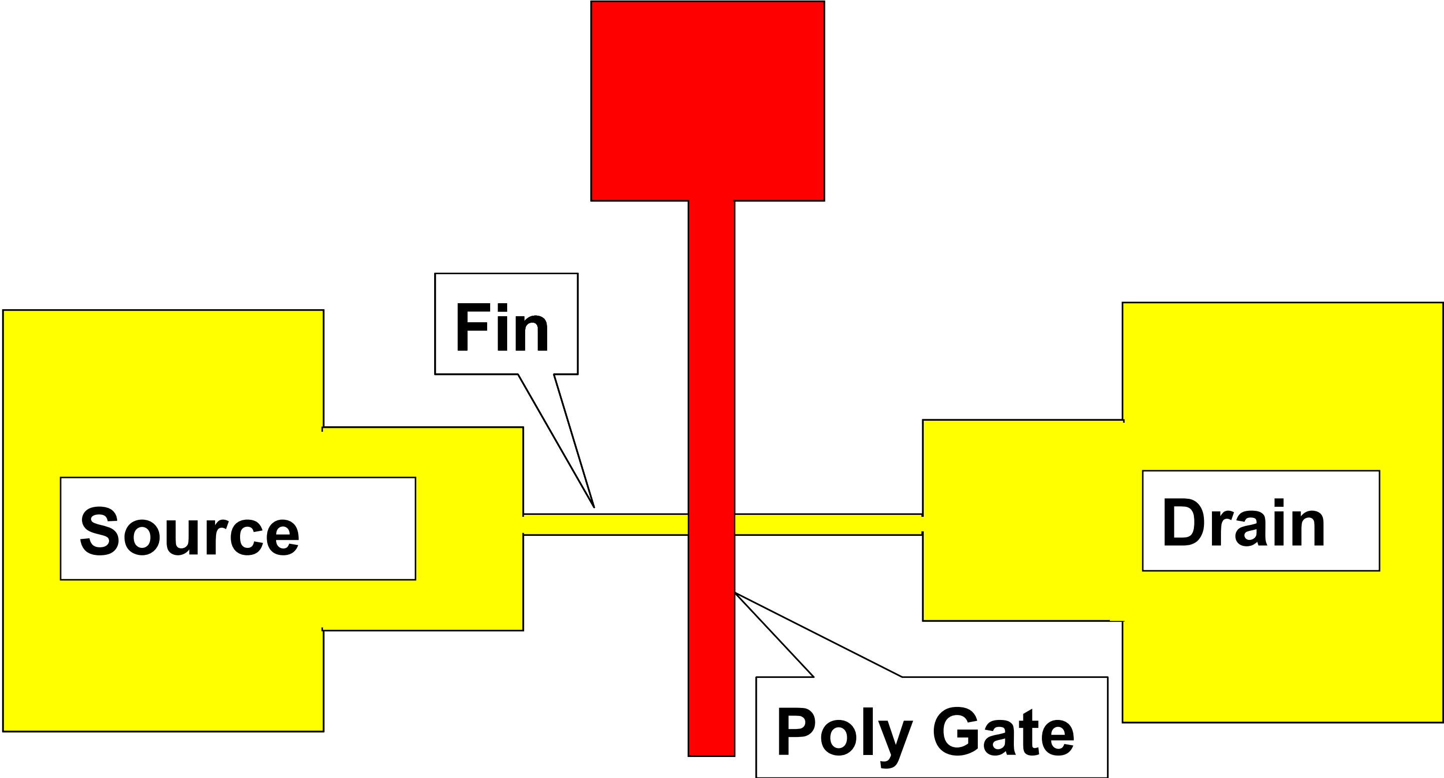
Band Engineered Semiconductor

Low Resistance Source/Drain

M2 S2

P.Gargini

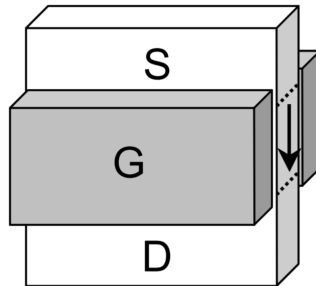
One Can Utilize Multiple Fins to Enhance Transistor Total Drive Current

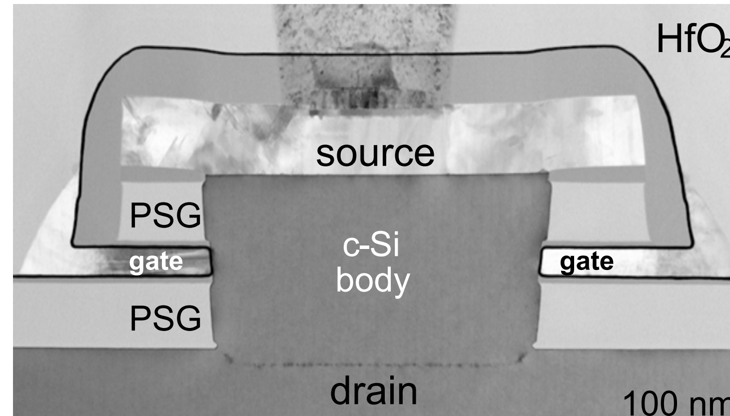


T-J. King and C. Hu, UC/Berkeley and
Mark Bohr, ECS Meeting PV **2001-2**, Spring, 2001

Other 3-D Transistor Structures

Vertical FET (one type of double-gate MOSFET)

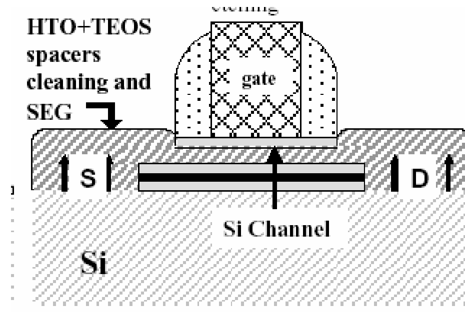


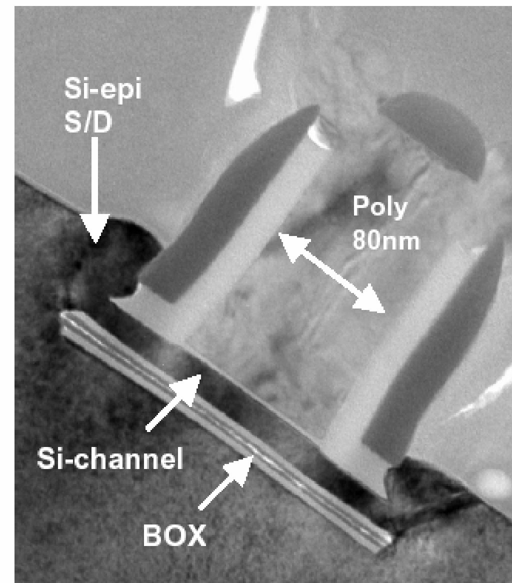


Agere '02

REF: Mark Bohr, ECS Meeting PV **2001-2**, Spring, 2001

Silicon on Nothing (SON): localized buried oxide (BOX)

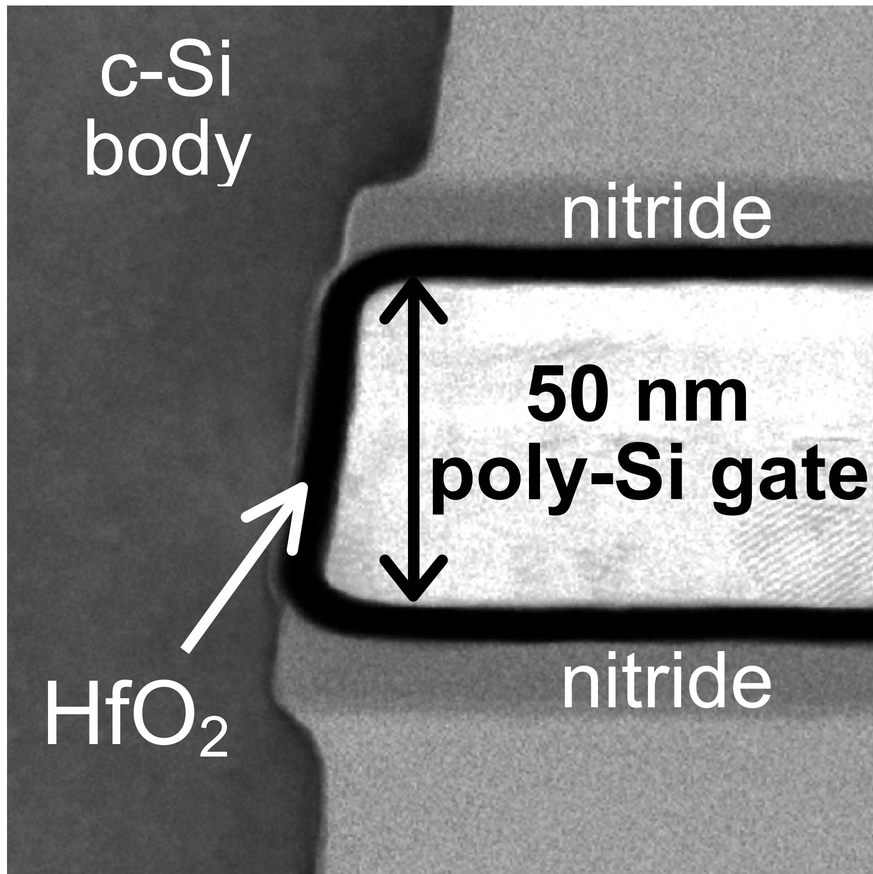


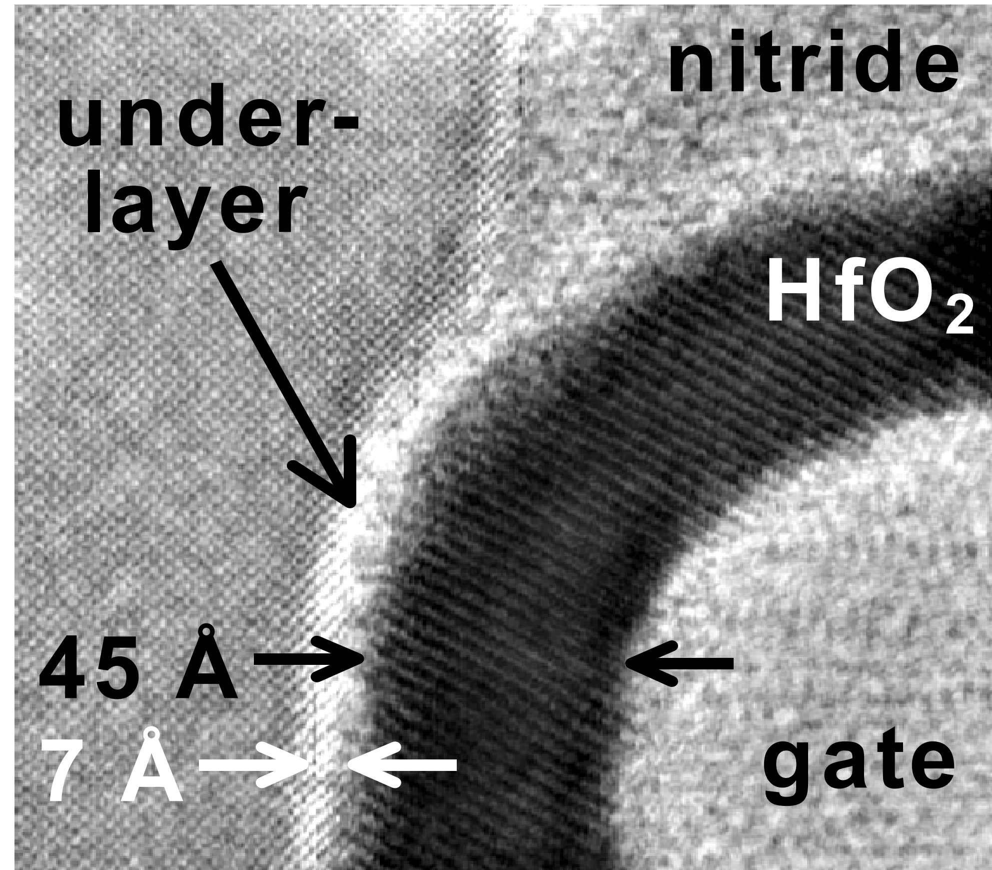


STM '01

S. Monfray et al., IEDM, 645-648 (2001) (© 2002, IEEE)

Other 3-D Transistor Structures (con't)
Agere '02





Jack Hergenrother et. al., 50 nm Vertical Replacement-Gate (VRG) nMOSFETs with ALD HfO_2 Gate Dielectrics, *Semiconductor Silicon/2002*, ECS **PV 2002-2**, 929-942 (2002)
Reproduced by permission of The Electrochemical Society, Inc.

Agenda

- Introduction
  - MOSFET scaling drivers
- Front-end approaches and solutions
- Non-classical CMOS structures
- Summary / Trends
- Acknowledgements

2001 ITRS Key MOSFET Scaling Results

- High-performance logic
  - Average 17%/yr improvement in $1/\tau$ attained
  - $I_{sd,leak}$ very high, particularly for 2007 and beyond
    - Chip static power dissipation scaling an issue
    - Assumption: $I_{gate} \leq I_{sd,leak} \Rightarrow$ unacceptably large I_{gate} under revision
- Low standby power logic
  - Very low $I_{sd,leak}$ target met
    - $I_{gate} \leq I_{sd,leak} \Rightarrow I_{gate}$ low, but difficult to achieve
  - $1/\tau$ scales considerably slower (14%) than high-performance MPU
- ITRS MOSFET targets are chosen to aggressively drive technology scaling

Summary

- MOSFET device scaling "raw material" for meeting projected overall chip power, performance, and density requirements
  - Goals/requirements/tradeoffs jointly established between designers and technologists
  - Considerable design innovation and focus required, even with aggressive technology scaling
- Scaling goals vary for different applications
  - High-performance logic driven by transistor speed requirements
    - Result: high speed, but high leakage, static power dissipation issues
  - Low standby power logic driven by transistor leakage requirements
    - Result: lower speed than high-performance logic
- Material and process potential solutions include high-k gate dielectric, metal gate electrodes, elevated source / drain, spike annealing, and eventually, novel S/D annealing and doping
  - High-k needed first for low standby power (mobile) chips in ~ 2005
- Structural configurations: non-classical CMOS
- Material, process and structural solutions pursued in parallel and may be combined in "ultimate," end-of-roadmap device
  - $L_g \leq 10$ nm MOSFETs anticipated end of ITRS in 2016 (if not earlier)
    - L_g~10 – 20 nm experimental devices reported in literature and simulations indicate 5 nm or less feasible

Summary

- **Gate stack is a multi-element arrayed structure wherein high-k and metal electrodes must be successfully integrated into planar, scaled CMOS processes**
  - **Extremely stringent material, electrical and integration challenges**
- **Impact of surface clean and wafer pre-conditioning prior to high-k deposition as well as post-deposition anneal (temperature, time and partial pressure of oxygen in ambient) significantly impacts EOT and leakage**
- **Control of electrical charges incorporated at interfaces and bulk high-k during high-k deposition /anneals critical**
- **Mobility complicated compilation of various contributors**
- **Interactive effects within Gate Stack process modules and IC fabrication process requires utmost attention to achieve requisite IC performance characteristics**

Non-Classical CMOS Summary

- Planar bulk CMOS < $L_g \approx$ 25 nm scaling difficult
  - Enhanced mobility required
    - Strained Si on relaxed or strained Si:Ge may be potential solution
- Key issues:
  - Effectiveness of planar bulk CMOS scaling regime
    - Working devices with $L_g \approx$ 10-20 nm recently noted
  - Effective non-planar solutions must rectify very difficult process issues for multi-gate, FD ultra-thin SOI
  - Control short-channel effects by gate shielding
  - Lg $\approx$ 5 nm may be possible with FD ultra-thin body SOI without excessive band-to-band tunneling
- Ultimate MOSFET (L_g < 10 nm) may be lightly doped channel, ultra-thin body SOI (multiple fins) with high-k gate dielectric, multi-gate metal electrodes (mid-gap work function), elevated source / drain, strained Si, etc. $\Rightarrow$ "ultimate" CMOS device

Evolving Trends of Alternative Novel Device Structures Beyond CMOS

- **Requirements**
  - Capability to be integrated with Si-CMOS
  - Room-temperature operation
  - Capability for SOC, including gigabytes of memory storage
  - Portable capability, with opportunity for large-scale market
- **Examples (non-ranked)**
  - Opto-electronic system (with multi-layered epitaxial structures)
  - Spintronics
  - Self-assembled nanostructures (including molecular structures)
  - Nanowire arrays
  - Microclusters/quantum dots in "SiO_2" (in higher-dimensional matrix)
  - Carbon nanotubes
  - Cellular automata
  - Fullerenes
  - Single-electron structures
  - Optical computers
  - DNA computers
  - Quantum computers

CMOL CONCEPT

gold nanowires

SiO_2 insulation

CMOS wiring

CMOS-
-to-MOL
plug

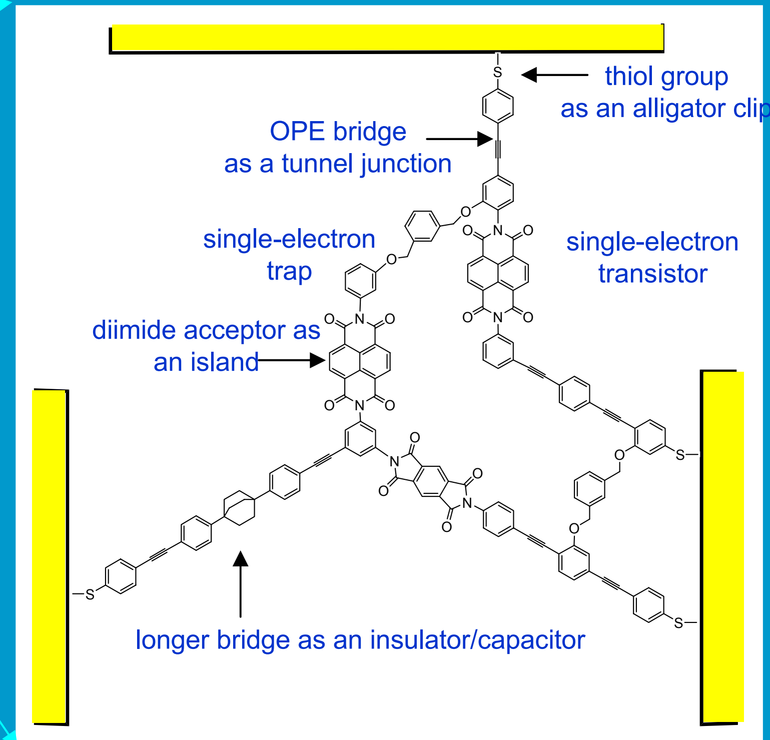
CMOS
plug

gate

SOI MOSFET

Si substrate

molecular single-electron latching switch



Possible density: 3×10^{12} functions per cm^2

K. Likharev and A. Mayr, 2002

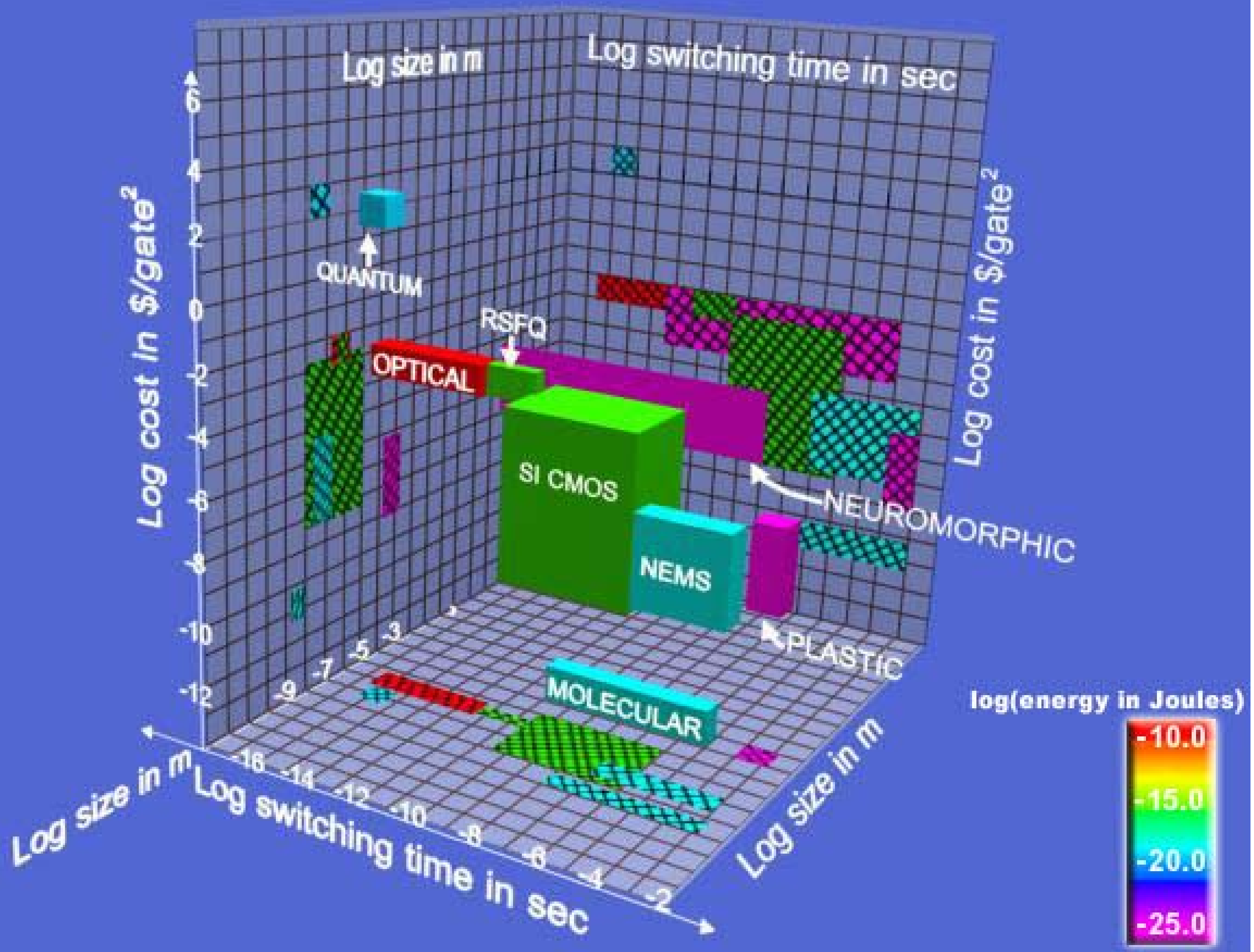
(see http://rsfq1.physics.sunysb.edu/~likharev/nano/GigaNano010603.pdf)

MOSFETS Below 10 nm: Quantum Theory

Konstantin K. Likharev – NanoMES 2003* – Tempe, AZ

- "Room-temperature devices with gate length (L_g) as short as 5 nm still have high transconductance and relatively small DIBL effects and thus may be suitable for nearly all digital applications. Moreover, transistors with L_g as small as 2.5 nm may still feature voltage gain above unity and hence may be the basis for digital electronics
- However, all characteristics of such devices are extremely sensitive to very small variations of their geometrical parameters (L_g, T_{Si} and T_{EOT}) as well as single charged impurities inside (or in the immediate vicinity of the channel)
- As a result of this sensitivity, fabrication of sub-10 nm devices with acceptable yield will require extremely tight specifications, far exceeding recent ITRS projections for the year 2016"

* To be published in Physica E (2003)

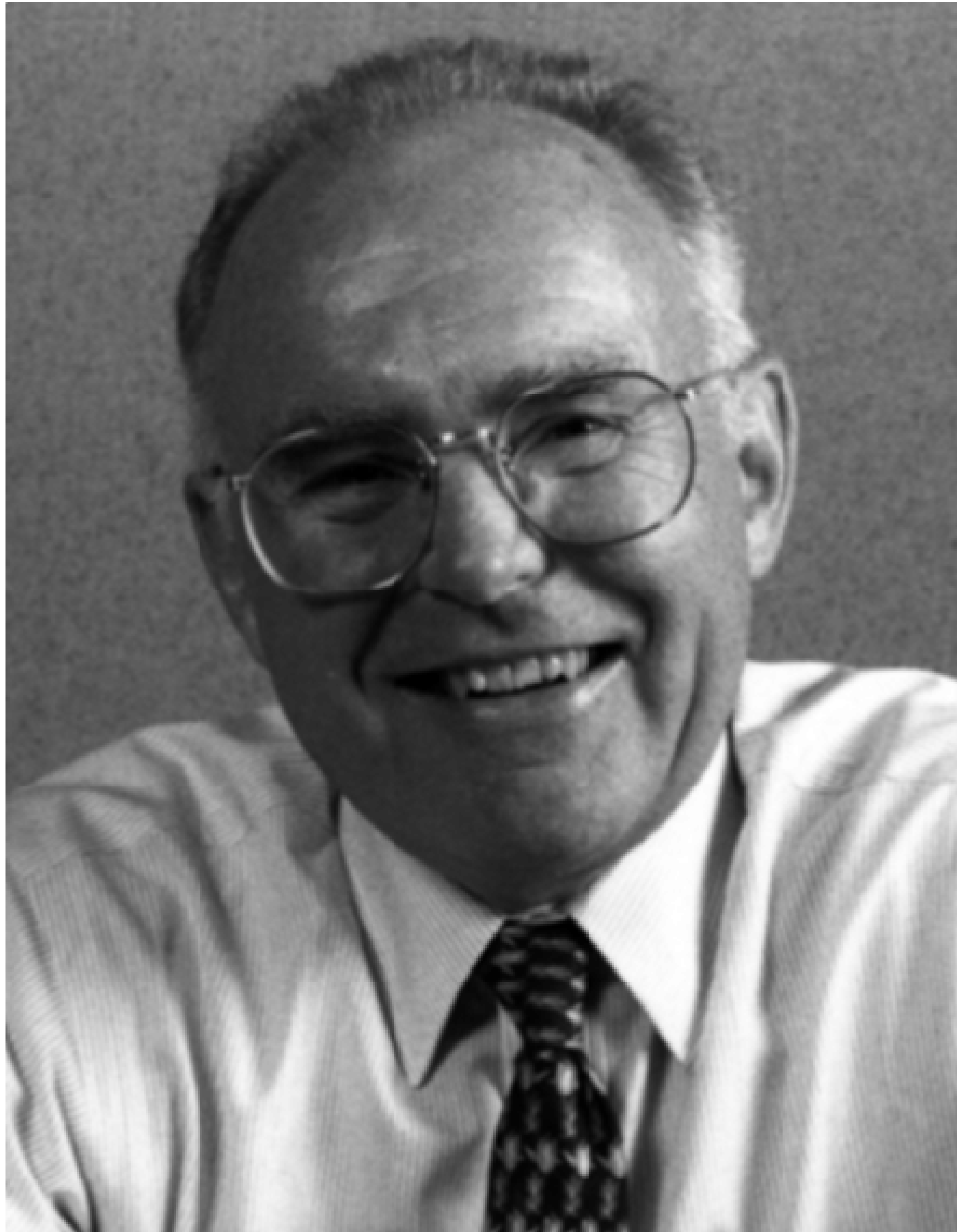

Emerging Technology Parametrization
Log size in m
Log switching time in sec
Log cost in $/gate²
Log cost in $/gate²
QUANTUM
RSFQ
OPTICAL
SI CMOS
NEMS
NEUROMORPHIC
PLASTIC
MOLECULAR
Log size in m
Log switching time in sec
Log size in m
log(energy in Joules)
-10.0
-15.0
-20.0
-25.0

Microelectronics Revolution

- **Gordon Moore (a)**
  - **"But then you see the numbers or hear your company's name on the evening news … and you are once again reminded that this is no longer just an industry, but an economic and cultural phenomenon, a crucial force at the heart of the modern world."**
- **Gordon Moore (b)**
  - **"No exponential is forever: but "forever" can be delayed!"**

(a) Beyond Imagination:Commemorating 25 Years, SIA (2002) [Introduction by Gordon Moore]
(b) ISSCC 2003 / Session 1/ Plenary 1.1 (2003)

Gordon Moore



Agenda

- Introduction
  - MOSFET scaling drivers
- Front-end approaches and solutions
- Non-classical CMOS structures
- Summary / Trends
- Acknowledgements

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