March 2017

Semiconductor Metrology:

Past Present and Future

g dan hutcheson

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VLSIresearch ... intelligence to make better decisions faster

Metrology Time Machine: Dawn of the IC

- Microscopes dominate
  - Wafers handheld under lights for film thickness uniformity
- SEMs used for off-line FA
- Demand first driven by military/aerospace
  - A computer w/tubes would be Empire State building sized for a moon shot

Wafer Inspection in the 60's at Fairchild Semiconductor

The Leading Edge: ~1980

IBM

Microsoft®

Metrology Time Machine: 1980’s

Two Philosophical Approaches:

Inspect to Cull

Make it Perfect

The Leading Edge Issues: 1980's

Breaking the 1µ Barrier

Move from 100 to 125 to 150mm

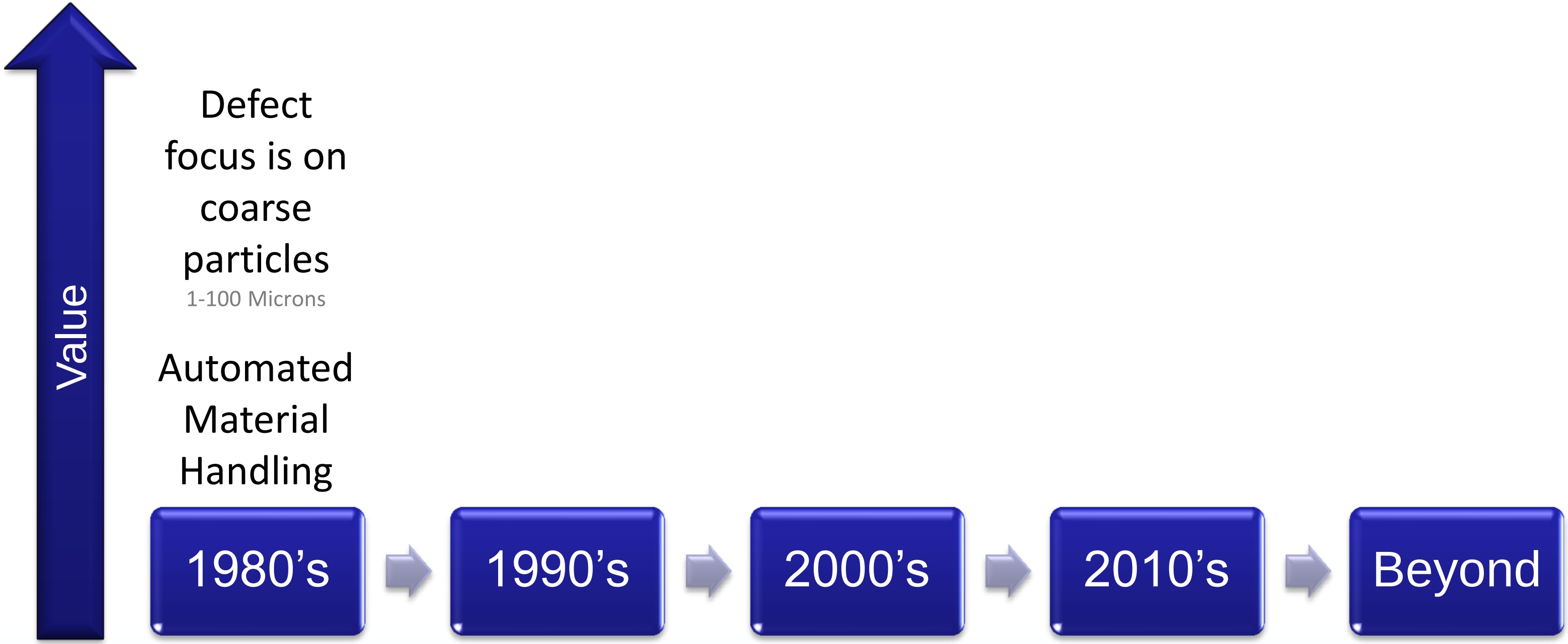
SPC, CD, and Overlay Control enter the scene

Optical dead Electrons & X-rays on the way

Move from Automated Microscopes to Inspection

Ramp yields go from 20% to 60%

History of Inspection



Value

Defect focus is on coarse particles

1-100 Microns

Automated Material Handling

1980's

1990's

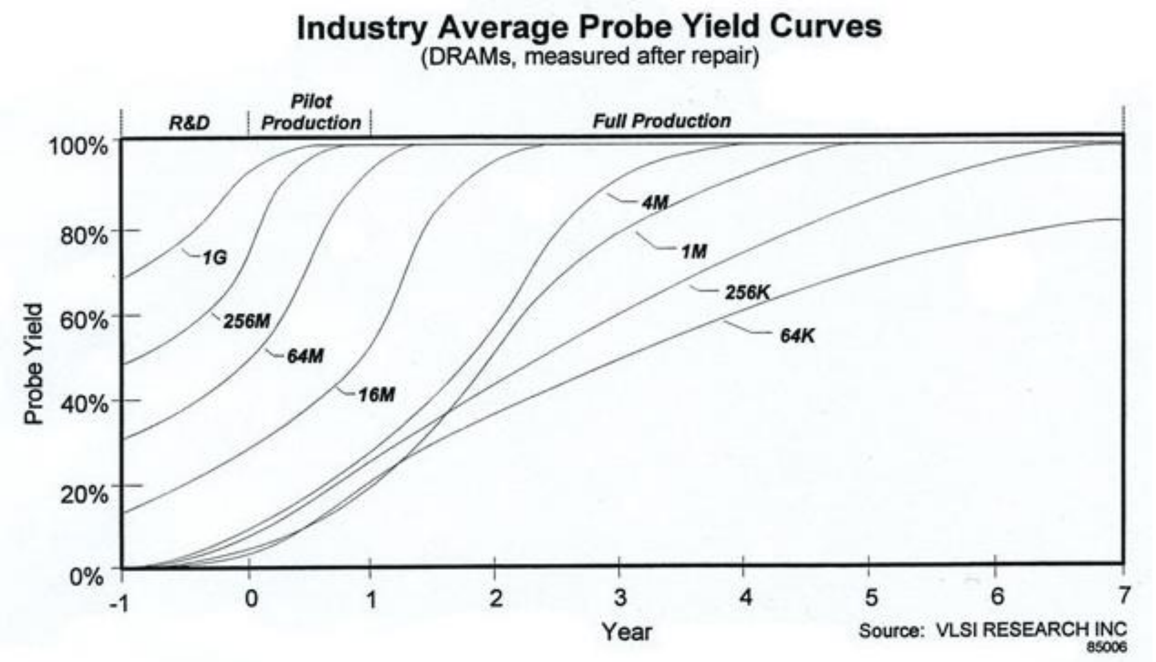
2000's

2010's

Beyond

Yield shifts gear in the 80’s

- It **started in memory**
  - And would follow in logic
    - By the 90’s
- **Metrology** and steppers
  - **made it possible**
- **Japan**’s great chip makers of the day brought **a live or die incentive** to the battlefield.



Industry Average Probe Yield Curves

(DRAMs, measured after repair)

Source: VLSI RESEARCH INC

Metrology Time Machine: 1980’s

KLA 2020, Circa 1984

The tool that sparked **the yield management revolution**

KLA

KLA 2020 WAFER INSPECTOR

“The Measured Difference”

KLA’s Revolutionary system takes you from human judgement to automated measurement.

Controlling a process is measuring the difference between a variable and a reference. The key words are *measured* and *difference*. A semiconductor process can approach a 100% yield by *“measuring the differences”* in the process and changing the parameters which control the fabrication system.

Today, people provide the information for controlling a semiconductor process. But is the accuracy and timeliness of the human “measured difference” good enough to control the fabrication of today’s circuits? And what about tomorrow’s circuit requirements?

Because of the need for a clean environment, are humans part of the process problem?

Now, the KLA 2020 Wafer Inspector provides solutions to these critical questions by allowing you to measure the differences in the most important lithographic process variables. This includes Critical Dimension—Linewidth, Registration and Area—and Defects—Random, Repeating and Pattern. And the system allows all of this without operator contamination.

Who would have thought that your best process engineer could be an inspector? With the multifunction KLA 2020, your best engineer can easily program the inspections to be executed—at the right location, the right frequency and to the correct specifications.

The KLA 2020 is not only fast and accurate, it can keep up with the output of several of your fastest steppers or printers. The results provided by the Wafer Inspector are statistically more precise, more consistent, and more timely than is possible with other methods in practice today.

There is much more that you should know about the “measured difference” from KLA Instruments Corporation. It could make a major difference to improving your process . . . and your profits.

Call or write today for our brochure which details information about the KLA 2020 Wafer Inspector.

KLA

The KLA 2020 is a fully automated
in-process wafer inspection system
with on-line, real time (process) feedback.

APPLICATIONS

A develop inspection/final inspection process monitor which can measure multi-level patterned wafers for:
- ☐ Linewidth
- ☐ Contact Area
- ☐ Registration Error
- ☐ Pattern Defects
- ☐ Random Defects
- ☐ Repeating Defects
- ☐ Large or Macro Defects

A stepper/reticle qualification system which can find repeating defects by image comparison:
- ☐ Wafer Reference
  - –Any die to any die on same wafer; multi-die reticles.
- ☐ Standard Reference
  - –Stored image for comparison to any selected die; single die reticle.
- ☐ Optional Design Reference
  - –Data base tape to any die on mono-level test wafer.

The ability to remove a major source of contamination from the fabrication area by doing inspections automatically without operators.

FEATURES

Process engineers can create (and store) a program to run the exact inspection to be performed. Programs can be created easily by selecting inspection options from a comprehensive set of menus.

Inspection output can be specified in various formats:
- ☐ Separating wafers into accept/reject cassettes
- ☐ Defect images/data stored for review
- ☐ Printout of defect data
- ☐ Graphs, plots and control charts.

PHYSICAL DESCRIPTION

Console:
- –Programming/operator station built around touch panel, joystick and keyboard.
- –Program/data stored on fixed and removable hard disks (80 Mbytes).
- –Monitor displays program, wafer image and inspection results.

Inspection Station:
- –Cassette-to-cassette wafer transport in a hepa-filtered, micro environment.
- –Vibration isolated optics capture high resolution, 256 gray level wafer images.

Image Computer:
- –Motorola 68000 microprocessor is used to control system.
- –KLA designed high speed image processing computer for image analysis.
- –Can be remote from inspection station and console.

SPECIFICATIONS

Measurement	Description	Magnification	Sensitivity
Macro Test	Topographical and pattern defects	1.6×	>25 μm
Micro Comparison	Pattern, repeating or random defects found using Wafer, Standard or Design Reference.	130×	≥2–4 μm
		260×	≥1–2 μm
		520×	≥0.5–1 μm
		1300×	≥0.5 μm
		3σ Precision	**Range**
Micro Measurement	Linewidth (For Thinfilms)	0.03 μm	1–25 μm
	Area	0.2 μm²	1–10 μm²
	Registration	0.05 μm	0–2 μm

THRU-PUT

Process Monitor—Sample Calculation:

Measurement	Frequency/Specification
Macro Test	Full wafer, every wafer.
Micro Comparison	Every wafer, ≥0.5–1 μm sensitivity, die-to-die reference, 20 inspections per wafer.
Micro Measurements	
Linewidth	3 measurements, every fourth wafer.
Registration	2 measurements, every wafer.

Thru-Put
- **Approximately 110 wafers/hr.**
- **Approximately 150 wafers/hr. without macro test.**

Reticle Qualification:

Reference	Sensitivity	Thru-Put
Wafer Reference (die-to-die)	≥0.5–1 μm	13 min./cm²
	≥1–2 μm	3 min./cm²
Standard Reference (die-to-stored image)	≥0.5–1 μm	20 min./cm²
	≥1–2 μm	5 min./cm²

OPTIONS

Design Reference Generator	Qualifies reticles by inspecting mono-level wafers with respect to a design data base tape.
Printer	Produces hard copy of numerical inspection data in tabular or graphical forms.
Image Hard Copy	Produces black and white copy of wafer image as it appears on the monitor.
Mass Storage	A mass storage device used to store additional images for use as standard reference.

KLA INSTRUMENTS CORPORATION

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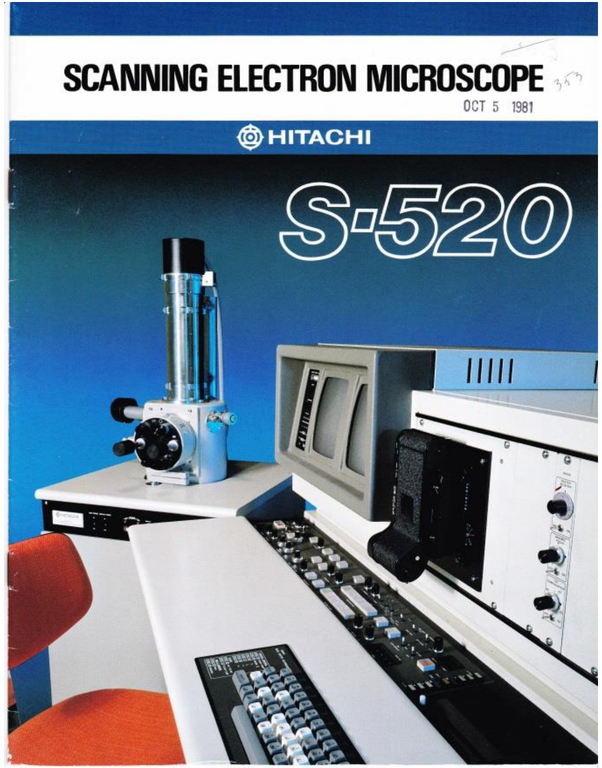
Metrology Time Machine: 1980’s



SCANNING ELECTRON MICROSCOPE 353

OCT 5 1981

HITACHI

S-520

NC 353,60

RECEIVED
JUN 18 1985
VLSI RESEARCH

MODEL EP-1035
HITACHI IMAGE PROCESSOR
CD MEASUREMENT ACCESSORY

– ITS FEATURES AND SPECIFICATIONS –

HITACHI

APPLICATION DATA

A simultaneous dual magnification split screen display
Specimen: IC
Split screen mode showing a high magnification of IC (left above) and a low magnification image simultaneously. This photograph is recorded from a frame memory.

A manual CD measurement by cursor
Specimen: IC
CD measurements of an IC line held between 2 sets of cursors are shown at the top left. Figures in parentheses indicate number of pixels (picture element). "D" indicates diagonal measurement.

① Auto measurement-1 |→←|
Specimen: IC pattern
CD measurements of an IC pattern selected by 2 sets of cursors were taken. Edges of the IC line are detected automatically by this system and are shown by white dots. The measured points are clearly seen on the picture. Figures in the middle right are a number of measurements (N=36), average value of measurements (AV=4.75 µm) and standard deviation (SD=0.02 µm). Data on the top left shows respective cursor separations.

② Auto measurement-2 ←| |→
Specimen: IC pattern
Space width of an IC was measured. Edges of the IC line were detected toward right and left from the cursors (X) and they are shown by white dots.

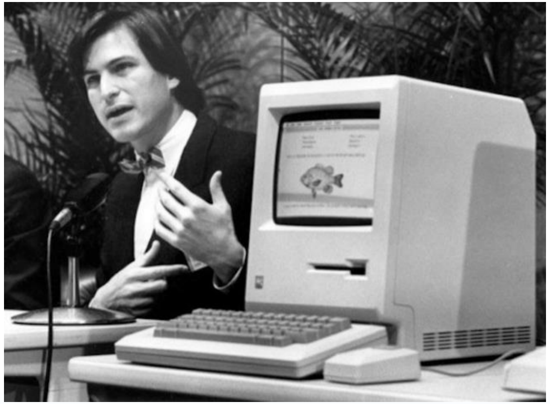
③ Auto measurement-3 |→ |→
Specimen: IC pattern
Pitch width of an IC pattern was measured. Edges of the IC line were detected toward right from the cursors (X). White dots represent the edge of the IC line.

④ Auto measurement-4
Specimen: IC pattern
This is an example of rotated image. In spite of the fact that the IC pattern is not aligned to the cursors, this system automatically detects the rotation and computes the true space width by cosine θ correction.

The star (*) marks at AV=4.97 µm* and SD=0.04 µm* indicate that these are rotation corrected values.

4

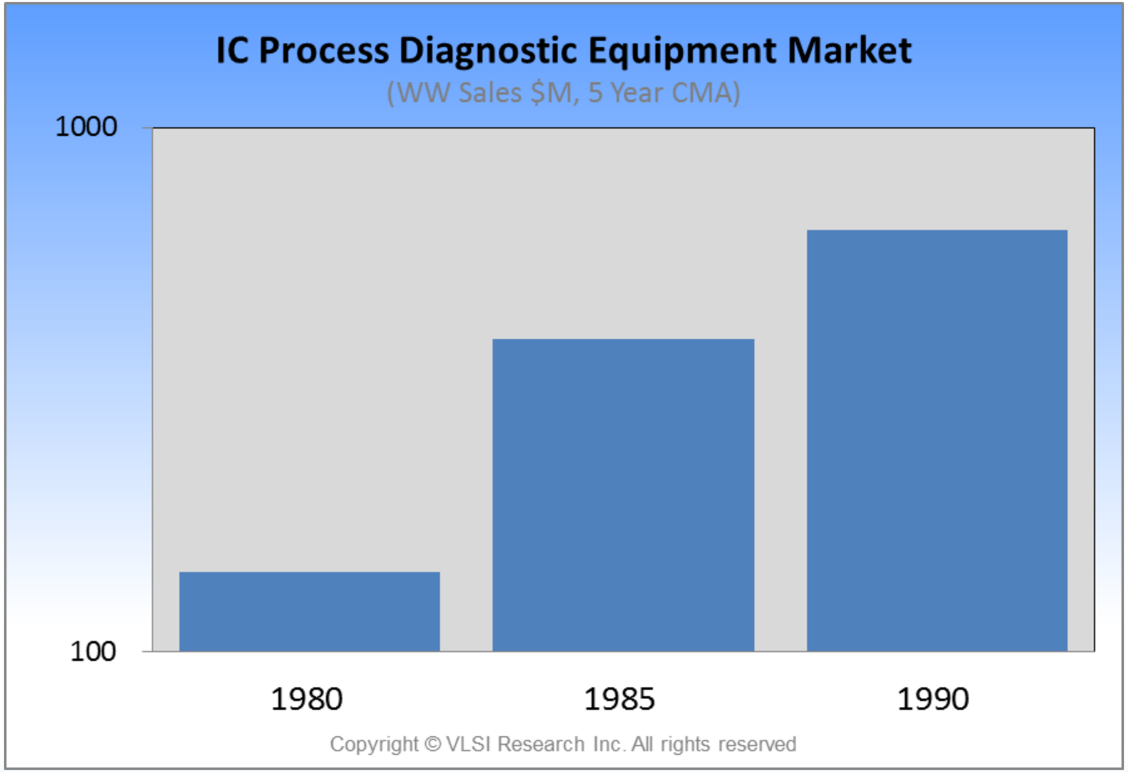
The Leading Edge: ~1985



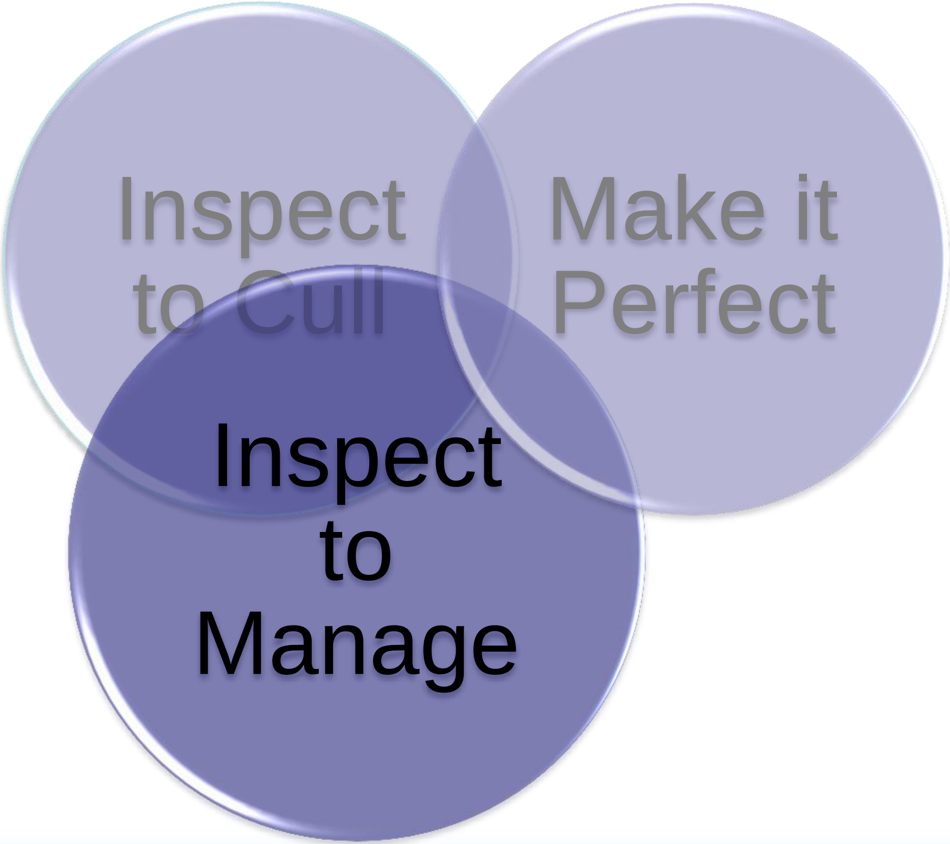
Microsoft

Yield dividend would drive metrology

- Ramp yields went from 20% to 60%
  - Between 1980 and 2000
- Yield added an additional kick to Moore's Law
  - Only possible with process diagnostic tools



Metrology Time Machine: 1990's



Inspect to Cull

Make it Perfect

Inspect to Manage

A New
Paradigm
Emerges:

The Leading Edge: ~1990

The Leading Edge Issues: 1990’s

Getting to “deep-sub-micron

Move from 150mm to 200mm

SPC rises to the top of the control issues

Optical dead for metrology… Electrons on the way

Threat of Japan

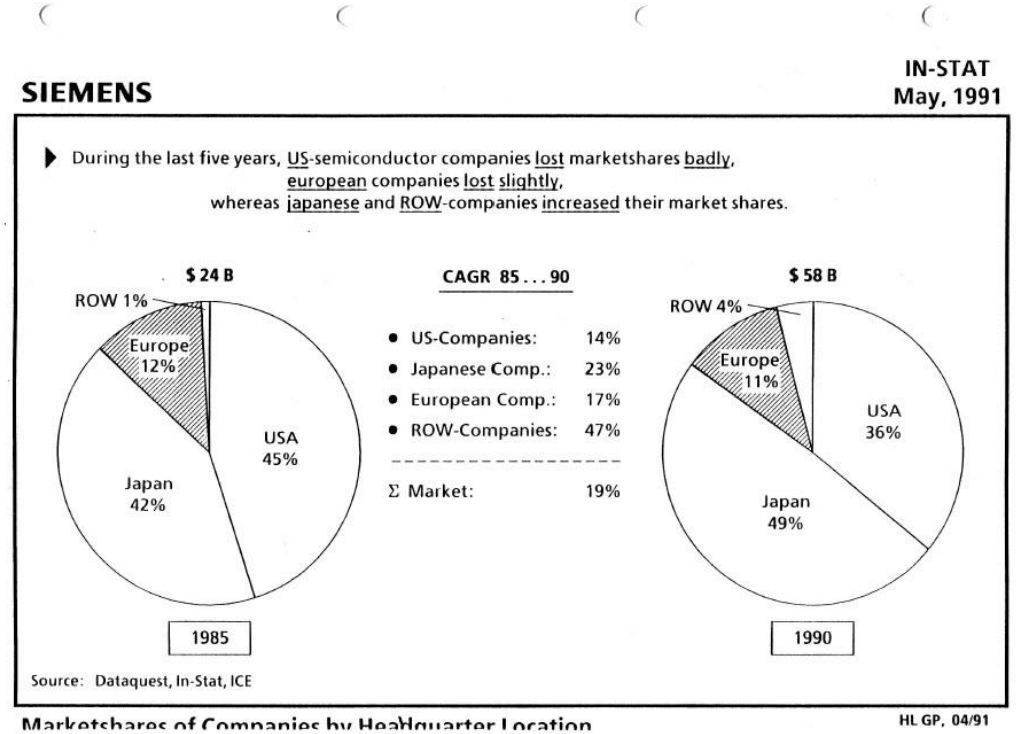
Rise of the Tigers: Korea & Taiwan

@ ISS Europe 1992:

There was a …

- Can’t beat Japan attitude
  - They “won by cheating”
- *But Europe was holding it’s own ground*
  - *Doing a much better job than America*

Why such a Dark Outlook?



SIEMENS

IN-STAT
May, 1991

During the last five years, US-semiconductor companies lost marketshares badly, european companies lost slightly, whereas japanese and ROW-companies increased their market shares.

CAGR 85 . . . 90

US-Companies:	14%
Japanese Comp.:	23%
European Comp.:	17%
ROW-Companies:	47%
Σ Market:	19%

Source: Dataquest, In-Stat, ICE

Marketshares of Companies by Headquarter Location

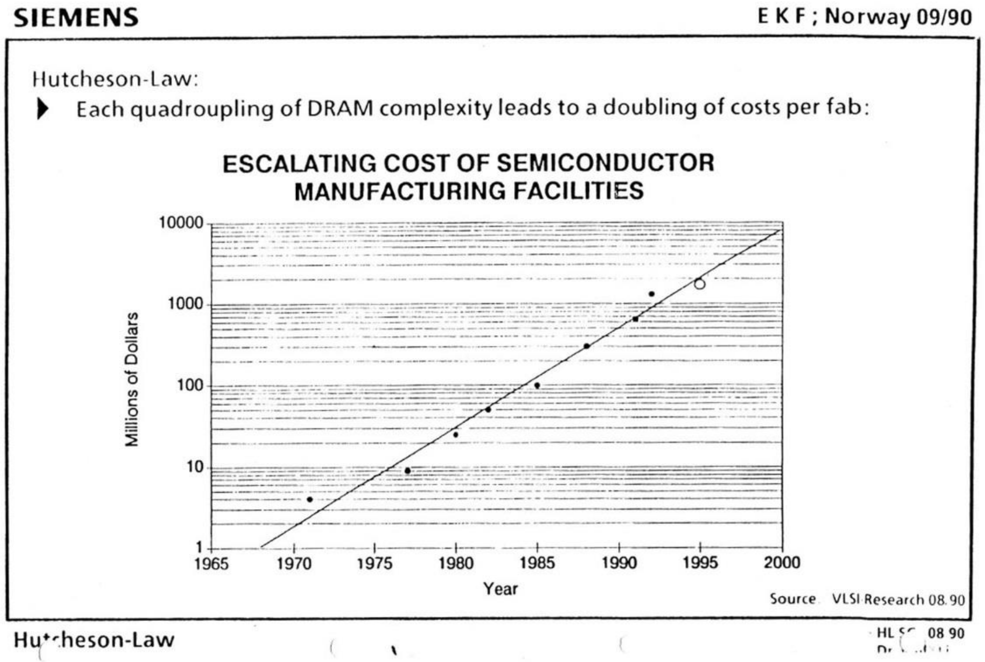
HL GP, 04/91

Source: ISS 1992, Hartwig Reull

What some said @ ISS Europe 1992:

- Fabs getting too expensive
- That Europe lacked:
  - – Strategic Planning
  - – Critical Scale
  - – Lacked a modern economic policy
    - Adam Smith vs. Keiretsu

The Future looked Dark to Europeans and many others



SIEMENS E K F ; Norway 09/90

Hutcheson-Law:

- Each quadroupling of DRAM complexity leads to a doubling of costs per fab:

ESCALATING COST OF SEMICONDUCTOR MANUFACTURING FACILITIES

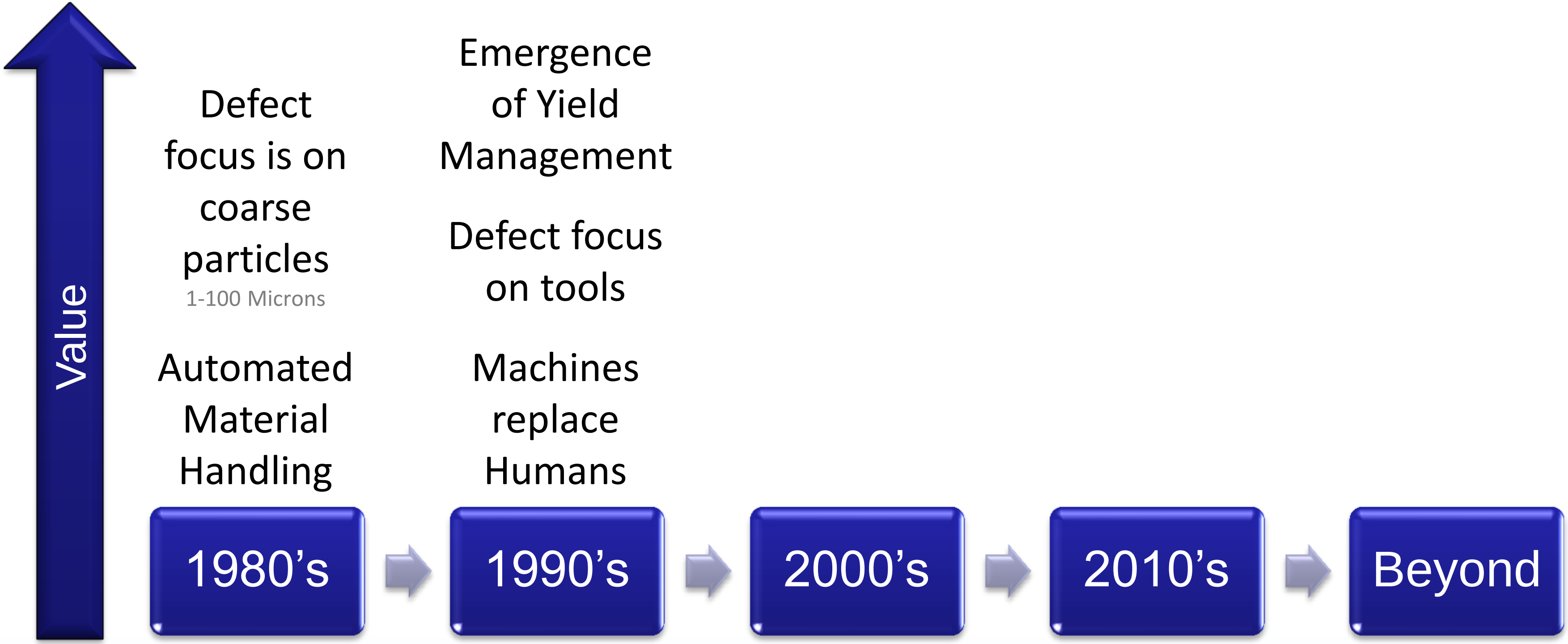
Source VLSI Research 08.90

Hutcheson-Law

HL [illegible] 08 90

Source: ISS 1992, Hartwig Reull

History of Inspection



Value

Defect
focus is on
coarse
particles
1-100 Microns

Automated
Material
Handling

Emergence
of Yield
Management

Defect focus
on tools

Machines
replace
Humans

1980’s

1990’s

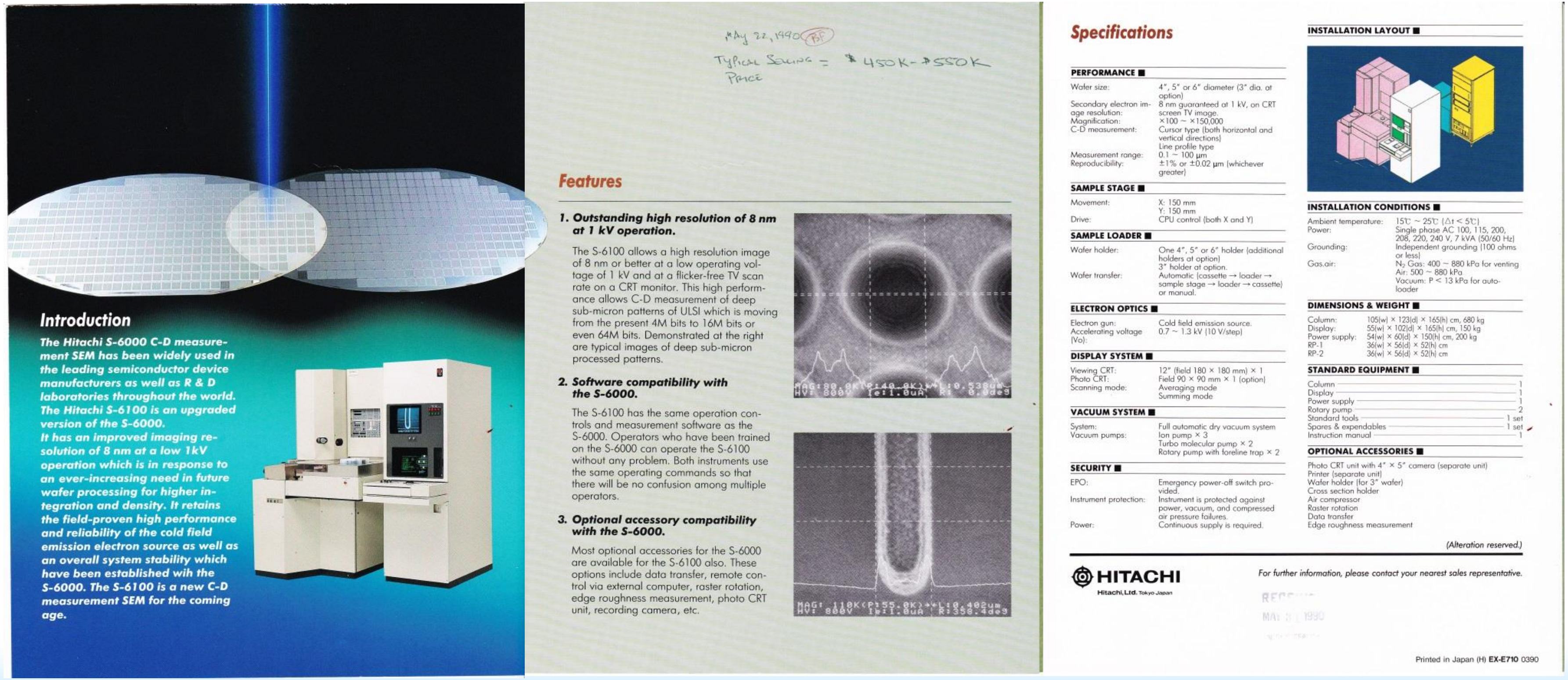
2000’s

2010’s

Beyond

Metrology Time Machine: 1990’s

Hitachi S6000



Introduction

The Hitachi S-6000 C-D measurement SEM has been widely used in the leading semiconductor device manufacturers as well as R & D laboratories throughout the world. The Hitachi S-6100 is an upgraded version of the S-6000. It has an improved imaging resolution of 8 nm at a low 1kV operation which is in response to an ever-increasing need in future wafer processing for higher integration and density. It retains the field-proven high performance and reliability of the cold field emission electron source as well as an overall system stability which have been established with the S-6000. The S-6100 is a new C-D measurement SEM for the coming age.

MAy 22, 1990 BF

Typical Selling Price = $450K-$550K

Features

1. *Outstanding high resolution of 8 nm at 1 kV operation.*

The S-6100 allows a high resolution image of 8 nm or better at a low operating voltage of 1 kV and at a flicker-free TV scan rate on a CRT monitor. This high performance allows C-D measurement of deep sub-micron patterns of ULSI which is moving from the present 4M bits to 16M bits or even 64M bits. Demonstrated at the right are typical images of deep sub-micron processed patterns.

2. *Software compatibility with the S-6000.*

The S-6100 has the same operation controls and measurement software as the S-6000. Operators who have been trained on the S-6000 can operate the S-6100 without any problem. Both instruments use the same operating commands so that there will be no confusion among multiple operators.

3. *Optional accessory compatibility with the S-6000.*

Most optional accessories for the S-6000 are available for the S-6100 also. These options include data transfer, remote control via external computer, raster rotation, edge roughness measurement, photo CRT unit, recording camera, etc.

Specifications

PERFORMANCE ■

Wafer size:	4", 5" or 6" diameter (3" dia. at option)
Secondary electron image resolution:	8 nm guaranteed at 1 kV, on CRT screen TV image.
Magnification:	×100 ~ ×150,000
C-D measurement:	Cursor type (both horizontal and vertical directions) Line profile type
Measurement range:	0.1 ~ 100 μm
Reproducibility:	±1% or ±0.02 μm (whichever greater)

SAMPLE STAGE ■

Movement:	X: 150 mm Y: 150 mm
Drive:	CPU control (both X and Y)

SAMPLE LOADER ■

Wafer holder:	One 4", 5" or 6" holder (additional holders at option) 3" holder at option.
Wafer transfer:	Automatic (cassette → loader → sample stage → loader → cassette) or manual.

ELECTRON OPTICS ■

Electron gun:	Cold field emission source.
Accelerating voltage (Vo):	0.7 ~ 1.3 kV (10 V/step)

DISPLAY SYSTEM ■

Viewing CRT:	12" (field 180 × 180 mm) × 1
Photo CRT:	Field 90 × 90 mm × 1 (option)
Scanning mode:	Averaging mode Summing mode

VACUUM SYSTEM ■

System:	Full automatic dry vacuum system
Vacuum pumps:	Ion pump × 3 Turbo molecular pump × 2 Rotary pump with foreline trap × 2

SECURITY ■

EPO:	Emergency power-off switch provided.
Instrument protection:	Instrument is protected against power, vacuum, and compressed air pressure failures.
Power:	Continuous supply is required.

INSTALLATION LAYOUT ■

INSTALLATION CONDITIONS ■

Ambient temperature:	15℃ ~ 25℃ (Δt < 5℃)
Power:	Single phase AC 100, 115, 200, 208, 220, 240 V, 7 kVA (50/60 Hz)
Grounding:	Independent grounding (100 ohms or less)
Gas,air:	N_2 Gas: 400 ~ 880 kPa for venting Air: 500 ~ 880 kPa Vacuum: P < 13 kPa for auto-loader

DIMENSIONS & WEIGHT ■

Column:	105(w) × 123(d) × 165(h) cm, 680 kg
Display:	55(w) × 102(d) × 165(h) cm, 150 kg
Power supply:	54(w) × 60(d) × 150(h) cm, 200 kg
RP-1	36(w) × 56(d) × 52(h) cm
RP-2	36(w) × 56(d) × 52(h) cm

STANDARD EQUIPMENT ■

Column	1
Display	1
Power supply	1
Rotary pump	2
Standard tools	1 set
Spares & expendables	1 set
Instruction manual	1

OPTIONAL ACCESSORIES ■

- Photo CRT unit with 4" × 5" camera (separate unit)
- Printer (separate unit)
- Wafer holder (for 3" wafer)
- Cross section holder
- Air compressor
- Raster rotation
- Data transfer
- Edge roughness measurement

(Alteration reserved.)

HITACHI
Hitachi,Ltd. Tokyo Japan

For further information, please contact your nearest sales representative.

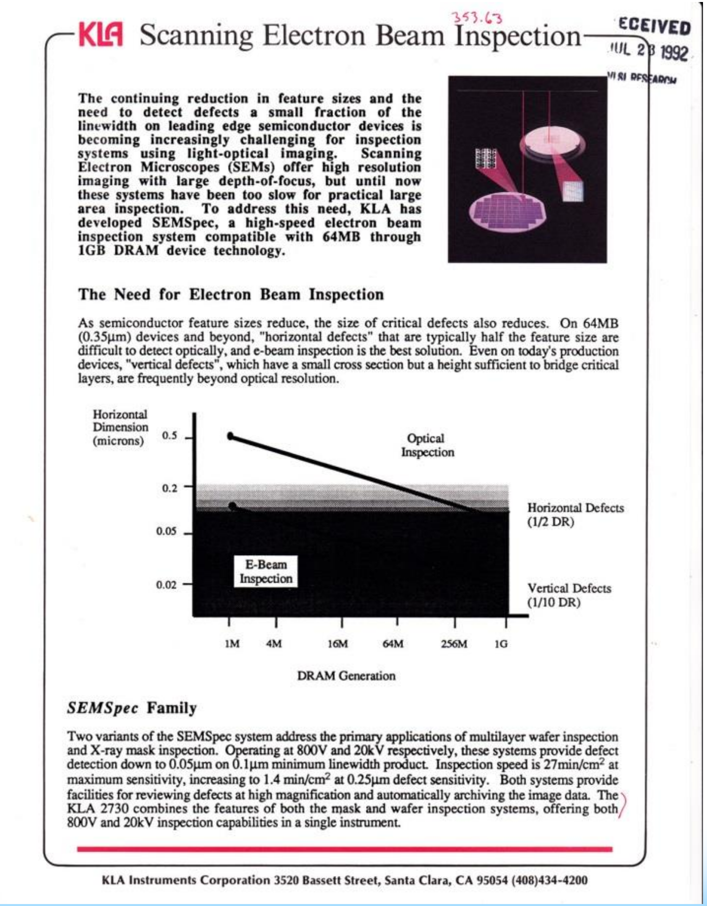
Printed in Japan (H) **EX-E710** 0390

Metrology Time Machine: 1990’s

Even KLA got on the e-beam bandwagon

- Optical would die out after 200nm …

- But we still were not in the nanochip era
  - They were microchips



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ECEIVED
JUL 28 1992
VLSI RESEARCH

KLA Scanning Electron Beam Inspection

The continuing reduction in feature sizes and the need to detect defects a small fraction of the linewidth on leading edge semiconductor devices is becoming increasingly challenging for inspection systems using light-optical imaging. Scanning Electron Microscopes (SEMs) offer high resolution imaging with large depth-of-focus, but until now these systems have been too slow for practical large area inspection. To address this need, KLA has developed SEMSpec, a high-speed electron beam inspection system compatible with 64MB through 1GB DRAM device technology.

The Need for Electron Beam Inspection

As semiconductor feature sizes reduce, the size of critical defects also reduces. On 64MB (0.35µm) devices and beyond, "horizontal defects" that are typically half the feature size are difficult to detect optically, and e-beam inspection is the best solution. Even on today's production devices, "vertical defects", which have a small cross section but a height sufficient to bridge critical layers, are frequently beyond optical resolution.

SEMSpec Family

Two variants of the SEMSpec system address the primary applications of multilayer wafer inspection and X-ray mask inspection. Operating at 800V and 20kV respectively, these systems provide defect detection down to 0.05µm on 0.1µm minimum linewidth product. Inspection speed is 27min/cm^2 at maximum sensitivity, increasing to 1.4 min/cm^2 at 0.25µm defect sensitivity. Both systems provide facilities for reviewing defects at high magnification and automatically archiving the image data. The KLA 2730 combines the features of both the mask and wafer inspection systems, offering both 800V and 20kV inspection capabilities in a single instrument.

KLA Instruments Corporation 3520 Bassett Street, Santa Clara, CA 95054 (408)434-4200

Metrology Time Machine: 1990's

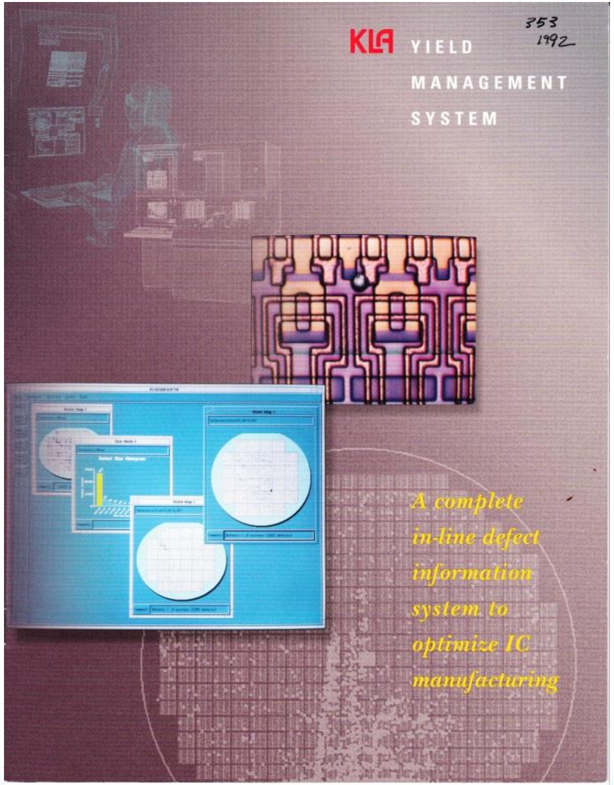
The big change was the KLA's concept of…

Yield Management

Developed in Korea with Samsung, it would upend the memory market

Samsung was trying to get the most **good die-out-per-wafer** by inspecting to cull out the yield killers

Japan was stuck on the old **make-it-perfect** philosophy: they were after **the perfect cleanroom**



353
1992

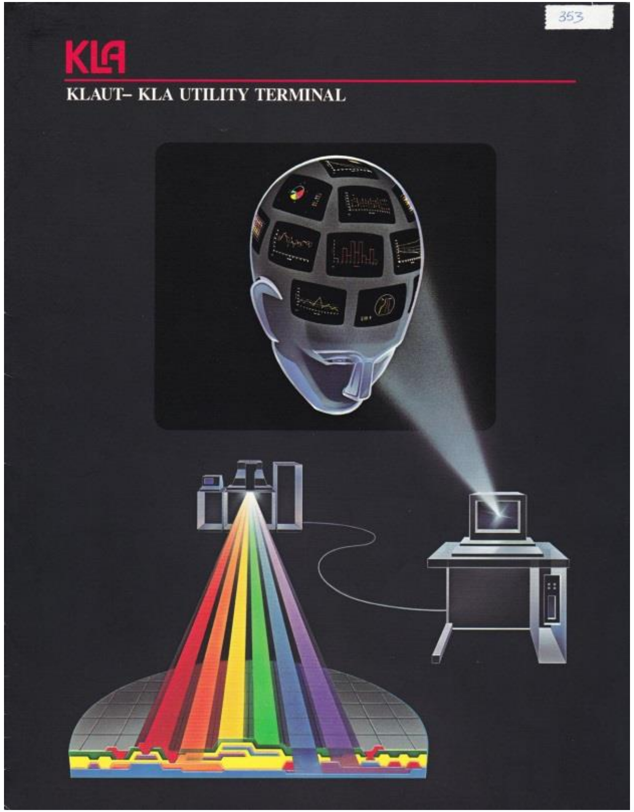
KLA YIELD MANAGEMENT SYSTEM

A complete in-line defect information system to optimize IC manufacturing

Metrology Time Machine: 1990’s

We were starting to **put it all together** with **data visualization** tools linked to distributed inspection and metrology platforms

It may not have worked well, but it was **visionary** – this was **the future**



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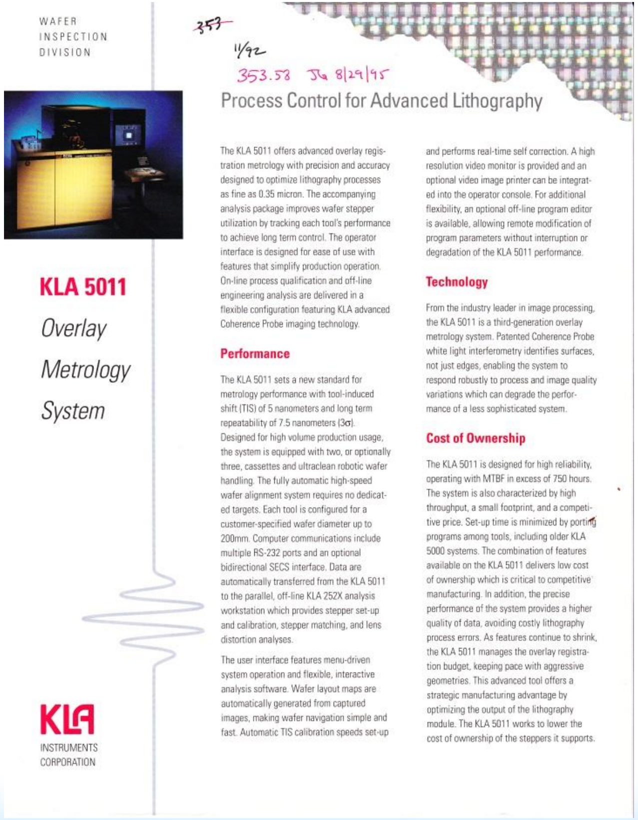
KLA

KLAUT– KLA UTILITY TERMINAL

Metrology Time Machine: 1990’s

Lithography was rising to the top of the issues

Overlay Control broke into the fab and **became** an **in-line** process step



WAFER
INSPECTION
DIVISION

~~353~~

11/92

353.58 JG 8/29/95

Process Control for Advanced Lithography

KLA 5011

Overlay
Metrology
System

The KLA 5011 offers advanced overlay registration metrology with precision and accuracy designed to optimize lithography processes as fine as 0.35 micron. The accompanying analysis package improves wafer stepper utilization by tracking each tool's performance to achieve long term control. The operator interface is designed for ease of use with features that simplify production operation. On-line process qualification and off-line engineering analysis are delivered in a flexible configuration featuring KLA advanced Coherence Probe imaging technology.

Performance

The KLA 5011 sets a new standard for metrology performance with tool-induced shift (TIS) of 5 nanometers and long term repeatability of 7.5 nanometers (3σ). Designed for high volume production usage, the system is equipped with two, or optionally three, cassettes and ultraclean robotic wafer handling. The fully automatic high-speed wafer alignment system requires no dedicated targets. Each tool is configured for a customer-specified wafer diameter up to 200mm. Computer communications include multiple RS-232 ports and an optional bidirectional SECS interface. Data are automatically transferred from the KLA 5011 to the parallel, off-line KLA 252X analysis workstation which provides stepper set-up and calibration, stepper matching, and lens distortion analyses.

The user interface features menu-driven system operation and flexible, interactive analysis software. Wafer layout maps are automatically generated from captured images, making wafer navigation simple and fast. Automatic TIS calibration speeds set-up and performs real-time self correction. A high resolution video monitor is provided and an optional video image printer can be integrated into the operator console. For additional flexibility, an optional off-line program editor is available, allowing remote modification of program parameters without interruption or degradation of the KLA 5011 performance.

Technology

From the industry leader in image processing, the KLA 5011 is a third-generation overlay metrology system. Patented Coherence Probe white light interferometry identifies surfaces, not just edges, enabling the system to respond robustly to process and image quality variations which can degrade the performance of a less sophisticated system.

Cost of Ownership

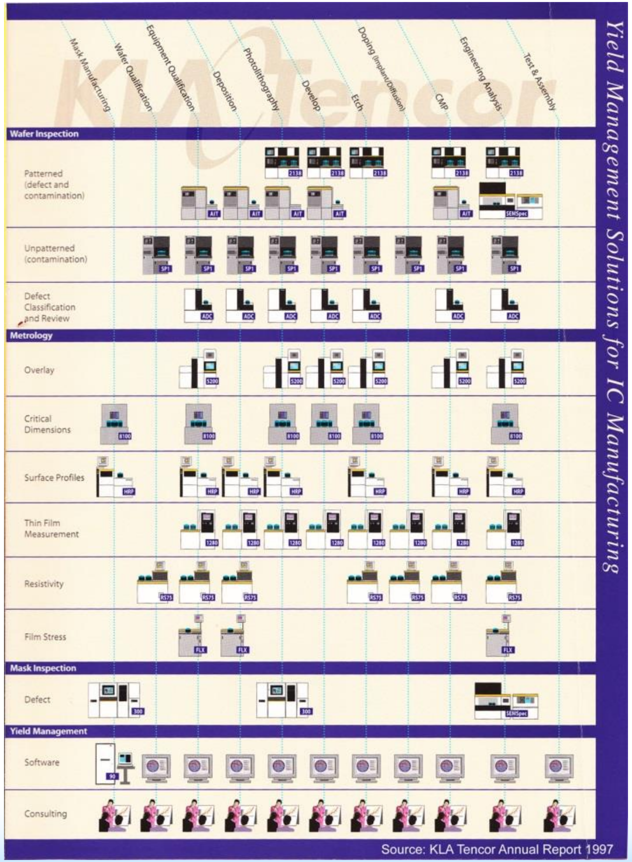
The KLA 5011 is designed for high reliability, operating with MTBF in excess of 750 hours. The system is also characterized by high throughput, a small footprint, and a competitive price. Set-up time is minimized by porting programs among tools, including older KLA 5000 systems. The combination of features available on the KLA 5011 delivers low cost of ownership which is critical to competitive manufacturing. In addition, the precise performance of the system provides a higher quality of data, avoiding costly lithography process errors. As features continue to shrink, the KLA 5011 manages the overlay registration budget, keeping pace with aggressive geometries. This advanced tool offers a strategic manufacturing advantage by optimizing the output of the lithography module. The KLA 5011 works to lower the cost of ownership of the steppers it supports.

KLA
INSTRUMENTS
CORPORATION

Metrology Time Machine: 1990's

In the 90's

- Process diagnostic tools used across …
  - **12 production areas**
  - **11+ critical applications**
- Versus 1 and 2 before 1980



Source: KLA Tencor Annual Report 1997

The Leading Edge: ~1995

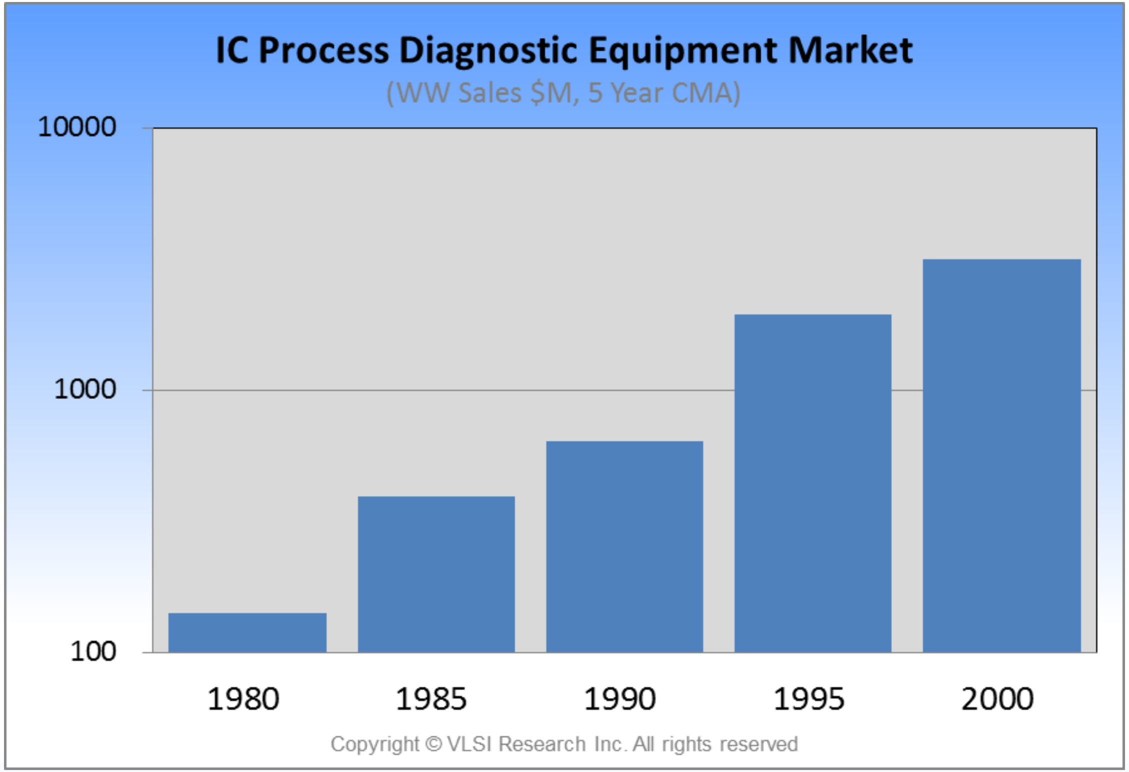
Metrology Time Machine: *As the 1990's close, you still see it as* ***humans clustered around a tool …*** *but it's data not images that are being looked at*

Source: KLA Tencor Annual Report 1996

Source: KLA Tencor Annual Report 1997

Yield dividend continues to drive metrology

- But it’s no longer the good-die, bad-die, and ugly story
- Profits now come from sort yields
  - Better performance yields better prices
- It’s now a good, better, best focus



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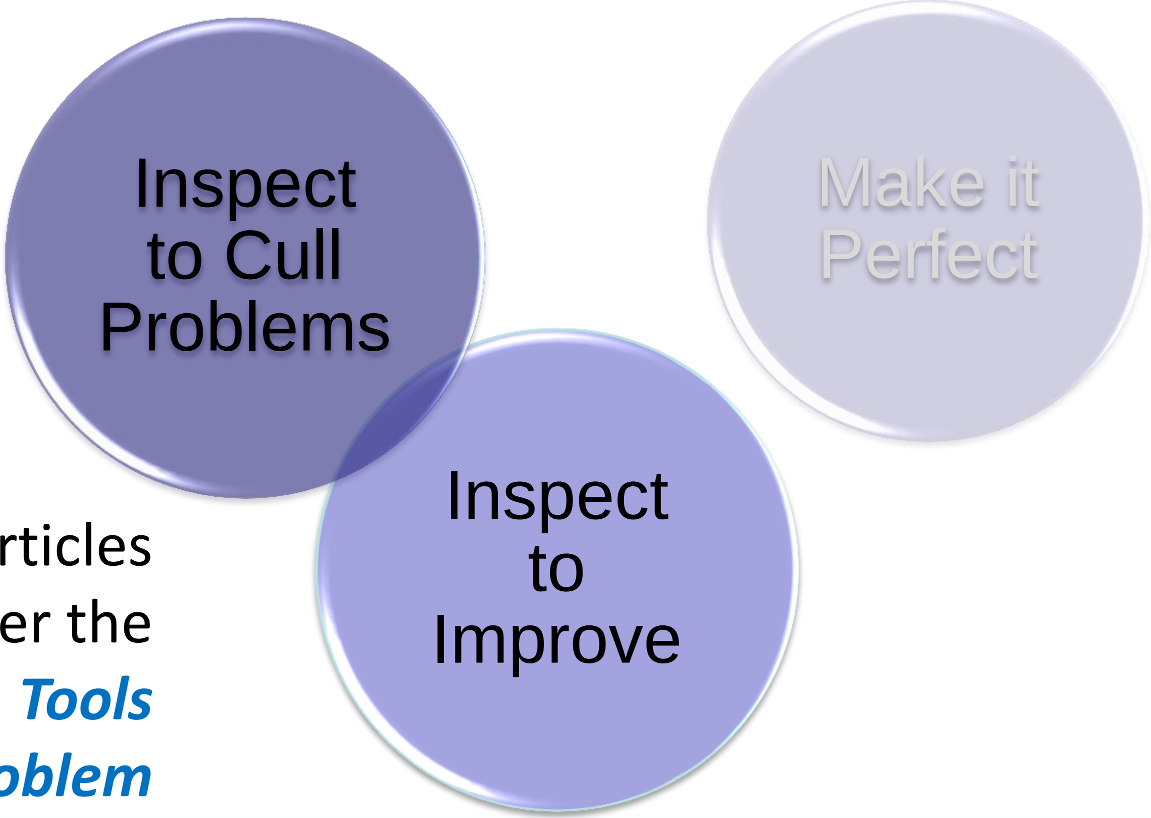
Metrology Time Machine: 2000's



Inspect to Cull Problems

Inspect to Improve

Make it Perfect

Cleanroom Particles were no longer the problem. ***Tools were the problem***

The Leading Edge Issues: 2000's

Microchips become Nanochips

The first mass-produced nantechnology

Move from 200mm to 300mm

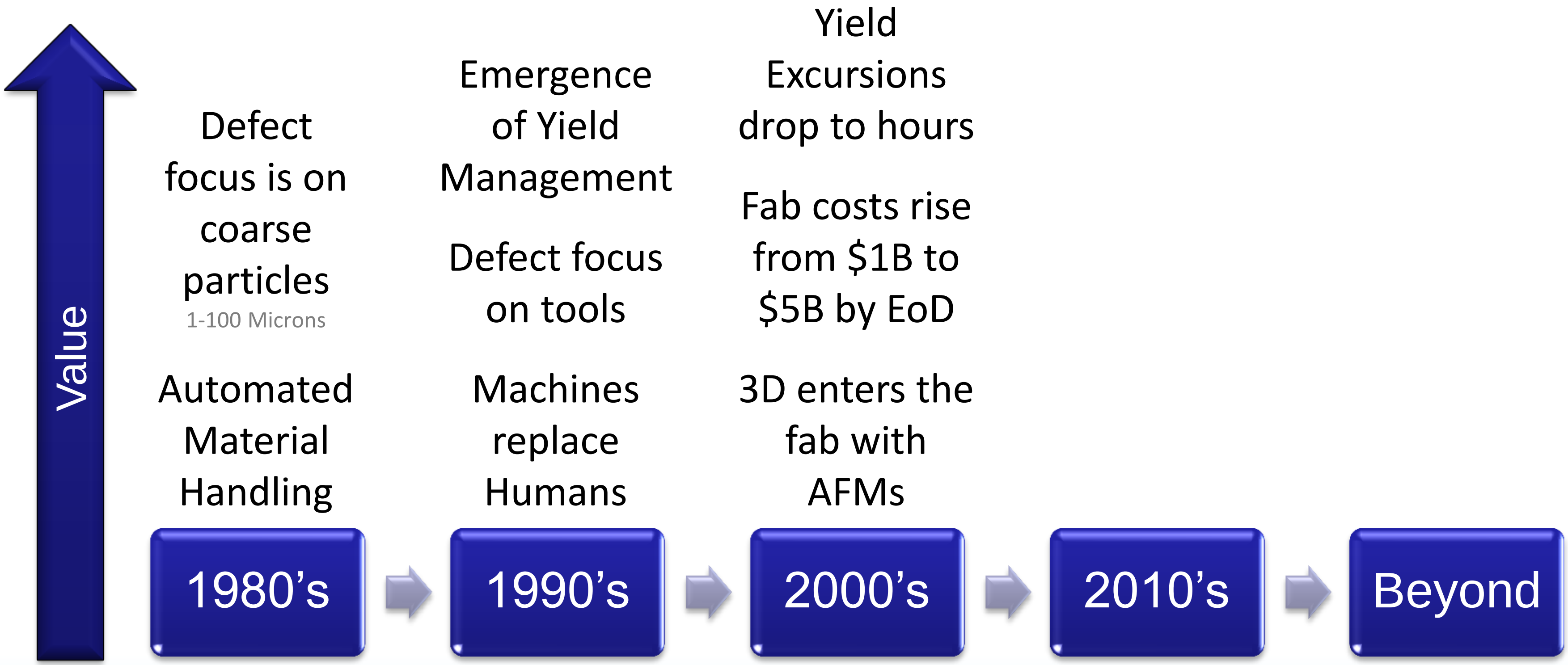
CDU, LER, and Overlay Control become big contributors to profitability

Electrons learn to live with their bigger brother: Optics

Millennium mania, the dot-com bust, and the Great Recession = the lost decade

Ramp yields go from 60% to 80% for memory

History of Inspection



1980's

Defect focus is on coarse particles

1-100 Microns

Automated Material Handling

1990's

Emergence of Yield Management

Defect focus on tools

Machines replace Humans

2000's

Yield Excursions drop to hours

Fab costs rise from $1B to $5B by EoD

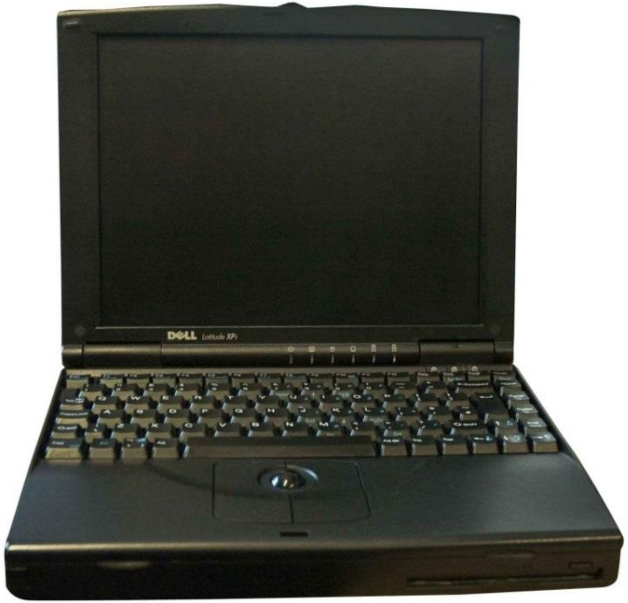
3D enters the fab with AFMs

2010's

Beyond

The Leading Edge: ~2000

Irwin Jacobs is trying to merge these two



amazon

is a book store

Google

is a start-up and like 1000’s of other internet startups … **it has no Business Model**

The Leading Edge: ~2005

Microsoft

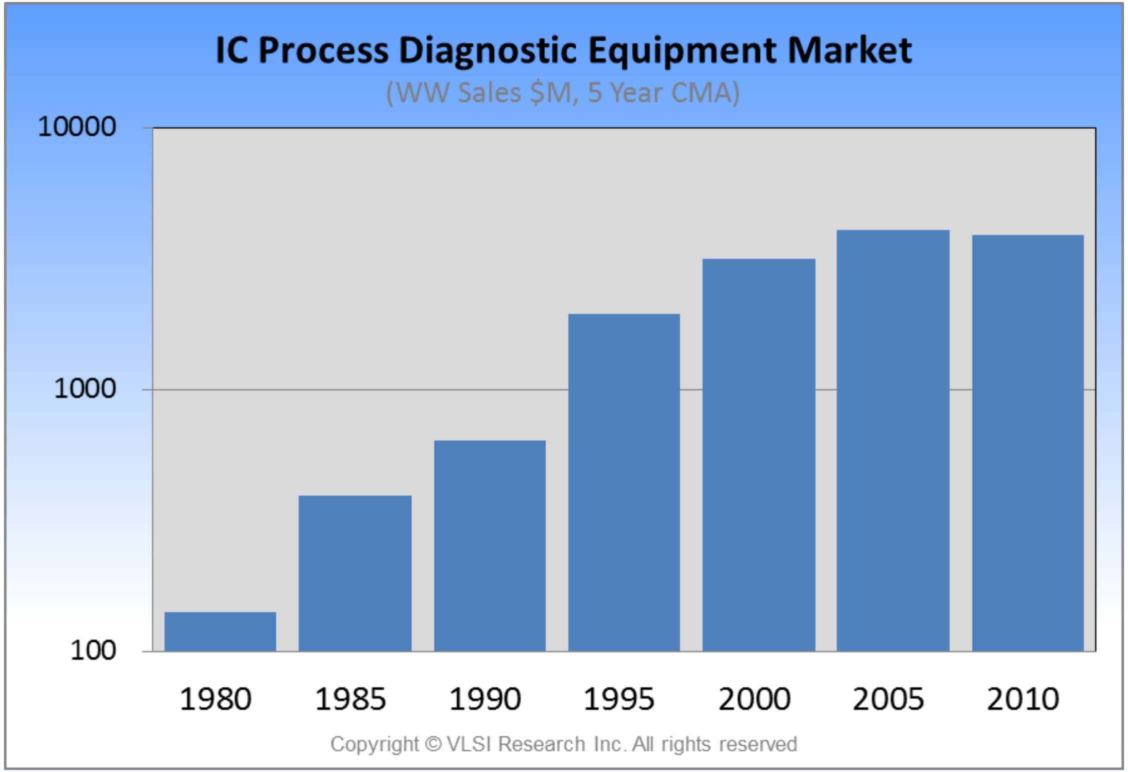
amazon

Google

Available on iTunes

The 2000’s: the Lost Decade

- Focus shifted to M&A
- Rationalization to control cost



The Leading Edge Issues: 2010’s

Microchips become Nanochips

The first mass-produced nanotechnology

We flirt with 450mm

CDU, LER, Overlay Control are the biggest contributors to profitability

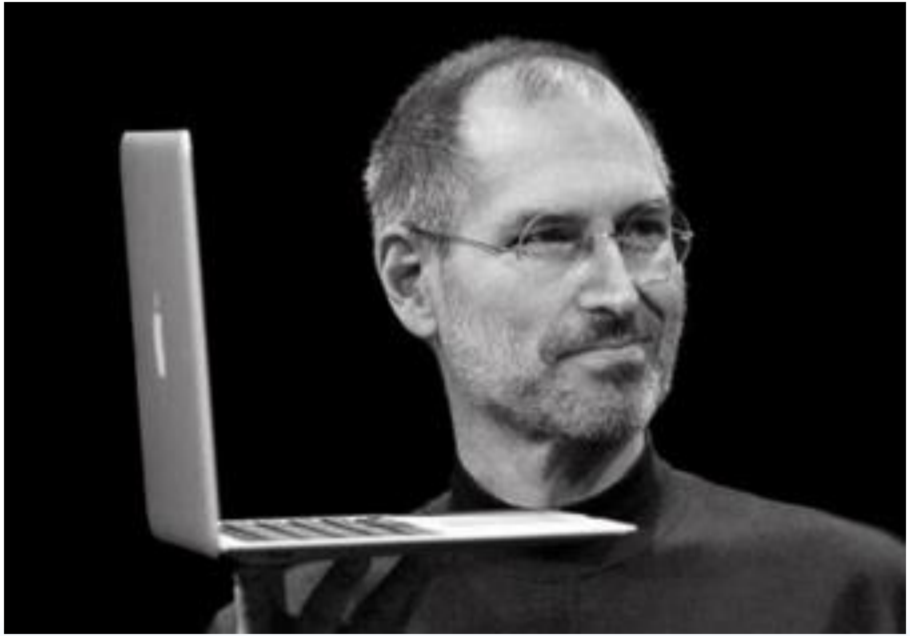
New materials and devices

3D emerges everywhere

Yields are expected

Fast ramps and time-to-market

The Leading Edge: ~2010



History of Inspection

Value

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2010's

HKMG & finFET

Deep Learning 1st applied

Fab costs >$15B by EoD

3D goes in-line

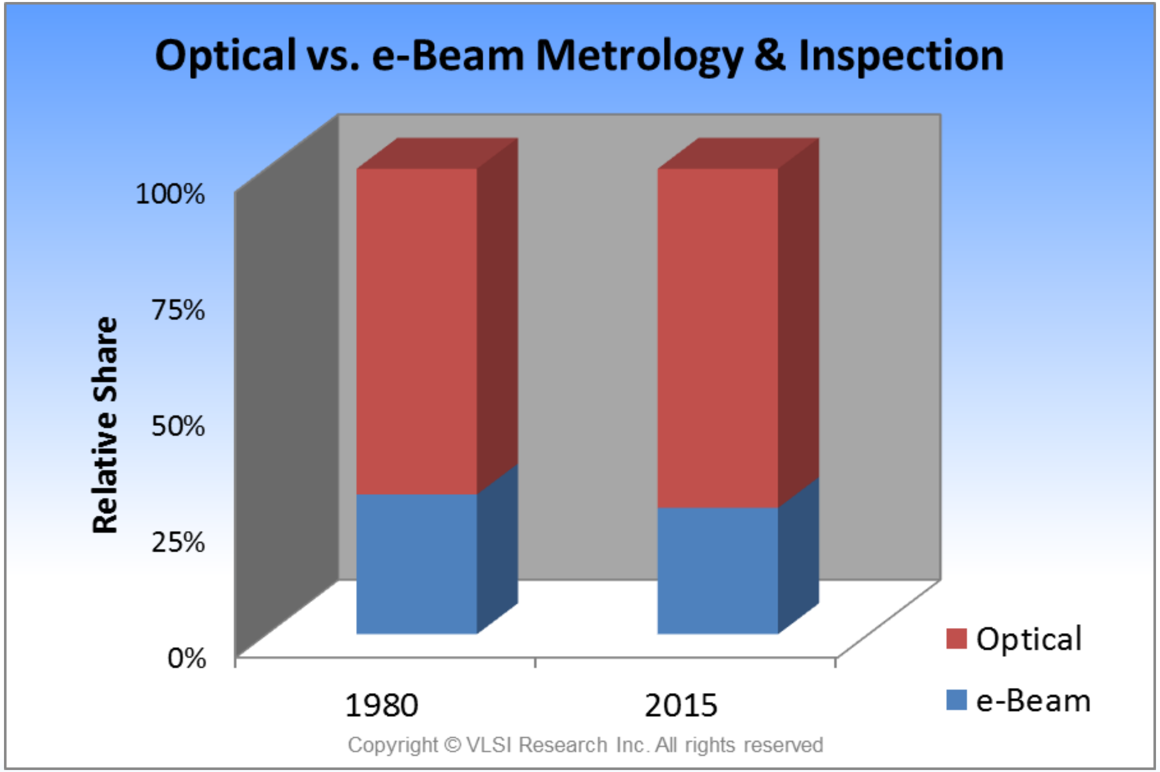
Beyond

The Leading Edge: Today

Metrology Technologies are Complementary

Proof: Share of optical relative to e-beam is slightly higher than it was 35 years ago

Both core technologies have not lost their usefulness. They have enhanced it with many new applications



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Why Complementary Metrology Technologies are **Triaged** in the Fab

E-beam	Brightfield	Darkfield
Low	Affordability	High
High	Resolving Power	Low
Low	Coverage	High
Low	Throughput	High

Every nanometer matters in 3D patterning

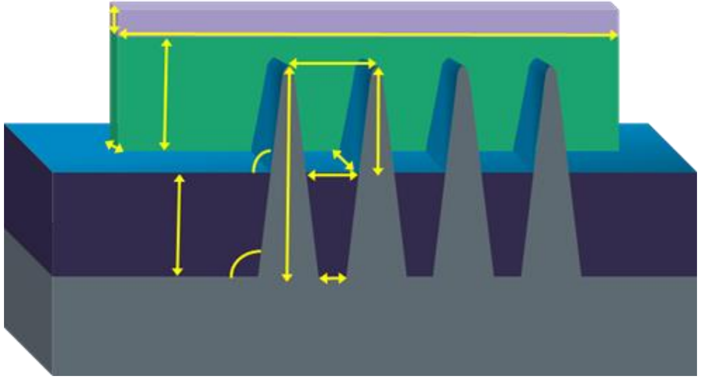
You can't fix what you can't find

You can't control what you can't measure

Source: KLA-Tencor

Smaller Process Window

Metrology / Performance

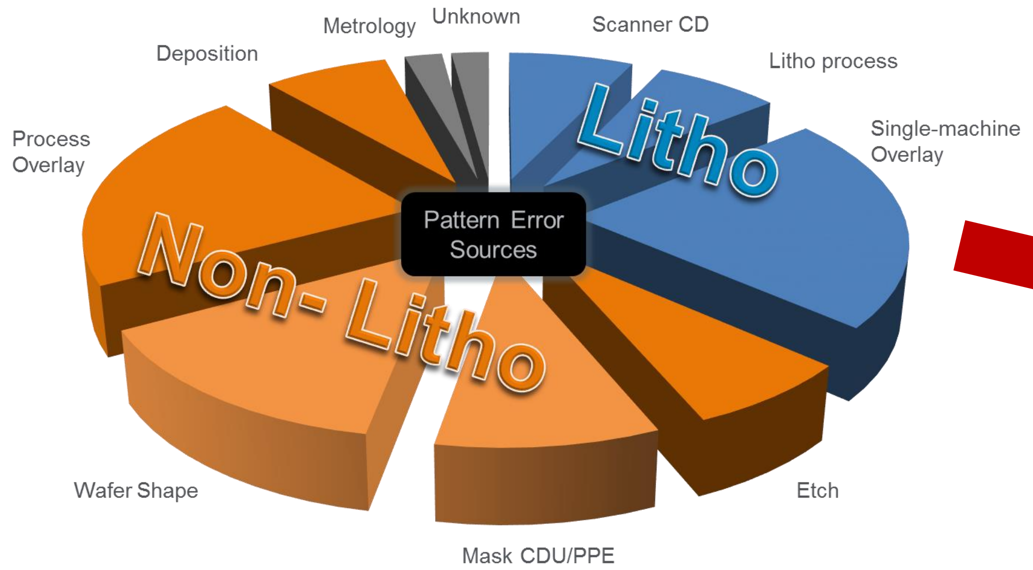


FinFET key parametric measurements

Metrology provides comprehensive data to decipher pattern issues

Non-Litho Errors Dominate Patterning

Emergence of Non-Litho Errors leads to more complex patterning control

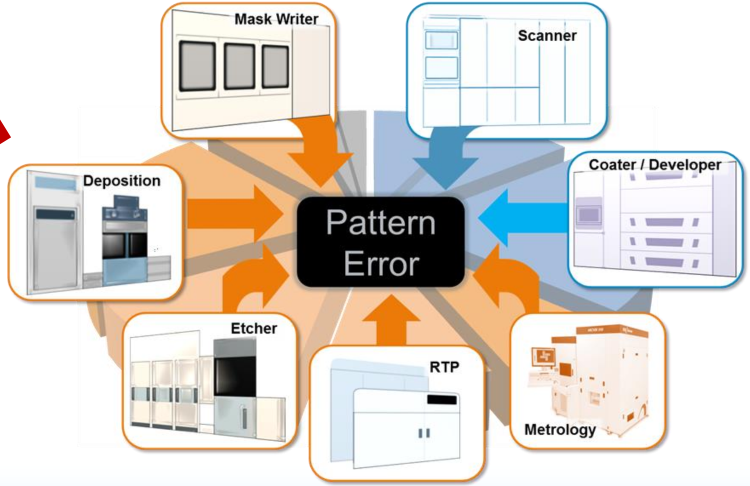


LELE CDU/Overlay budget example

Source: KLA-Tencor

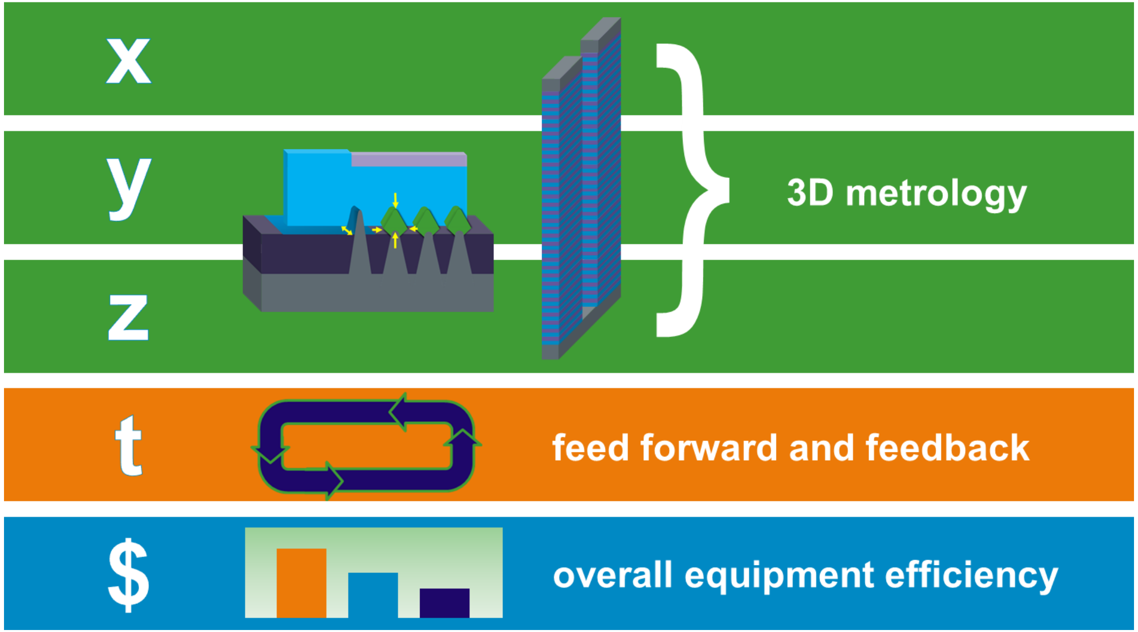
CDU = Critical Dimension Uniformity
PPE = Pattern Placement Error

Process control inside and outside the litho cell is critical for meeting patterning requirements



Dimensions of Process Control

- **x, y & z**
- **Feed-forward** in addition to Feedback
  - Optimized algorithms
  - Ability to correct process backward and forward



Source: KLA-Tencor's 5D™ Patterning Control

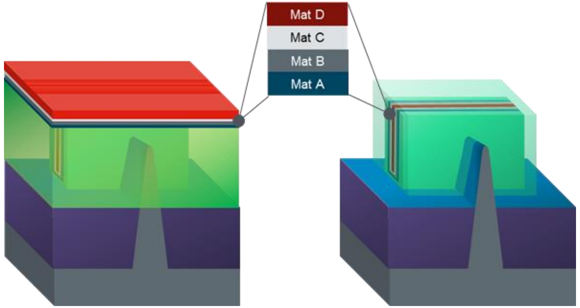
SpectraFilm Capabilities

supports a diverse range of film applications

- **BBSE**
  - **Broadband Spectroscopic Ellipsometer**
- **SWE**
  - **Single Wavelength Ellipsometer**
- **IRSE**
  - **Infrared Spectroscopic Ellipsometer**

Source: KLA-Tencor

Targeted Applications
Thin Multi-Layer Films NO, ONO, SiGe
Thick Single Layer Films Oxide, Photo Resist, α-Carbon
Thick Multi-Layer Films DARC/Oxide, OPO, ULK Stack
Extreme Multi-Layer Films 3D NAND

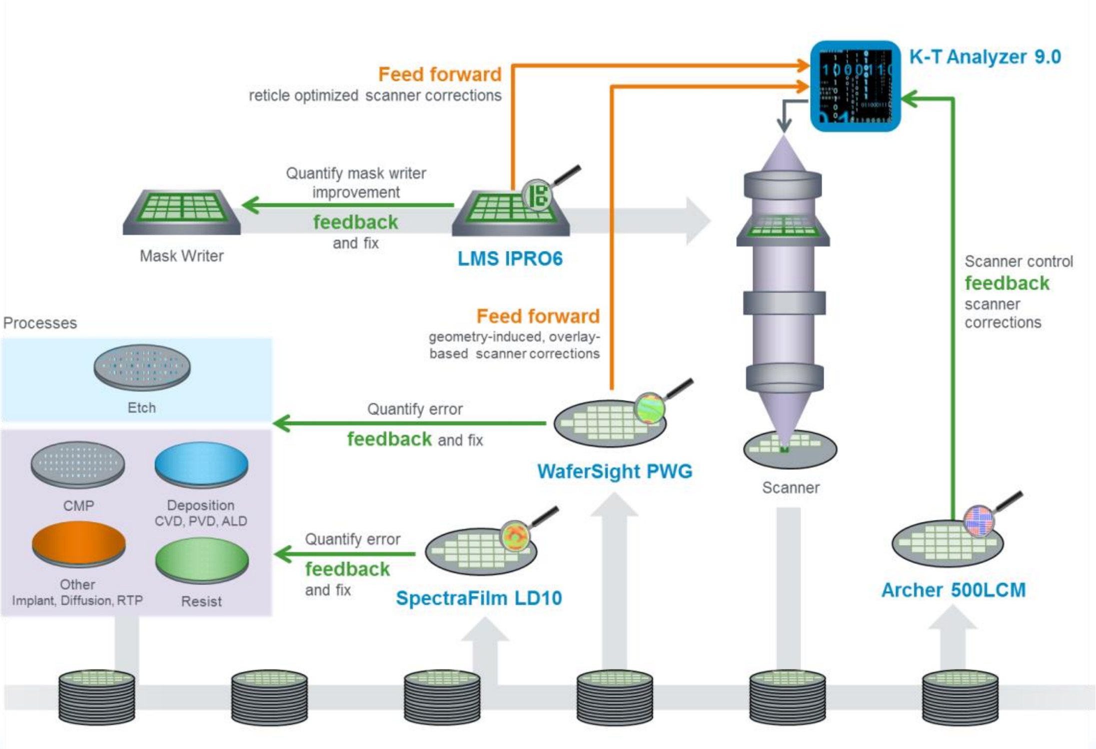


Fab-Wide Process Control

Metrology data drives feedback and feed forward control loops

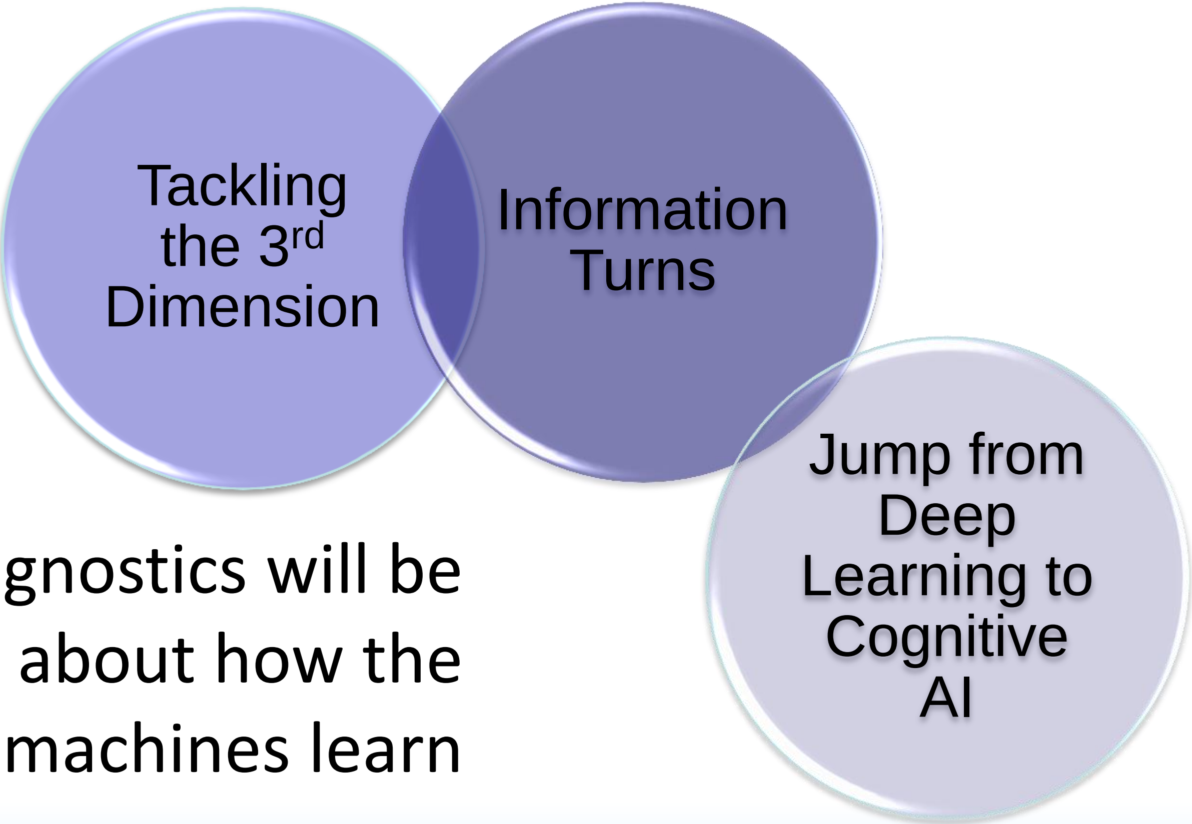
Address fab-wide sources of pattern variation

- Optimize processes that can affect patterning
- Augment information available for scanner corrections



Source: KLA-Tencor

Metrology Time Machine: 2020 & Beyond



Tackling the 3rd Dimension

Information Turns

Jump from Deep Learning to Cognitive AI

Process diagnostics will be much more about how the machines learn

History of Inspection

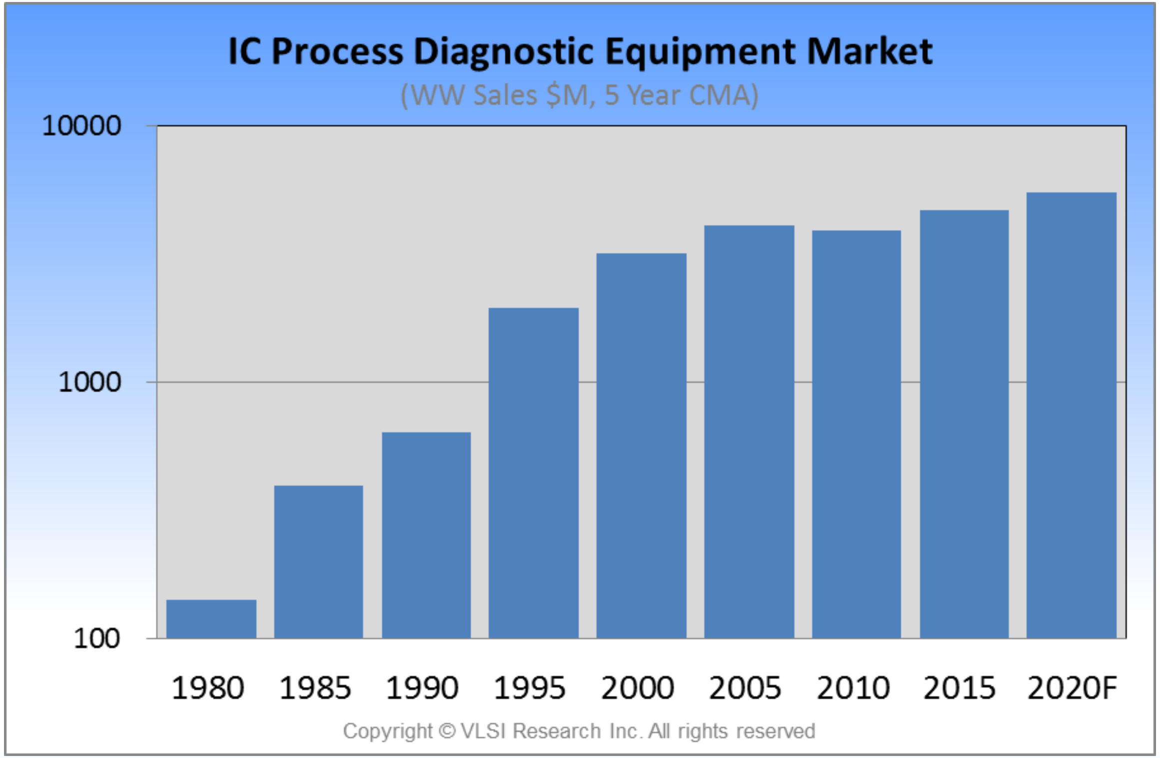
Value

1980’s	1990’s	2000’s	2010’s	Beyond
Defect focus is on coarse particles 1-100 Microns Automated Material Handling	Emergence of Yield Management Defect focus on tools Machines replace Humans	Yield Excursions drop to hours Fab costs rise from $1B to $5B by EoD 3D enters the fab with AFMs	HKMG & finFET Deep Learning 1st applied Fab costs >$15B by EoD 3D goes in-line	Yield Excursions drop to minutes New parameters used (stress), 3D to see deep in film stack **More Innovation Needed**

Growth has come back

While it won't be the go-go era before 2000, it will still be solid growth

As long as we continue to deliver on new technology



The Leading Edge: Tomorrow

amazon

Microsoft

Google

facebook

IBM

Oculus VR™

And???

Metrology Time Machine: What’s After Tomorrow?

Cognitive Computing

- The wave after IoT/Cloud
- Watson is 5 years old
  - Won Jeopardy in 2001
  - Now it’s working with Doctors to solve cancer
  - It is a decision making tool
    - ***Not a replacement for decision makers***

Watson knows what …

you don't know,

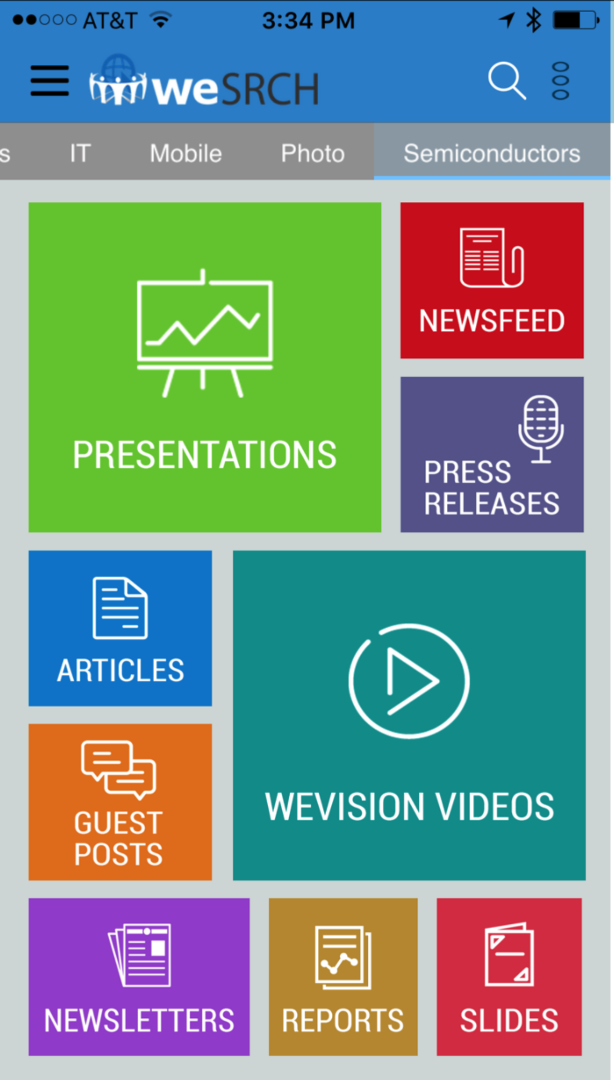
what you forgot,

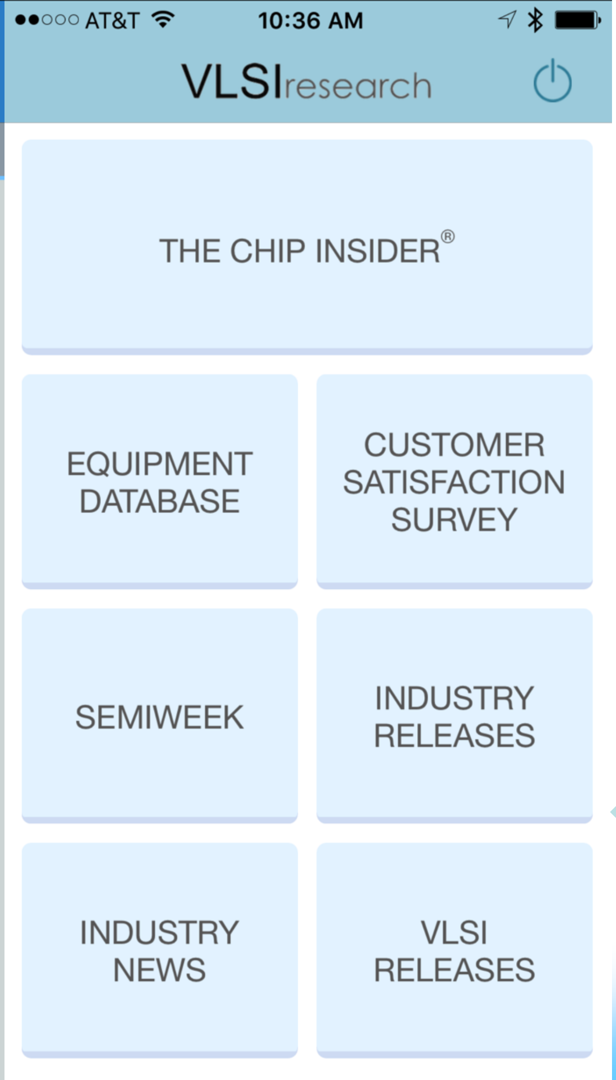
or forgot that you forgot.

Cognitive and Process Diagnostics

- AI as the Next Big Thing. It's that and more
  - The reason is similar to our history of NBTs
- Cognitive is going to require completely new types of device structures and architectures.
  - More compute performance that uses less power
  - That is the inalienable truth of the history of silicon.
  - That means better ways to move that data between memory and processor

- Cognitive will be as disruptive as what's come before,
  - Smart is not good enough, Smart is the new dumb
    - Things have to think ahead
    - They have to anticipate
    - They have to decide and act
    - ***And that's the future of silicon***
- ***The question is …***
  - ***What to do in the cognitive fab?***
    - ***Metrology on steroids with FF & FB***
    - ***How to apply the new technology?***
    - ***IoT + Big Data + Cloud + …***





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- Virtual history museum
- Based on industry donations

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- Where Technology = Opportunity
- A virtual science & engineering conference
- Ads reach > 1M visitors per month
  - 15-20 mins/visit, >1 visit/week
  - High signature authority and income viewership
  - High Yield on Targets for your business

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