Beyond-CMOS for Computing: Prospects and Best Bets

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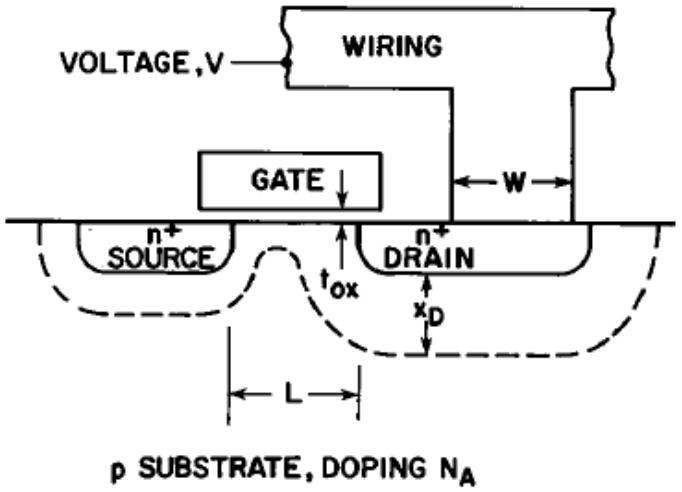
Exploring Revolutionary: Energy Efficient Devices for Computing

Exploring Revolutionary: Energy Efficient Quantum Nano-Electronic & Quantum Nano-Magnetic Devices for Computing

Traditional Dennard MOSFET Scaling

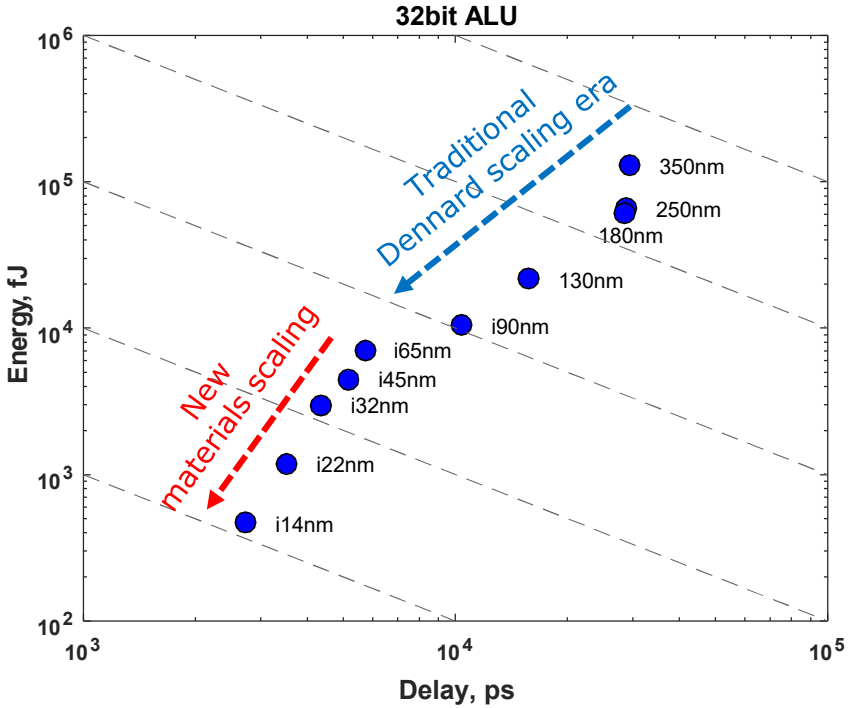
Device or Circuit Parameter	**Scaling Factor**
Device dimension *tox, L, W*	= 1/κ
Doping concentration *Na*	= κ
Voltage *V*	= 1/κ
Current *I*	= 1/κ
Capacitance *εA/t*	= 1/κ
Delay time/circuit *VC/I*	= 1/κ
Power dissipation/circuit *VI*	= $1/\kappa^2$
Power density *VI/A*	**= 1**

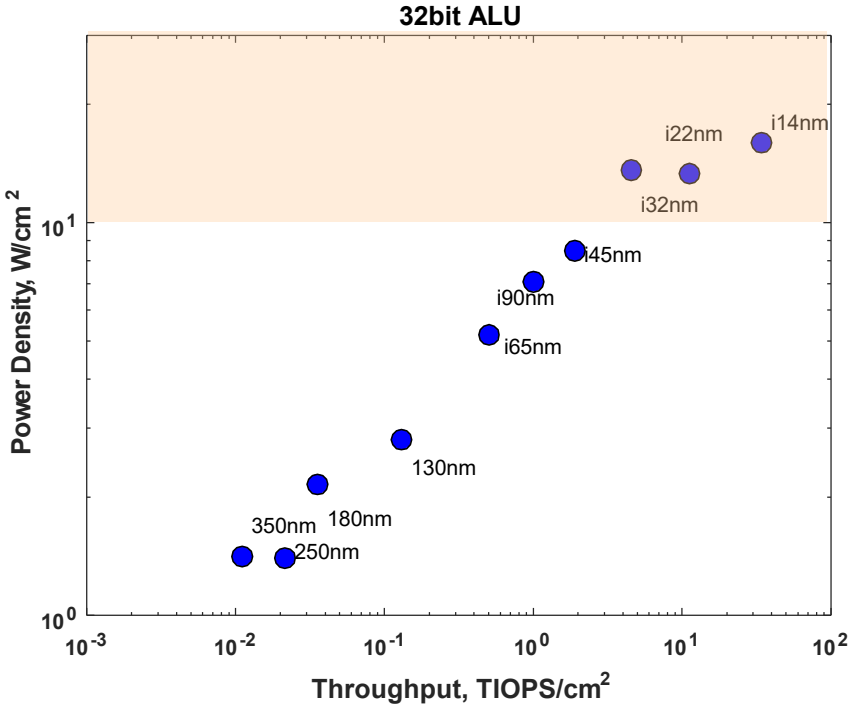


R. Dennard, IEEE JSSC, 1974

Traditional MOSFET scaling served our industry well for ~30 years and ended in 2003

CMOS Challenge With Energy*

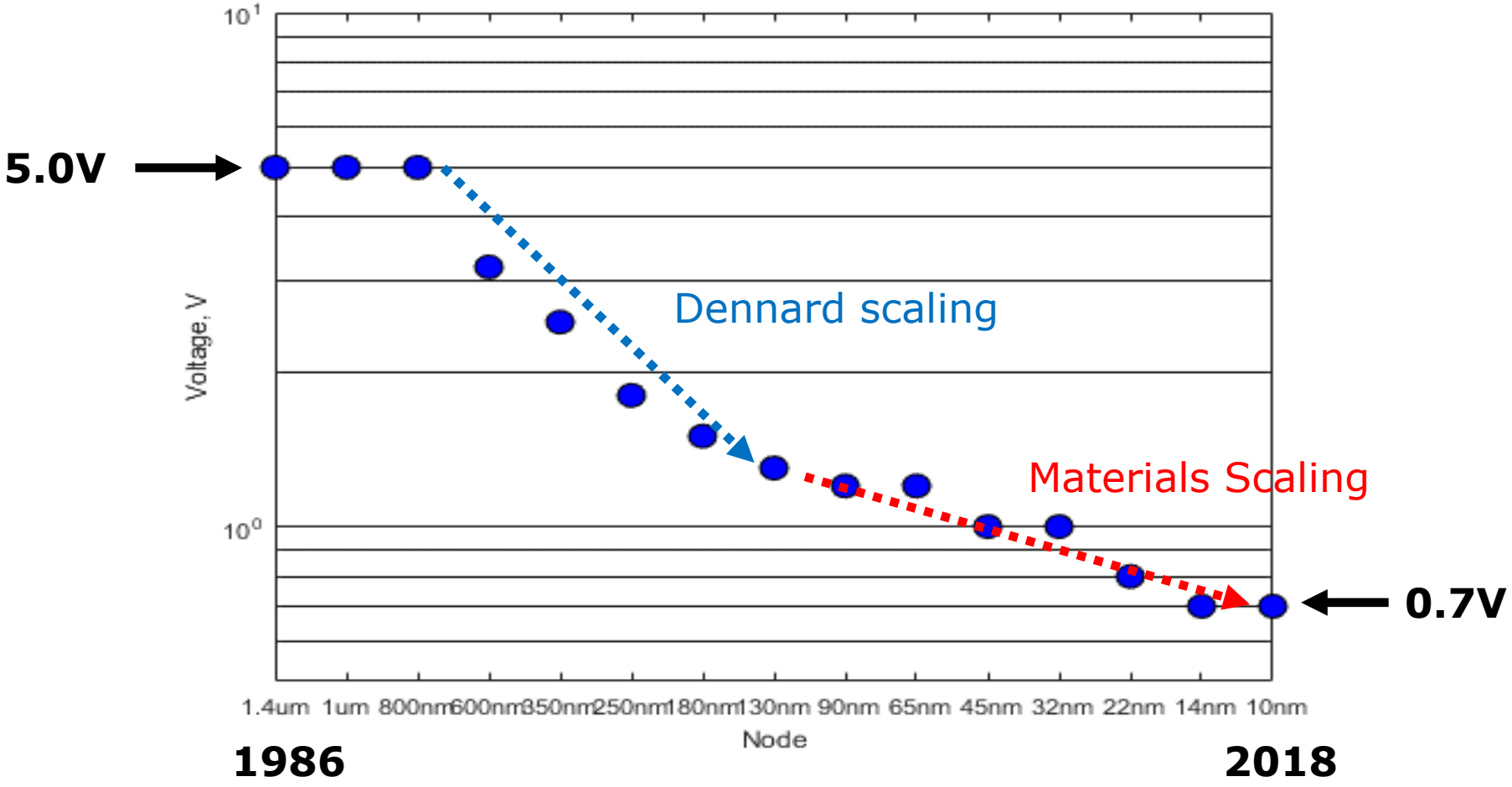




- **As CMOS scales -> energy decreases.**
- **But not fast enough.**
- **Power density approaches a constraint e.g. 10W/cm²**

* Source Intel. Projections based on best device data in papers published by Intel at IEDM in 1994 to 2014. Nikonov, Young Benchmarking Method.

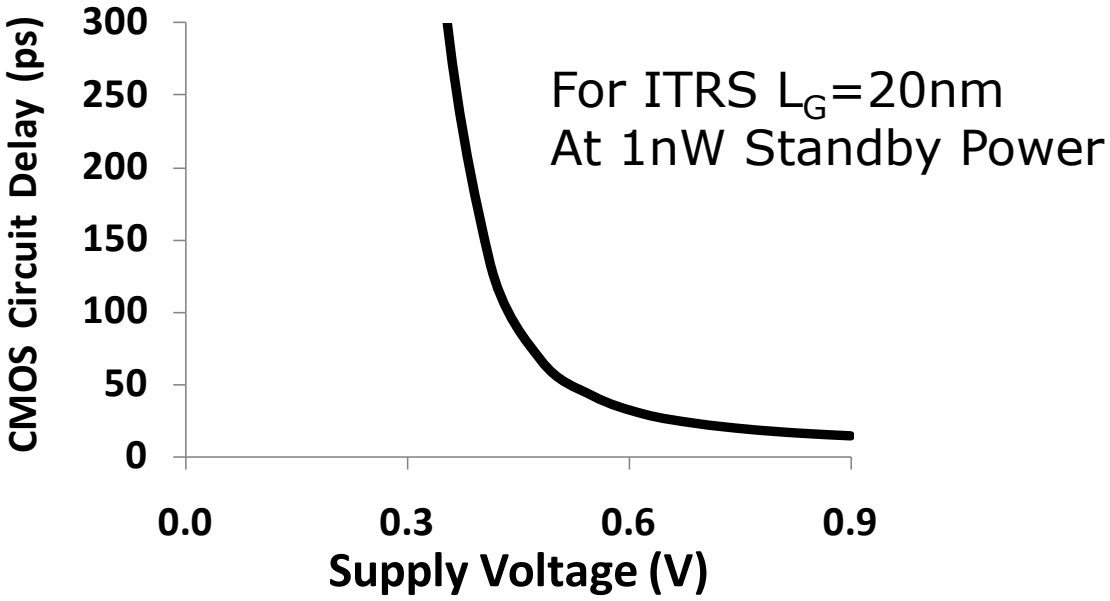
CMOS Supply Voltage - Historical Trend



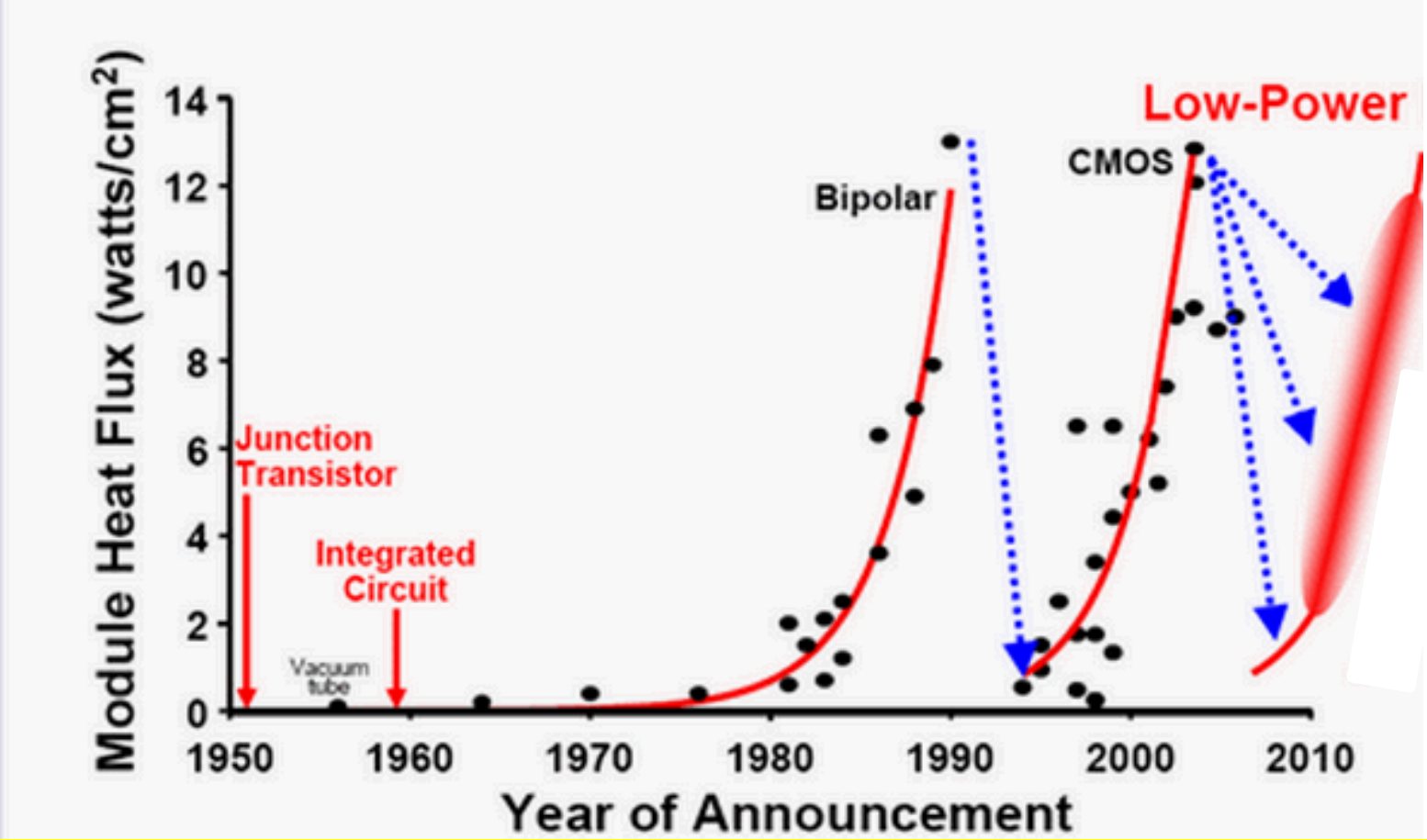
Why are we looking beyond CMOS?

Computation Efficiency needs maximum performance at lowest supply (V_{dd})

- Switching Energy α CV_{dd}^2
- At $V_{dd} \leq V_{th}$, performance suffers significantly
- Lowest V_{th} is limited by leakage
- Computation efficiency of CMOS limited by 60 mV/dec I_d/V_{gs} sub-threshold Slope



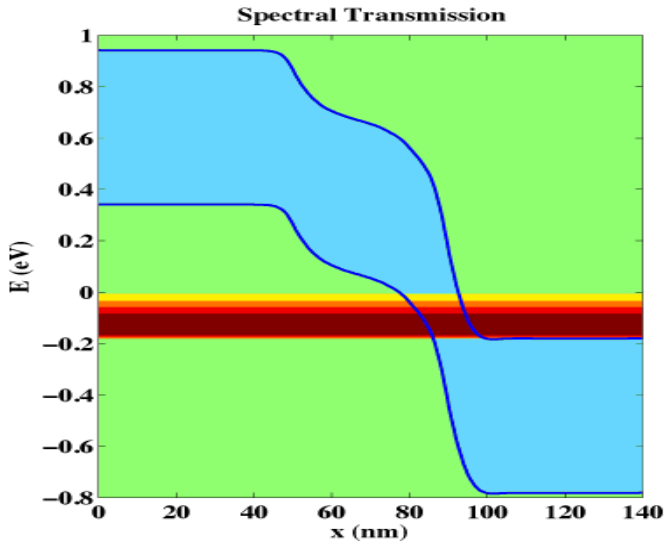
CMOS Challenge With Energy



Semiconductor industry faced this situation before with bipolar transistors.

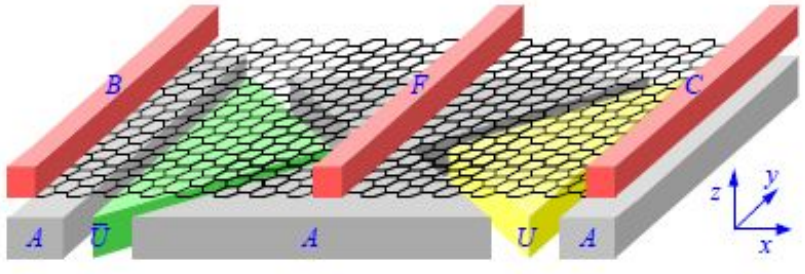
Source: Chen (IBM), ISS Europe, 2007.

Beyond CMOS Devices - Electronic*

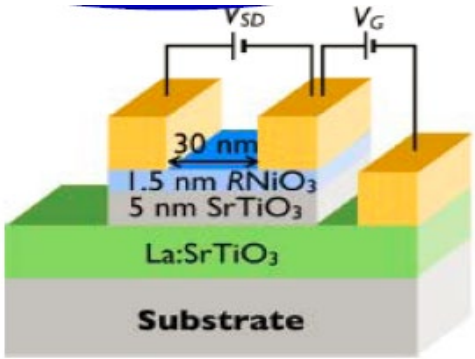


Tunneling FET

III-V TFET (IIIV TFET)
Heterojunction TFET (HJ TFET)
Graphene Nanoribbon TFET (Gnr TFET)



Graphene pn Junction (GpnJ)

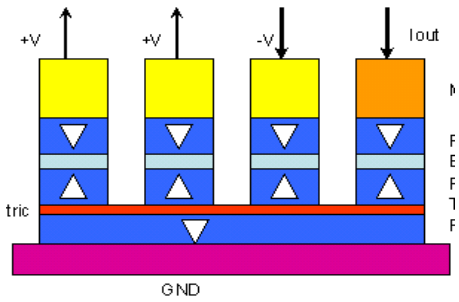


Metal-Insulation Transition FET (MIT-FET)

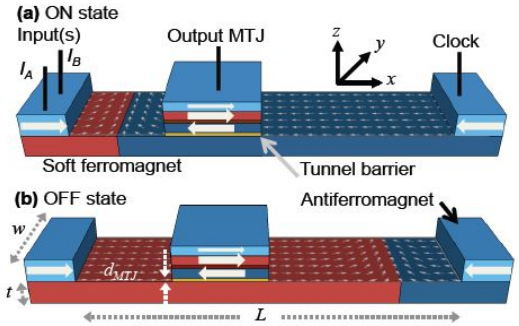
D. Nikonov and I. Young, 2012 IEDM

* Includes Tunneling, Ferroelectric, Straintronic, Orbitronic Devices

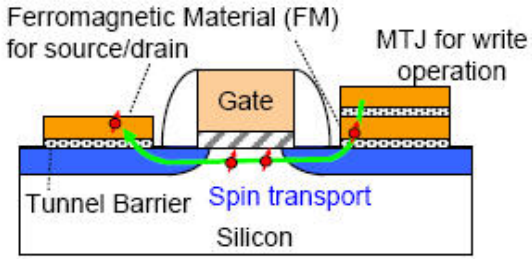
Beyond CMOS Devices - Spintronic



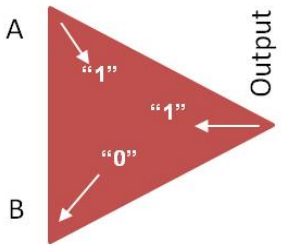
Spin Torque Majority Gate (STMG)



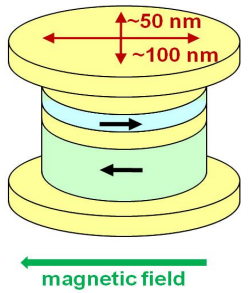
Spin Torque Domain Wall (STT/DW)



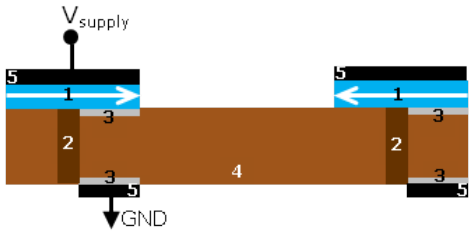
SpinFET



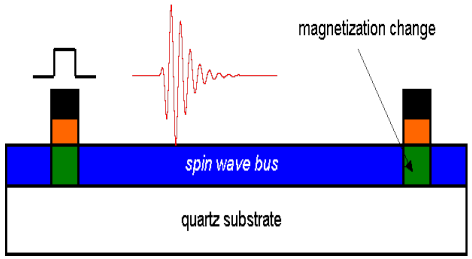
Spin Torque Triad (STTriad)



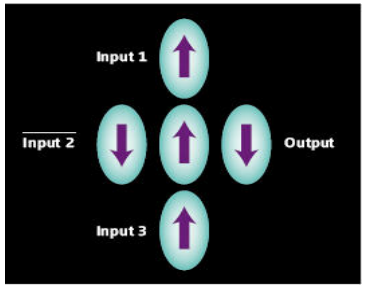
Spin Torque Oscillator (STO)



All Spin Logic (ASLD)



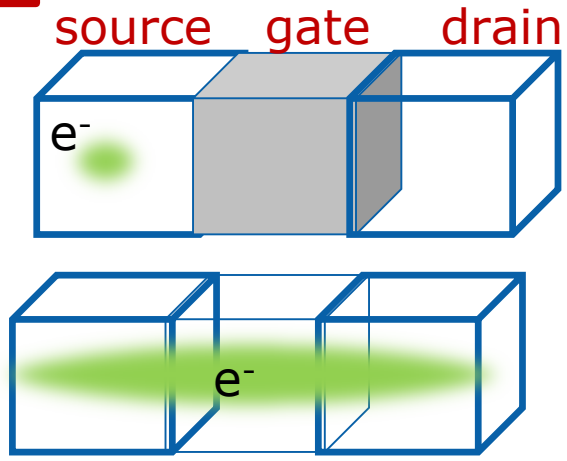
Spin Wave Device (SWD)

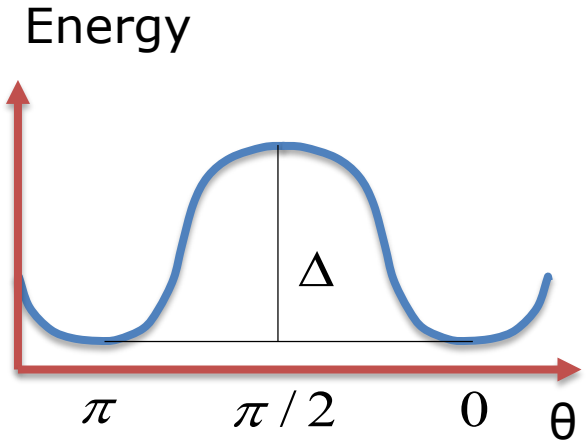


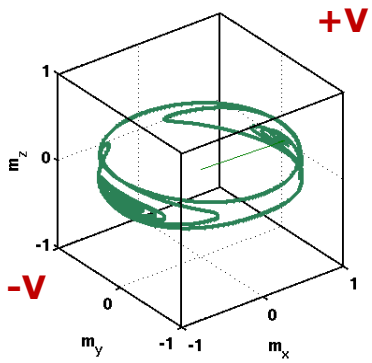
Nanomagnetic Logic (NML)

D. Nikonov and I. Young, 2012 IEDM

2 Collective States = Energy Efficiency







	Generic Electronic Switch	Generic Spintronic Switch
Barrier	20 kT (from Ion/Ioff)	60 kT (non-volatile)
Voltage	0.5 – 1 V	10-100 mV
Particles	Ne = 200 electrons	Ns = 10000 spins
Sw. Energy Limit	4000kT = Ne*20kT	60 kT
Phenomenon	Non collective	Collective

$$E = e\Delta VN \sim 4000kT \quad (1)$$

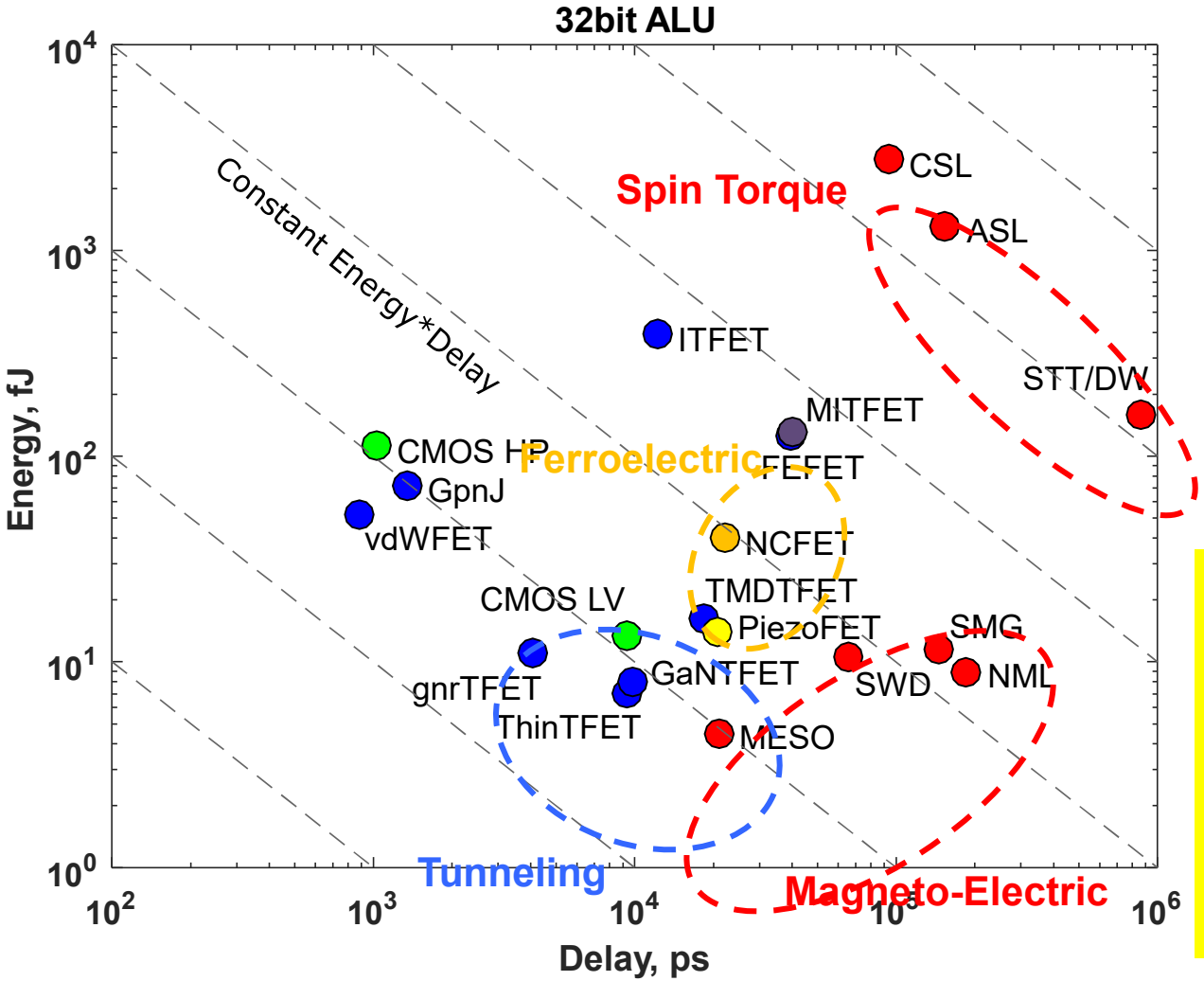
Leakage determined by barrier

$$I_{on}/I_{off} < \exp(\frac{e\Delta V}{kT}) \quad (3)$$

$$E = \frac{1}{2}\mu_0\mu_B N_s H_k \sim 60kT \quad (2)$$

Leakage not related to barrier

4 Lower Voltage = Best Path for Low Energy



CMOS Ref

Electronic

Spintronic

Ferroelectric

Orbitronic

Straintronic

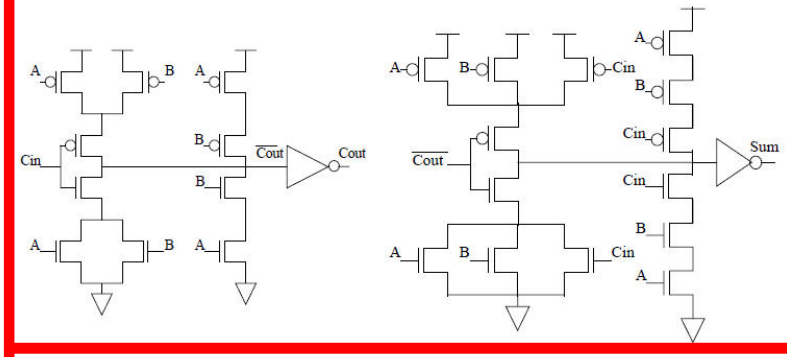
Tunnel FETs:
Lower E*D than CMOS.

Magnetoelectric Spintronics:
Slower,
but lower energy; and
Non-Volatile.

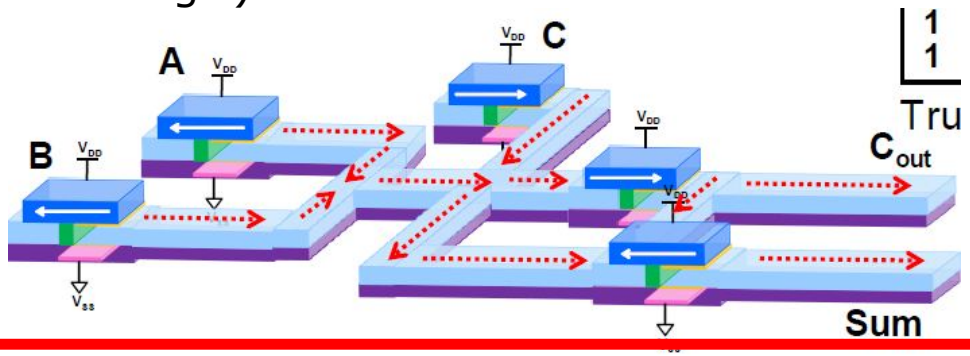
Ref: DE Nikonov, IA Young - IEEE Journal on Exploratory Solid-State Computational Devices & Circuits, vol. 1, 2015

6 Majority Gates = More Efficient Compute

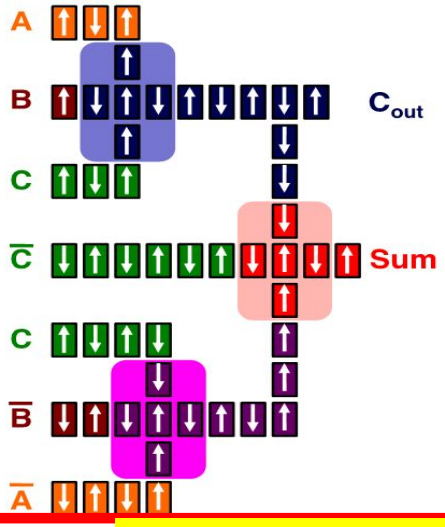
Adder = 28 transistors (at least)



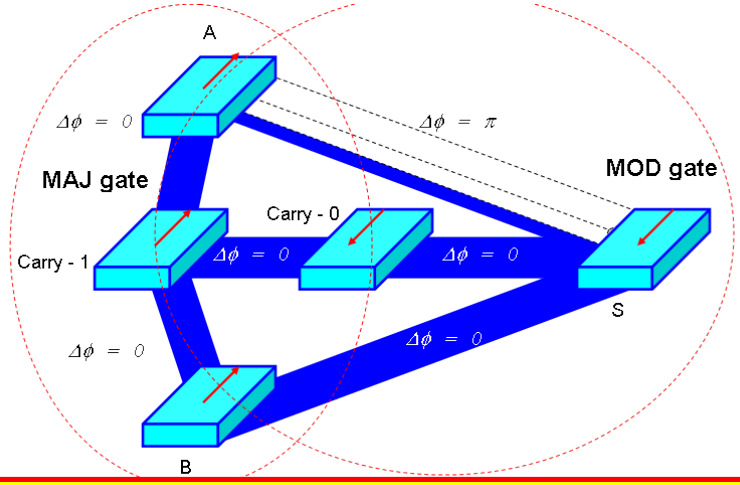
… or just 2 majority gates (All Spin Logic)



… or just 3 majority gates (Nanomagnetic Logic)

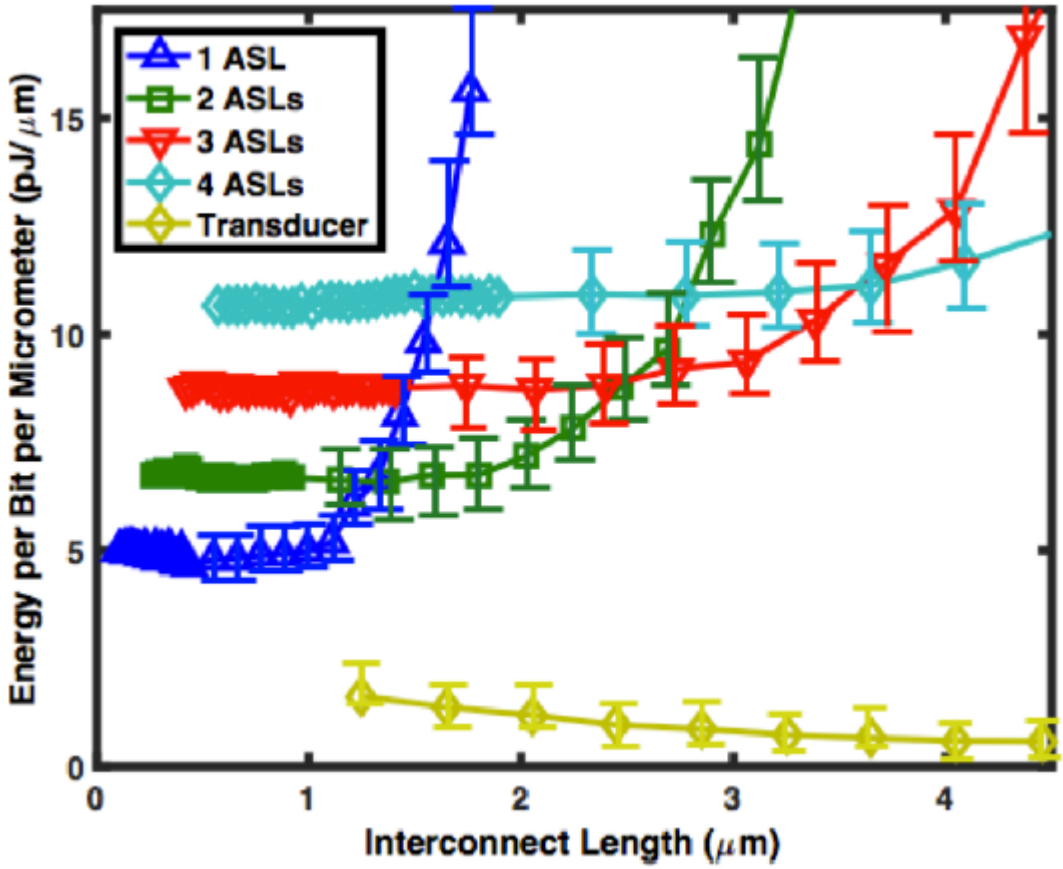


… or just 1 majority gate (Spin Wave Devices) !



Fewer devices for same computing function

7 Electrical Interconnects for Long Spans

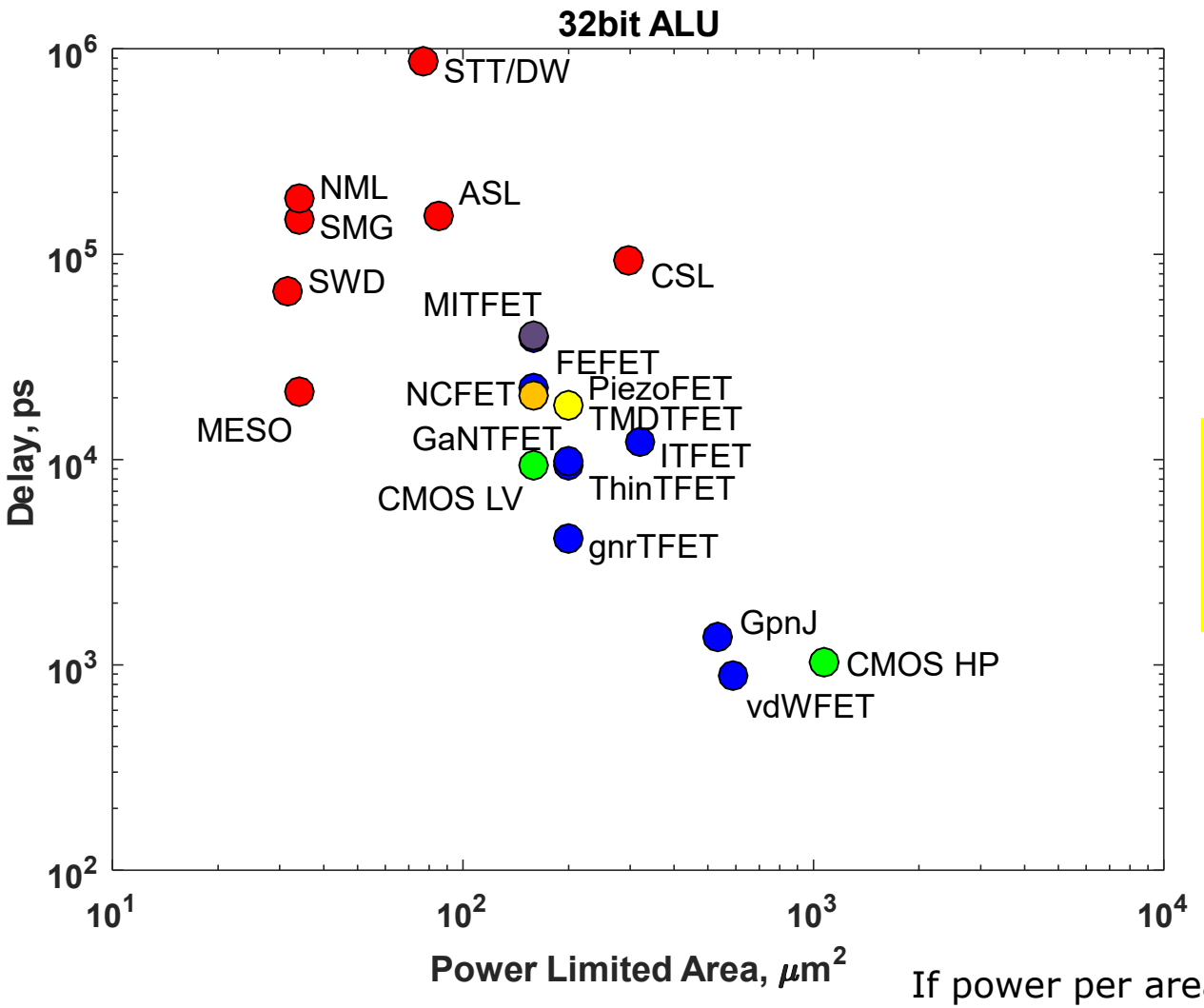


Spin interconnect: Energy/bit using All-Spin Logic (ASL) for Repeaters

"Spin interconnects" are limited by much higher attenuation with length, compared to "electrical interconnects".

Ref: R. M. Iraei et al., IEEE Journal on Exploratory Solid-State Computational Devices & Circuits, vol. 1, 2017.

Delay vs. Area



CMOS Ref

Electronic

Spintronic

Ferroelectric

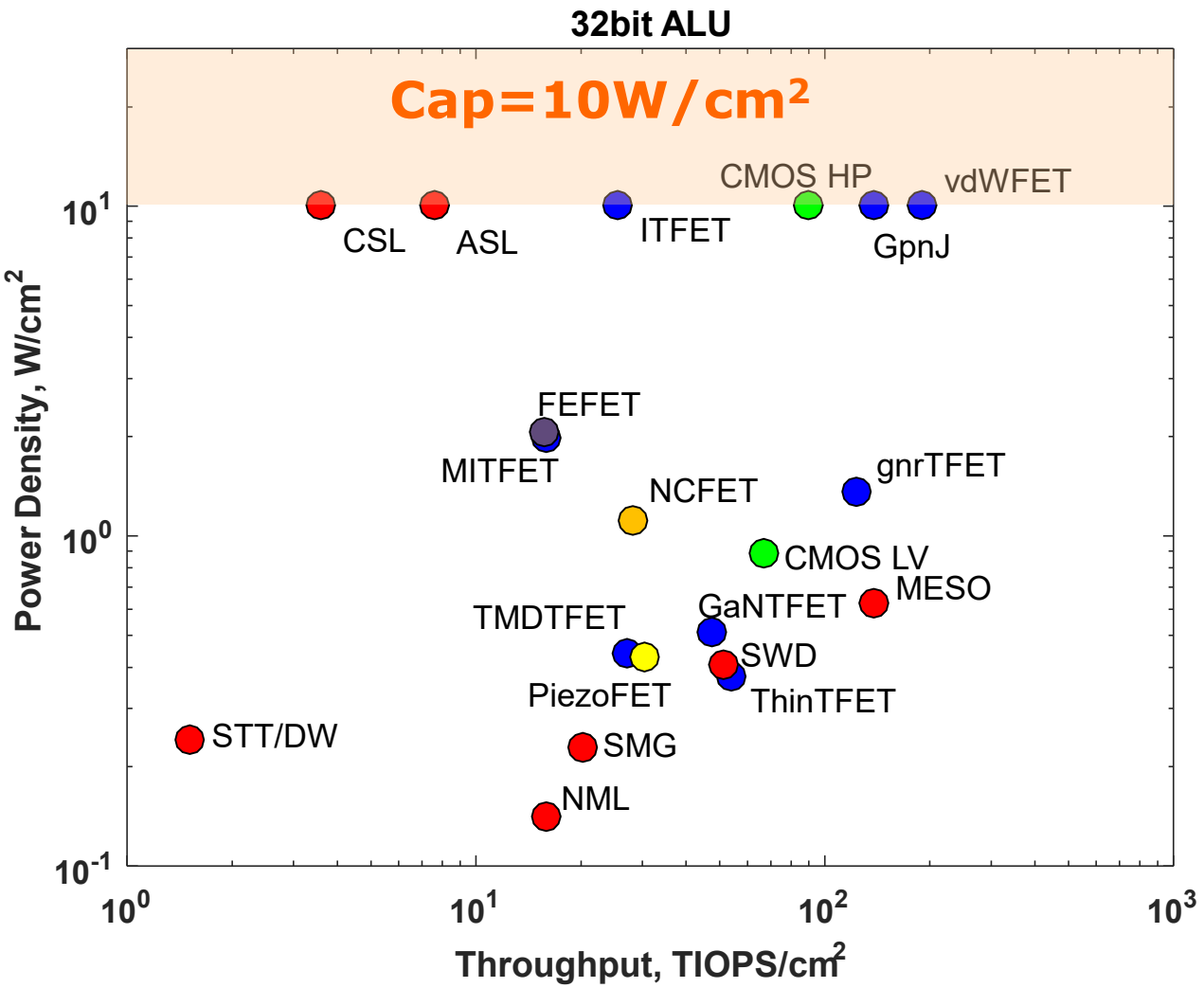
Orbitronic

Straintronic

Spintronics is slower than electronics, but more compact

If power per area exceed the cap (10W/cm^2), effective area is rescaled to be larger

Throughput vs. Capped Power



CMOS Ref

Electronic

Spintronic

Ferroelectric

Orbitronic

Straintronic

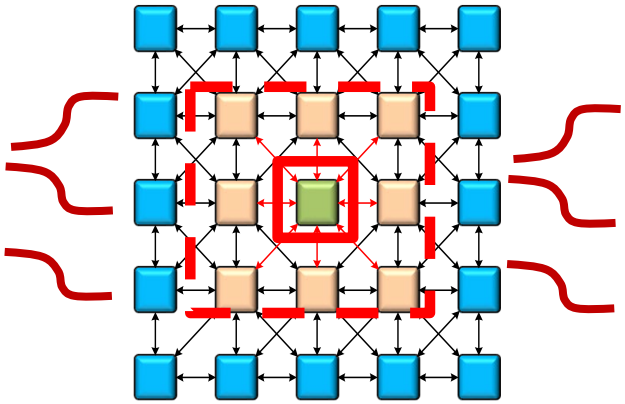
Tunnel FETs:
Rival CMOS in throughput at lower power.

Magneto-electric Spintronic:
Very low power.

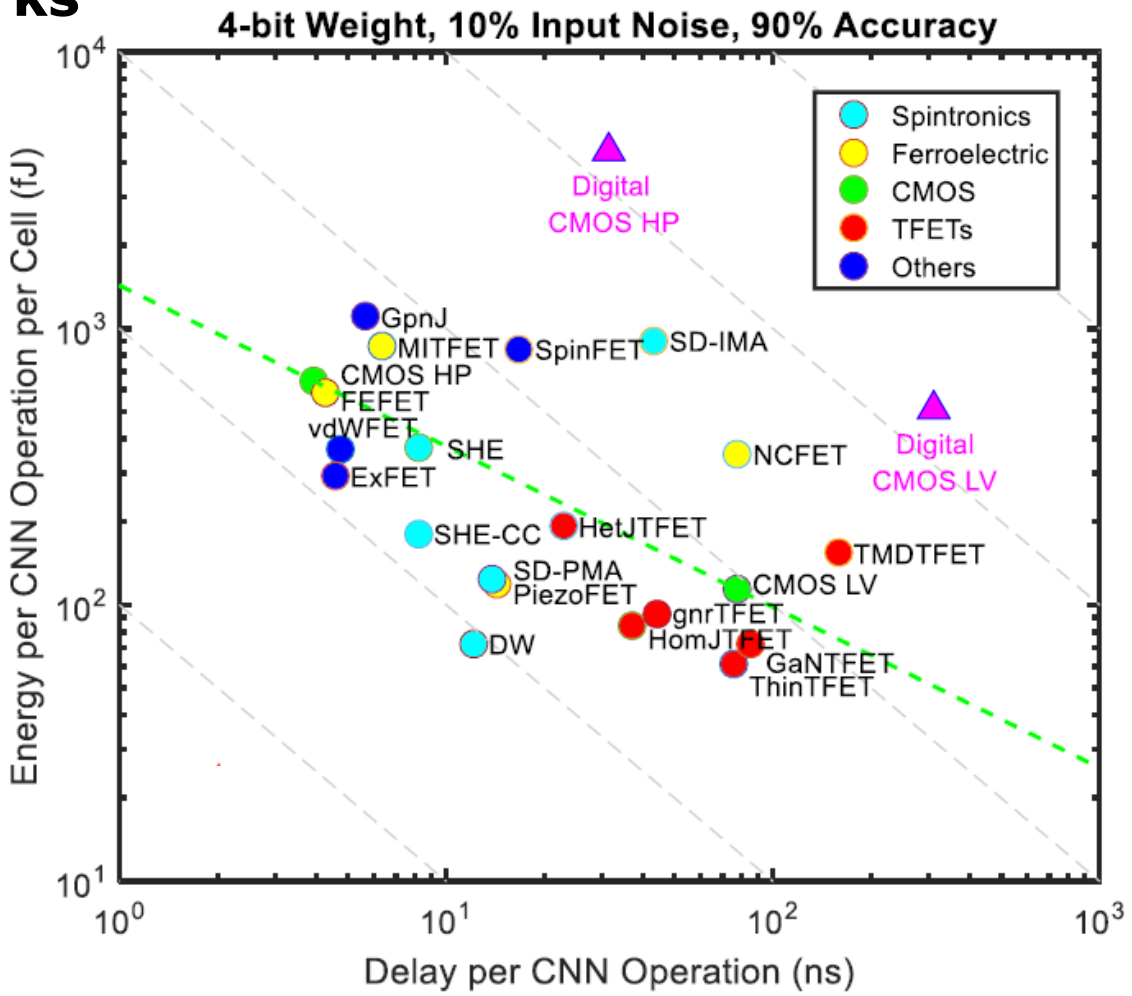
TIOPS = **T**era **I**nteger **O**perations **P**er **S**econd

9 Neuromorphic Efficient with Beyond-CMOS

Cellular Neural Networks

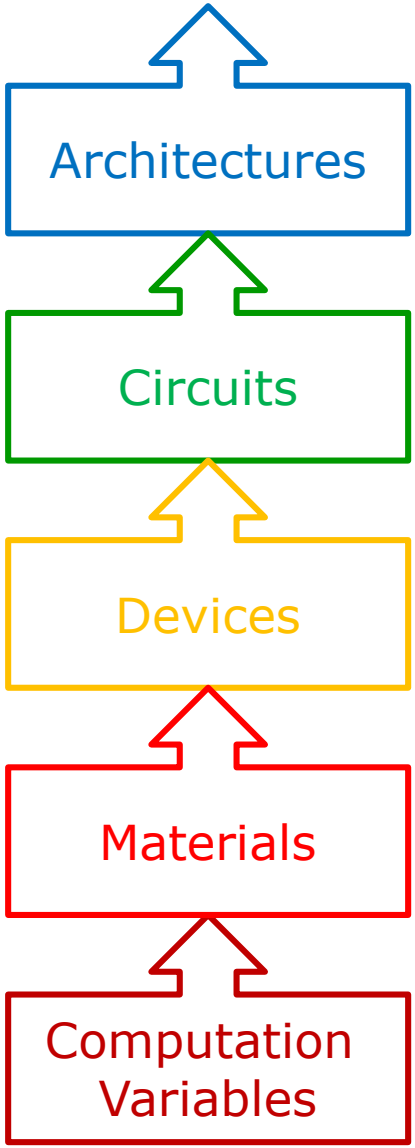


Spintronic Devices better than Electronic Devices !



Ref: C. Pan and A. Naeemi, IEEE JXCDC, 2016.

Principles to Beyond CMOS for Computing



9: Neuromorphic computing more efficient with beyond-CMOS circuits.

8: Convincing non-volatile computing paradigm;
general enough = valid for more than one architecture,
specific enough = no claims of essential aspects missed

7: Use electrical interconnects for longer propagation spans.

6: Majority gates = more efficient circuits, especially for more complex computation functions.

5: Start benchmarking with modeling of devices, build up from simple to more complicated circuits.

4: Low voltage devices = most direct way to low energy operation.

3: Choice for an optimal beyond-CMOS device = compatibility with an efficient and effective interconnect.

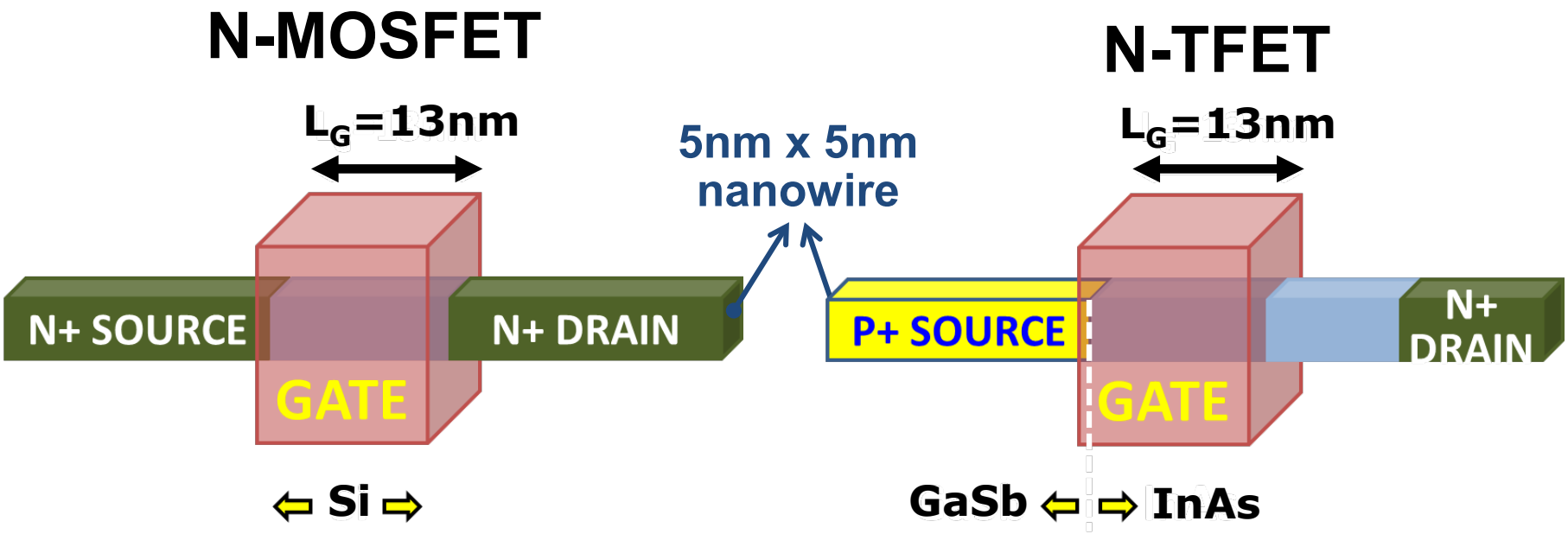
2: Some devices utilize collective states = advantages of non-volatility or more energy efficient operation.

1: Beyond-CMOS circuits require CMOS as an integral part. They will work alongside and augment CMOS computing blocks.

Tunneling FET (TFET) Geometry

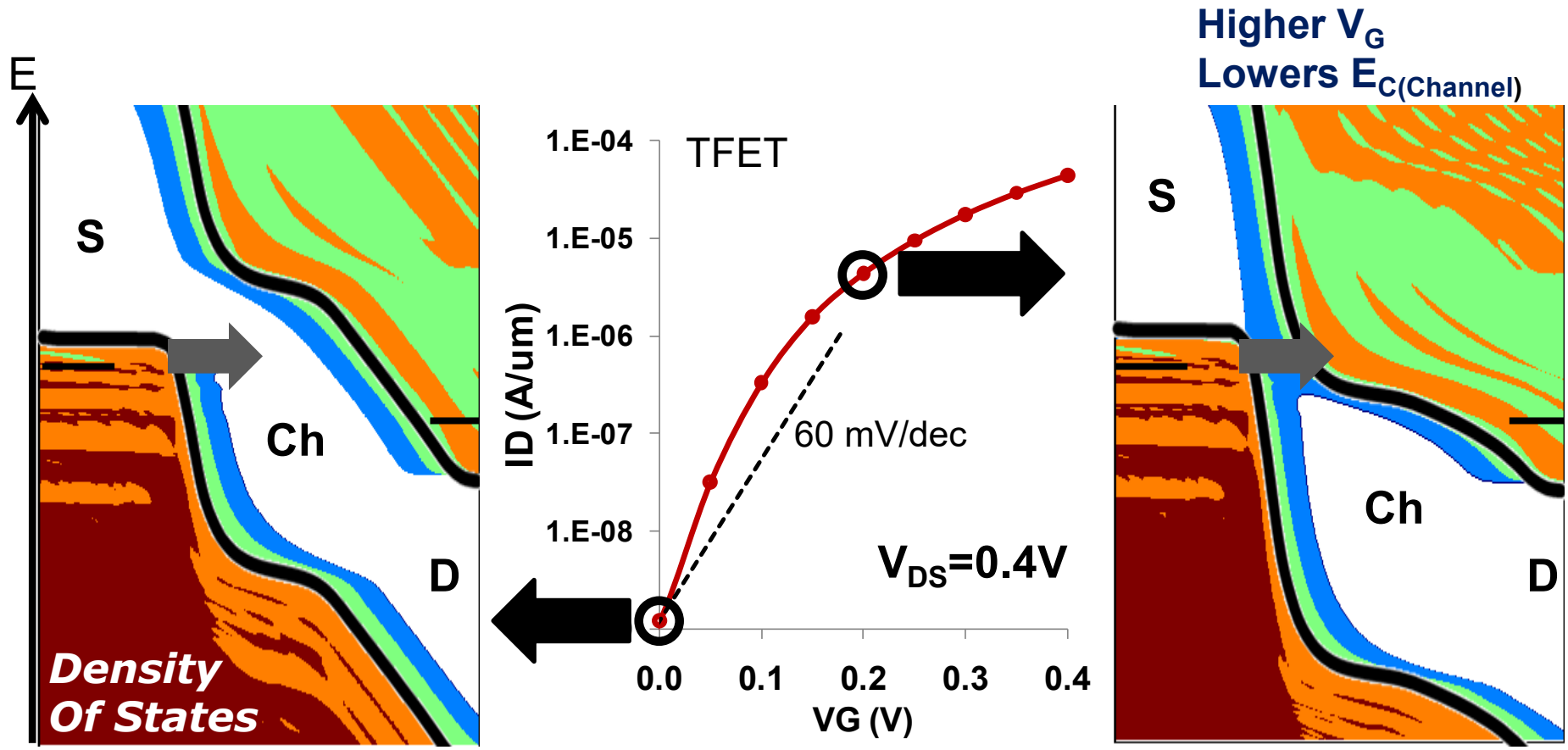
L_G = 13nm: ITRS 2018 MOSFET requirement

5nm-NW: TFET requirement *(Avci, IEDM 2013 4.3)*



TFET Sub-threshold Slope

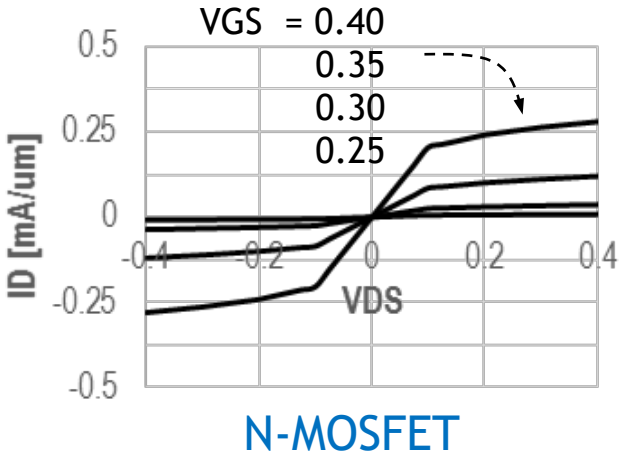
Tunneling probability increases sharply at the onset of Source Valance Band and Channel Conduction Band overlap



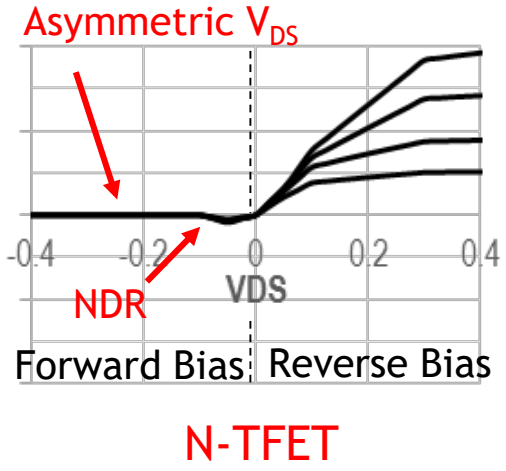
N-TFET compared N-MOSFET I_{DS} - V_{DS}

N-MOSFET conducts with Neg.-V_{DS}

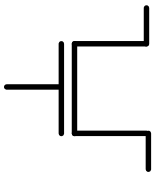
N-TFET has low conduction with Neg.-V_{DS}

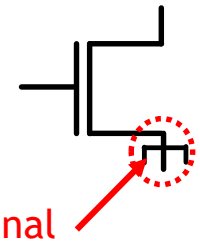


N-MOSFET

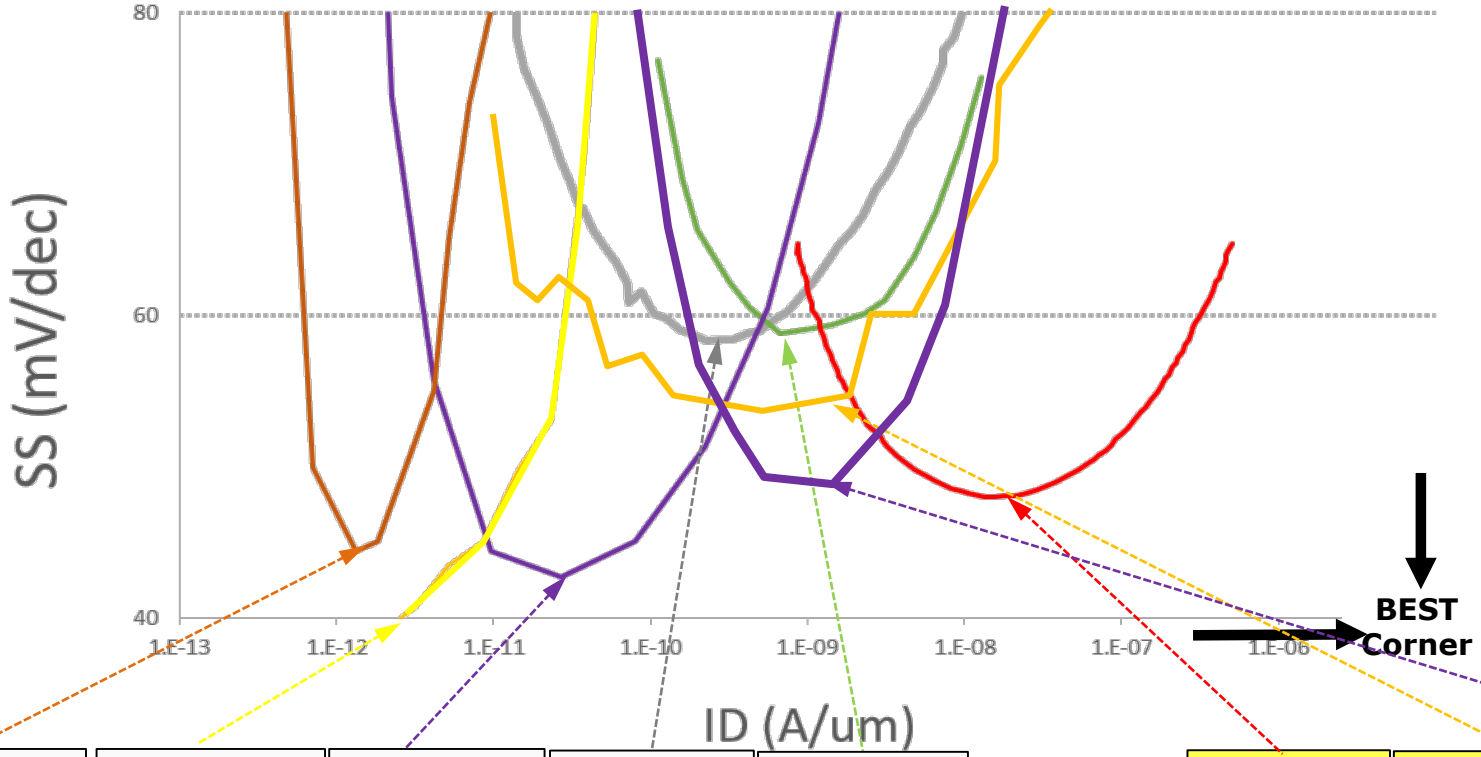


N-TFET





Steep-SS Experimental TFET Benchmark



2012 EDL
***48** mV/d*
InP-GaAs
85nm NW

UCSB
09-2015
Nature
***<10** mV/d*
Ge/Ox/MoS2
2nm MoS2

Hokkaido
9-2015
SSDM Conf.
***42** mV/d*
InGaAs/Si
50nm NW

U. Tokyo
01-2016
VLSI Symp
***57** mV/d*
InGaAs
Bulk SG

Intel
12-2011
IEDM
***59** mV/d*
InGaAs-InAs
>4um DG

Lund
12-2016
IEDM
***48** mV/d*
InGaAs-GaAsSb
20nm NW

MIT
07-2017
EDL
***53** mV/d*
InGaAs-InAs pocket
40nm NW

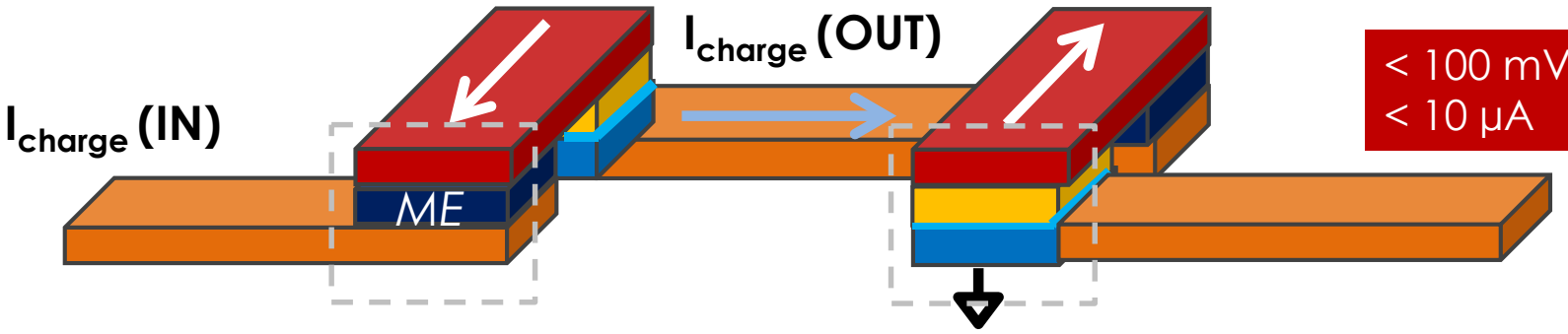
IMEC
06-2018
VLSI
***47** mV/d*
InGaAs-GaAsSb
30nm NW

MESO: Magneto-Electric – Spin Orbit Logic

Interconnect (charge) and Low Voltage (<100mV)

aJ switching.

< 100 mV
< 10 µA



Voltage Controlled Magnetization

Multiferroic – e.g. $BiFe0_3$

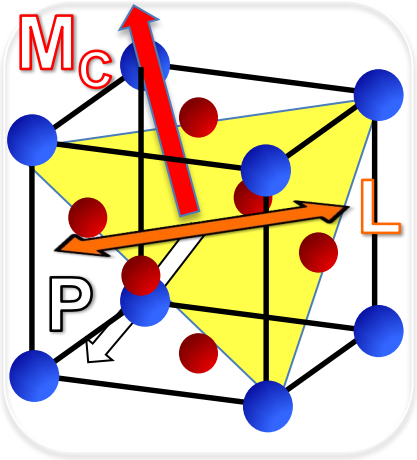
Magnetization to Voltage

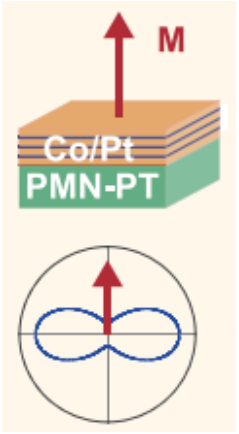
Inverse Spin Orbit – e.g. Ag/Bi, Bi_2Se_3

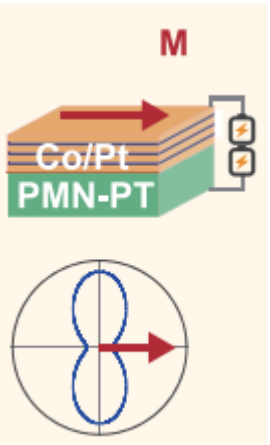
Magnet	20 X 32 nm
Δ (stability)	45 kT
Interconnect	12 X 45 nm
R_{ic}, C_{ic}	4.5 Ω, 4 aF
Energy per bit	(600 kT) 2.5 aJ

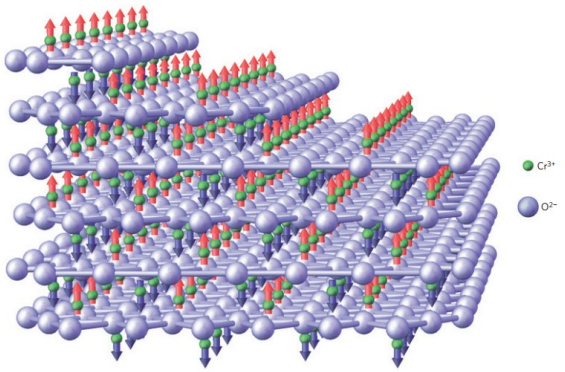
Ref: Manipatruni, S., Nikonov, D.E. and Young, I.A., 2015. arXiv:1512.05428.
Ref: Scalable energy-efficient magnetoelectric spin–orbit logic, Manipatruni, S., et al, Nature Dec. 3, (2018)

II: Electrical Control of Ferromagnet with Magneto-Electricity









Multiferroics	Magneto-Strictive	Chromia-class
$BiFeO_3$, $LaBiFeO_3$, $BiCeFeO_3$, $LuFeO_3$	Fe_3Ga, $Tb_xDy_{1-x}Fe_2$, FeRh	Cr_2O_3, Fe_2TeO_6

FE w. 180° switching

FE w. 90° switching

Para-electric w. 180° switching

Magneto-electrics with multiferroics provide

a) Multi-ferroic nature enables FE control of state

b) 180° switching

c) Voltage scalability

Khomskii, Daniel. "Trend: Classifying multiferroics: Mechanisms and effects." Physics 2 (2009): 20.

D. N. Astrov, JETP 38, 984 (1960)

BFO: R. Ramesh science 299.5613 (2003): 1719-1722

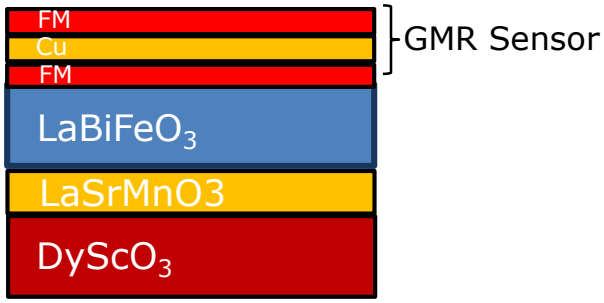
LFO: J. Mundy Nature 2016

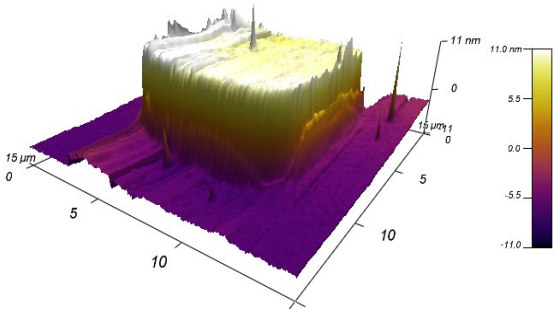
Cr_2O_3/FM *Binek et al, PRL 2005*

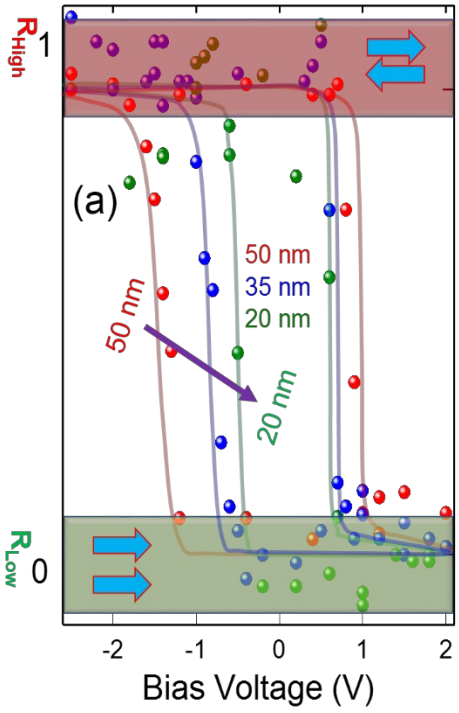
BFO/CFO *C. Ross et al APL 2012 e.g*

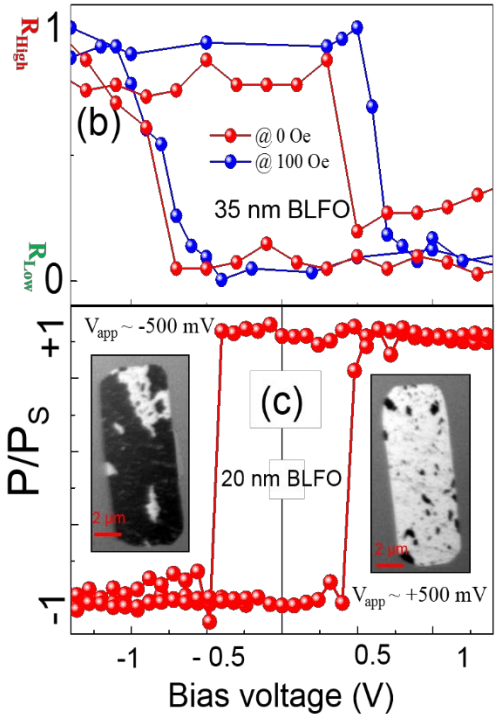
PZe/(A)FM *J. Atula et al, 2014, Manuel Bibes et al*

Scaling a Magneto-Electric to 500 mV Switching







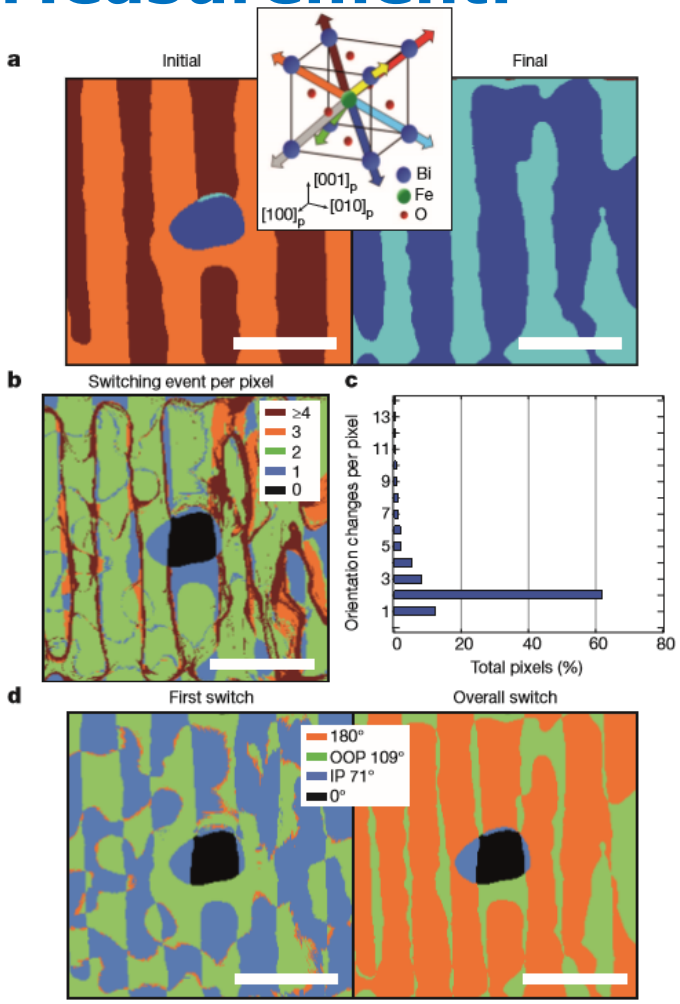


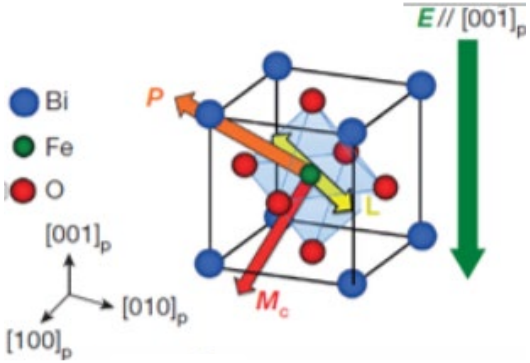
Lowest switching voltage for an ME device.

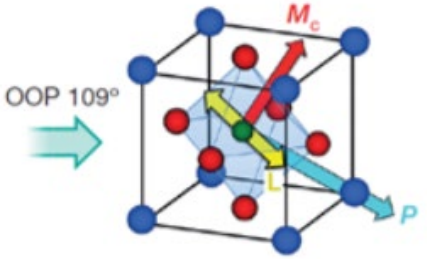
Source: Ramesh Ramamoorthy, UC Berkeley

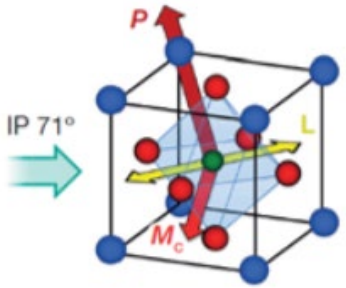
$BiFeO_3$: Two Step FE Polarization Switching:

PFM Measurement:



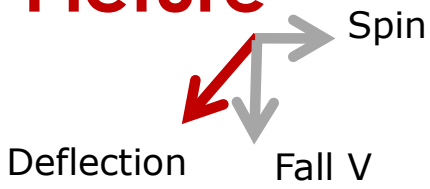






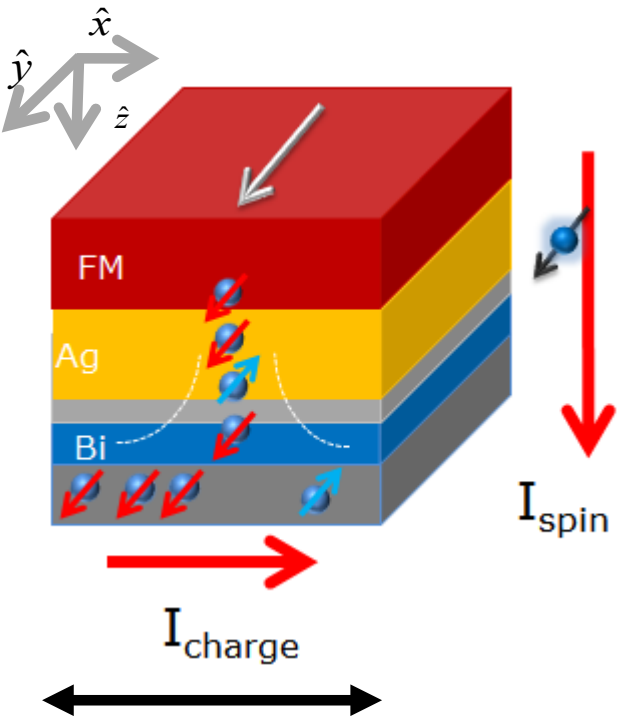
Deterministic switching of ferromagnetism at room temperature using an electric field, JT Heron, JL Bosse, Q He, Y Gao, Morgan Trassin, L Ye, JD Clarkson, C Wang, Jian Liu, S Salahuddin, DC Ralph, DG Schlom, J Iniguez, BD Huey, R Ramesh, Journal Nature, Volume 516, Issue 7531, (2014)

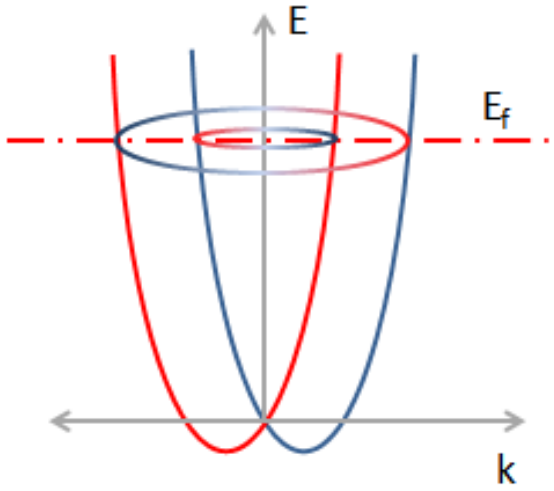
Spin Momentum Locking : Mechanical Picture

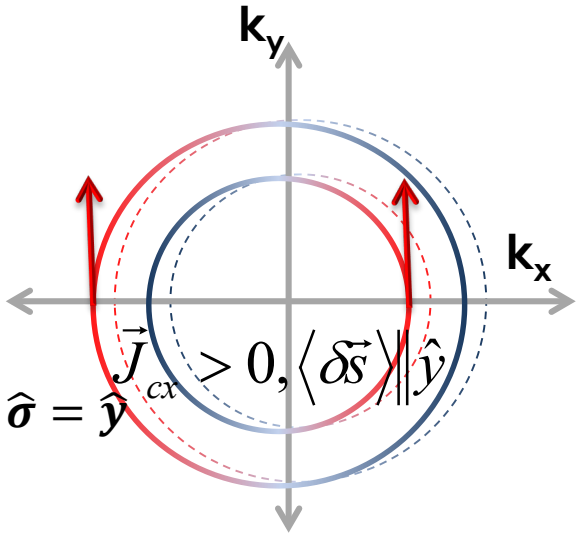


What happens when a spinning ball is dropped down a dam ?

Inverse Rashba Edelstein Effect : Efficient Spin to Charge Conversion







$$j_{Cx} = \frac{\alpha_R \tau_s}{\hbar} j_{sy} = \lambda_{ISOC} j_{sy}$$

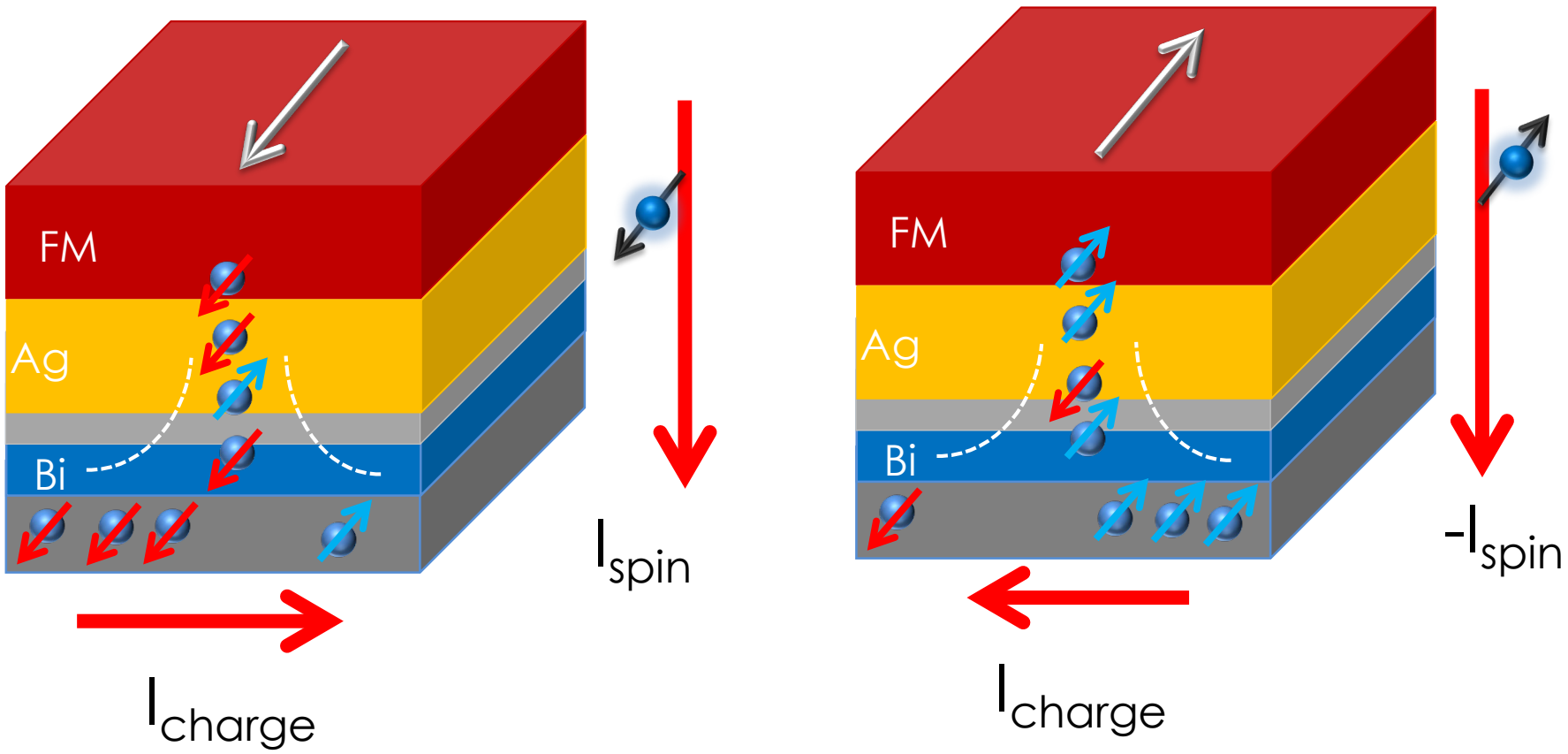
$$I_c = \frac{\lambda_{ISOC} I_{spin}}{w_m}$$

Favorable scaling !!

High efficiency spin to charge conversion is feasible using spin orbit effects.

Edelstein, V. M. Solid State Commun. 73, 233–235 (1990)
Bi/Ag: Fert Nat. Comm. 2013; (Bi/Ag) *Otani, Fert APL 2014; (Bi/Cu)* Casanova Arxiv. 2014
BiSe: JPWang 2014, MoS2: Cheng 2015, Alfa-Tin : Sanchez 2015

Efficient Spin to Charge Conversion With Spin Orbit Effects



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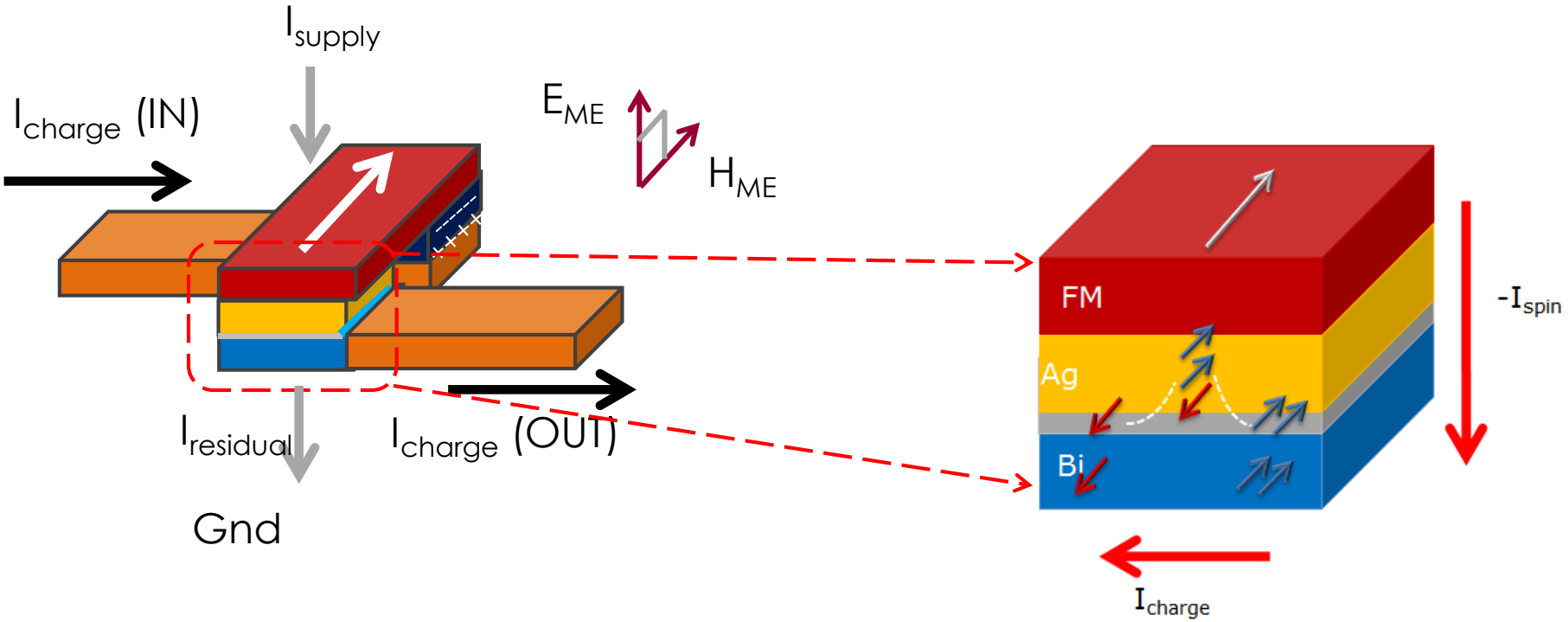
BiSe: JPWang 2014, MoS2: Cheng 2015, Alfa-Tin : Sanchez 2015

Spin Orbitronic Logic Gate with Magneto-electric Switching



IN **OUT**

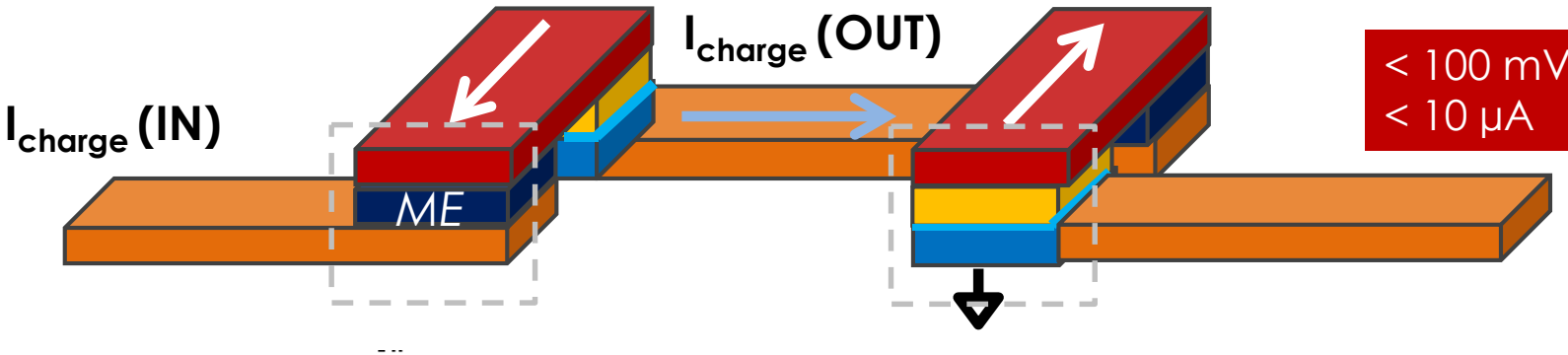
Charge Interconnect → **Electric Field In ME Oxide** → **Magnetic Field From ME Oxide** → **Spin injection From Magnet** → **Charge Interconnect**

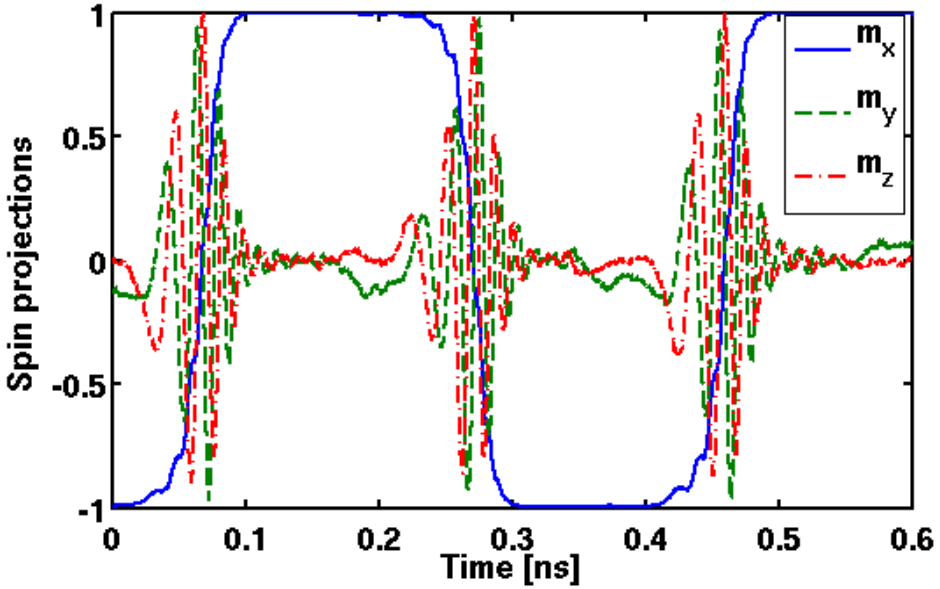
MESO: Magneto-Electric – Spin Orbit Logic

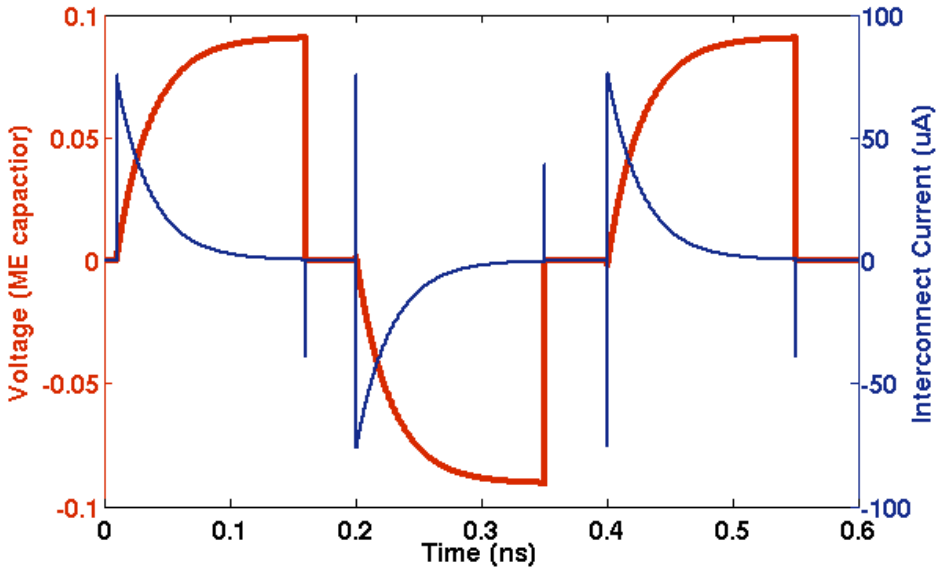
Interconnect (charge) and Low Voltage (<100mV)

aJ switching.

< 100 mV
< 10 μA







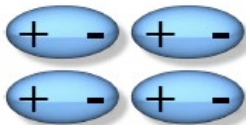
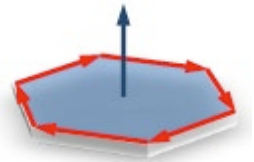
CONCLUSIONS:

- Trends in the benchmarking of Beyond CMOS Quantum Nano-Electronic and Nano-Magnetic Devices
- Nine key principles enable devices to realize practical computing technologies
- Where do we focus the research effort out of many equally important thrusts?
  - Tunneling FET transistors (0.3V power supply)
  - Magneto-Electric based logic (0.1V power supply)
  - Neuromorphic Beyond-CMOS Circuits (The Physics of AI)
- Progress is being made to realize these beyond CMOS devices

BACKUP

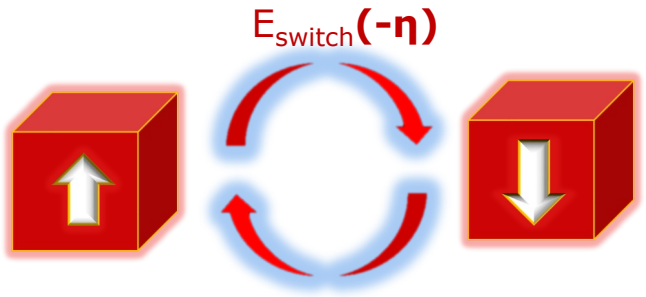
HP CMOS	High Perf CMOS
LP CMOS	Low Power CMOS
VdWFET	Van der Walls FET
HomJTFET	Homojunction III-V TFET
HetJTFET	Heterojunction III-V TFET
GnrTFET	Graphene nanoribbon TFET
ThinFET	2D hetero interlayer TFET
GaNFET	GaN TFET
TMDTFET	Trans met dichalchogenide
GpnJ	Graphene pn junction
FEFET	Ferroelectric FET
NCFET	Negative capacitance FET
SpinFET	Spin FET
ASL	All spin logic
CSL	Charge spin logic
STT/DW	Spin torque domain wall
SMG	Spin majority gate
STO	Spin torque oscillator
SWD	Spin wave device
NML	Nanomagnetic logic

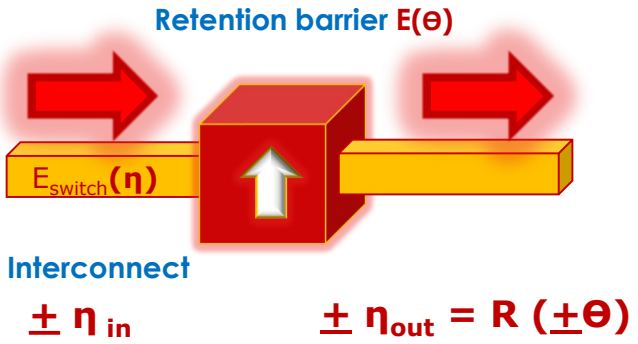
Logic Switch as reversal of an Order Parameter (State Variable) of a material

Ferro-magnetism	Ferro-electricity	Ferro-elasticity	Ferro-torodicity
			
Order Parameter: Magnetic moment	Dipole moment	Strain	Toroidal moment
Carrier: Electron Spin	Electron charge	Phonon	Meso scale Carrier ?
$E = I_{STT} V_d t_{stt} = 10\,fJ$ *	$E = 2PV_c \approx 1aJ$		

**Exception : Topological insulators and anti-ferromagnets (Neel-SOT)*

Logic Switch as reversal of an Order Parameter (State Variable) of a material



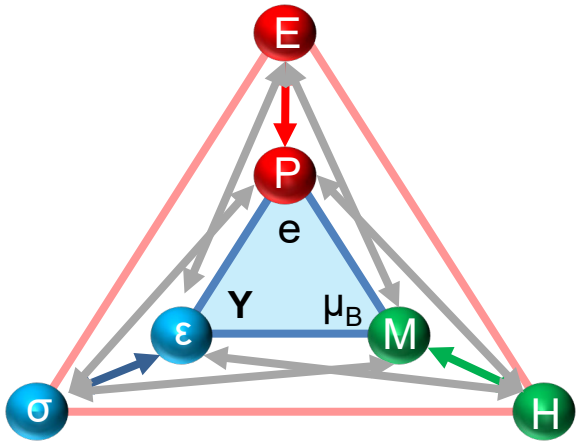


$$\lambda = \frac{E_{SW}}{E(\Theta)} \sim 2(FE), > 1000(STT)$$

The ratio of the switching energy to the barrier is optimal for Ferro-electricity

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

(JXCDC)



Scope:

Multi-disciplinary research in solid-state circuits using exploratory materials and devices for novel energy efficient computation beyond
standard CMOS technology.

JXCDC Scope

Focus is on the exploration of materials, devices and circuits for computation to enable Moore's Law to continue for computation beyond a 10 to 15 year horizon (beyond end of the roadmap for CMOS technologies) with the associated density scaling and improvement in energy efficiency.

Examples of appropriate topics are research milestones in the integration of materials, devices and circuits for computation based upon any of the following;

- Quantum electronics (e.g. tunneling), Spintronics and Nanomagnetics,
- Straintronics (piezo-electric devices), Plasmonics,
- Functional materials,
- High fan-in, fan-out logic circuits,
- Reconfigurable and non-volatile computational circuits,
- Computational circuits comprehending the on-chip communication.