Advancement in Massively Parallel Electron Beam Inspection Technology for 7nm and Below Process Development and Manufacturing

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Outline

- Introduction
- Progress toward a Multi-Beam Inspection (MBI) system
- Massive metrology using a single beam system
- Challenges in applying MBI to metrology
- Summary

Introduction

- **The semiconductor industry has thrived by delivering major leaps in functionality and performance every two years.**
- **As we transition from 7nm to 5nm and 3nm technology, inspection and metrology face two major new challenges because of shrinking critical defect size and process margins.**

A. High speed detection of critical defects.

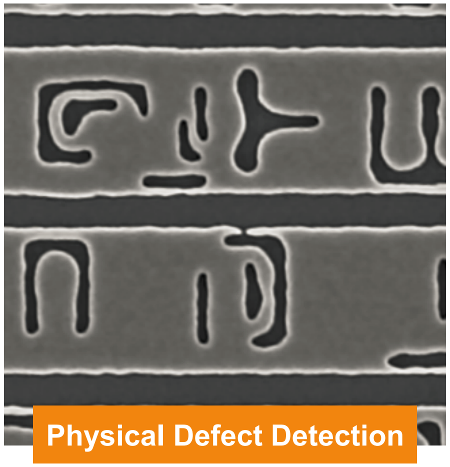
- Optical inspection has limited effectiveness.
- E-beam physical defect inspection too slow.
- Multi-beam Inspection (MBI) proposed as a solution.

B. High speed metrology for precise control of CDs across lot, wafer, reticle field, die and local CD effects

- Tradition CDSEM limited for throughput.
- Massive Metrology capability of E-beam inspection tools provides a >10x faster solution.
- Not currently on the roadmap for MBI.

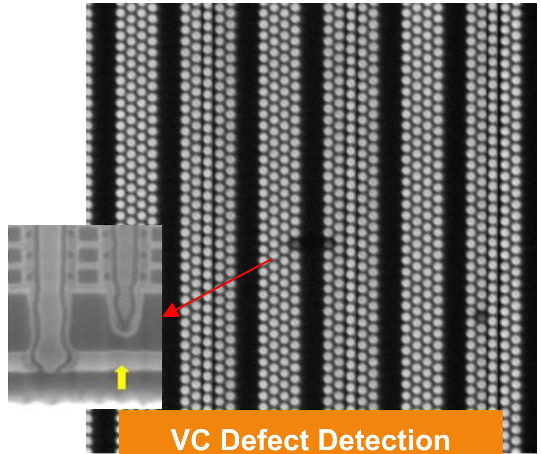
E-Beam Inspection Already Critical for Semiconductor Development

Physical Defect Inspection



- 1nm pixel size vs 30+ nm for optical inspection
- Used as Gold standard
- Used as primary inspection.
- Recently playing key role for EUV mask qual and stochastics.
- Inherent filtering of prior level defects
- Patch images allow 100% auto defect classification

Voltage contrast (VC) Inspection



- Detects electrically active defects
- Particularly useful for buried and very small defects
- Logic Devices: Gate / Contact / BEOL
- DRAM Devices: Contact for Cell & Periphery
- 3DNAND Devices: Channel Hole/ Contact

Multi-Beam Solution Demanded by Our Customers

- Incumbent optical inspection → Lack of sensitivity
- Single e-beam inspection → Not enough throughput

Challenges for equipment suppliers

Technology	Sensitivity (nm)	TPT (Wafer/hr)	How To get there
E-beam Inspection	Sub-1nm	1 die/hour	>1000 beams @ Sub-1nm resolution
BF Inspection	<5nm in SRAM	1 wafer/hour	<10nm pixel size @ ultra-bright short λ with full d2db
DF Inspection	<15nm in SRAM	1 wafer/hour	Oblique & Normal illumination with multiple λ's, with full aperture and limited d2db. Role-reversal with Unpattern

→ **Multi-Beam**

* Tuyen K. Tran, "Defect Inspection for Advanced Technology Nodes", The International Conference on Frontiers of Characterization and Metrology for Nanoelectronics(FCMN), (2015)

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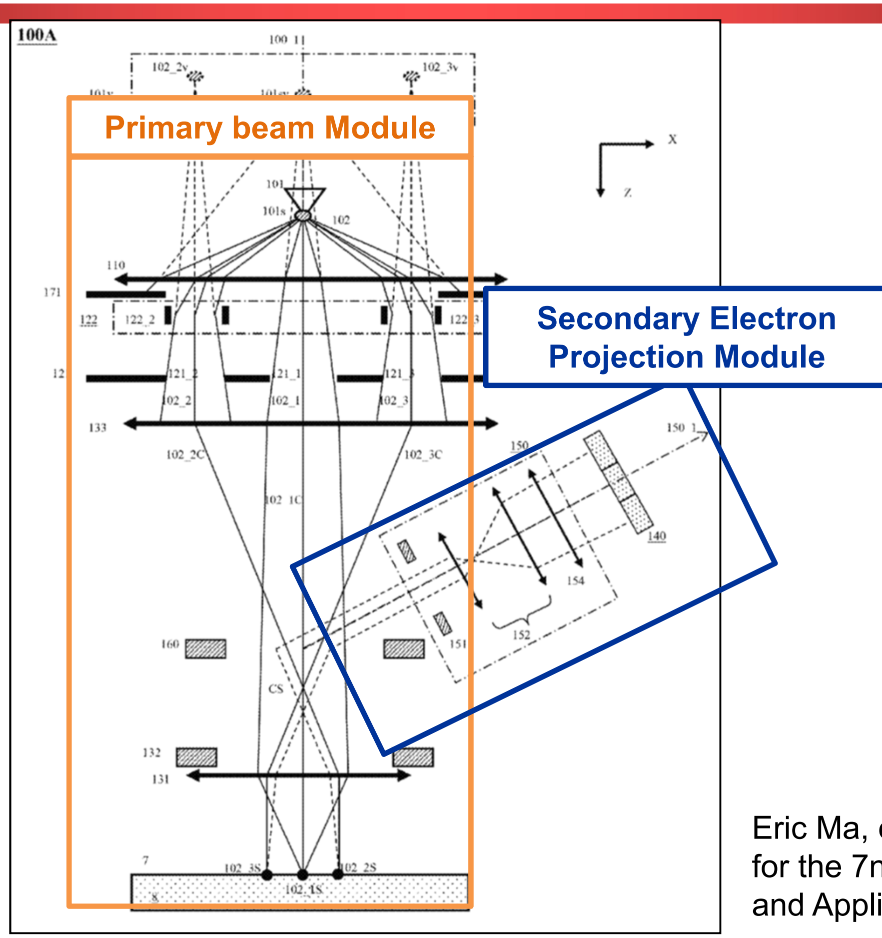
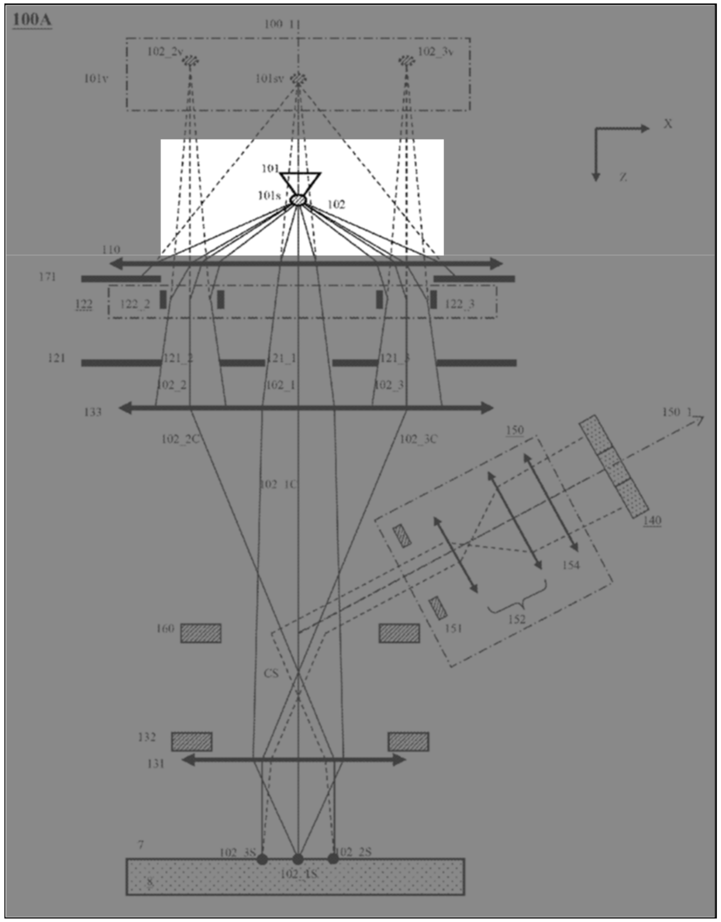
Multi-Beam Electron Optics Technology

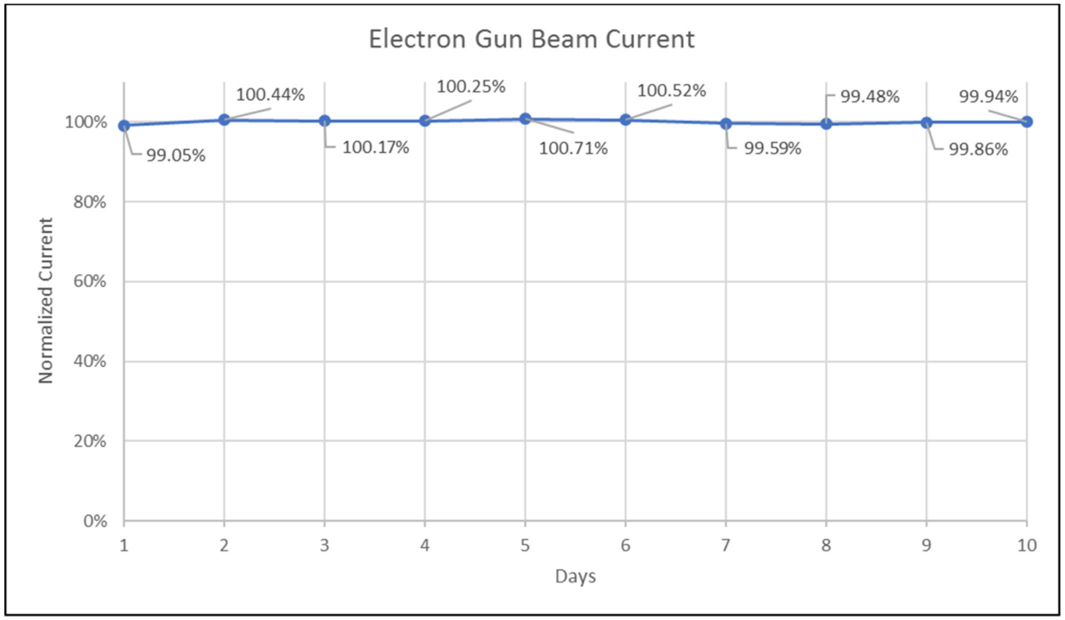


Schematic of HMI MBI Electron optics system

Eric Ma, et. al. Multi-Beam Inspection(MBI) for the 7nm Node and Beyond: Technologies and Applications, SPIE 2019.

Development Milestone: Electron Source Stability





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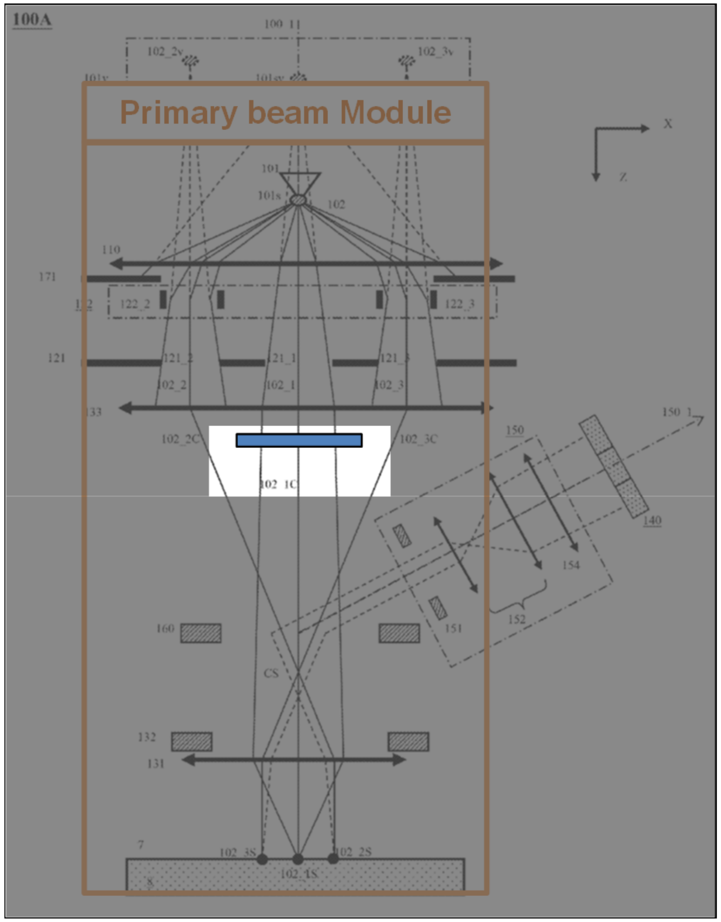
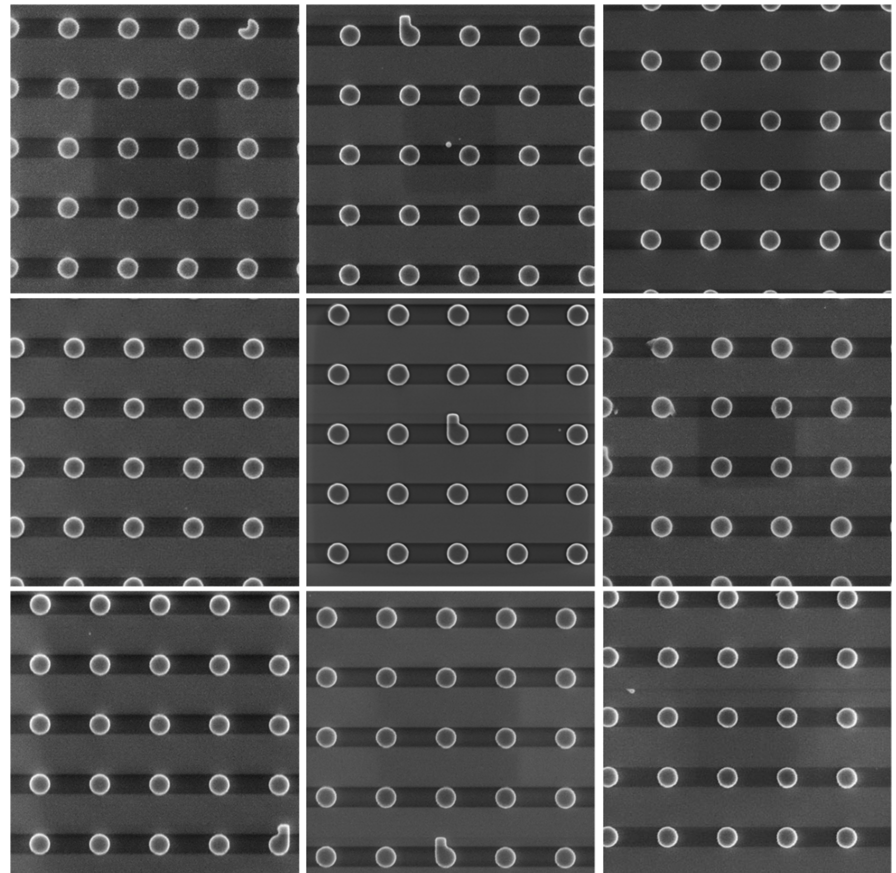
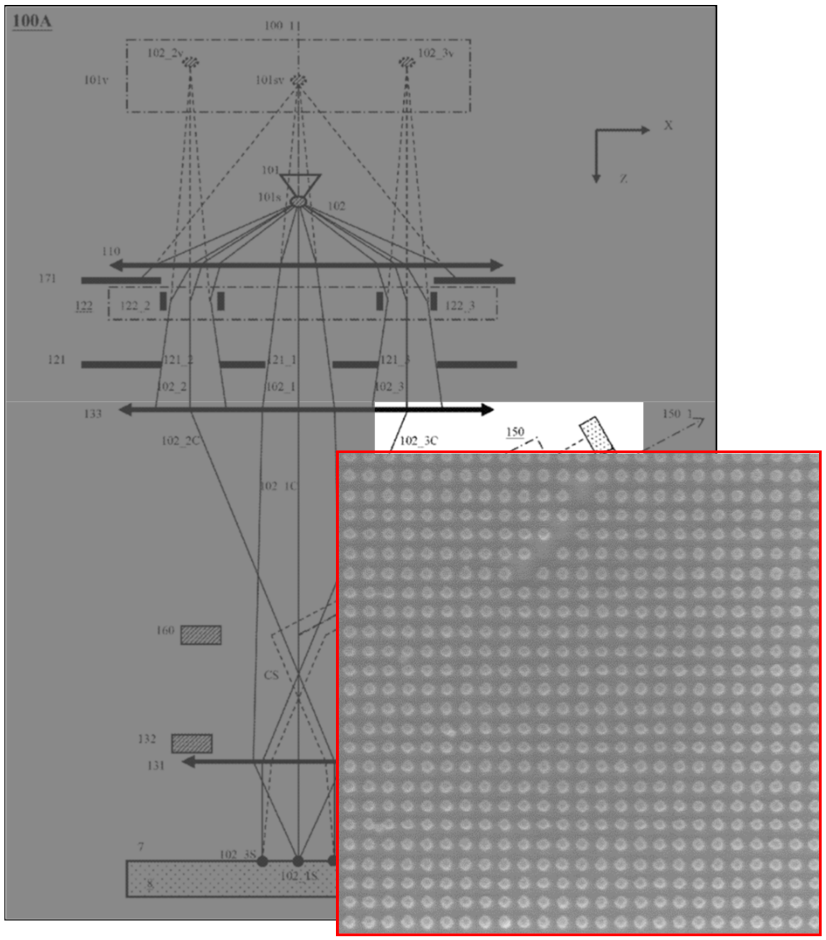
Development Milestone: Verification of Beam Splitting Mechanics

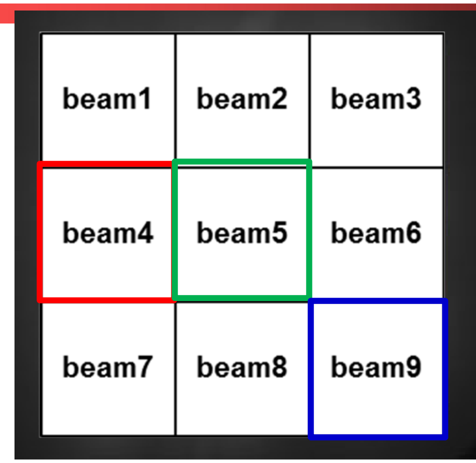


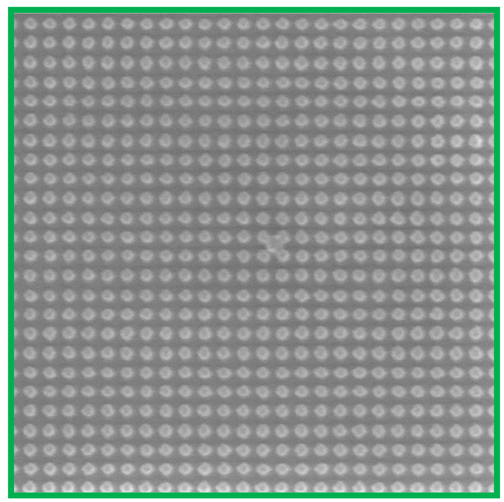


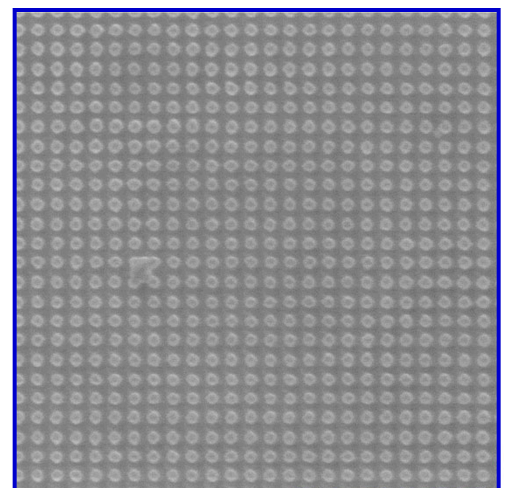
3 x 3 images by each beamlet on DOT pattern

Development Milestone: Good Image Matching

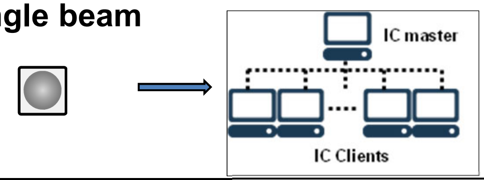
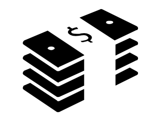
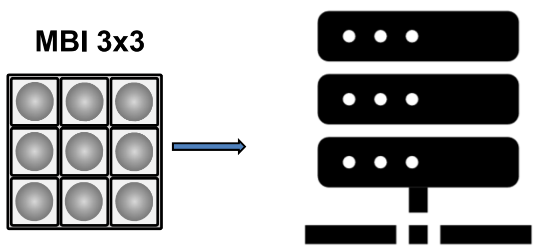
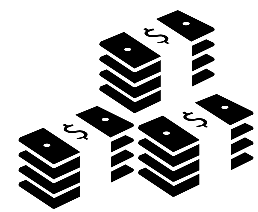








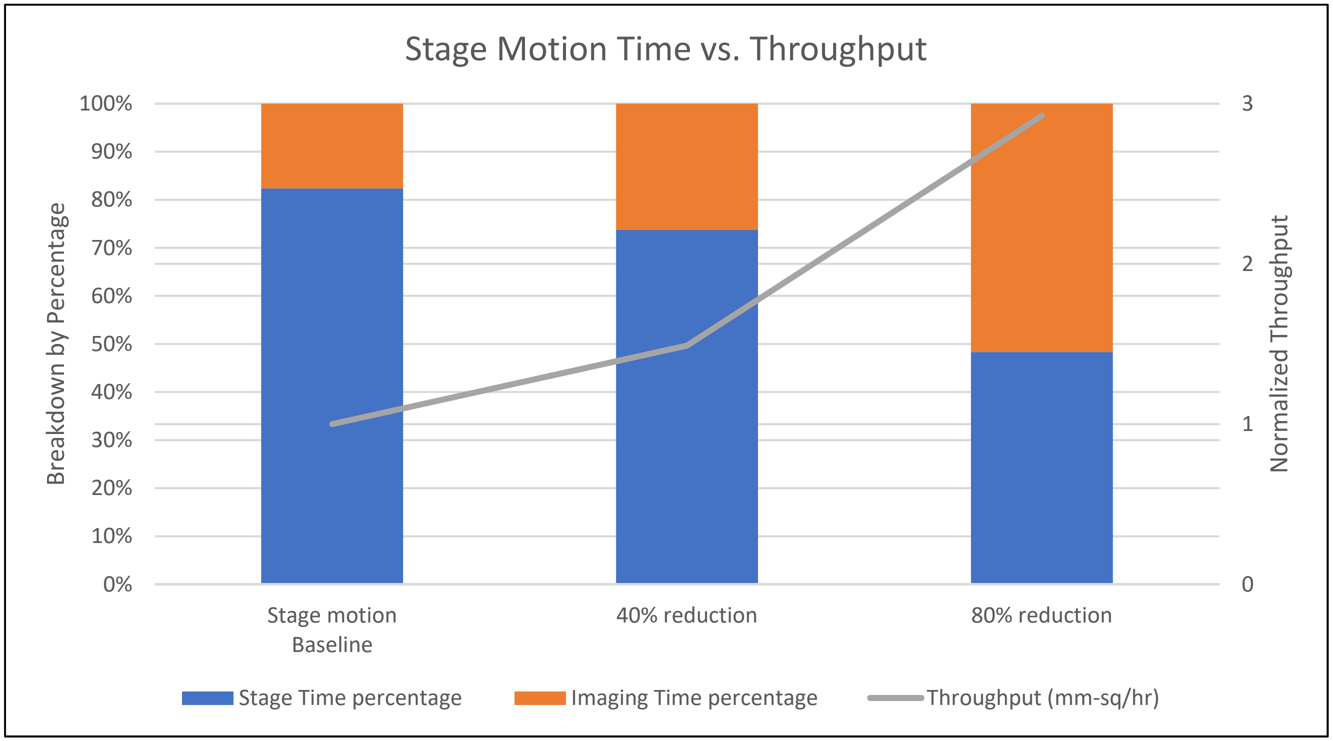
Other New Technologies for MBI: New Computational Architecture

Traditional Computational Architecture		Cost
Single beam 		
MBI 3x3 	New computational Architecture	

- **New computational architecture**
  - 50GBps data rate
  - Smaller footprint
  - Low COO
- **Major improvements in image processing algorithms**

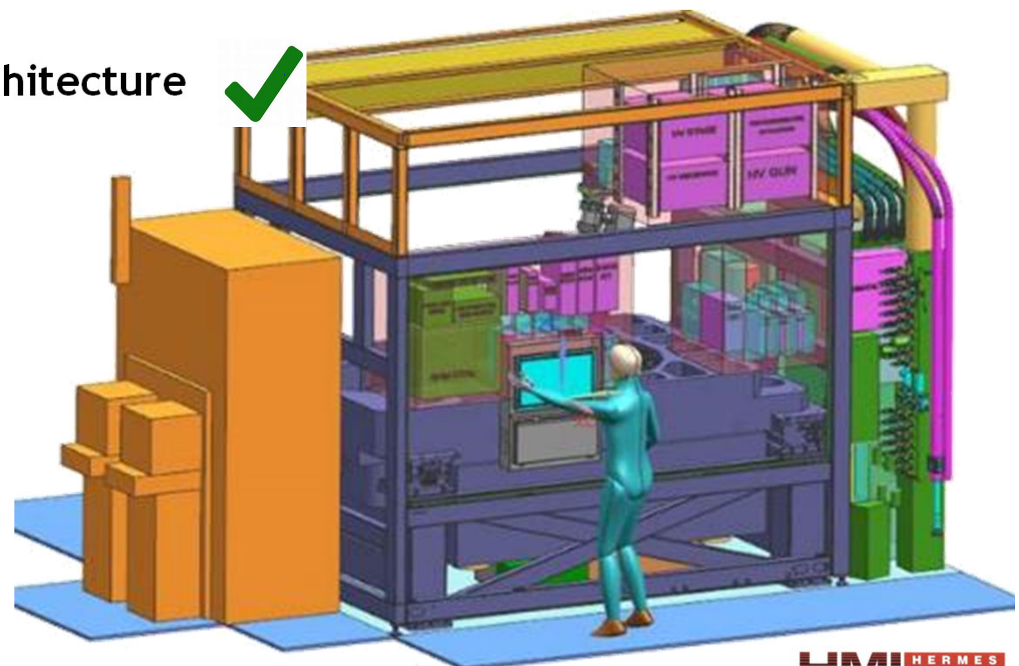
Other New Technologies for MBI: Fast Wafer Stage

- An ultra fast stage will further improve throughput.
- Also much more accurate and thermally stable.



MBI System Milestones and Plan

- Verification of gun source stability
- Independent control of multiple beams
- Bending beams to detector while minimizing crosstalk.
- Matching of beamlet quality
- New efficient 50GHz Computational Architecture
- New Ultra-fast and Stable Stage



- Initial system being evaluated now.
- Roadmap of systems staircasing up in beam number.
- Upgrade strategies for cost effective reaping of throughput gains.

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Massive Metrology using single beam EBI

- **HMI EBI tools have offered a CD measurement capability for ~8 years.**
- **Resolution is now approaching CD SEM resolution.**
- **E-beam inspection tools have a large field of view (FOV) and the ability to measure all locations within that FOV.**
  - Current tool has 144x the FOV of the standard CDSEM at 1nm pixel size.
  - Less than 0.1% distortion and 0.1nm single CD measurement precision within the FOV.
  - In some scenarios, 68x throughput advantage vs. cutting edge CDSEMs.
- **Extensive incorporation of design information for**
  - Recipe setup
  - Complex measurements
  - Pattern search
- **Contour extraction capability for comparison to design intent (MXP) and statistical analysis.**

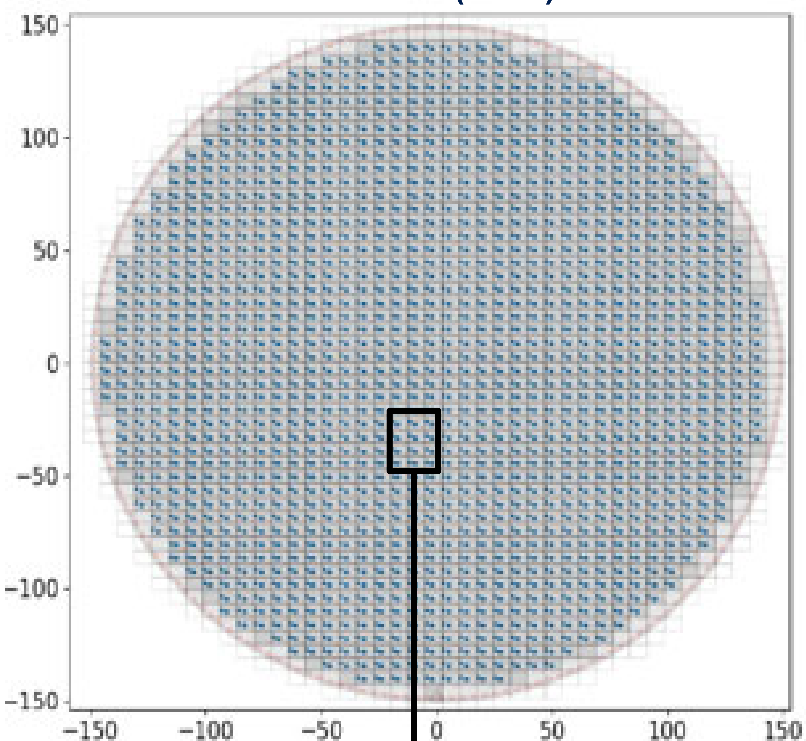
Applications

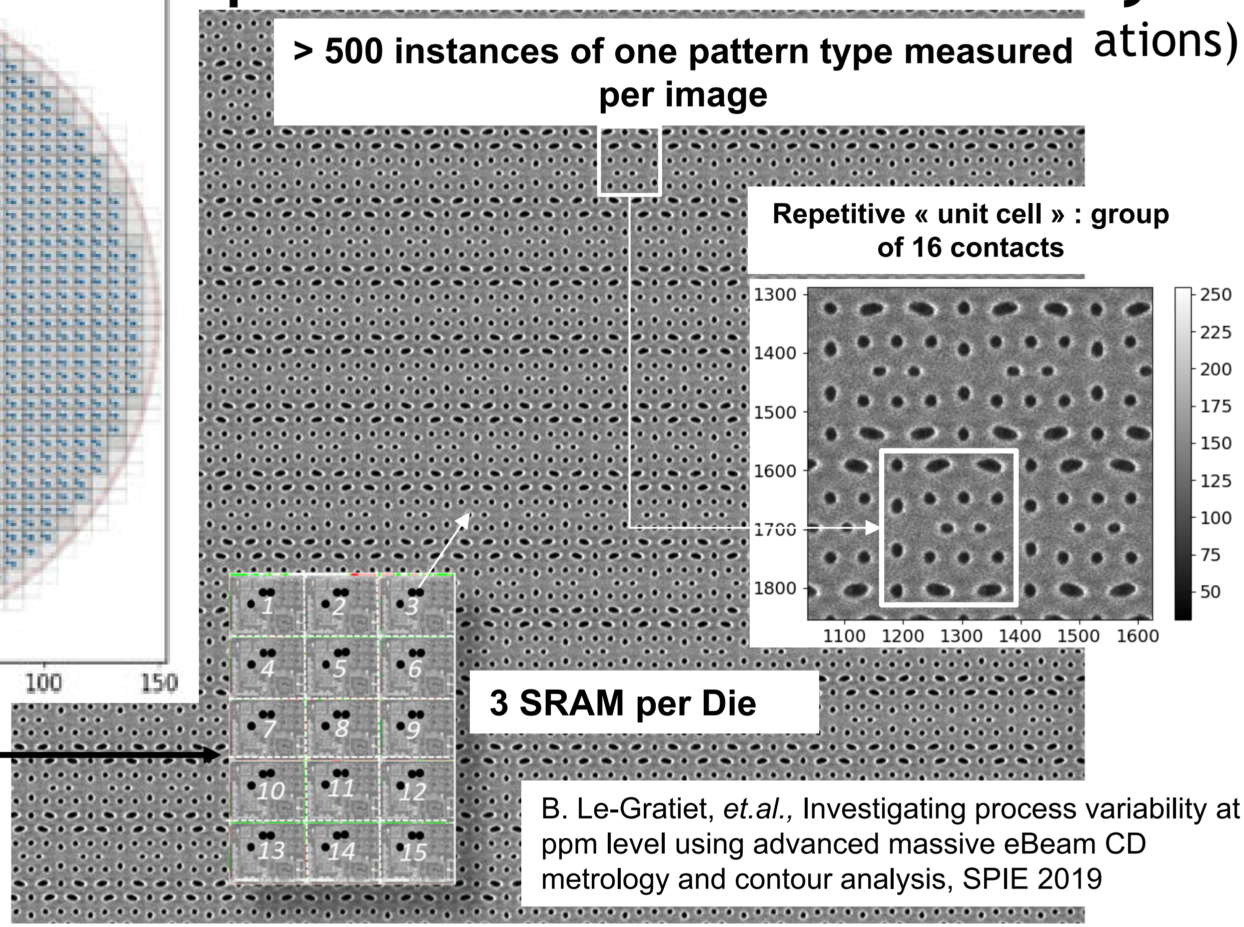
- **Massive metrology useful to track local as well as across reticle and wafer CD variation.**
- **Can study process margin variation across a much larger area and across many levels or layers. Examples:**
  - Fin…Gate…Contact
  - Litho….etch…cmp
- **Recent FINFET technologies constrain pitch and feature width using SADP and SAQP.**
  - Can compare alpha, beta, gamma spaces for various mandrel size. Can study fin bending.
- **Can determine root cause of a CD related failure mode.**
- **Can track the "fingerprint" of different litho or etch tools for excursion detection.**

…mple for SRAM contact lay…

…ations)

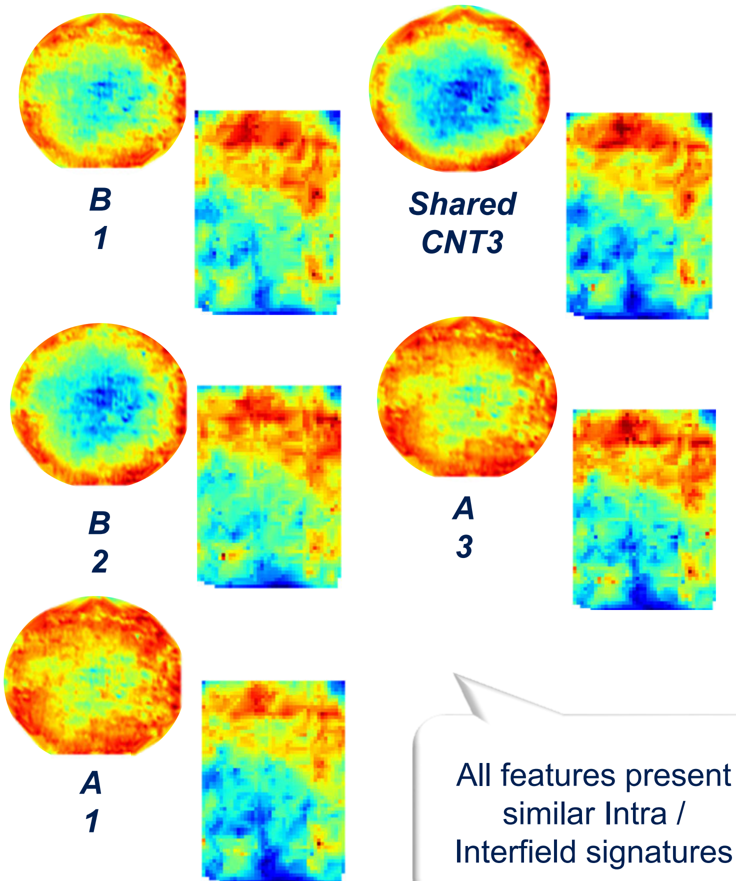
All full die measured (1455)



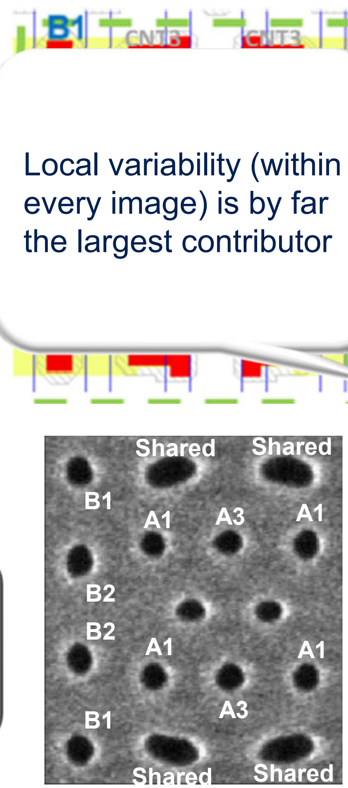


B. Le-Gratiet, *et.al.*, Investigating process variability at ppm level using advanced massive eBeam CD metrology and contour analysis, SPIE 2019

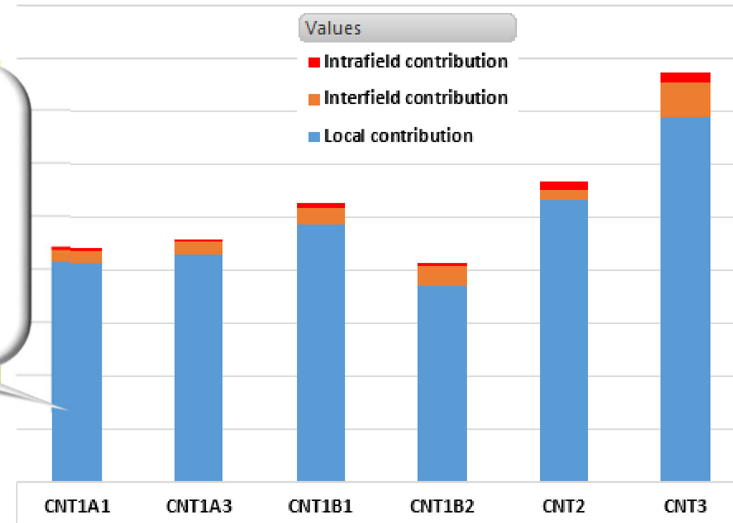
CD variability breakdown



All features present similar Intra / Interfield signatures

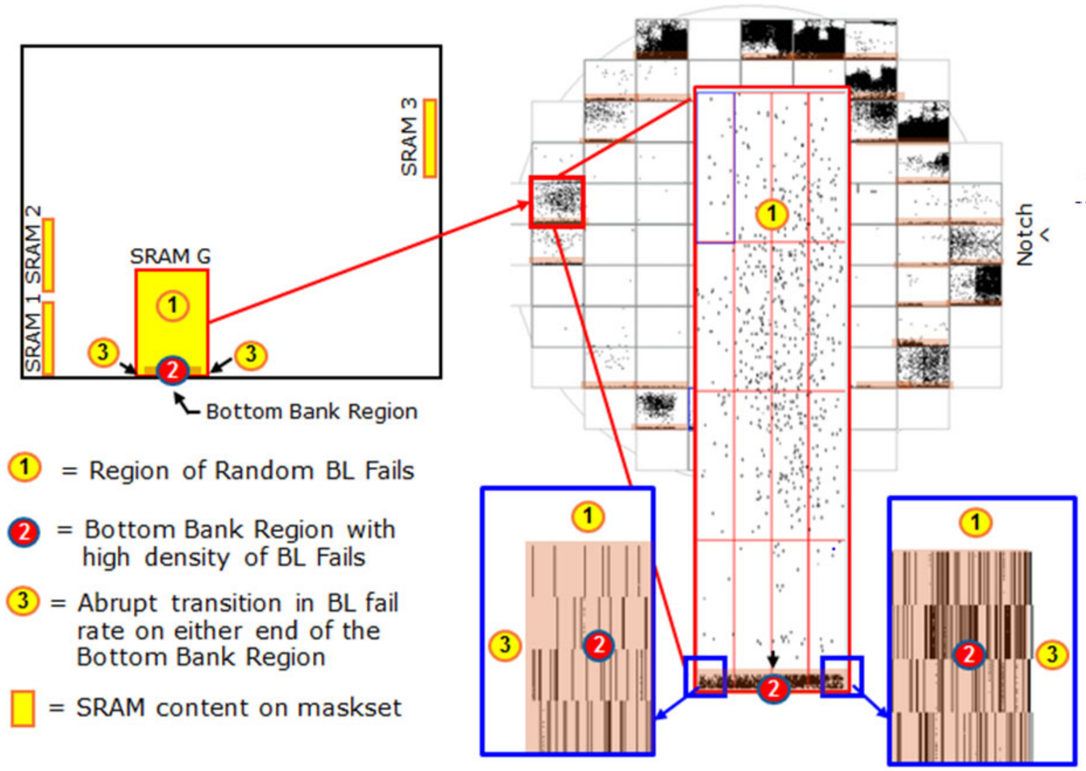


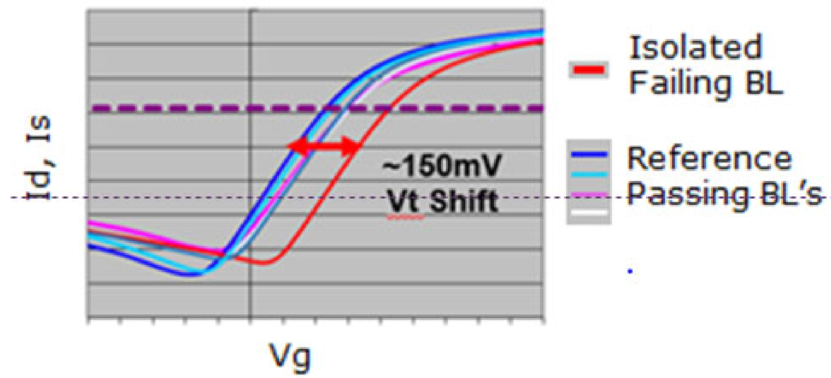
Local variability (within every image) is by far the largest contributor



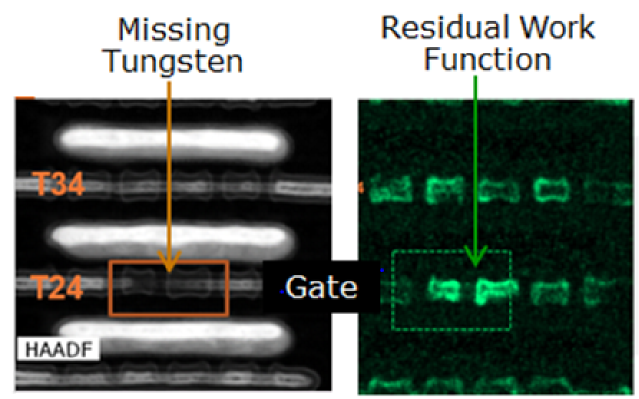
CNT	Local_% vs total	Interfield_% vs total	Intrafield_% vs total
CNT1B1	92%	6%	2%
CNT1B2	92%	9%	1%
CNT1A1	90%	5%	1%
CNT1A3	94%	5%	1%
CNT1_all	94%	5%	1%
CNT2	94%	3%	3%
CNT3	94%	9%	2%

Small gate linewidth causing yield loss at GLOBALFOUNDRIES





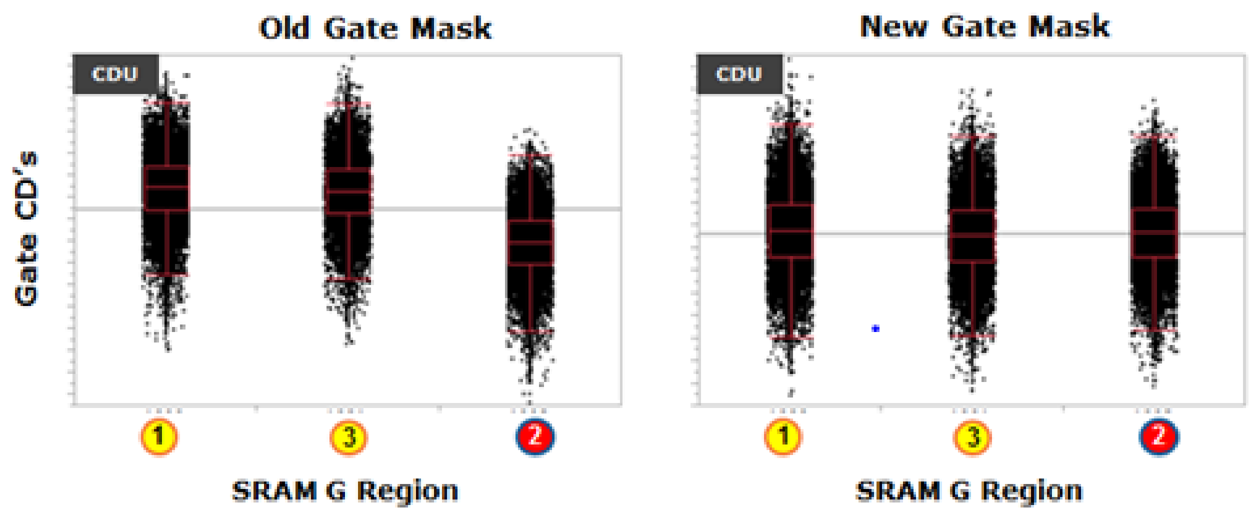
- **Work function shift in transistors in bad region 2.**
- **Linked to gate CD.**



Steve Lucarini, *et. al.* “Chasing Ghosts: How an SRAM Detected the Subtle Impact of Stray Light”, ASMC 2016.

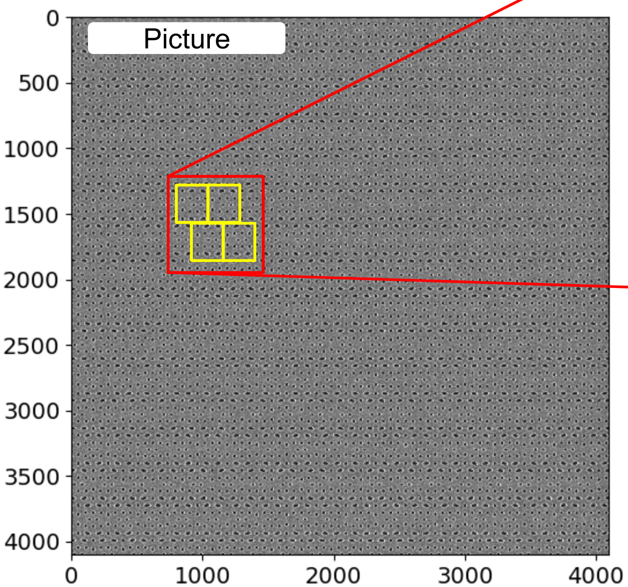
Small gate linewidth causing yield loss at GLOBALFOUNDRIES

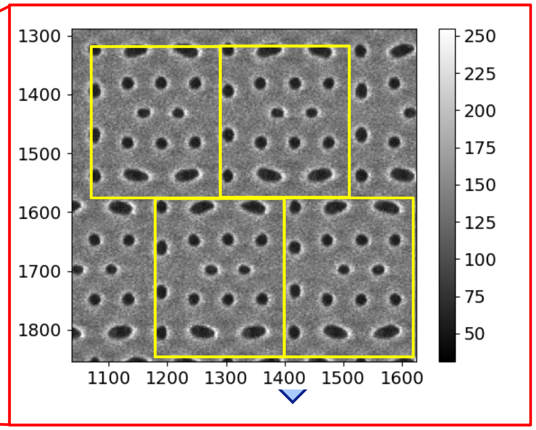
- Massive metrology CD measurement found gates were smaller in this region.
- Used for early validation of the solution.



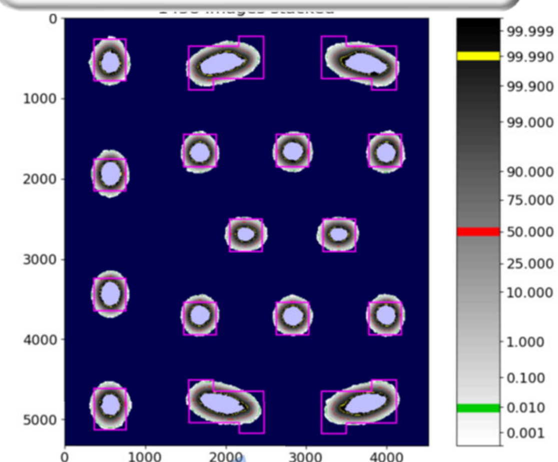
Contour Extraction

Each picture contains 238 unit cells

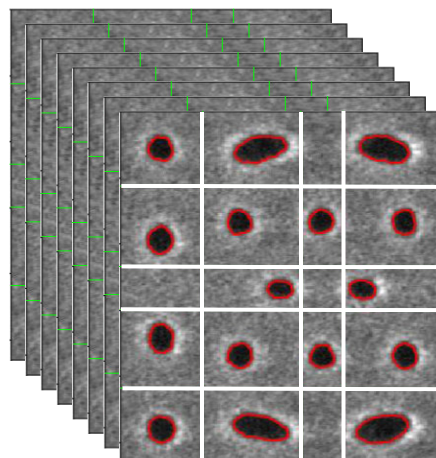




1455 images x 238 unit cells contours are stacked (about 350k unit cells)



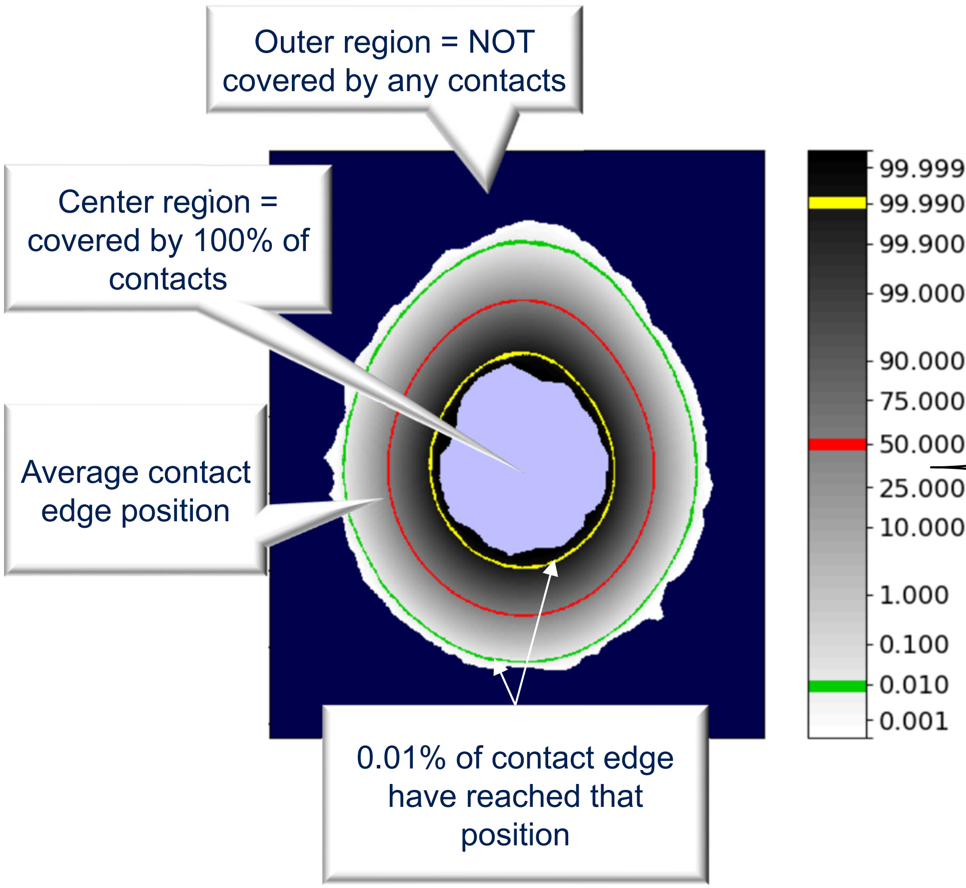
For every unit cell contours are extracted and converted to labelled polygons

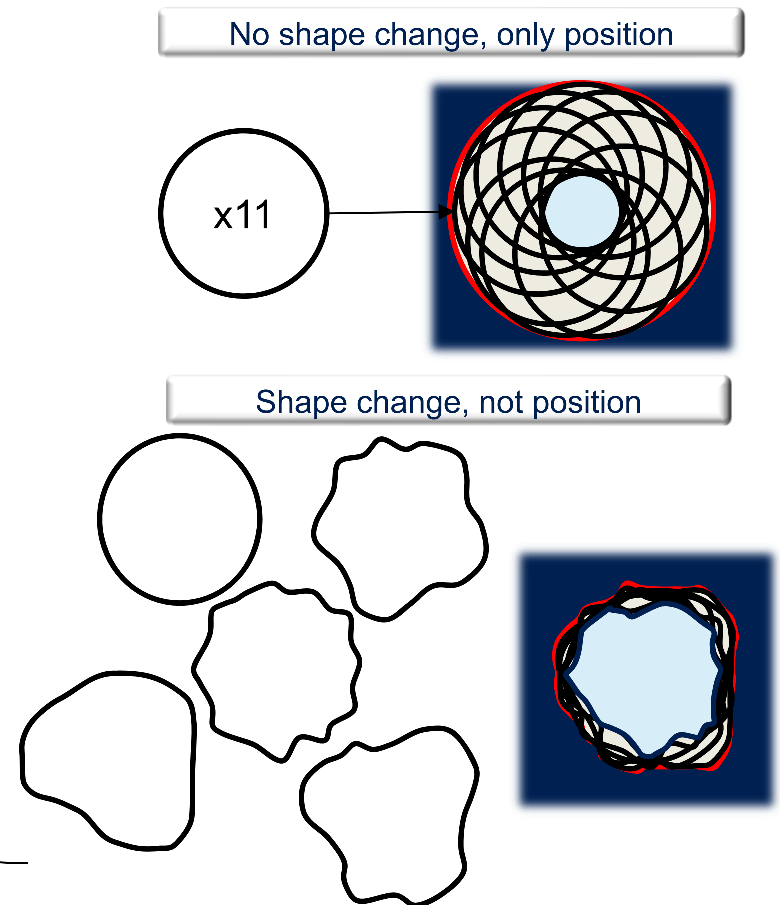


Contours are aligned and stacked to draw an Edge position probability map

-Gratiet, … ppm level using advanced massive eBeam CD metrology and contour analysis, SPIE 2019

Contour Stacking





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Challenges applying MBI to metrology

- Metrology applications have greater resolution requirements. -> Matching our best our best single beam tool resolution will be quite difficult.
- Metrology applications have much greater image consistency requirements. -> Matching large numbers of beamlets adds tremendous complexity.
- Most metrology applications are not an ideal match for Multi-beam. Multi-beam tools best for large areas since the pitch of the beams is fixed.

- Once Multi-beam inspection successful for inspection, we'll consider again whether to adapt this technology for metrology applications.

Summary

- **For development of 5nm and 3nm technology nodes, gaps exist for:**
  - High speed detection of critical defects
  - High speed metrology for precise control of CDs across lot, wafer, reticle field, die and local CD effects
- **Major progress made towards a multi-beam inspection system.**
- **Physical, Voltage contrast and EUV mask qual applications targeted.**
- **Application to metrology not currently on our roadmap, but our single beam massive metrology capability offers a giant step up in throughput for interested customers.**