# Electromigration Power Grid Checking – Novel Design and Reliability Metrology

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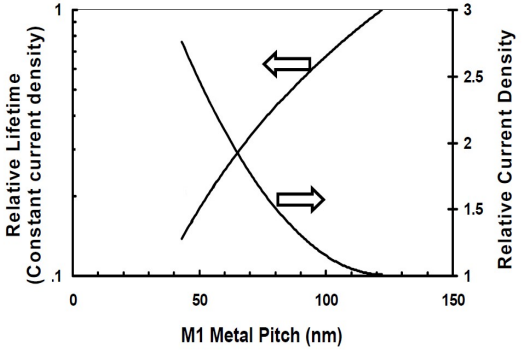
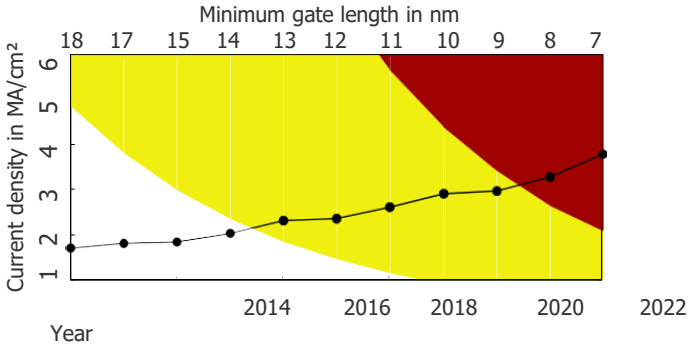
# Introduction – EM is a Major Design Concern

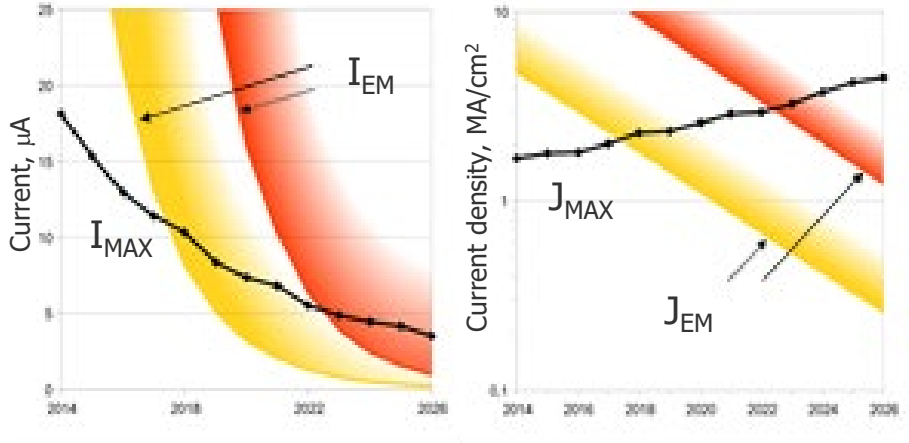
**With technology scaling:** electromigration has become a major reliability concern for design of large integrated circuits.

- The ongoing IC component miniaturization results in a reduction of the metal interconnect cross-sections and, hence, **an increase of the current densities**, because the required currents cannot be reduced to the same extent, even by reducing the supply voltages and gate capacitances.
- **The electromigration (EM) lifetimes of metal lines have been decreasing.**




*Jens Lienig, ISPD'13, p. 33-40, 2013.*

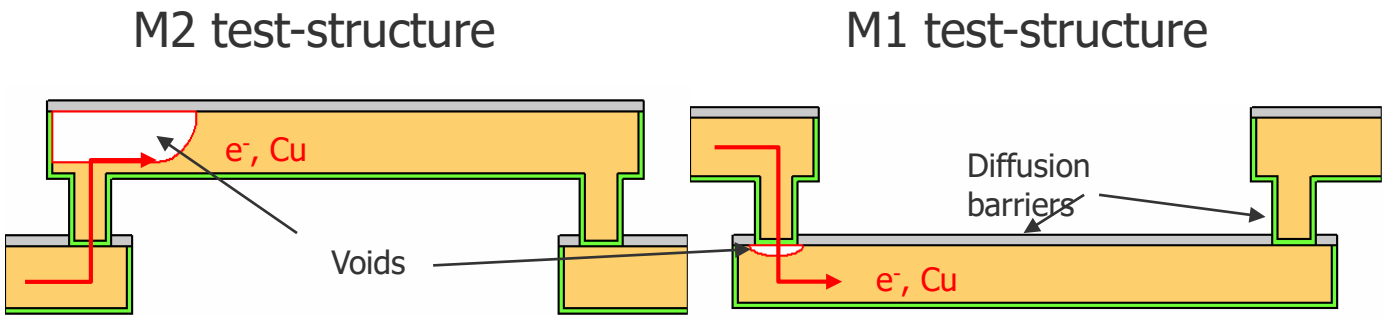


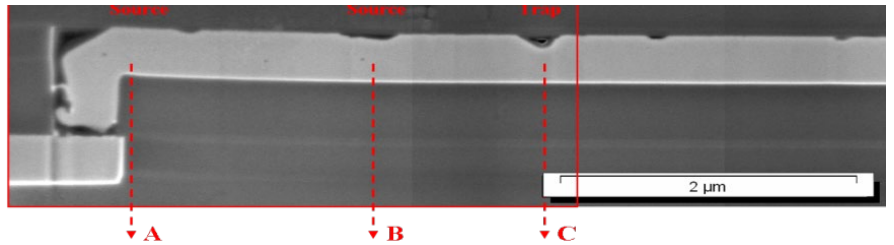

Expected development of currents ($I_{max}$) and current densities ($J_{max}$) needed for driving four inverter gates, according to ITRS 2011. EM degradation needs to be considered when crossing the yellow barrier of currents ($I_{EM}$) and current densities ($J_{EM}$).

**As for now, manufacturable solutions are not known in the red area.**

# Problem Caused by Electromigration

- Electromigration is the movement of metal atoms along the wire by the applied electric current.
- When many atoms were moved out of the cathode region **voids can be formed**

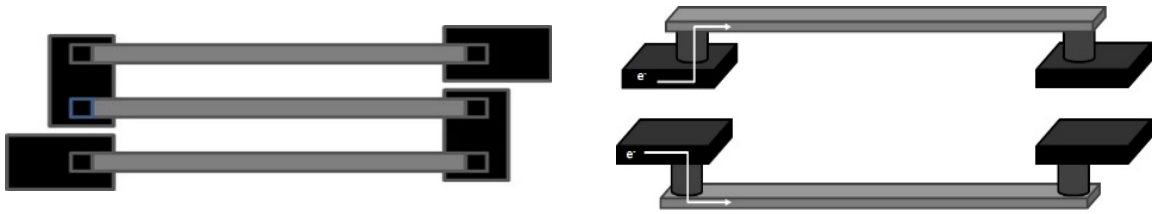



- **Voids increase resistances** of the affected metal wires.
- This can lead to undesirable changes in chip operations, for example, the timing violations can be developed.
- An intensity of void generation and, hence, a **rate of resistance degradation** can be reduced by **limiting wire electric currents**.
- Foundries introduce special design rules – **CURRENT DENSITY DESIGN RULES**, which should be obeyed in all chip designs.

# Existing EM Checking

## Test-structures



Multi-link test structure (a), upstream and downstream EM test-structures (b). Arrows indicate the electron flow directions.

## The empirical Black's model:

$$MTTF = \frac{A}{j^n}\exp\left(\frac{E_a}{k_B T}\right)$$

$$j_{MAX} = j_{test}\left(\frac{MTTF_{test}}{MTTF_{TARGET}}\right)^{\frac{1}{n}}\exp\left\{\frac{E_a}{k_B}\left(\frac{1}{T_{use}}-\frac{1}{T_{test}}\right)\right\}$$

- A large number of identical test structures are used for measurements of resistance degradation caused by big elevated electric current load and high temperature
- An exiting metal microstructure variation provides different TTF for different lines (TTF is an instant in time when a line resistance increase equals, say, 10%)
- From measured TTFs two parameters of Black's equation: $n$ – a current density exponent, and $E_a$ – an activation energy are extracted
- These parameters are used for calculating MTTF for other load conditions – $j$ and $T$
- If one knows a desired $MTTF_{TARGET}$, then a max current density, which "kills" this segment not faster than $MTTF_{TARGET}$ can be estimated

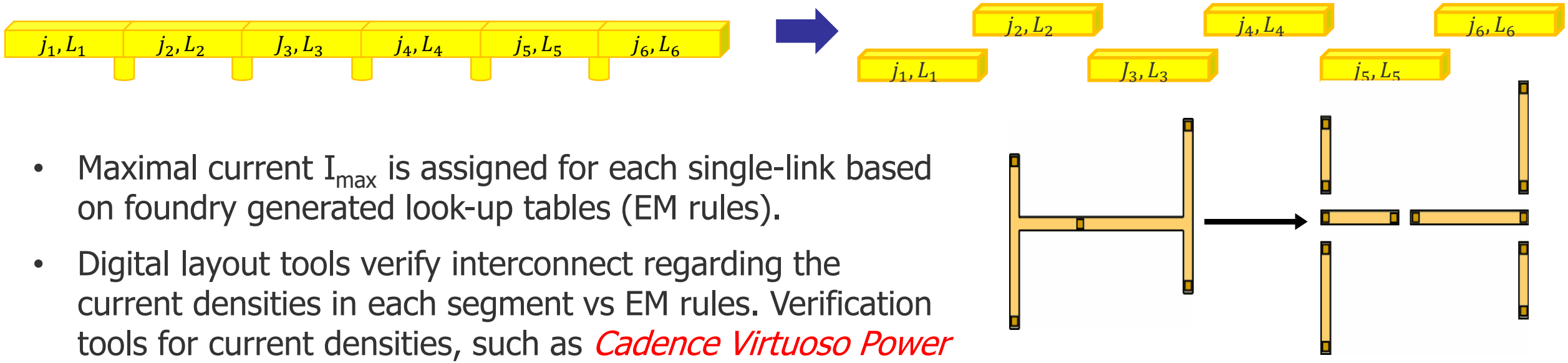
# Existing EM Checking

- Foundries use the described methodology for extracting $j_{max}$ for different interconnect segments characterizing by a variety of geometries.
- Foundries generate the EM Reliability Rules, which provides metal $I_{max}$ dependence on metal length & width, and temperature. For example for $T$ = 110°C:

| Metal Wiring Level | Metal Length, L (um) | Metal Width, W (um) | $I_{max}$ (mA) |
|---|---|---|---|
| M1 | L <= l | Any width | 3 x B x (w – W1) |
| | L > l | w >= W | 2 x B x (w – W1) |
| | L > l | w < W | B x (w – W1) |

# Industry Adopted EM Checking Methodology

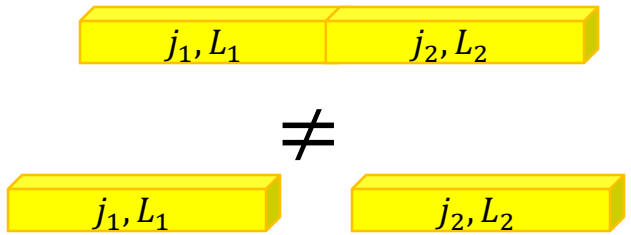
- All interconnects are decomposed into single-links:

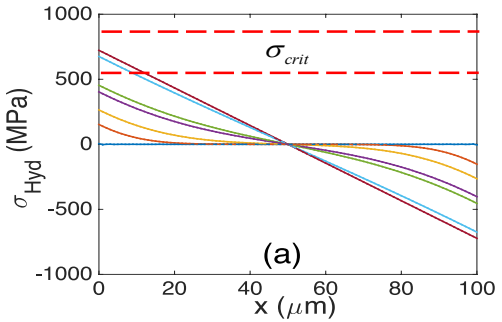



- Maximal current $I_{max}$ is assigned for each single-link based on foundry generated look-up tables (EM rules).
- Digital layout tools verify interconnect regarding the current densities in each segment vs EM rules. Verification tools for current densities, such as *Cadence Virtuoso Power Systems, Synopsys CustomSim, Mentor Calibre PERC*, and *Apache Totem MMX*, are employed.
  - They extract a netlist from the layout (parasitics).
  - This netlist is then used to simulate the currents in all wires.
  - If any of the extracted current densities exceeds an EM-relevant boundary, a violation is detected, highlighted, and repaired by a line widening.

# Problems with Current Approach

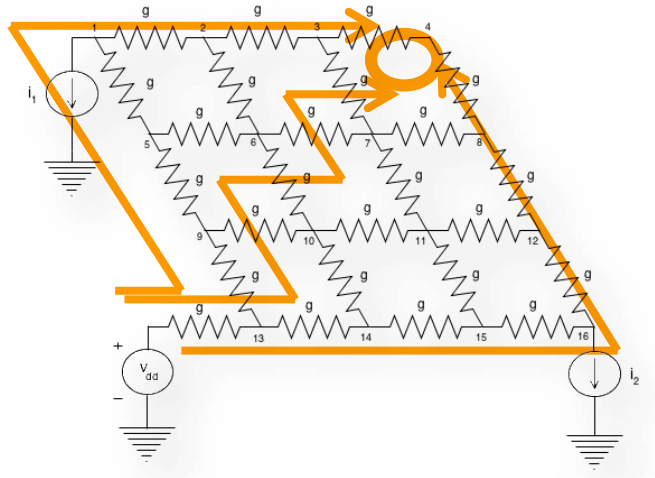
## ❑ Material Flow is ignored




- There are no diffusion barriers between segments of P/G, so atoms can freely flow from one segment to another
- Thus, there is no atom depletion and accumulation at segment ends
- Voids are not expected to be formed at any cathode ends

## ❑ Redundancy is unaccounted for

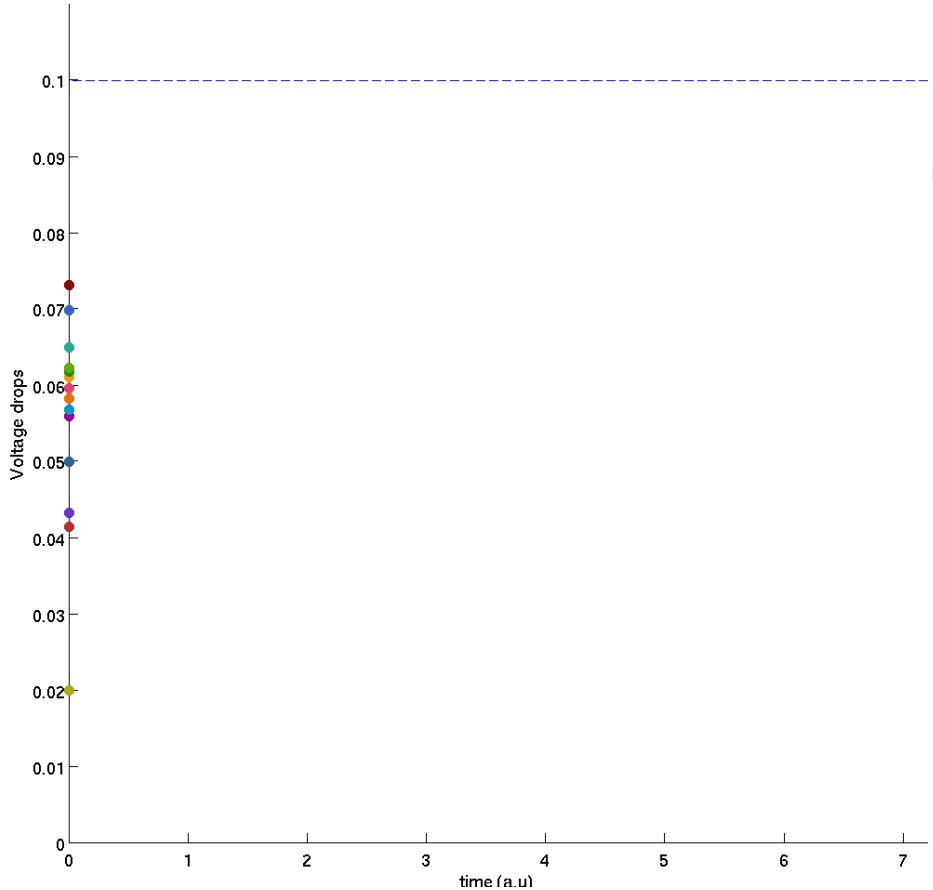


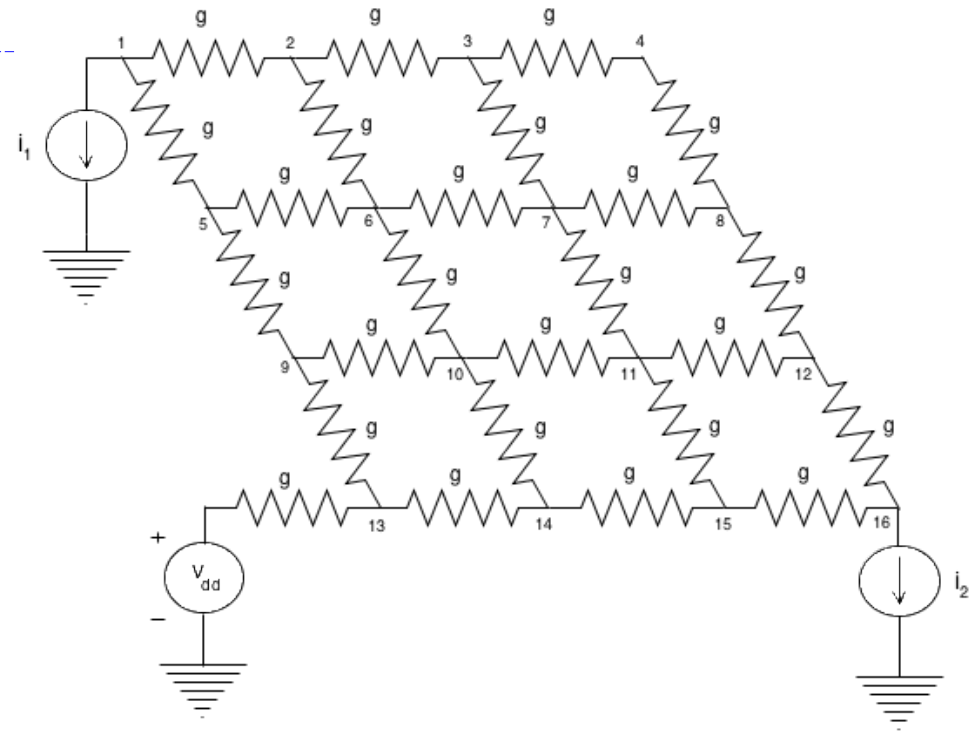
- The grid has redundancy and can survive several line failures

## ❑ The series model assumption.

A series model is the case where a power grid is deemed to have failed as soon as the first of its branches has failed, typically due to an open circuit. However, modern power grids use a mesh structure. As such, there are many paths for the current to flow from the flip-chip bumps to the underlying logic, a characteristic we are referred to as a redundancy. As such, it is highly pessimistic to assume that a single branch failure will always cause the whole grid to fail. **("Pessimism never won any battle."- Dwight D. Eisenhower, U.S. president and general (1890 - 1969))**

# Progress Toward Failure



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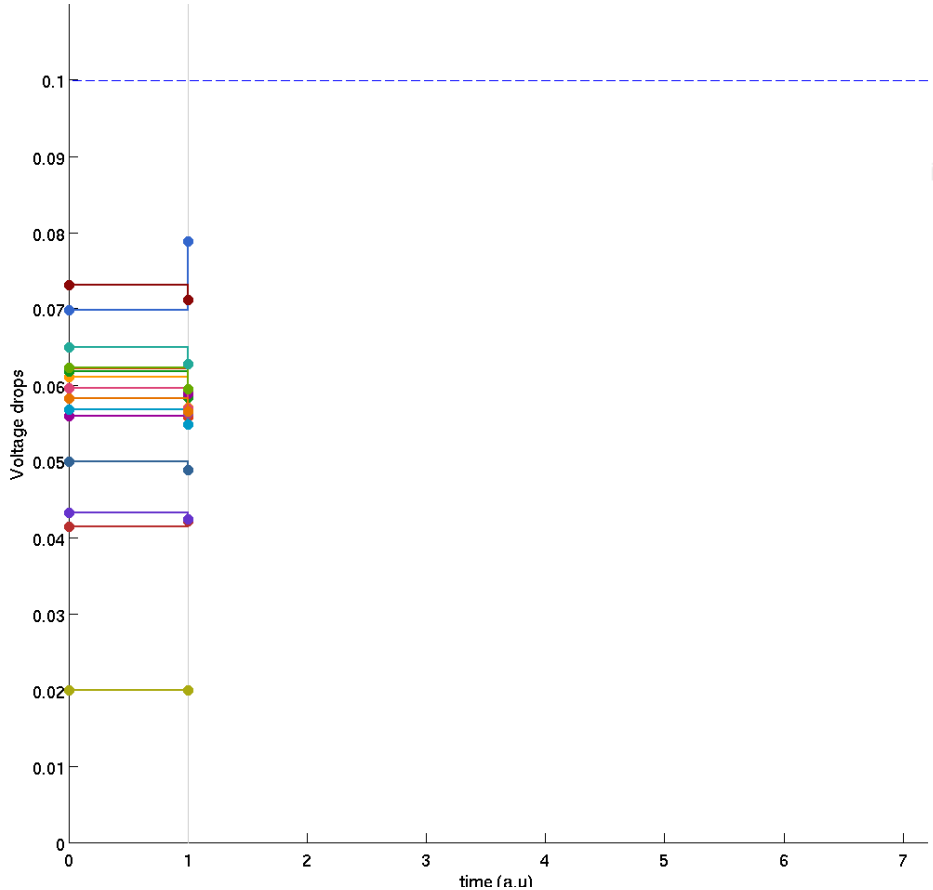


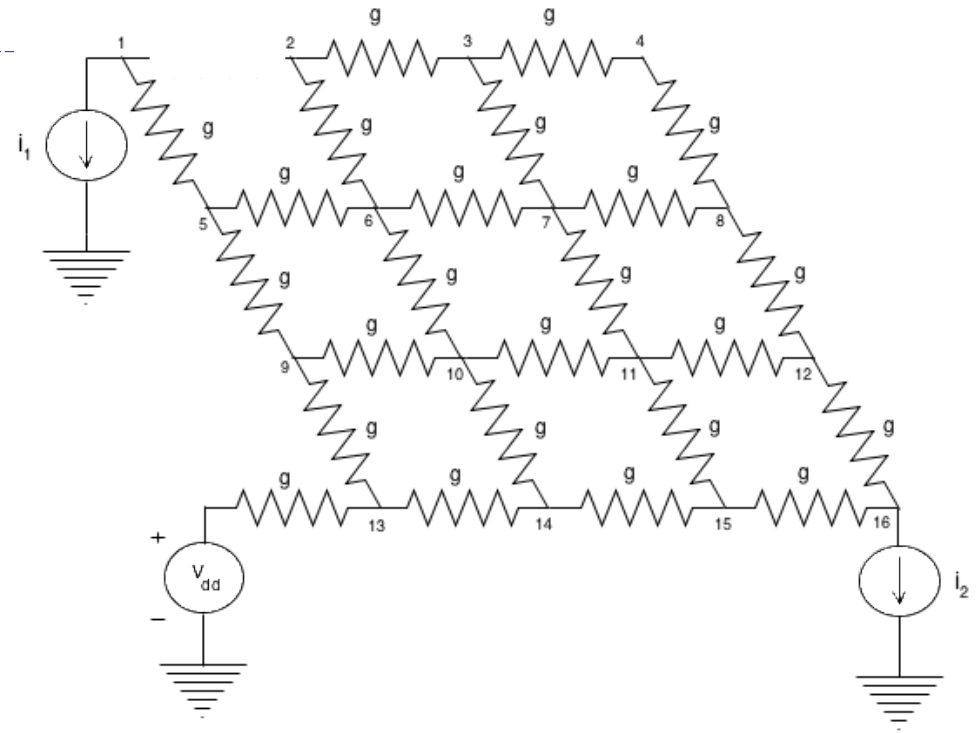

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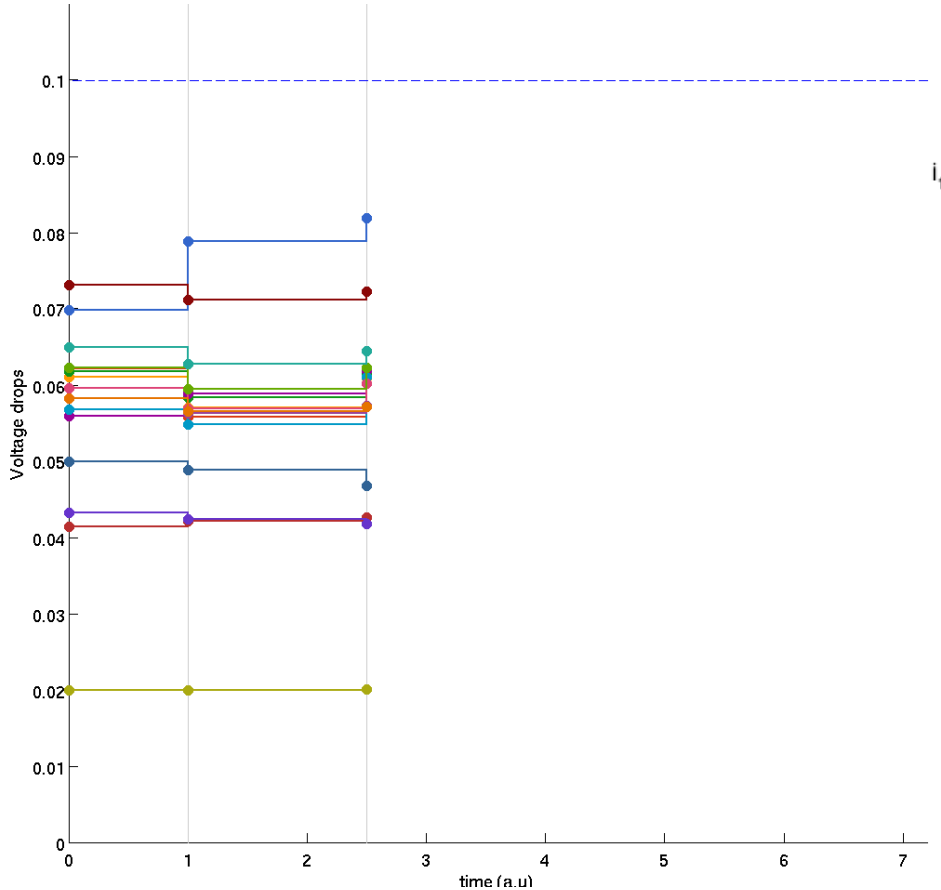


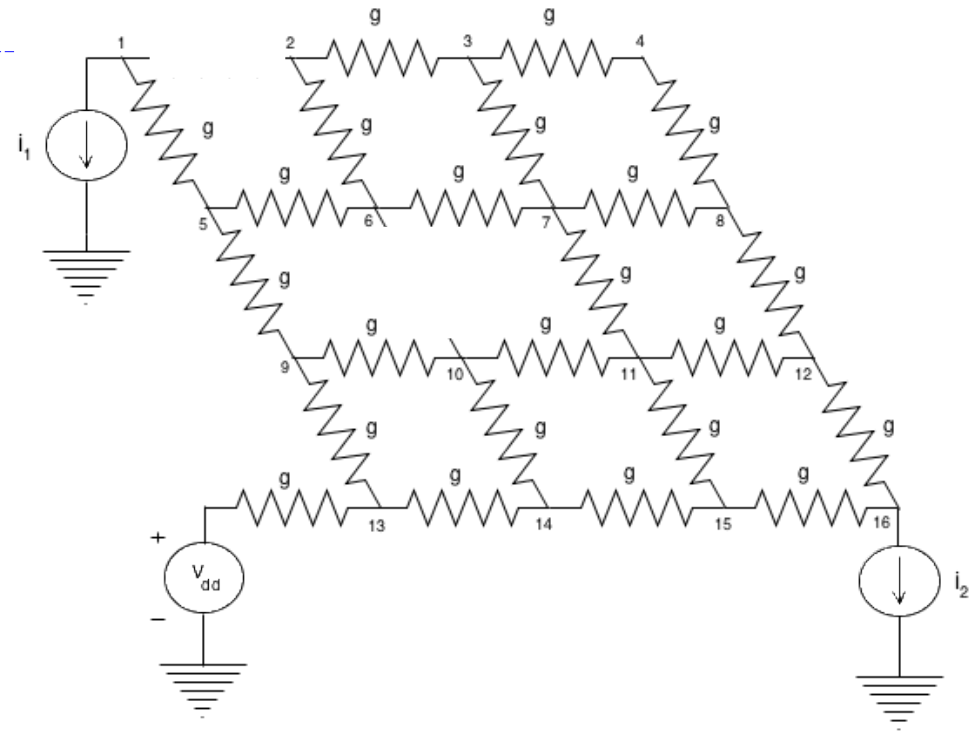

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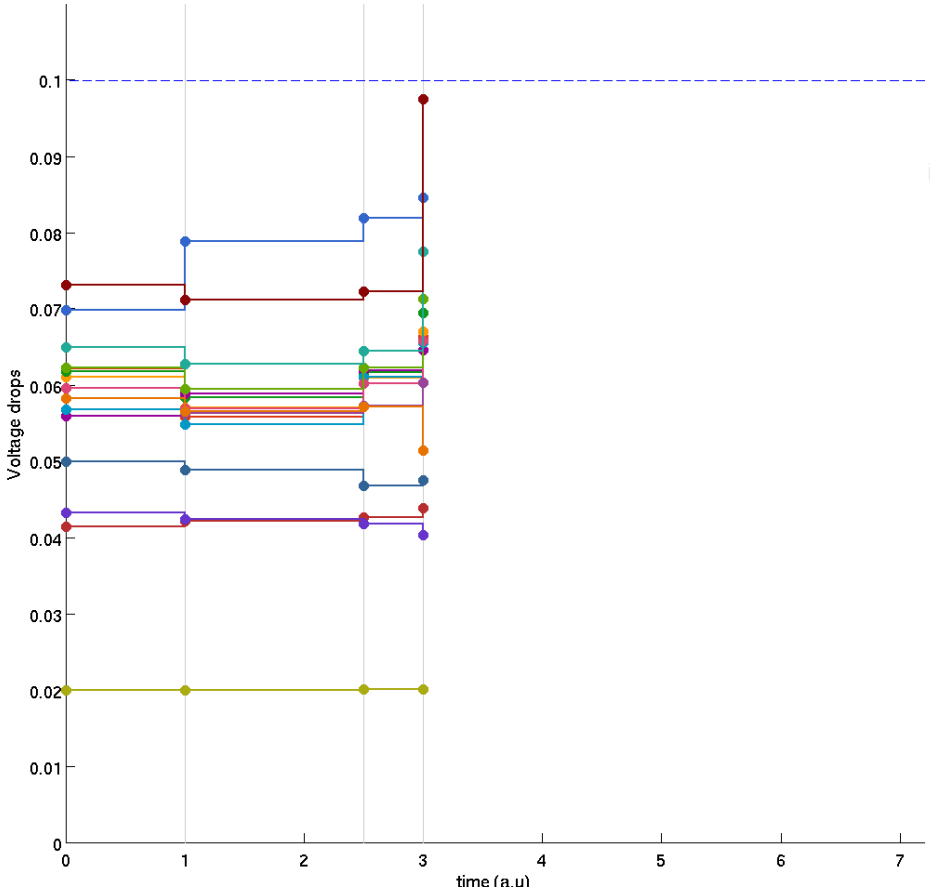


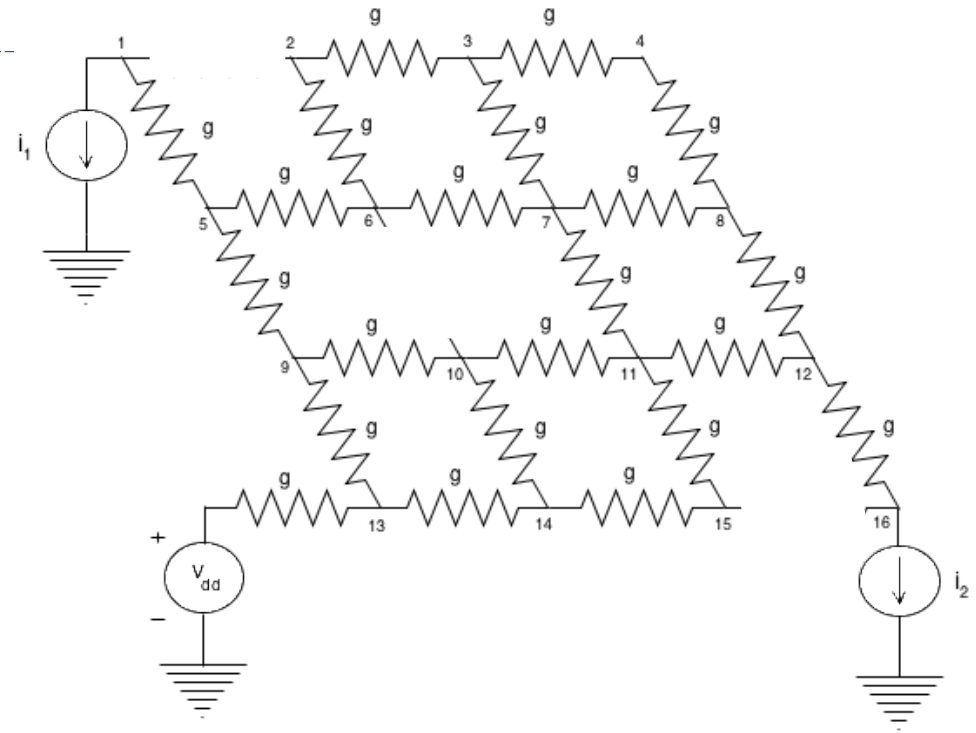

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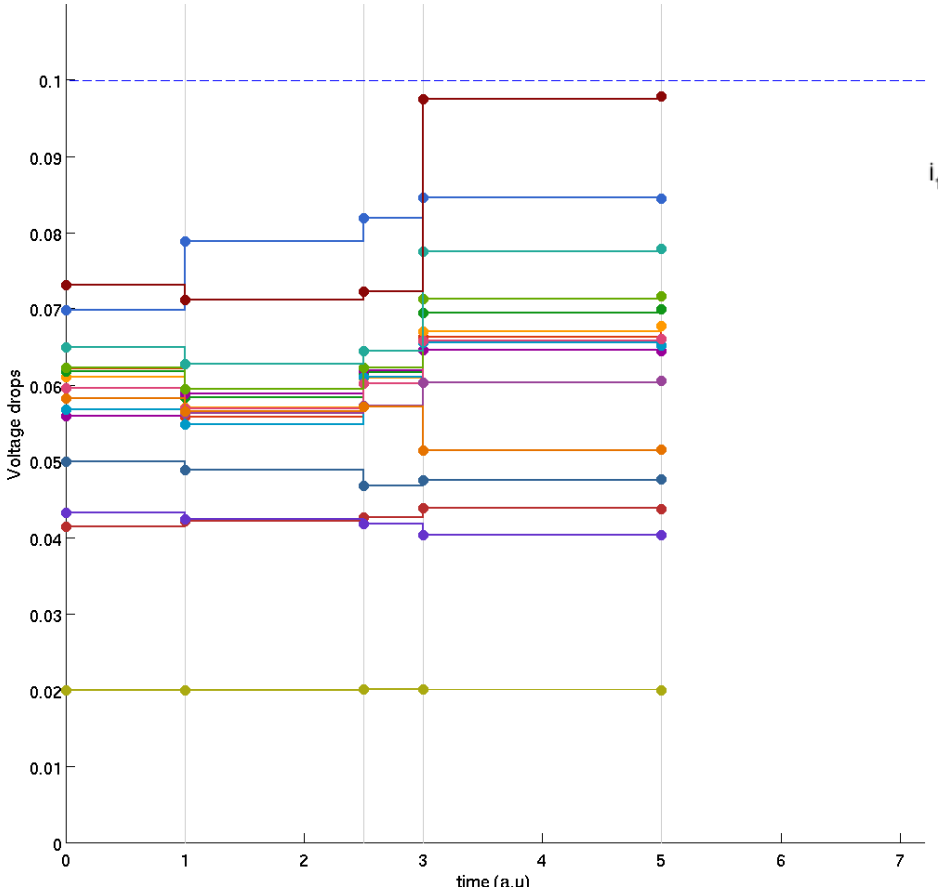


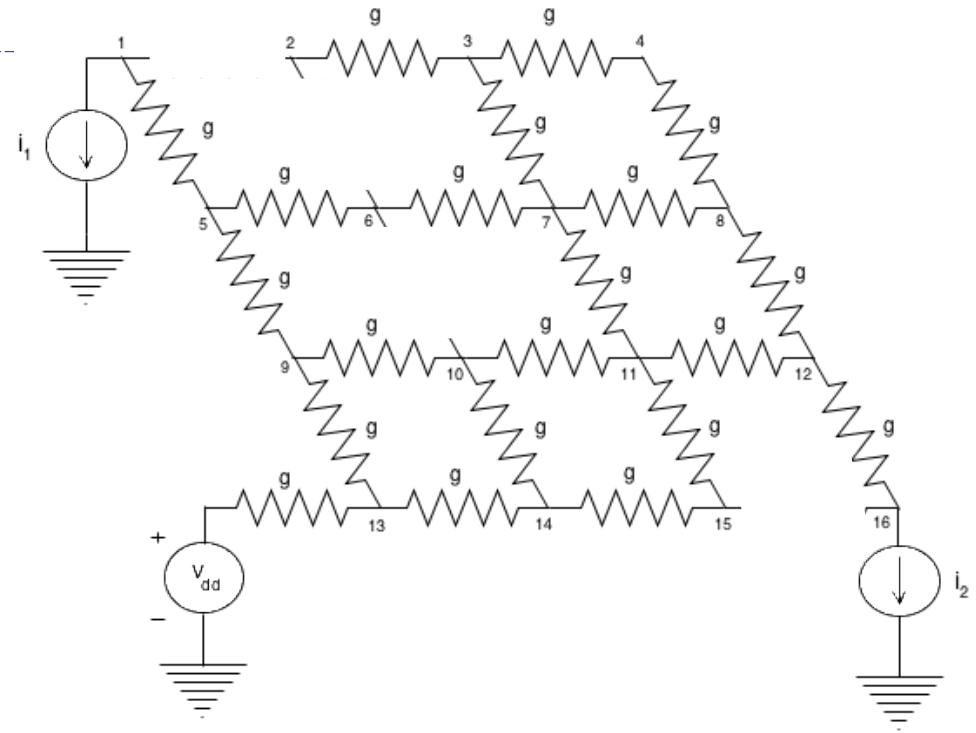

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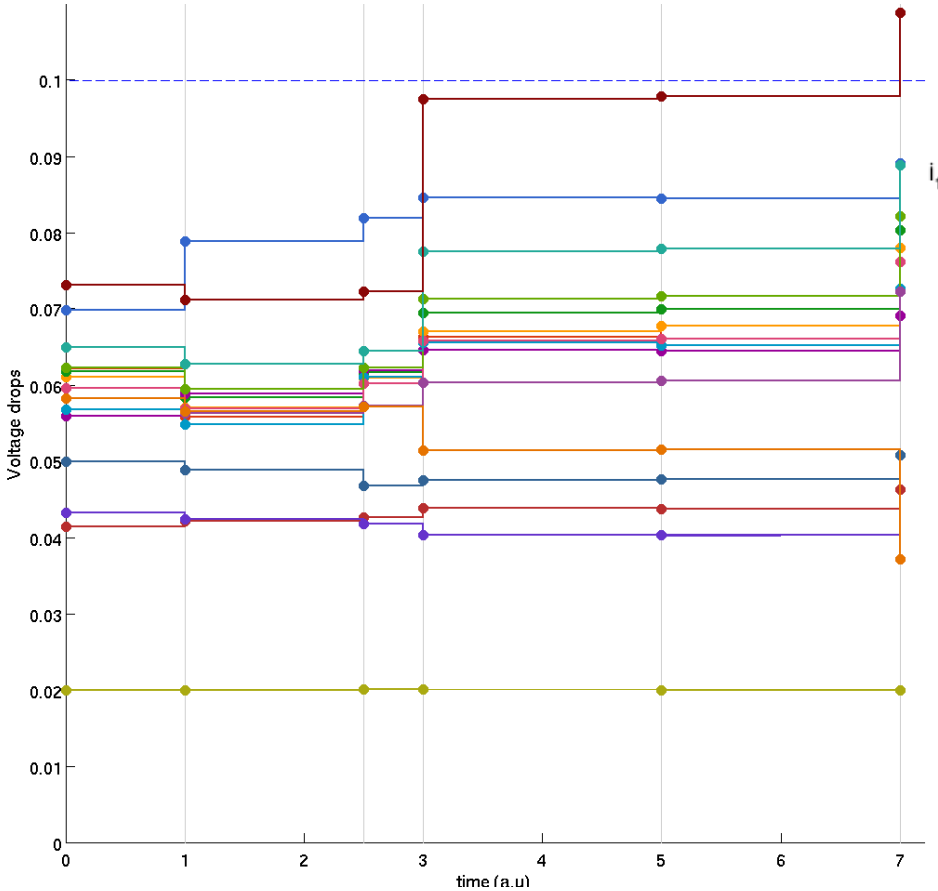
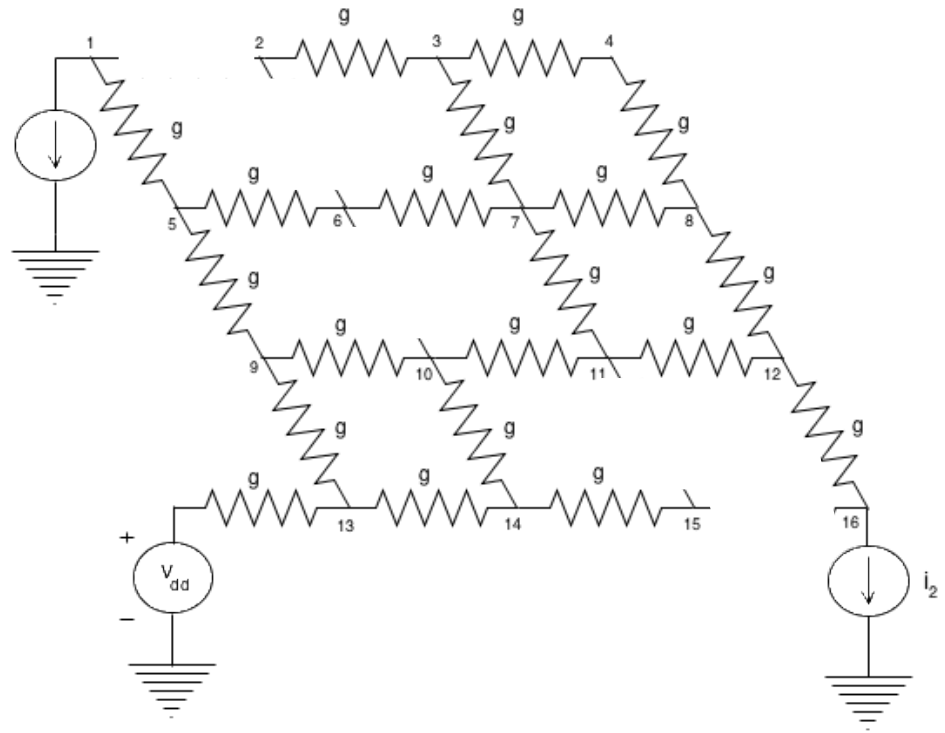



The key feature is that a grid is deemed to have failed, not when the first line fails, but when the voltage drop at any grid node exceeds a user specification.

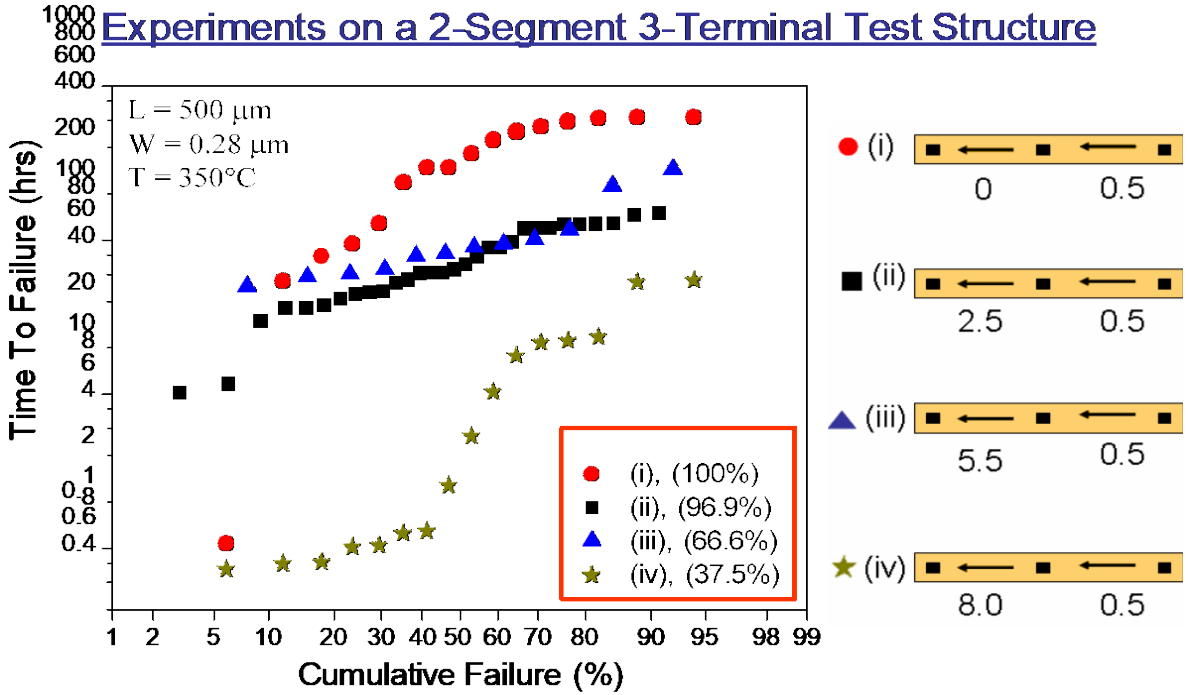
# Problems with Current Approach

- This leads to inaccurate EM prediction during design, sometimes optimistic and often too pessimistic
  - A tree may be deemed immortal if lines are too short (Blech)
  - The grid has redundancy and can survive several line failures
- This calls for significant over-design. However, today, there is very little margin left for electromigration!
- We find that the pessimism is very high: grids that must survive 10 years, are being designed to survive ~40 years. One might think that pessimism is not a bad strategy in VLSI. However, too much pessimism in the power grid can be a big problem. It leads to overuse of metal area, leaving little room for signal routing, which makes EM signoff extremely difficult in modern designs, thus increasing design complexity and design time.
- Traditional empirical models are no longer sufficient and we need better physical models:

  A. S. Oates (TSMC) ""*… it is necessary to include electromigration-induced mechanical stresses in addition to current densities to accurately predict failure of circuit interconnects." In:*

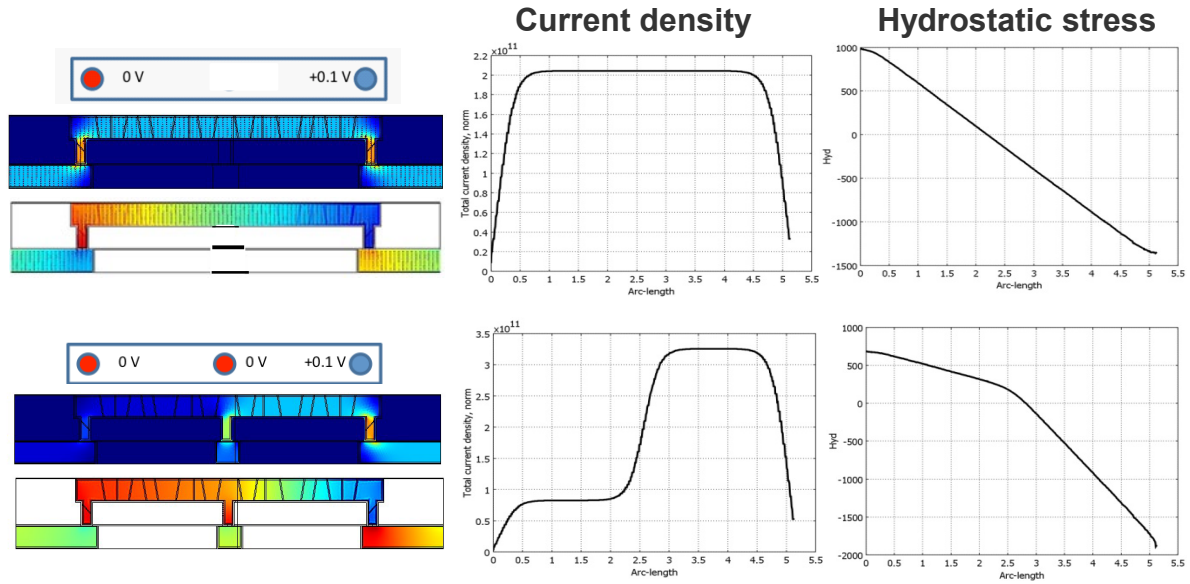
  Interconnect reliability challenges for technology scaling: A circuit focus," in 2016 IEEE International Interconnect Technology Conference, May 2016.

# Experimental proof of role of mass transfer between segments




Most failures occur in the right limb (i-iii), even though the current density is much higher in the left limb.

C. Gan, C. Thompson, et. Al, J. Appl. Phys. 94, 1222 (2003).



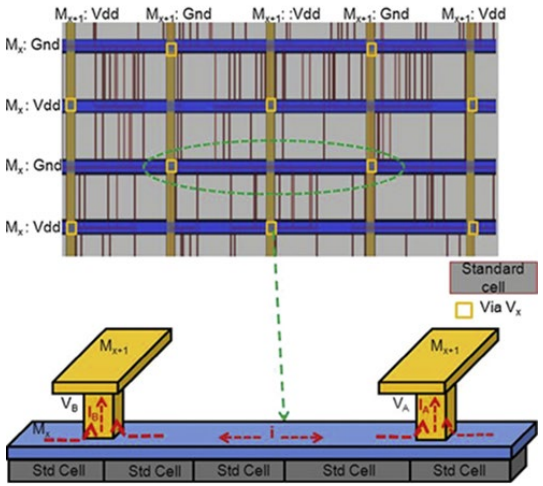

Simulation-based validation.

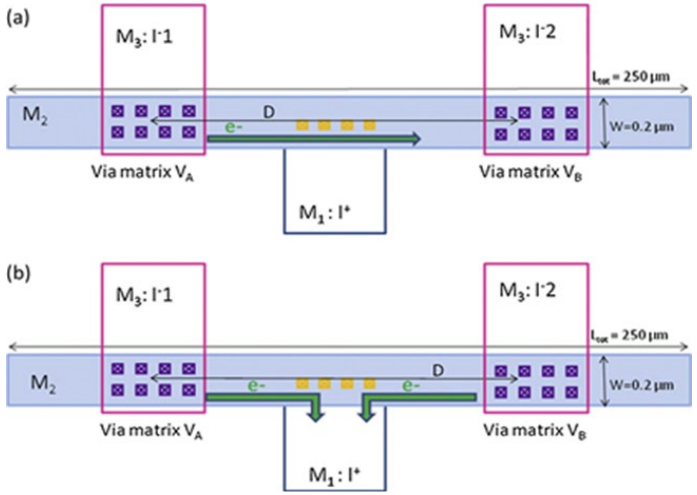
X Huang, T Yu, V Sukharev, SXD Tan, 2014
51st ACM/EDAC/IEEE Design Automation Conference (DAC).

Reservoir effect increasing EM resistance is based on the atomic migration between the links.

# Experimental proof of a role of redundancy in resistance to EM

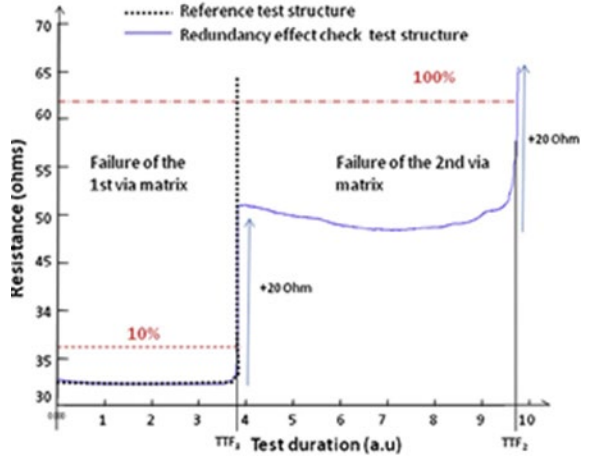
**B. Quattara, L. Doyen, et al., "Power grid redundant path contribution in system on chip (SoC) robustness against electromigration", Microelectronics Reliability, 54 (2014), 1702.**

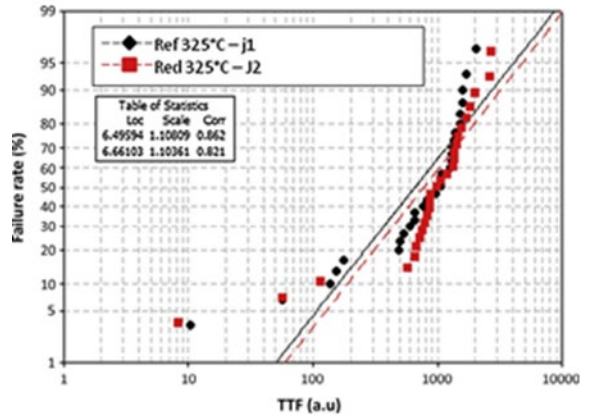



**Reference structure.**

**Redundant structure.**

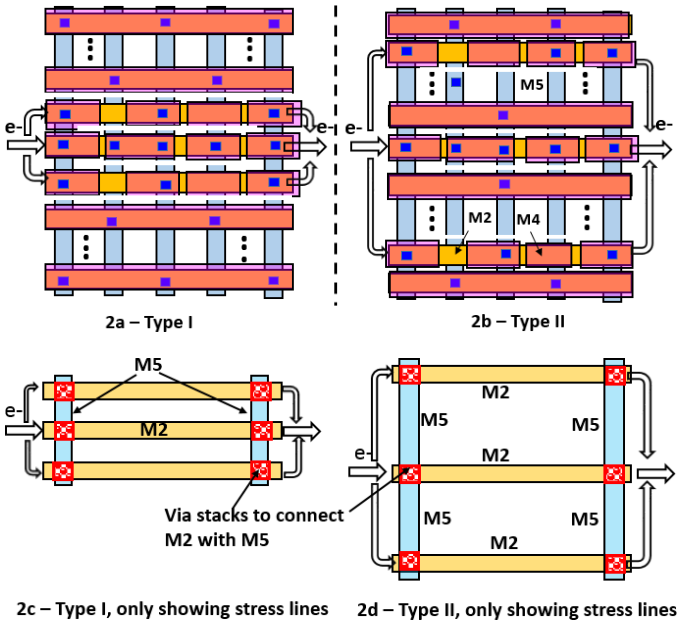


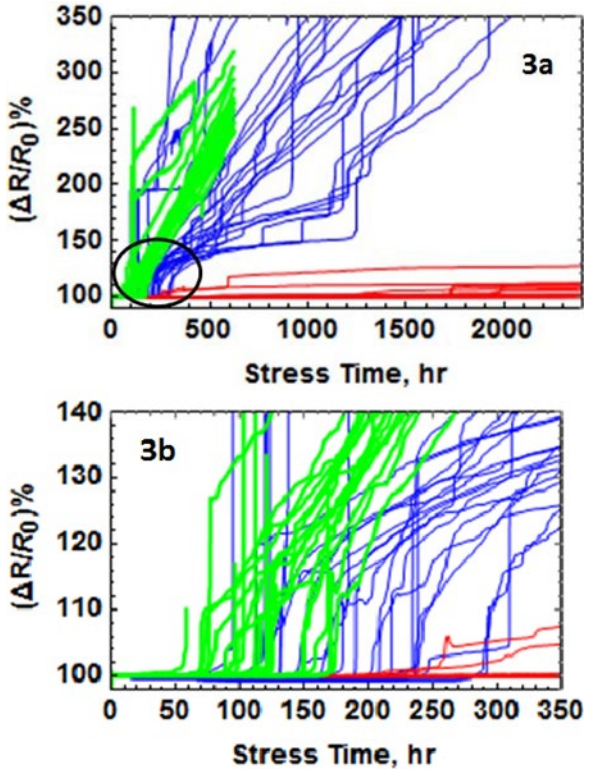

Redundant structure is characterized by two abrupt jumps of resistance, while the reference structure demonstrated just one coincident with the first jump in redundant. Same MTTF are obtained for both structures although the total current in the redundant structure is two times higher.

# Experimental proof of a role of redundancy in resistance to EM

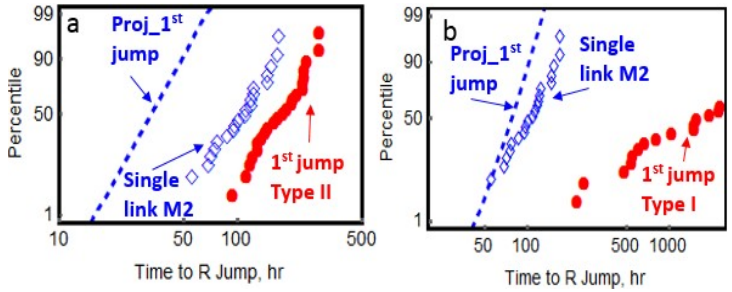
**B. Li, A. Kim, P. McLaughlin, B. Linder, and C. Christiansen, "Electromigration characteristics of power grid like structures", in *IEEE International Reliability Physics Symposium Proceedings*, South San Francisco, CA, 2018, pp. 4F3.1 - 5.**




Schematics of the two EM test structures extracted from a power grid design.




Resistance change vs stress time of 3 EM structures. (3b) is the expansion of early stress time portion of (3a). Red is for Type I, Blue is for Type II of power grid like structures. Green is for a traditional single link V2/M2 EM structure.




Distributions of time to first resistance jump. (a) For Type II and (b) for Type I power grid-like EM structures. Blue diamonds are for single link V2/M2, and solid red circles are for the 1st resistance jumps of power grid like structure Type I & II. The dashed blue lines are the projections of the 1st resistance jumps from single link structures to power grid like structures of Type I & II.

Redundancy doesn't only provide the alternative current paths, but also allows the electric current to redistribute when the EM induced void causes a local resistance increase. The differences in the times to the first resistance drop observed for different types of power grid-like structures is explained by the larger initial current flowing through the central leg and slower current redistribution caused by the growing void in the Type II structure in comparison with Type I.

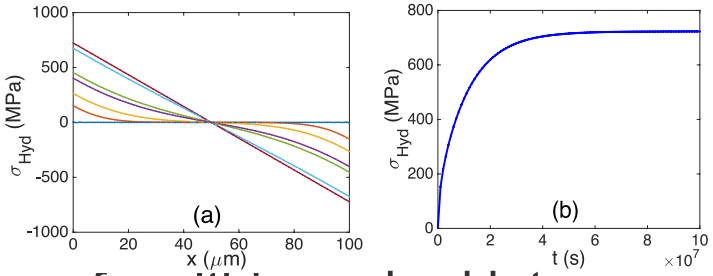
# Bottom Line

- Decomposition of interconnect layout on individual segments and their individual assessment is against the physics of electromigration
- A weak segment approach for P/G grid EM assessment is wrong! The grid has redundancy and can survive several line failures
- P/G grid will fail when voltage variation caused by EM induced resistance increase will exceed a designer specified threshold at any node! It can cause, for example, a timing violation.
- Thus, EM-induced degradation of P/G grid is an IR-drop degradation!
- **A new P/G grid voltage-based EM failure criterion is needed!**

# Korhonen's Model Extended on the P/G Grid

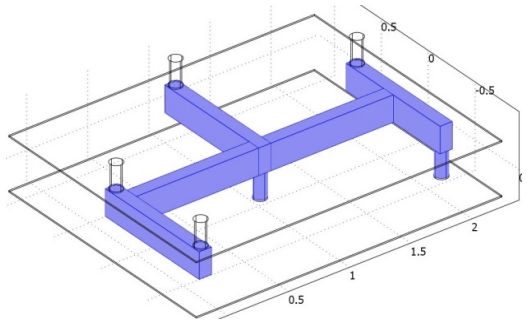
- 1-D Korhonen's model provides EM-induced stress evolution inside single-link interconnect segment:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{D_a B \Omega}{k_B T}\left(\frac{\partial \sigma}{\partial x} + \frac{eZ^* \rho j}{\Omega}\right)\right]$$




Evolution of the hydrostatic stress (a) along the metal line loaded with DC current, and at the cathode end of line, (b) $j = 5 \times 10^9 A/m^2$, T = 400K.

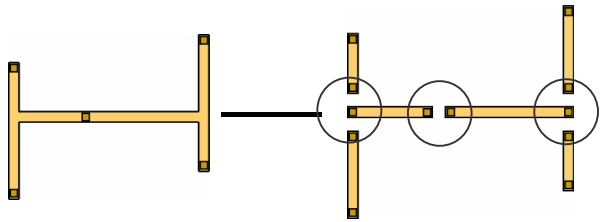
- 1D EM approximation works well in the case of multi-branched interconnect segments, when individual segments are linked by proper boundary conditions.



  - Stress evolution is analyzed in each segment of all interconnect trees, which are the continuously connected conductor metals within one layer of metallization confined by the diffusion barrier liners:

- Interconnect tree; sidewalls and bottoms of the lines and exit vias are covered by metal diffusion liners (Ta/TaN).

  - Solutions of partial-differential equations (PDE) for all branches characterized by different current densities and geometries (length and width), are linking to each other through the BC representing the continuity of stress and atomic fluxes:



Brunch junctions where the continuity BC are applied:

$\sigma_1(L_1, t) = \sigma_2(0, t)$ and $w_1 h_1 J_{a,1}(L_1, t) = w_2 h_2 J_{a,2}(0, t)$

# EM-induced MTTF Analysis: Methodology/Tool-prototype

Novel EM assessment tool-prototype was developed in collaboration with the University of Toronto – Prof. Farid N. Najm

- Applying Korhonen's model at every point, combined with the boundary laws, gives a fully determined system
- Stress evolution PDE:

$$\frac{\partial \sigma_n}{\partial t} = \frac{\partial}{\partial x}\left[\kappa_n^2\left(\frac{\partial \sigma_n}{\partial x} + G\right)\right]$$

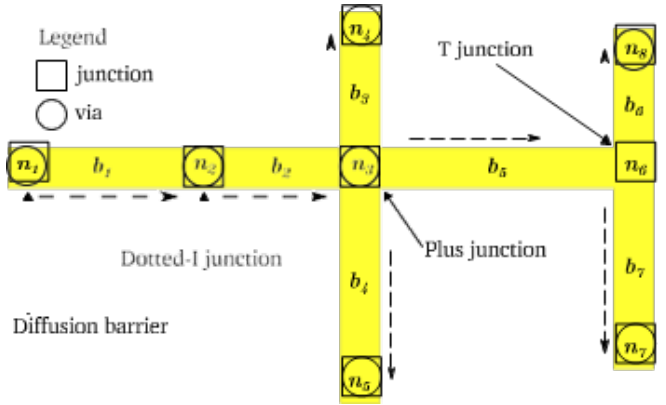
$$\sigma_n(x,t) = \sigma_{n+1}(x,t) \qquad x = x_n, t > 0$$

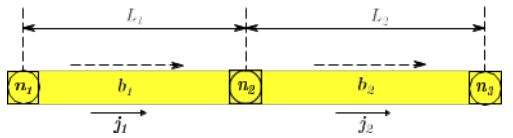
$$\kappa_n^2\left(\frac{\partial \sigma_n}{\partial x} + G\right) = \kappa_{n+1}^2\left(\frac{\partial \sigma_{n+1}}{\partial x} + G\right)$$

- Boundary conditions:

$$\frac{\partial \sigma_1}{\partial x} + G = 0 \qquad x = 0, t > 0$$

$$\frac{\partial \sigma_N}{\partial x} + G = 0 \qquad x = L, t > 0$$



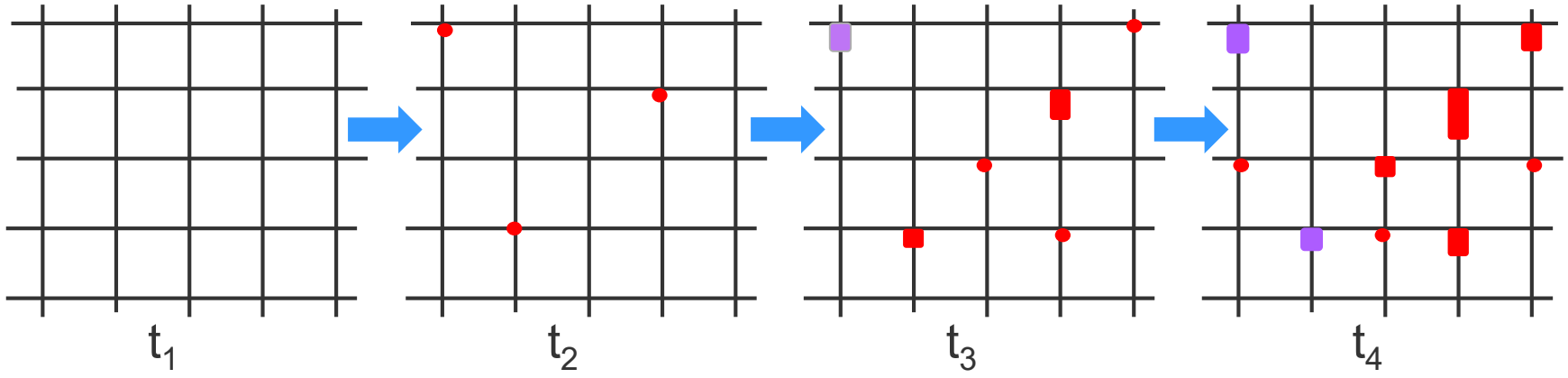
- We discretize this in time and space and solve it to give the stress evolution at every point of interconnect tree

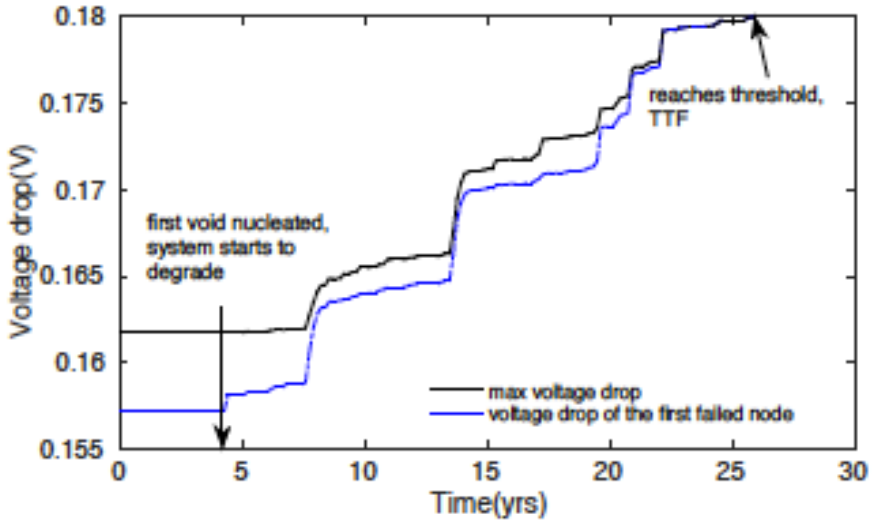
# Novel EM Assessment Flow and Tool-Prototype

- Stress evolution is calculated at each P/G grid segment with correct boundary conditions at the segment ends, which account for the continuity of atomic flow and stress – Extended Korhonen's Model (EKM).
- When stress somewhere exceeds a threshold, a void is deemed to nucleate and the part of a grid (interconnect tree) may be disconnected.
- Simulation is aborted, grid equations rebuilt, grid currents recomputed, and fresh system of stress evolution PDEs are constructed.
- A fresh batch of simulations is started, from the previous state.
- A Monte Carlo loop around all this with new distributions of the atomic diffusivity through all interconnect segments provides the MTTF.

- **Final verification**: check if the designed grid is safe regarding the required life-time with the developed physics-based EM checker employing user provided source currents.

# EM-Induced Supply Voltage Degradation



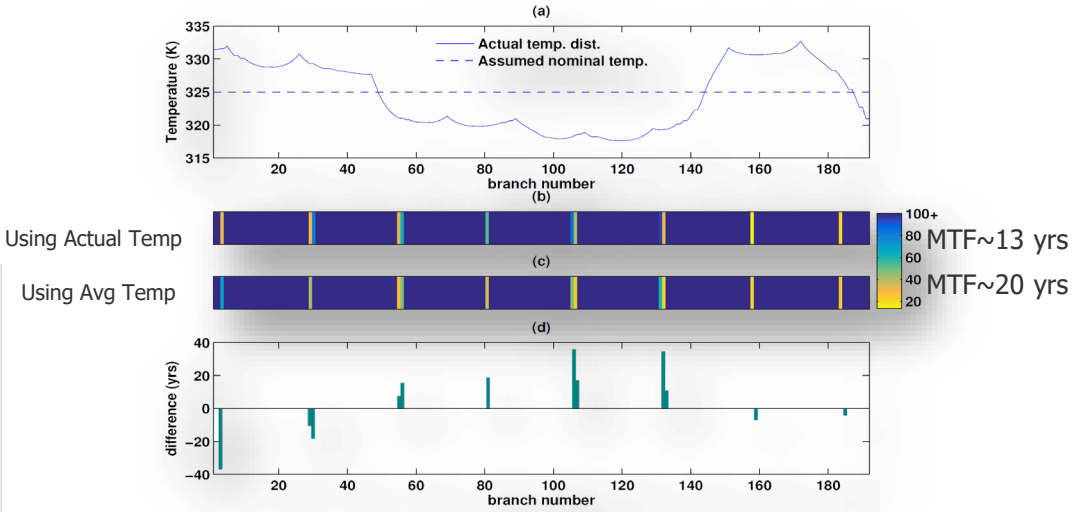




- Nucleated void
- Growing void
- Saturated void

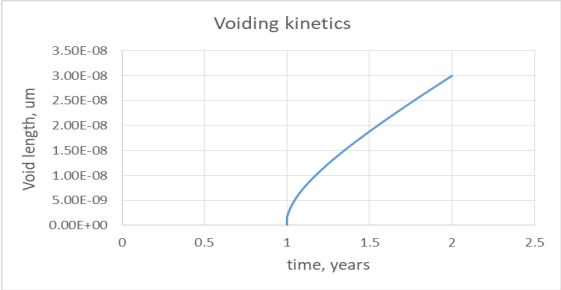
EM induced voltage degradation in IBMPG power net

# Model Enhancements

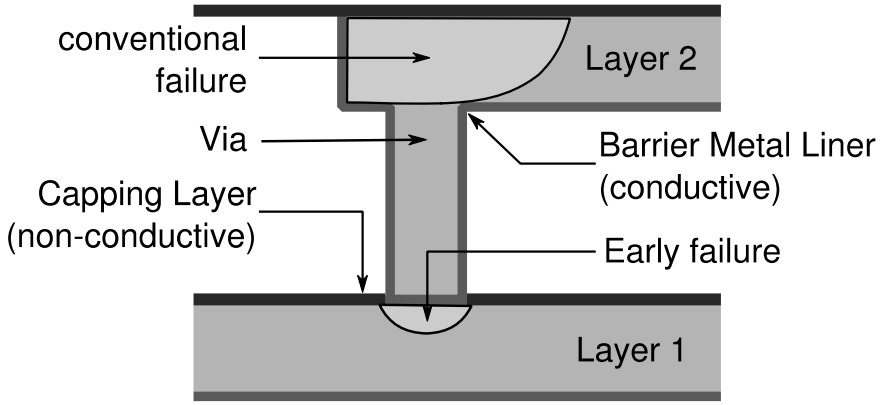
- Effect of temperature on MTF
  - Accounting for the temperature distribution across the metal layers is done by employing a standard compact thermal model that represents a die as array of cuboidal thermal cells with effective local thermal properties.

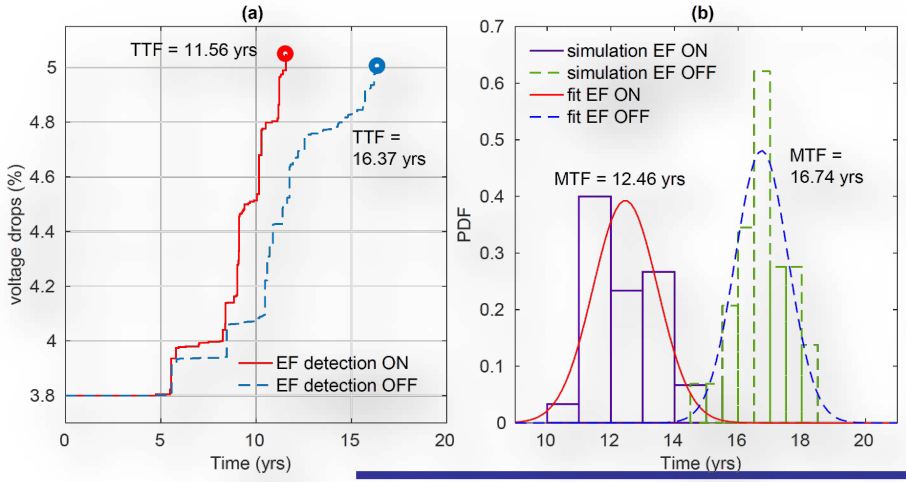



- Voiding kinetics
  - For more accurate simulations, void growth model was implemented: after detecting void nucleation, the tool tracks void length $l_{void}(t)$

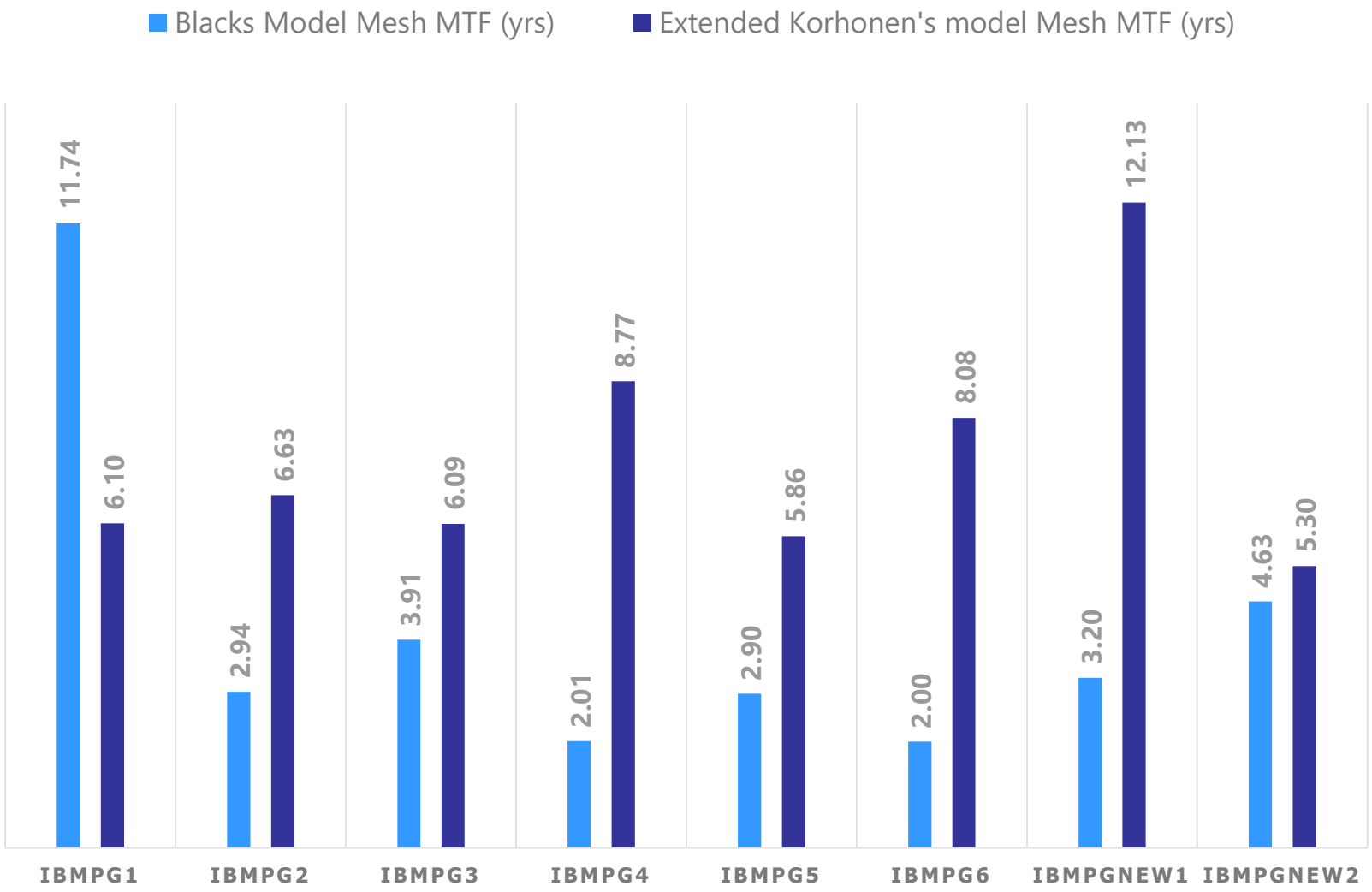



- Early failure
  - A large void right below a via can lead to an open circuit because capping layer is non-conductive: early failures.



# Experimental Results



# Performance

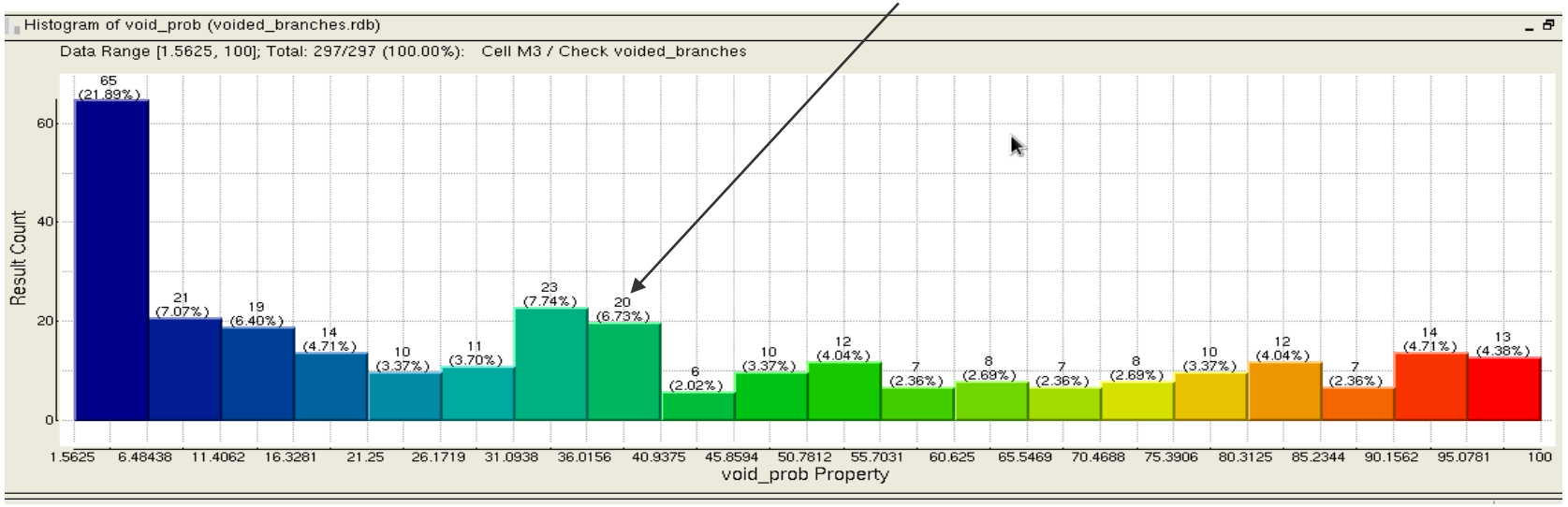
| Power Grids | | | | | Performance |
|---|---|---|---|---|---|
| **Grid** | **# of nodes** | **# of branches** | **# of trees** | **# of current sources** | **CPU time** |
| Ibmpg1* | 6K | 11K | 709 | 11K | 0.6min |
| Ibmpg2* | 62K | 61K | 462 | 61K | 1.2min |
| Ibmpg3* | 410K | 401K | 8.1K | 401K | 4.2min |
| Ibmpg4* | 475K | 465K | 9.6K | 465K | 6.6min |
| Ibmpg5* | 249K | 496K | 2K | 496K | 1.8min |
| Ibmpg6* | 404K | 798K | 10.2K | 798K | 14.0min |
| Ibmpgnew1* | 316K | 698K | 19.5K | 698K | 4.8min |
| Ibmpgnew2* | 718K | 698K | 19.5K | 698K | 3.6min |
| Power Grid1 (65nm) 14.4x12.8 mm | 13.167M | 10.708M | 2.459M | 768 | To add |
| Power Grid2 (28nm) 4.1x6.1 mm | 15.520M | 12.448M | 2.784M | 3.150M | 6.5h |

*S. R. Nassif, "Power grid analysis benchmarks," in *Proc. Asia South Pacific Design Automation Conf. (ASPDAC)* , 2008, pp. 376–381.

# Probability of EM Voiding in Interconnect Wires

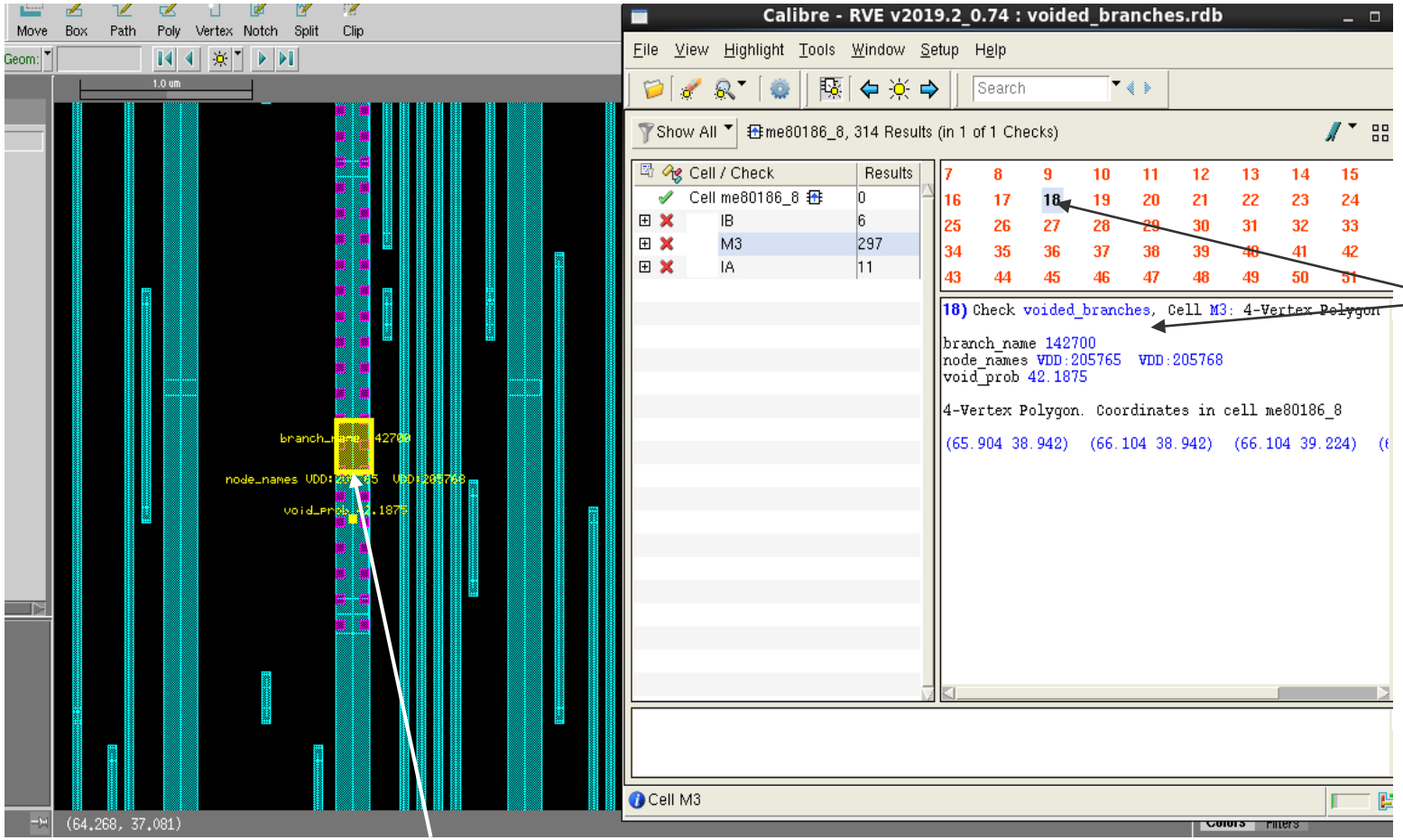
- Void nucleation in a junction requires that EM-induced stress achieved a critical value.
- Due to the dependency of atoms diffusivity on the metal micro-structure, the diffusivity value for different interconnect segments can be different. The location of void nucleation  depends on the distribution of diffusivities in the branches of an interconnect tree.
- Monte-Carlo approach allows to study the random distribution of diffusivities in wires, and to estimate the voiding probability for branches of the simulated interconnect trees.
- Each Monte-Carlo experiment provides a list of all voided branches. The lists of voided branches, generated by all performed MC iterations, allow to get voiding statistics (i.e. the voiding probability for each branch). This information is visualized in Calibre RVE.

For 20 branches voiding probability is in the range ~36 – 41%; this is 6.73% of total number of branches in M3 layer for which voiding was detected (297)




https://www.mentor.com/products/ic_nanometer_design/verification-signoff/physical-verification/calibre-rve/

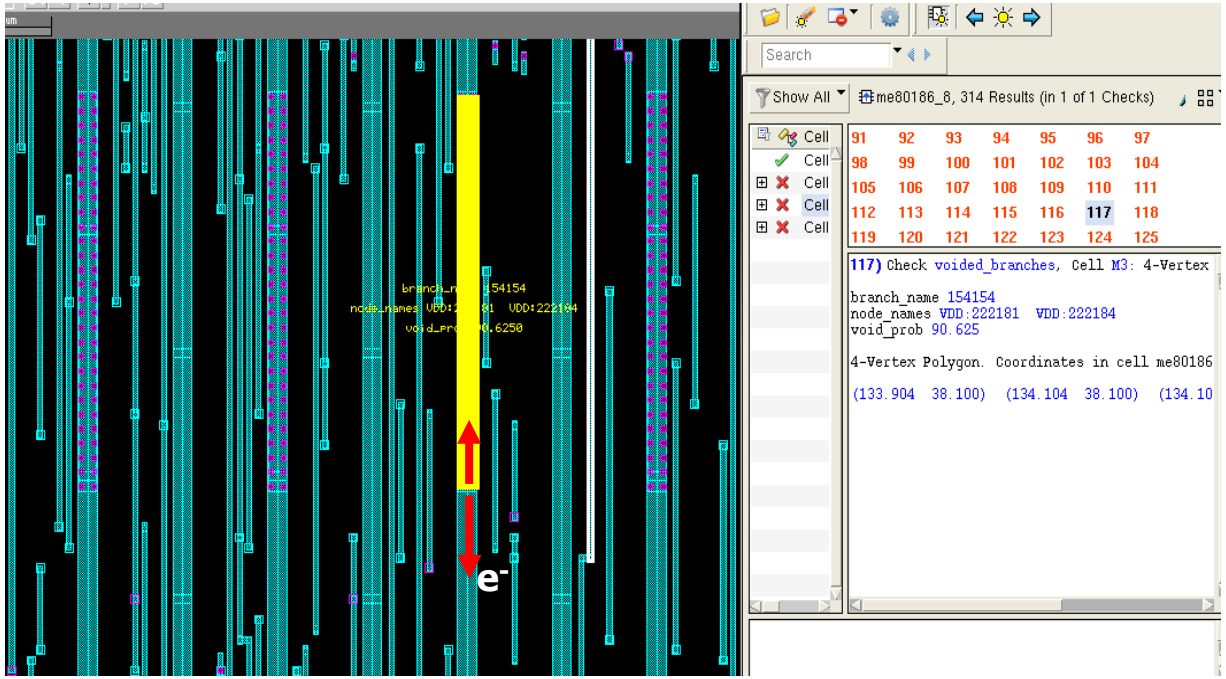
# Voided Branch Information in CalibreRVE and Visualization



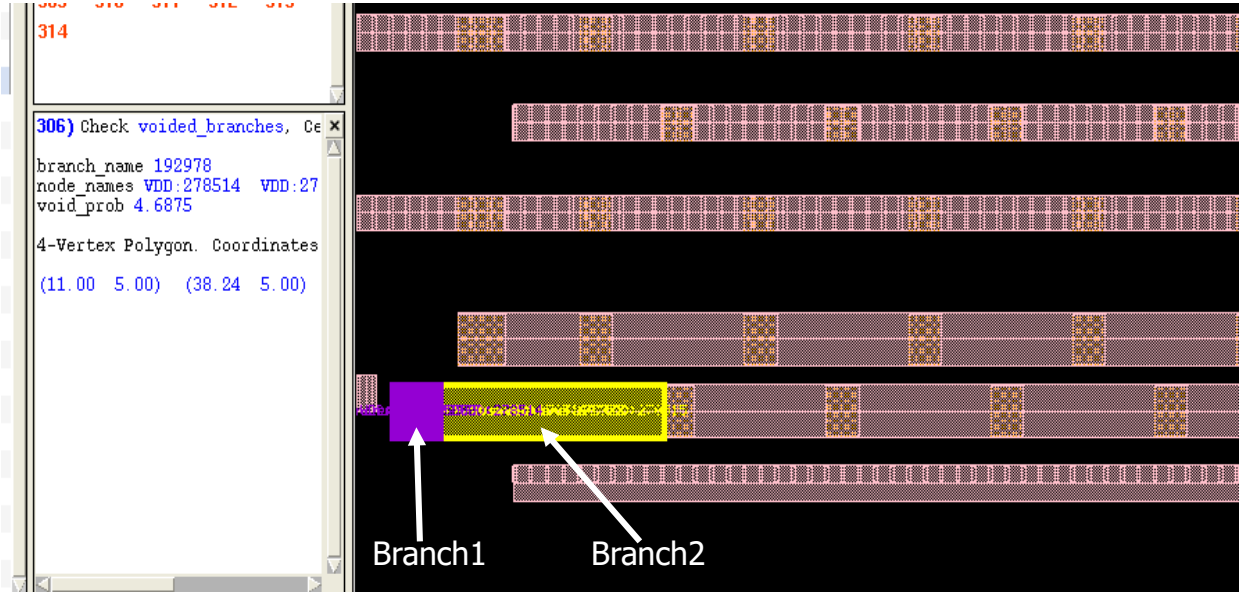

**Info of voided branch #18: name, nodes, voiding probability**

**Voided branch in M3 layer highlighted in design**

# Examples of Voided Branches



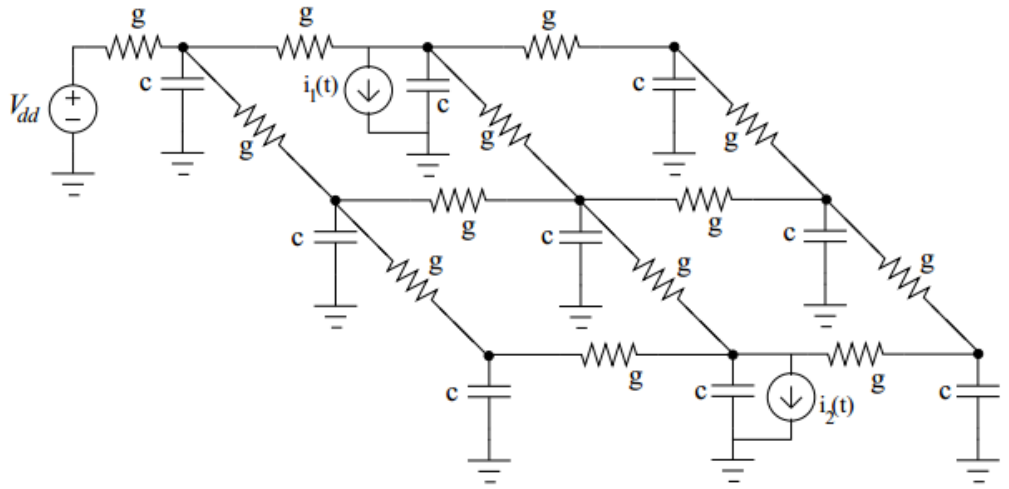

High voiding probability (P=90.625%) in the highlighted branch is due to high current inflow.




- For Branch1 voiding probability is 76.56%, for Branch2 – 4.69%.
- For Branch2 voiding occurs in few experiments, when very low diffusivity in Branch1 prevents the atoms outflow from this branch.

# Developed Physics-Based EM Assessment

- Given:
  - Power Grid (DC, RC, or RLC netlist)
  - Tolerance for grid node voltage fluctuations ($V_{th}$)
  - Effective DC for block currents
- Find:
  - Evolution of the voltage drop variations on the grid caused by EM induced segment resistance growth



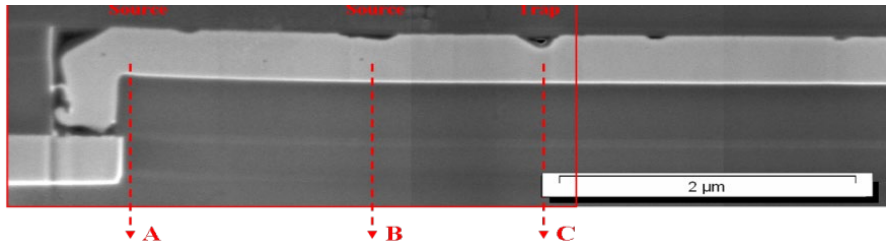

- Features:
  - Based on user-provided source currents
- Results:
  - Power Grid Mean Time to Failure (MTF)
  - There are many improvements in performance, power, time-to-market and design cost that become possible if the developed physics-based EM checking is used.
- **FORWARD EM ASSESSMENT PROBLEM IS SOLVED!**

# Novel Characterization for Tool Validation/Calibration

- Acceptance of the developed technology will allow to avoid and in the perspective to remove the over conservative foundry-based current design rules, which can help to extend a technology-node life-time!
- But before a validation and verification of the proposed methodology should be done.

To reach this target, we propose to use an approach combining the traditional failure analysis methods with the measurements of voltage degradation and temperature variation by embedded voltage/temperature sensor circuits.

- Demonstrated above capability of the tool toward predicting the locations of void nucleation sites and void growth can be utilized for **postmortem SEM studies**.
  - A number of samples containing the pieces of interconnect with voided segments could be cut of the chip. Then, the samples should be cut parallel to the test structure of interest in a distance of about 20 µm. The final cross-section for the *in-situ* SEM investigation should be prepared by focused ion beam (FIB) milling. Approximately 50…100 nm of the dielectric material surrounding the metal line should be left over in front of it. With this procedure, all voids will be remained in the segment.



A. Kteyan, V. Sukharev, et al. AIP Conference Proceedings **945**, 42 (2007)

- The **process, voltage, and temperature (PVT) sensors*** can be used for high accuracy, low power measurements of the temperature variation and voltage degradation in interconnect p/g grid.
  - Comparison between the measurement results and the predicted temperature and voltage will allow to calibrate the tool by adjusting some of the model parameters.

*S-W Chen, M-H Chang, et al., Proc. 2010 IEEE Int. Symp. on Circuits and Systems.

# Conclusion

- **For many decades, EM checking for complex metal structures under realistic currents has been unavailable!**
  - Only option has been the venerable but limited Black's model.
  - We have been missing the ability to handle:
    - Dynamics of failure over time, how it is impacted by stress in the metal around it, how it depends on the current dynamics, etc.
- **With an accurate 1D physical model, extended to large metal structures, we can properly deal with EM damage**
  - We can simulate it, much like familiar circuit concepts like voltage and current.
- **We have integrated this new knowledge into the design tool. We have made a first step in that direction.**
  - Availability of the sensor measurements will allow us to decide which additional model enhancements should be implemented and which shouldn't to minimize the increase of the numerical complexity.
  - New additional physical model enhancements are planning:
    - Implementation of a random nature of the critical stress.
    - Implementation of microstructure into each grid segment with reduced node counts based on analytical solution for the stress evolution kinetics.
    - Implementation of the effective bulk modulus variability (look-up table).