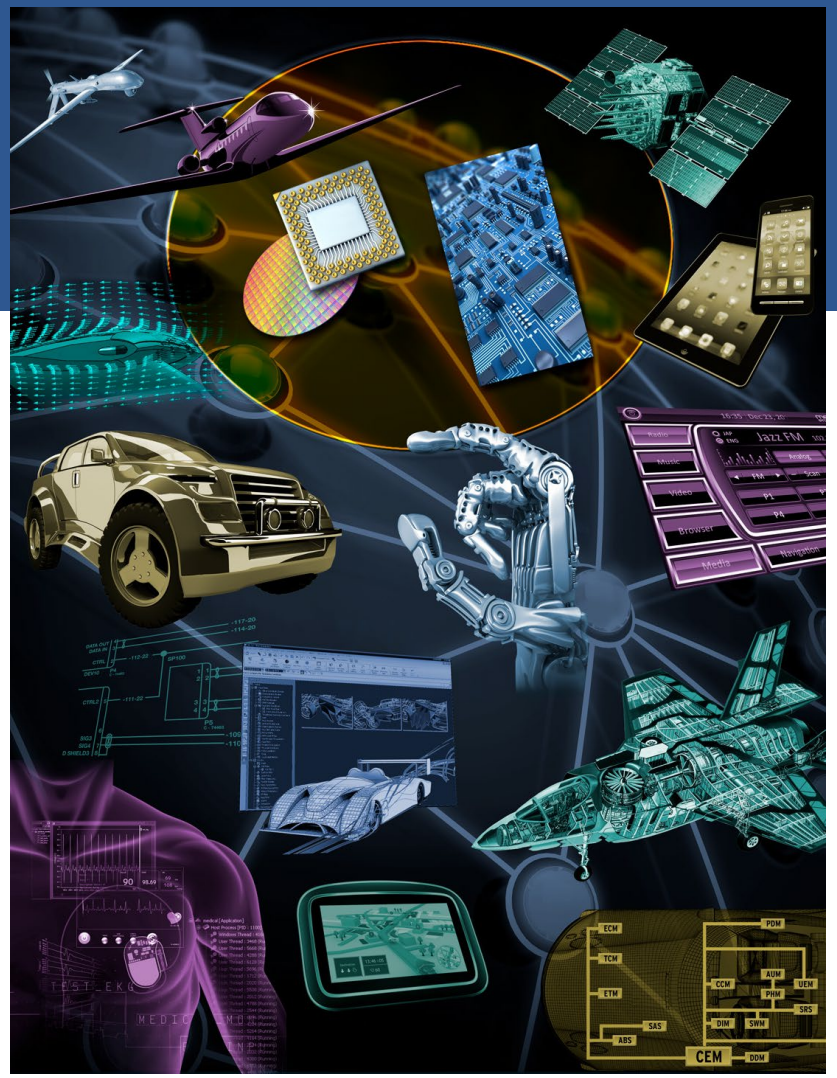


Simulation-based Metrology for Intra-layer and Inter-layer Hotspots

John Sturtevant

FCMN 2019

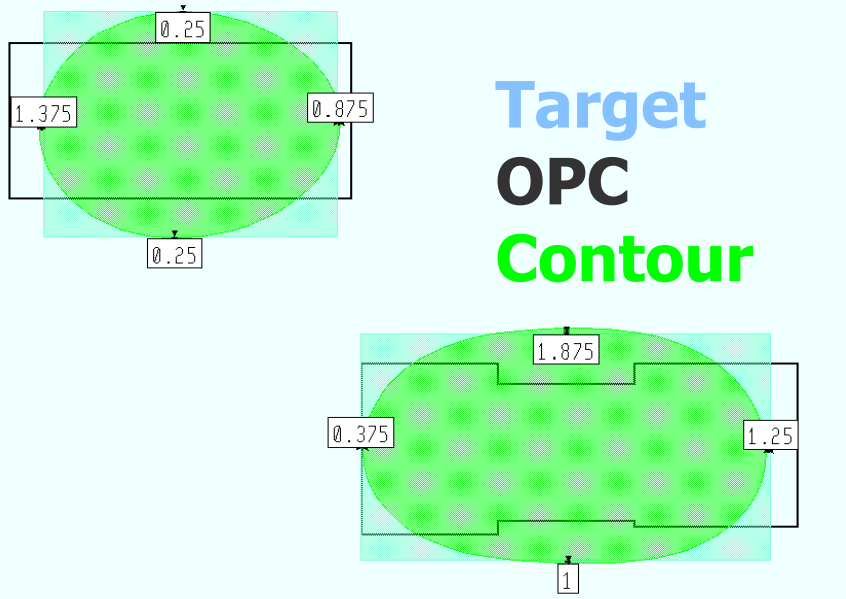
April 3, 2019

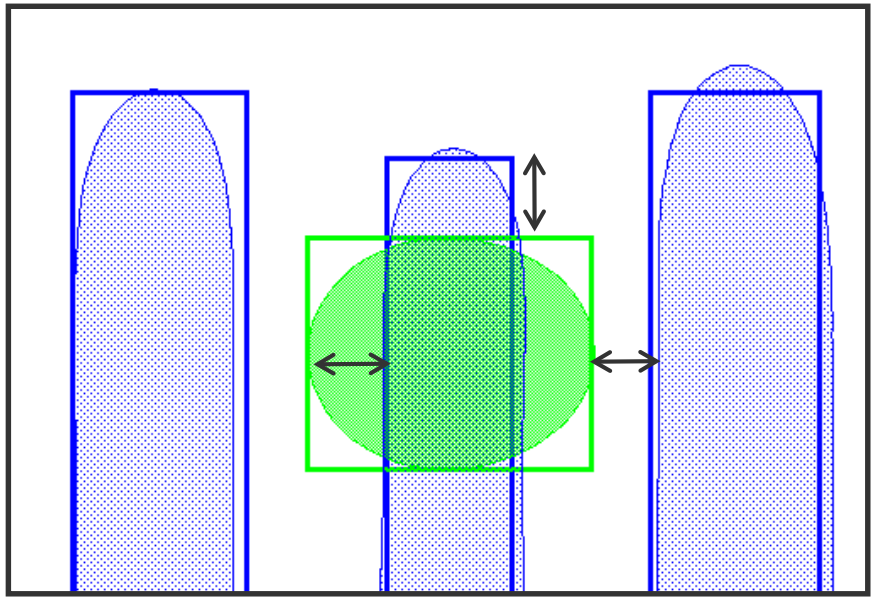
20 YEARS
Calibre: OPC Leadership 1999-2019

Mentor®
A Siemens Business

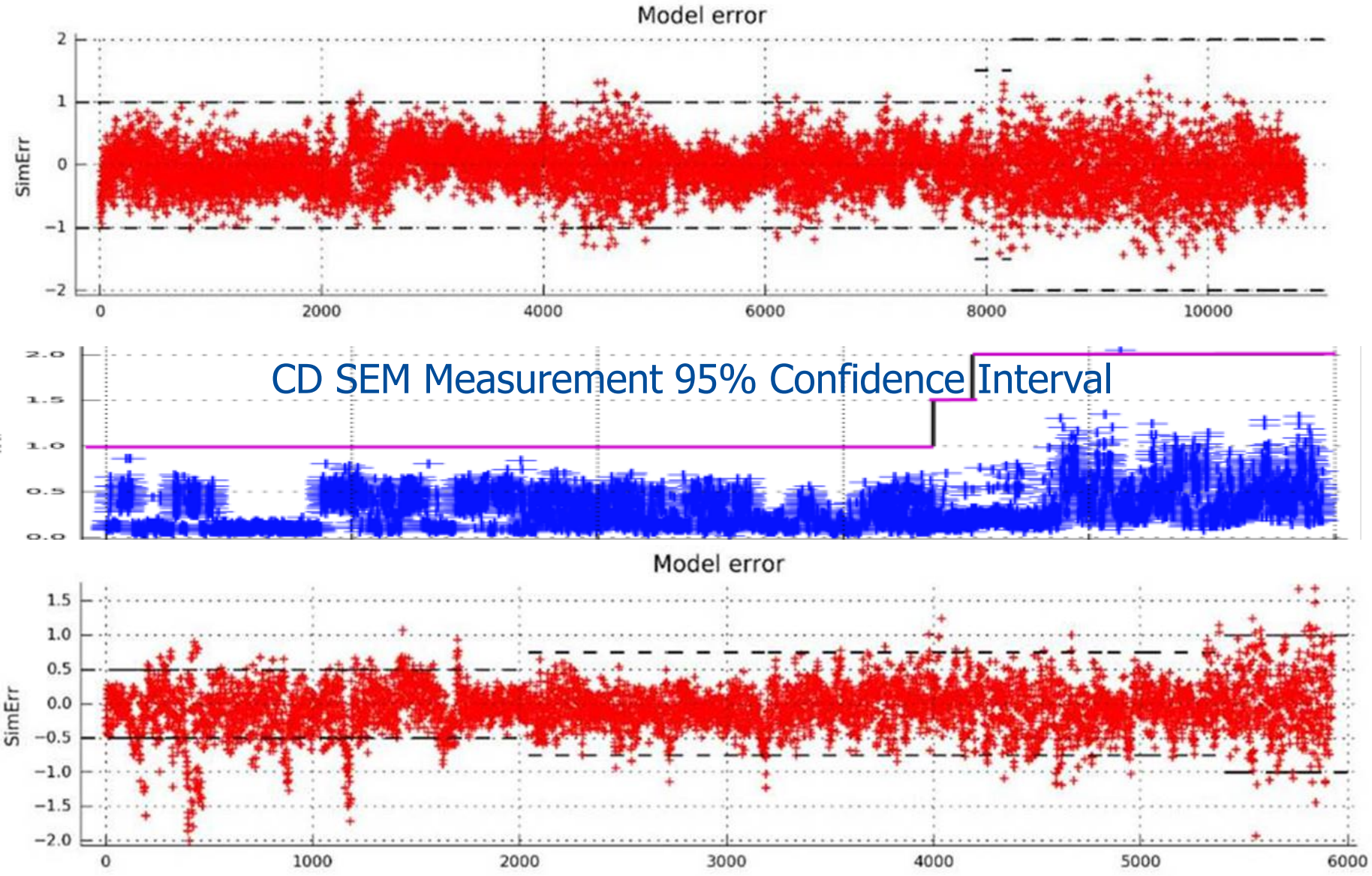
Edge Placement Error (EPE)

- **Simulation**: EPE = {Simulated contour– design target}: Can account for multiple sources of placement error.
  - — Intra-layer EPE
  - — Inter-layer edge placement between critical segments of two or more layers.
- **Fab**: EPE = {Wafer contour edge – design target edge}
  - — Intra-layer EPE not (easily) directly measurable,
  - — Inter-layer edge placement errors: can measure critical edge to edge distances.





Excellent Model Accuracy to CD SEM meas on large diversity of patterns (N3 EUV, min CD ~ 20 nm)



Case 1:
RMS = 0.35nm
99.7% in spec
Range = 3nm

95% CI (~ 2 ($\sigma/\sqrt{n}$)

Measurement Uncertainty

Case 2:
RMS = 0.34nm
94.4% in spec
Range = 3.7nm

Simulation-based metrology augments the value of real wafer metrology

- Guide judicious inspection of Intra-layer, Inter-layer hotspots through simulation of global DC offsets of input parameters.
  - Identify specific potential hotspot locations to guide e-beam metrology
  - Characterize process windows, which can in turn be used to estimate die failure probability
  - Determine Best Focus through simulation
  - Full-chip edge-placement simulation-based metrology accounting for EUV aberrations across multiple scanners
- Inform simulations with spatially-specific dose, focus, mask CD, overlay data from tool diagnostics and (sparse/dense) metrology data: Generate full-chip, full-wafer simulation-based metrology with multiple possible applications.

The evolution of lithographic "Process Window" characterization *(for measured or simulated data)*

- Bossung plot: (*Bossung, Perkin Elmer 1977*) Per feature CD as f(Z, E)
- ID/ED tree / forest: EL vs DoF (*Lin, IBM 1980, 1993*)
  - — *"+/- 10% CD"*
- PWA -> *Mack, PROLITH 1995, Mansfield et al. IBM 2000*): Per feature or multiple features (cDoF)
- Optical Rule Checking "ORC" (*SONY 2001*)
  - — Full-chip image metrics (**EPE**, ILS, I_{max}, I_{min}, MEEF, … DoF)
- pv-Band (*Torres, Mentor Graphics 2005*): Full-chip contour vs dose, focus, mask CD *or any other variable*

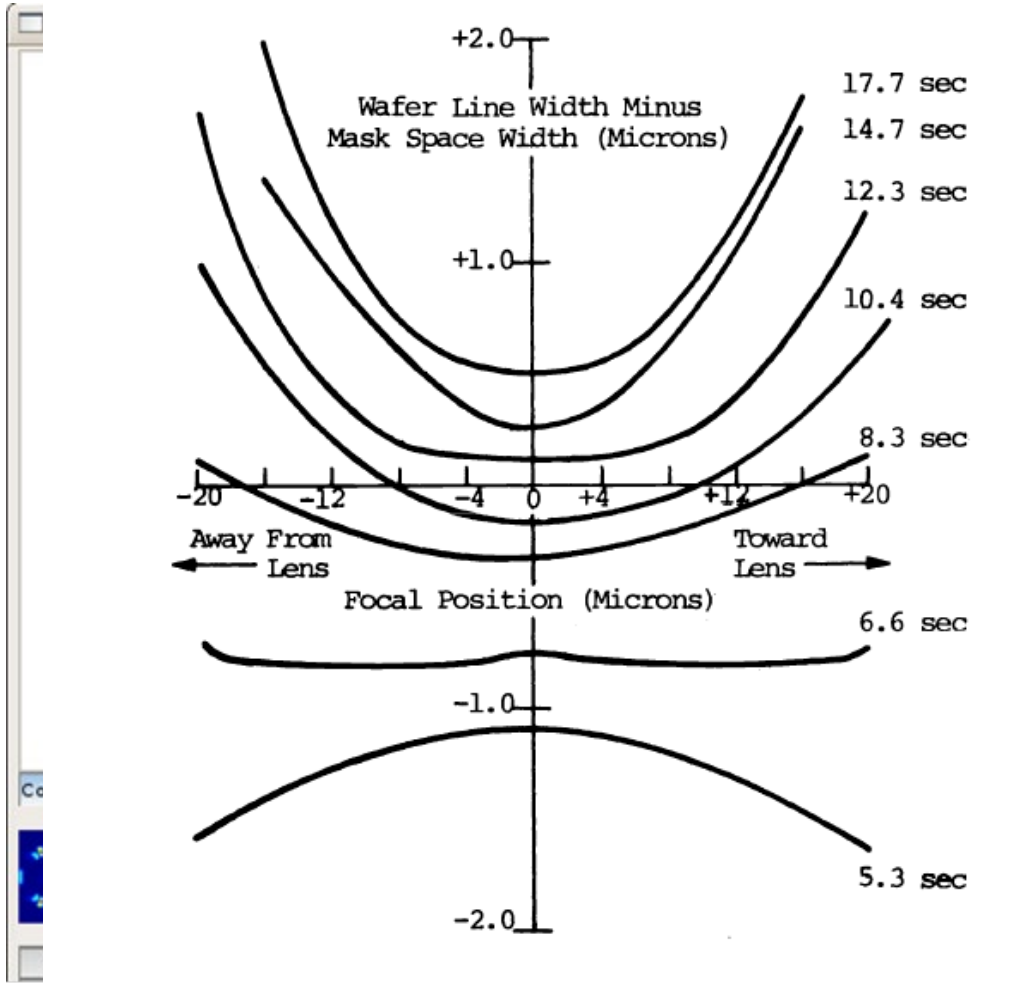
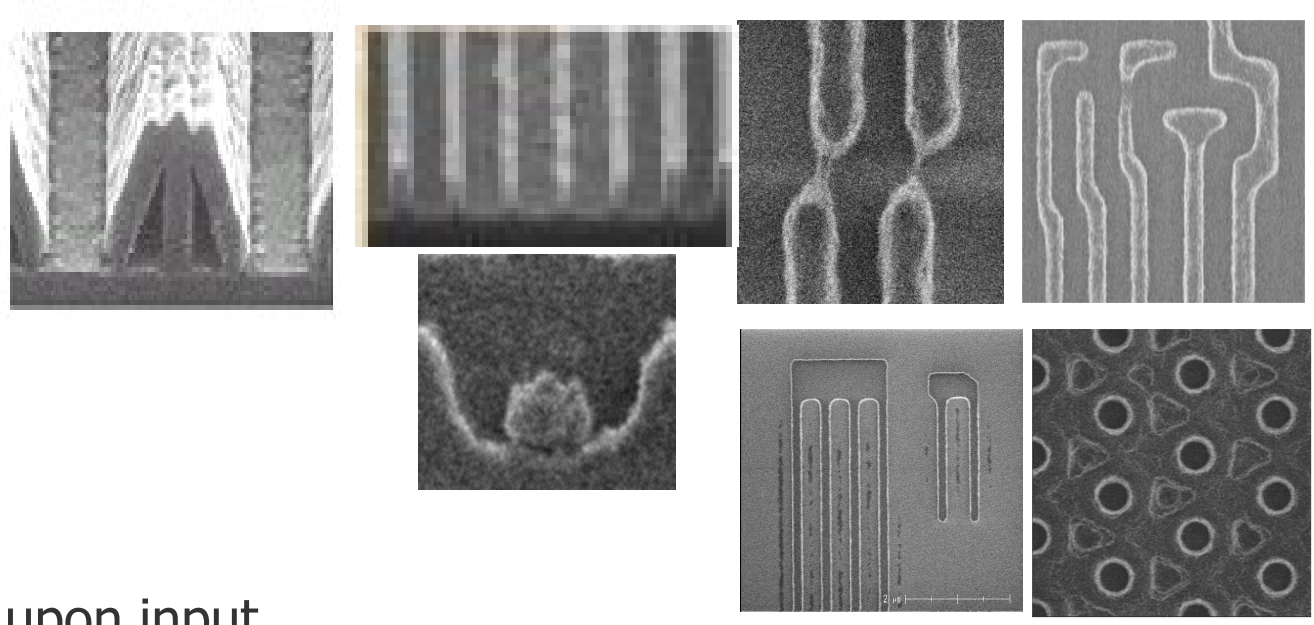
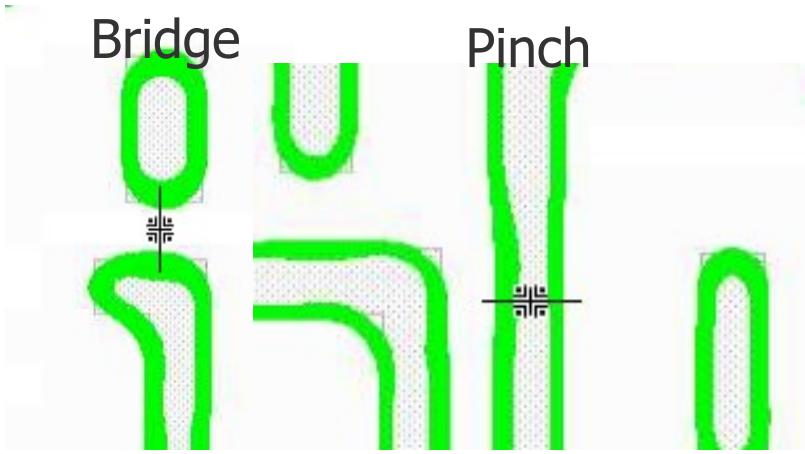


Fig. 5. Focal Position Versus Line Width Size for Various Exposure Values

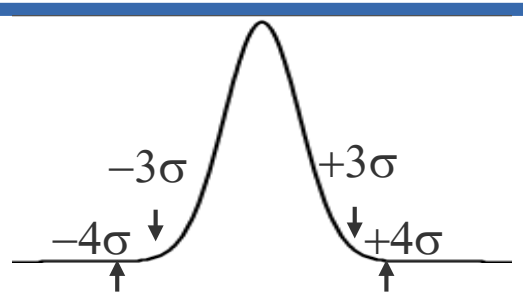
Simulation of Pattern Failure (aka “Hotspots”)

- Intra-layer
  - Pinch, Bridge, Pattern Collapse, SRAF printing, PR Toploss
- Inter-layer
  - Insufficient overlap, bridging
- Deterministic simulation
  - Failure mode-specific 3D models
  - Through process window dependence
  - Failure probability calculation depending upon input parameter variability and number of patterns within chip
- Stochastic simulation
  - Failure probability (ie microbridge or missing via) depending upon stochastic model
- Combined deterministic and stochastic simulation
  - Overall failure probability due to input parameter variation and stochastics

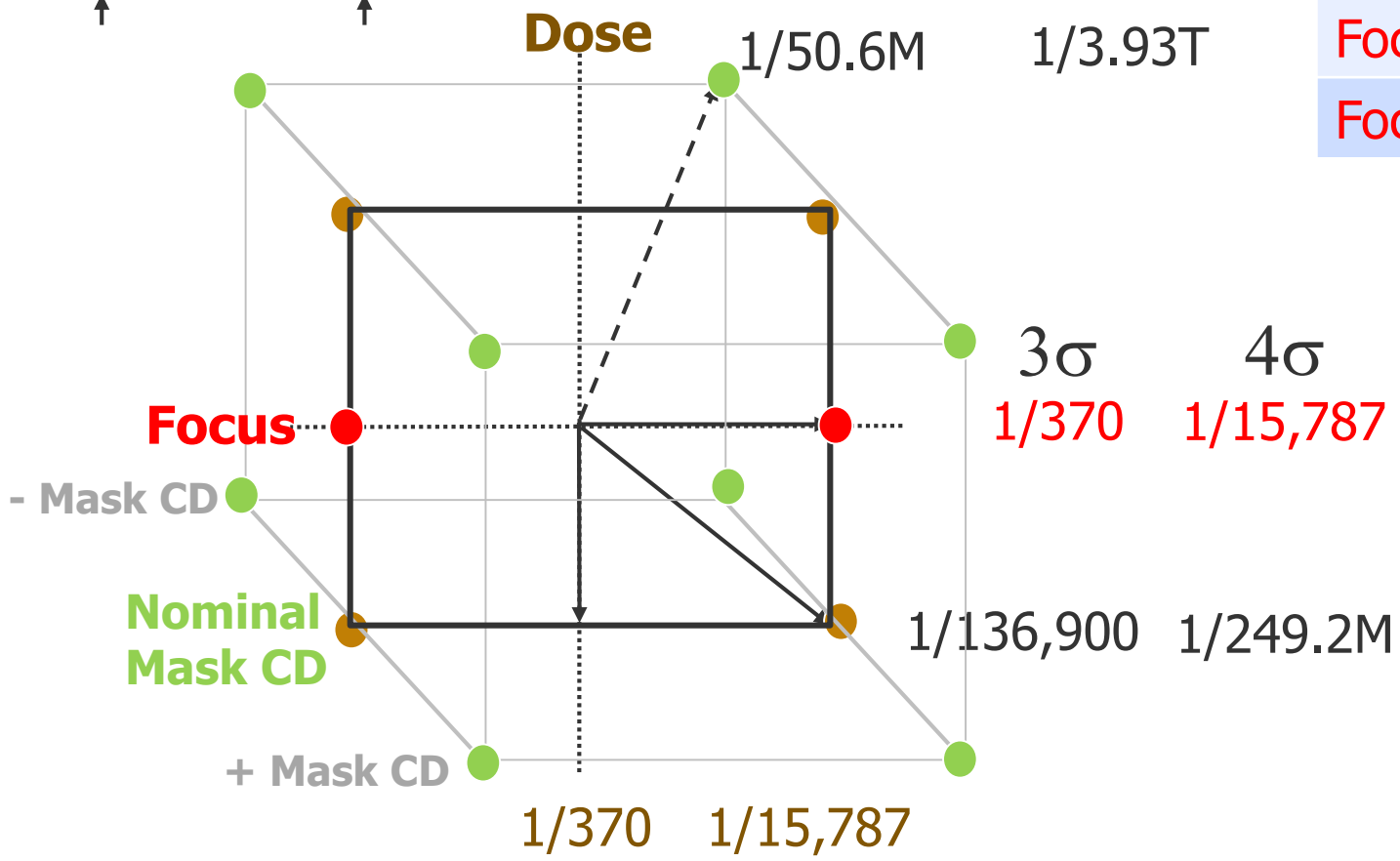




Beyond 3σ: proper variation in dose/focus/mask CD to consider, relative to overall mfg variability



50 nm x 50 nm "sites"
100mm² die ~ 40B



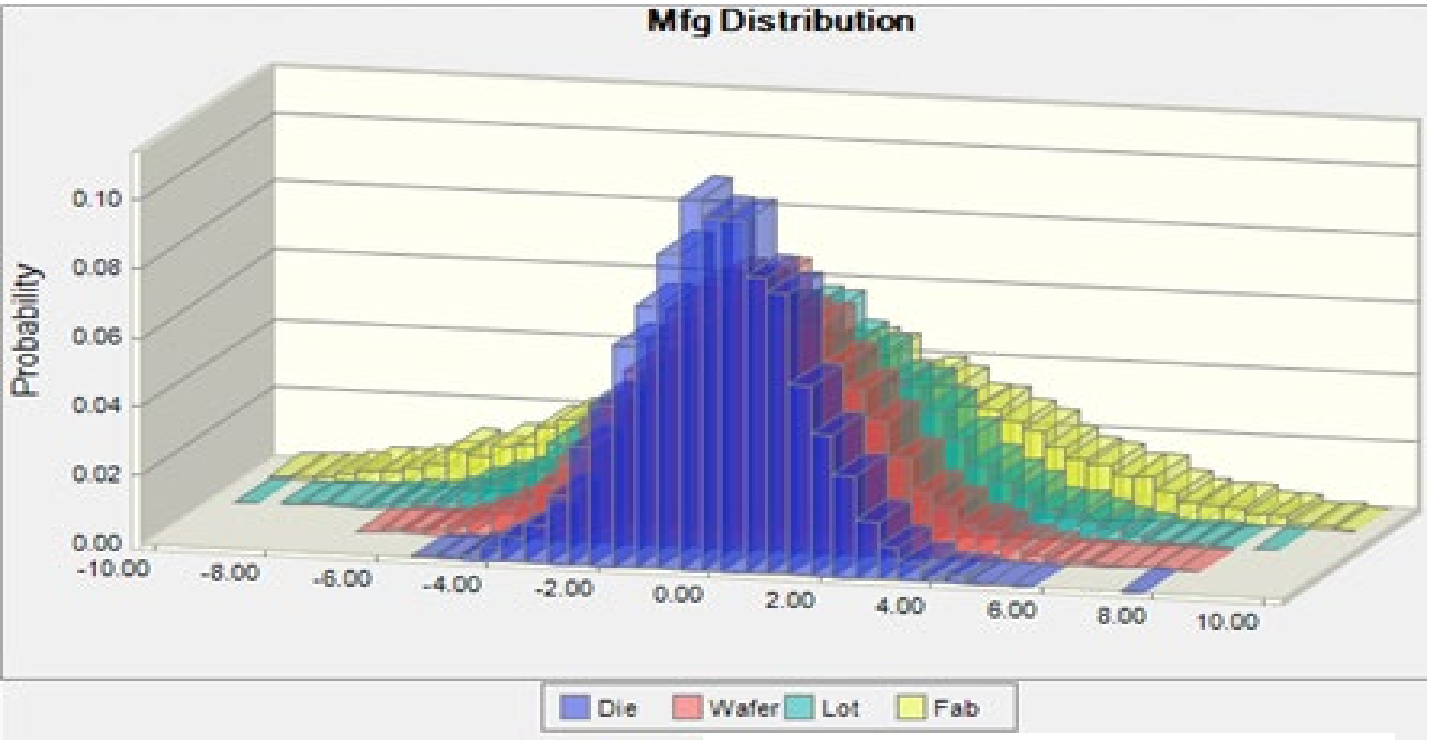
# events/ 40 B trials	3 σ	4 σ
Focus OR Dose	108.1M	2.5M
Focus AND Dose	292K	160
Focus AND Dose AND Mask	791	0.01

$$40B = 1/(1 - \mathrm{erf}\left(\frac{\sigma}{\sqrt{2}}\right))^{n}$$

To safeguard 40B sites:

n = 1	Dose or Focus only:	**6.7σ**
n = 2	Dose + Focus:	**4.57σ**
n = 3	Dose + Focus + Mask:	**3.62σ**

Drives need for appropriate understanding of process variable distributions in manufacturing



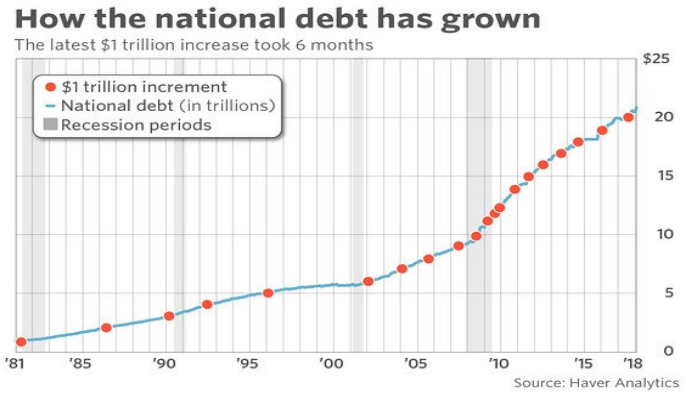
- And spatial/temporal correlation properties, since assumption of complete independence of errors breaks down at small enough length scale
- Must be sure that for known best dose / best focus exposed field, that the intrinsic min variation in dose/focus across that field can safeguard all within die locations
- "Good die" model appropriate.

Arnold, W., "Overlay Simulator for Wafer Steppers", Proc. SPIE 0922, doi: 10.1117/12.968406 (1988).

Gabor, A., et al. "Edge placement error fundamentals", JM3 (2018).

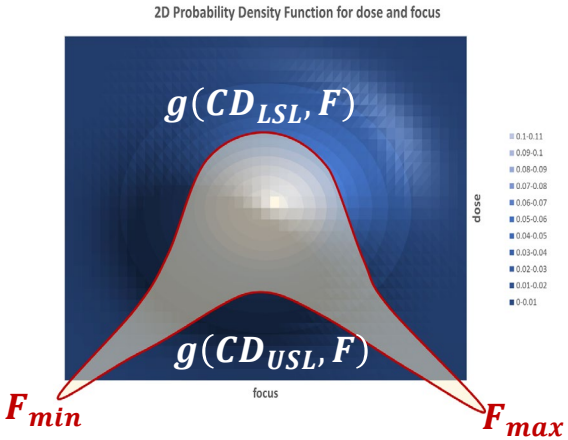
Failure Opportunities:

~40B per die
~20T per wafer
~0.5Q per lot
Quintillions per fab life

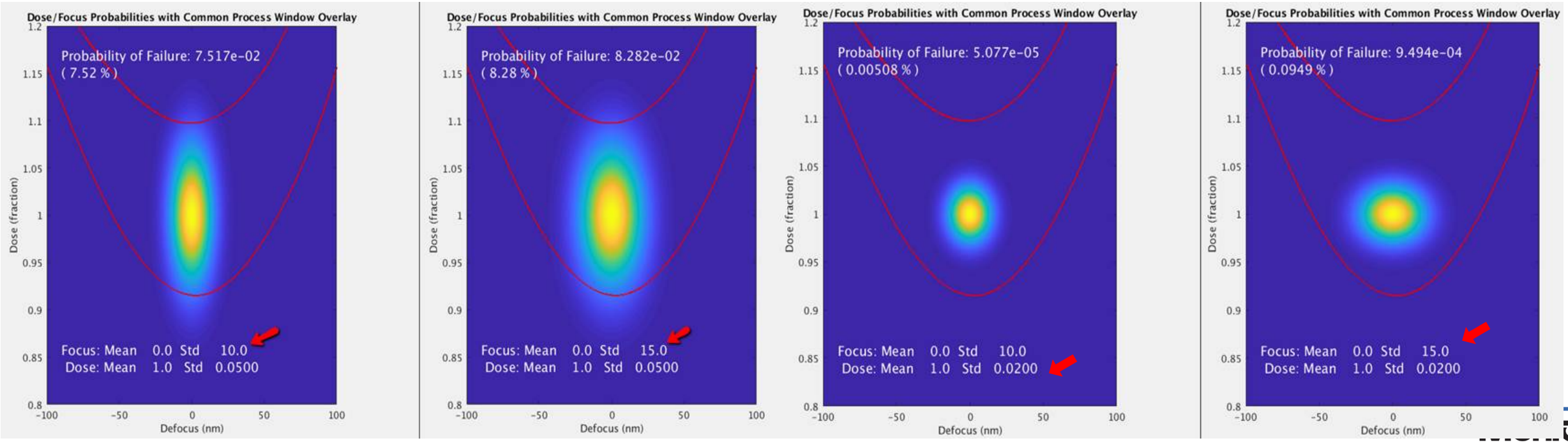


Non-Monte Carlo based estimation of Intra-layer Failure rate for individual feature as f(E,F)

$$p_{fail} = 1 - \int_{F_{min}}^{F_{max}} \int_{g(CD_{USL},F)}^{g(CD_{LSL},F)} \frac{1}{2\pi\sigma_E\sigma_F} exp\left(-\left(\frac{(E-E_0)^2}{2\sigma_E^2} + \frac{(F-F_0)^2}{2\sigma_F^2}\right)\right) dEdF \qquad E = g(CD,F)$$



- Window for "Failure": Can be CD defined, or by direct simulation of soft/hard P/B
- Assume knowledge of manufacturing σ_E and σ_F



Full-chip Intra-layer Failure probability

- Need to account for multiple placements of patterns within chip.

$$P_{fail} = (1 - ((1 - p_{fail})^{N}))$$

Single feature appearing N times

$$P_{chip\ fail} = (1 - (\prod_1{}^{M}(1\text{-}p_{fail})^{N_M}))$$

M features appearing N_M times each

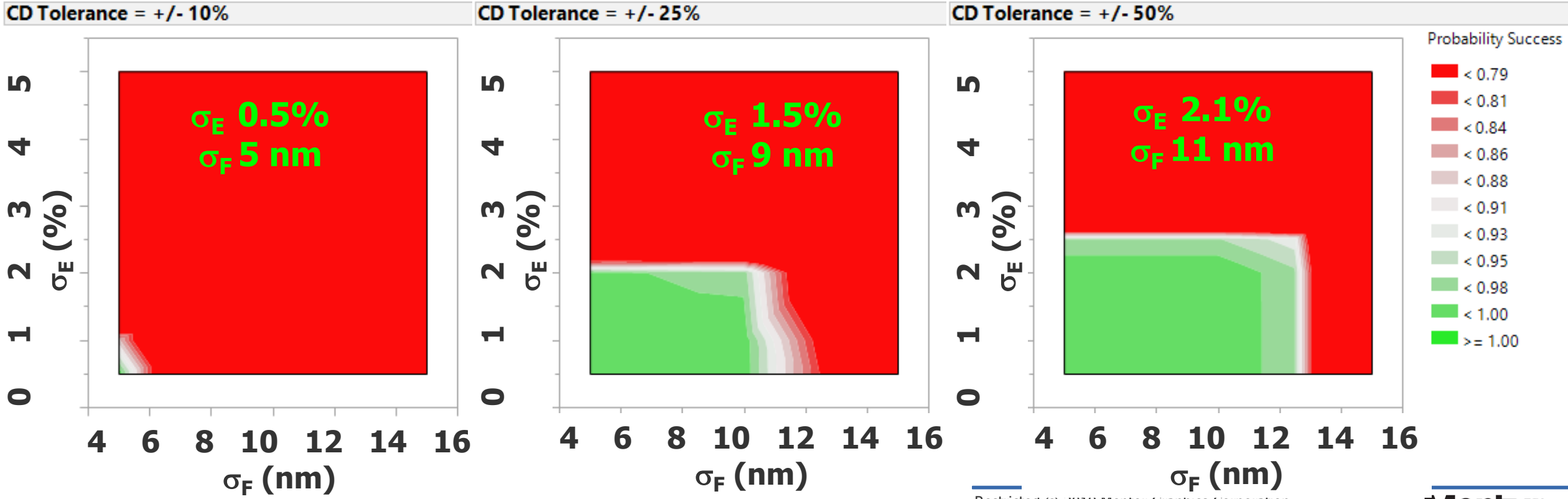
$$P_{chip\ fail} = (1 - (\prod_1{}^{M} e^{-p_{fail} * N_M}))$$

Poisson approx. to binominal distribution when p_{fail} small and M, N large.

Full-chip Failure Probability as a function of CD Tolerance, and assumed focus, dose distributions

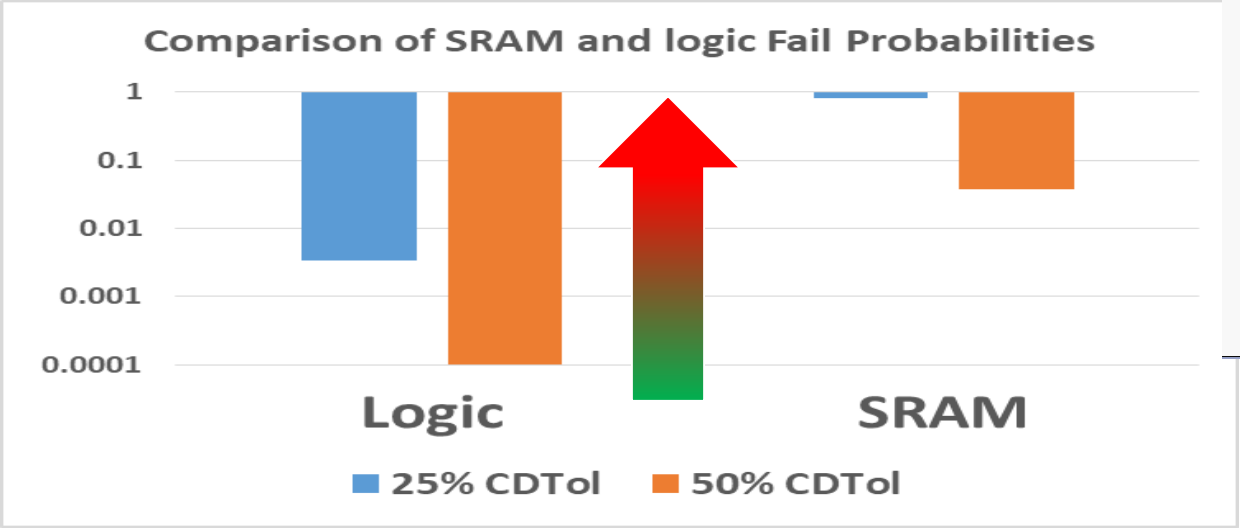
- Identify worst several thousand potential PW hotspots, and # of repeat placements within die. Simulate each through fine-stepped dose/focus.
- Determine PW versus assumed tolerance and dose/focus distribution.
- Calculate full-chip failure probability map and max allowable variability to maintain 0% failure

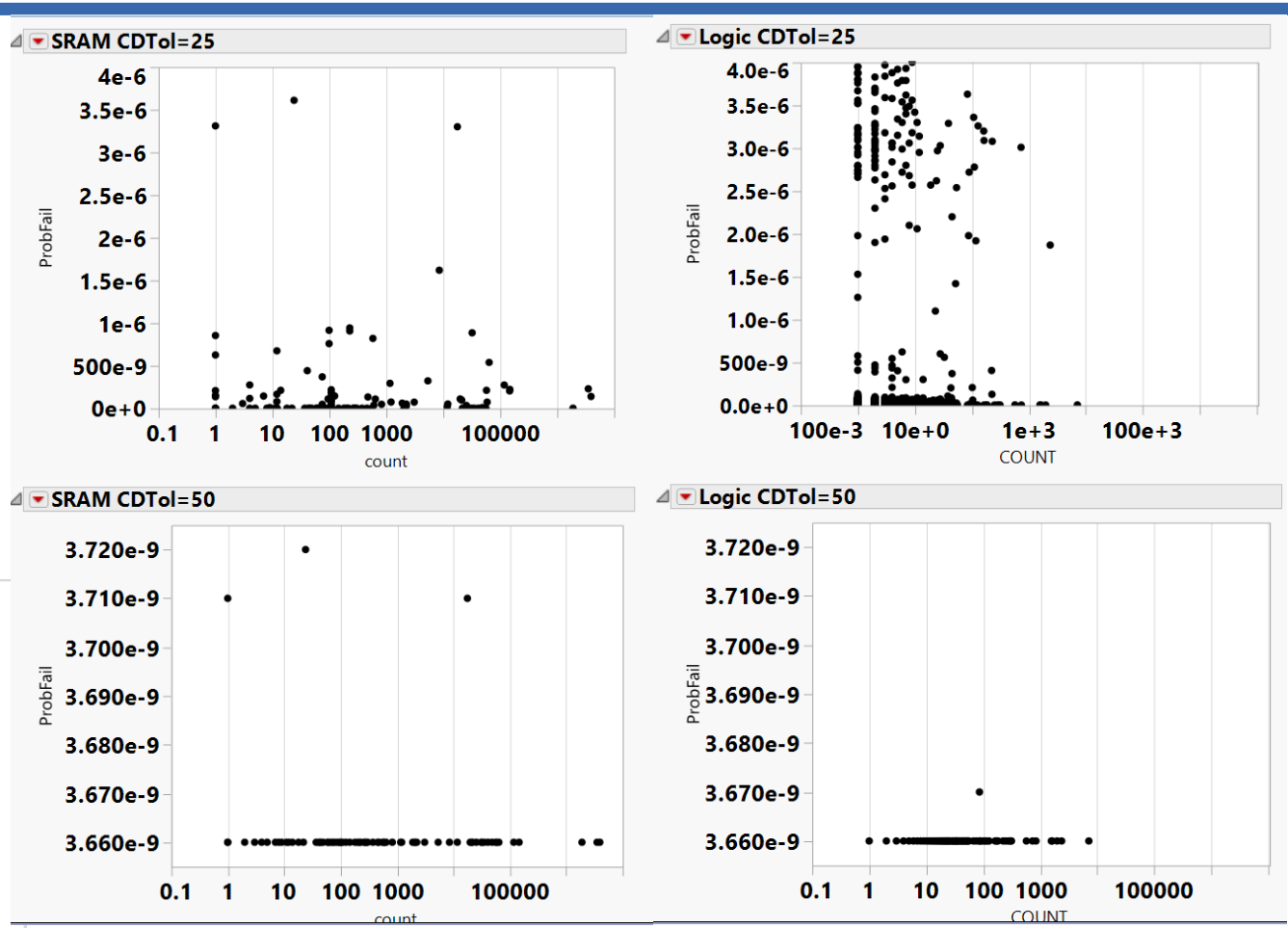
14nm Metal Logic chip



Comparing different chips for overall fail rate

- 14 nm Metal chiplet with mostly SRAM cells compared to logic chiplet.
- SRAM several million placements of some hotspots, greatly increases fail likelihood.
- But validity of logic to SRAM comparison of same dose/focus distribution is questionable due to spatial correlation lengths.

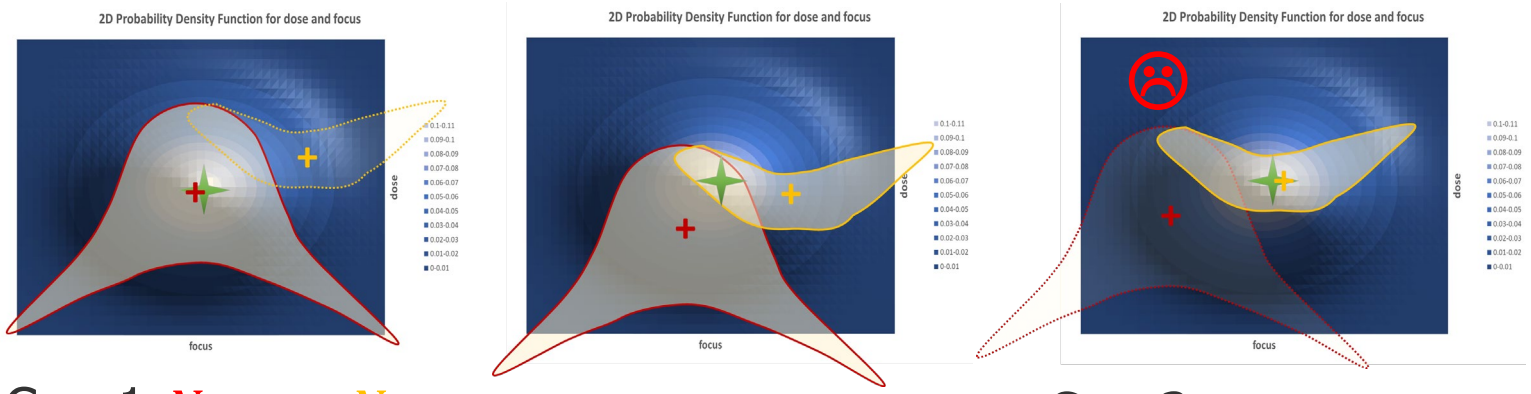




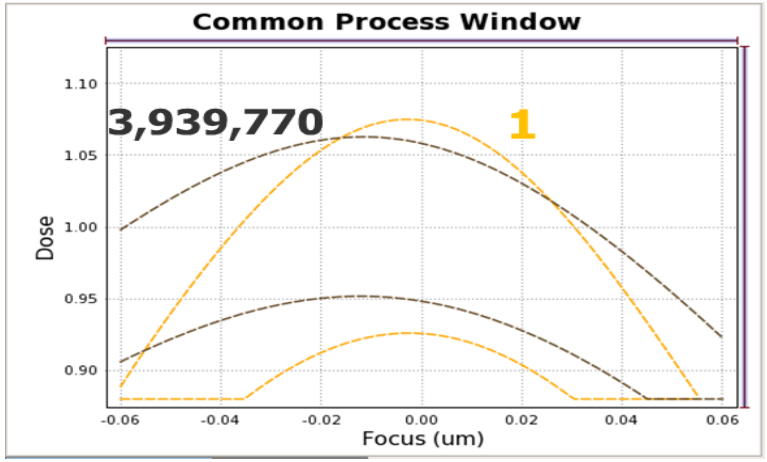
σ_E 2% σ_F 10 nm

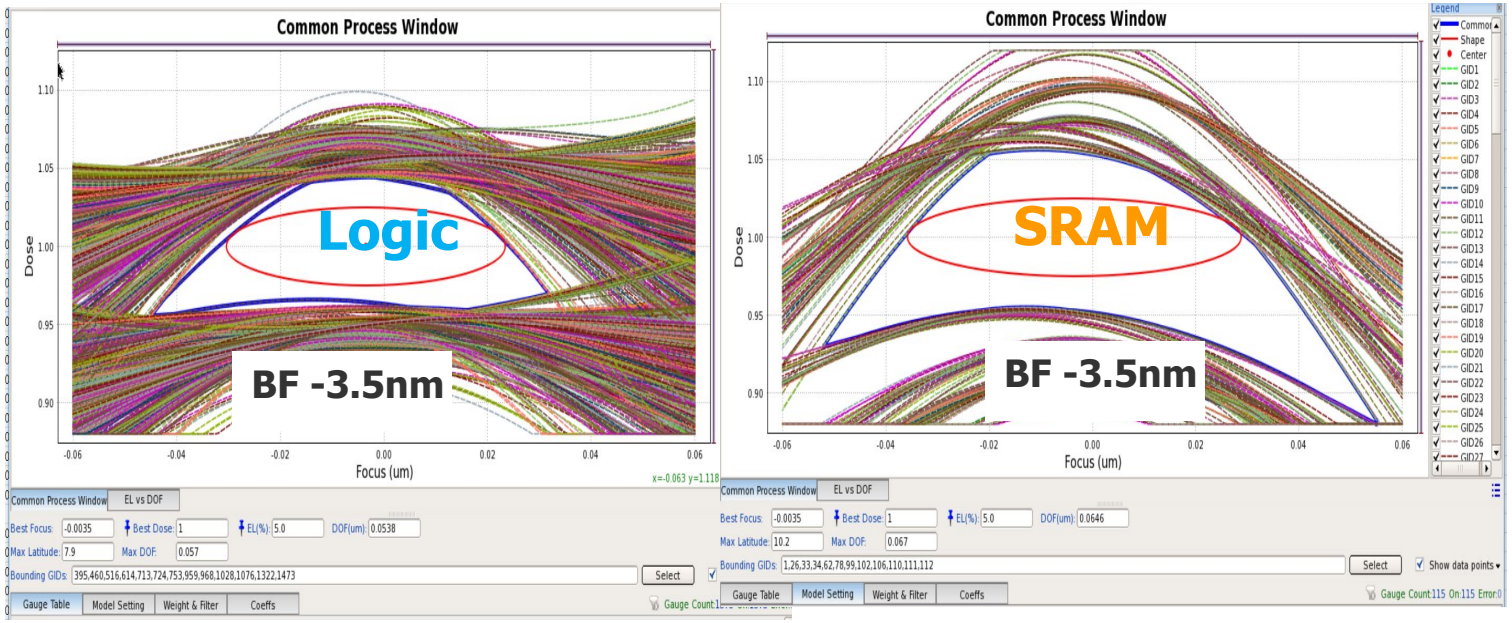
Choosing Best Focus for yield maximization:

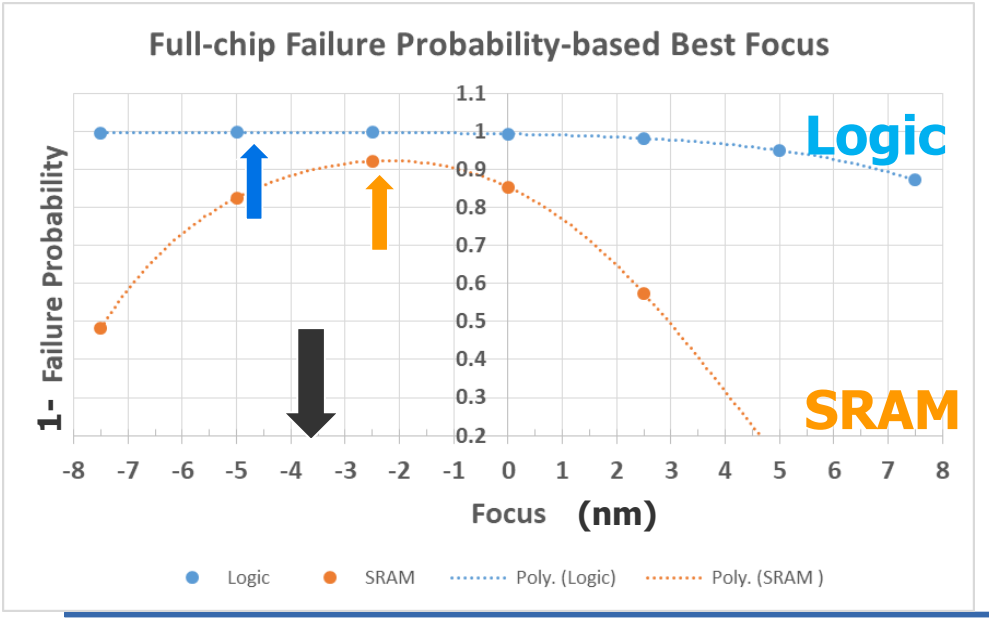
$$P_{chip\ fail} = (1 - (\Pi_1{}^{M} e^{-p_{fail} * \mathbf{N_M}}))$$



Case1: $N_{M,A} \gg N_{M,B}$ Case2: $N_{M,A} \approx N_{M,B}$ Case3: $N_{M,A} \ll N_{M,B}$

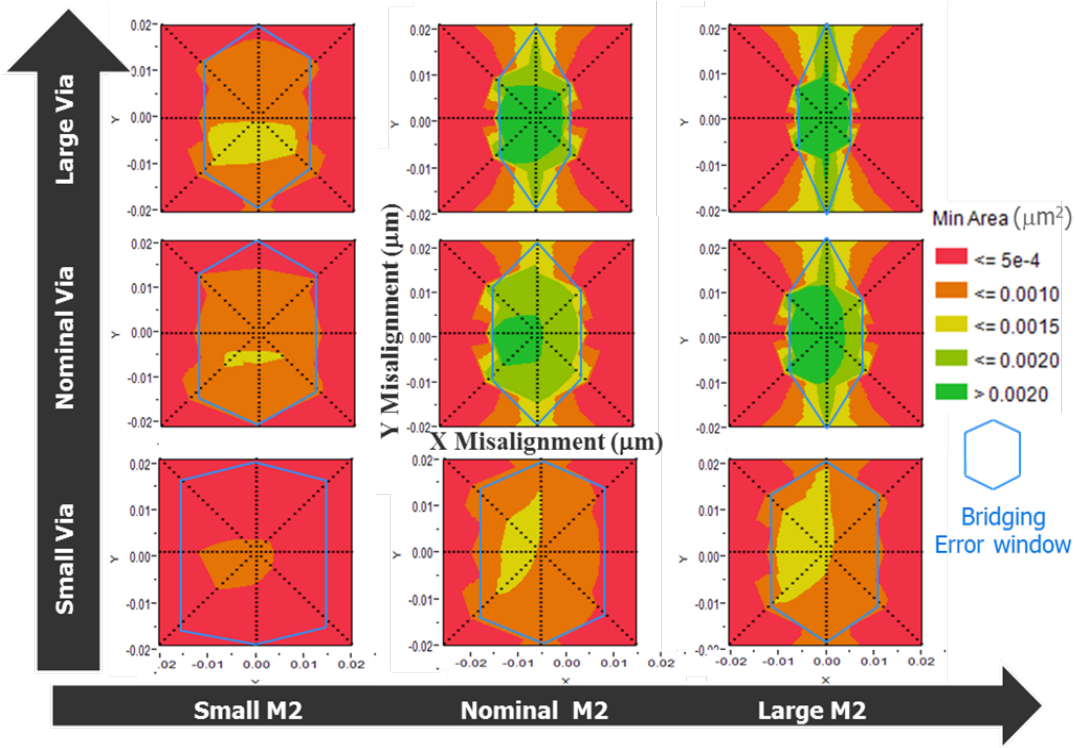






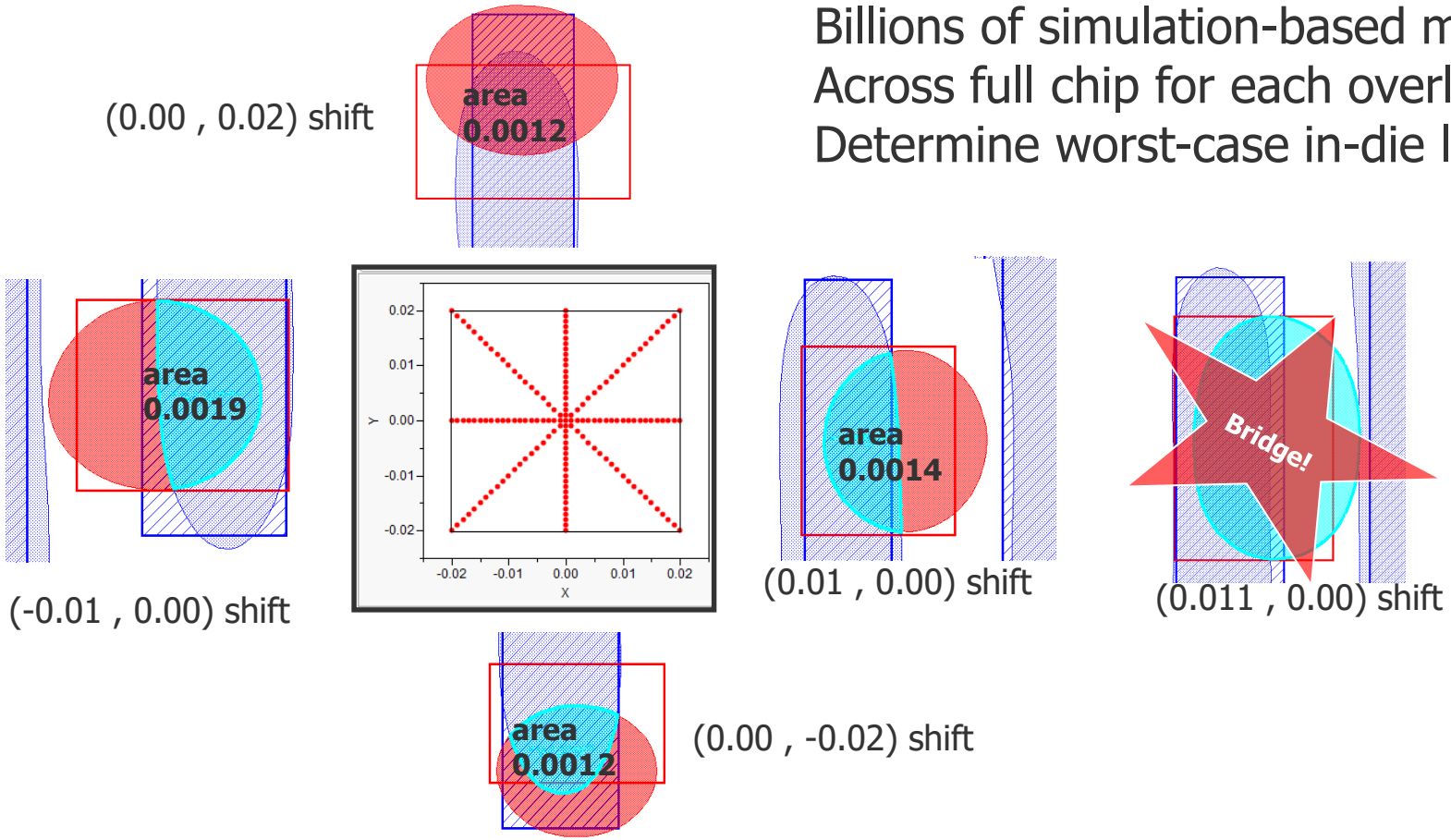
Inter-layer hotspot Process Window

- For each design, there will be unique worst case layout locations corresponding to specific CD, overlay error vectors.
  - CD layer A; CD layer B; Overlay vector
- Build a design-specific inter-layer edge placement hotspot library.
- This library could be merged with available dense on-product wafer state data and used in a variety of ways:
  - *Yield learning through intelligent directed inspection*
  - *Cost savings / Yield Increase / Mfg capacity expansion through litho rework reduction*



Sturtevant, J., "Two-layer critical dimensions and overlay process window characterization ane improvement in full-chip computational lithography", Micro/Nanoithography, MEMs, MOEMs, 15 (2), 021406 (2016)

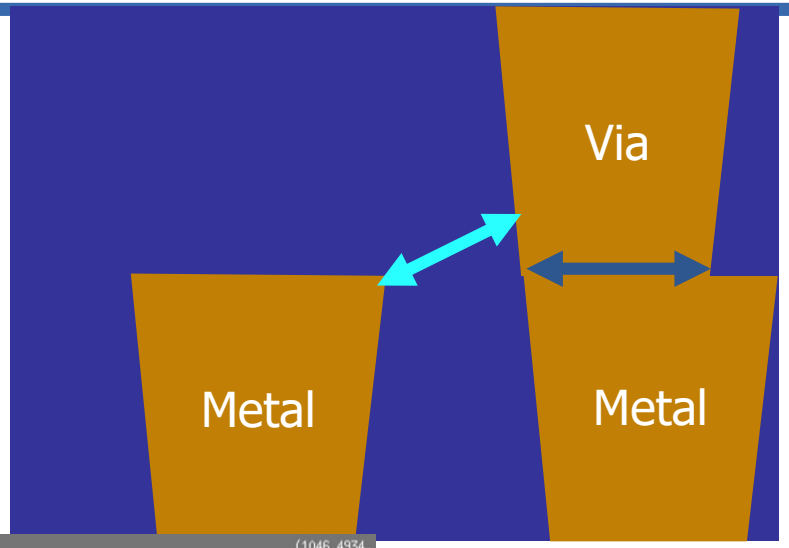
Min Area Metal-Via Overlay: Nominal CD Condition

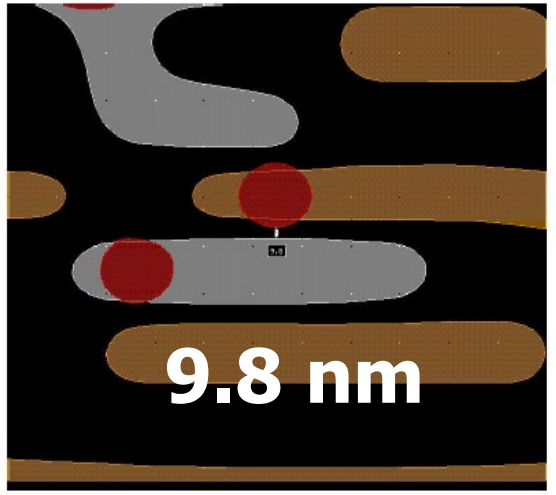


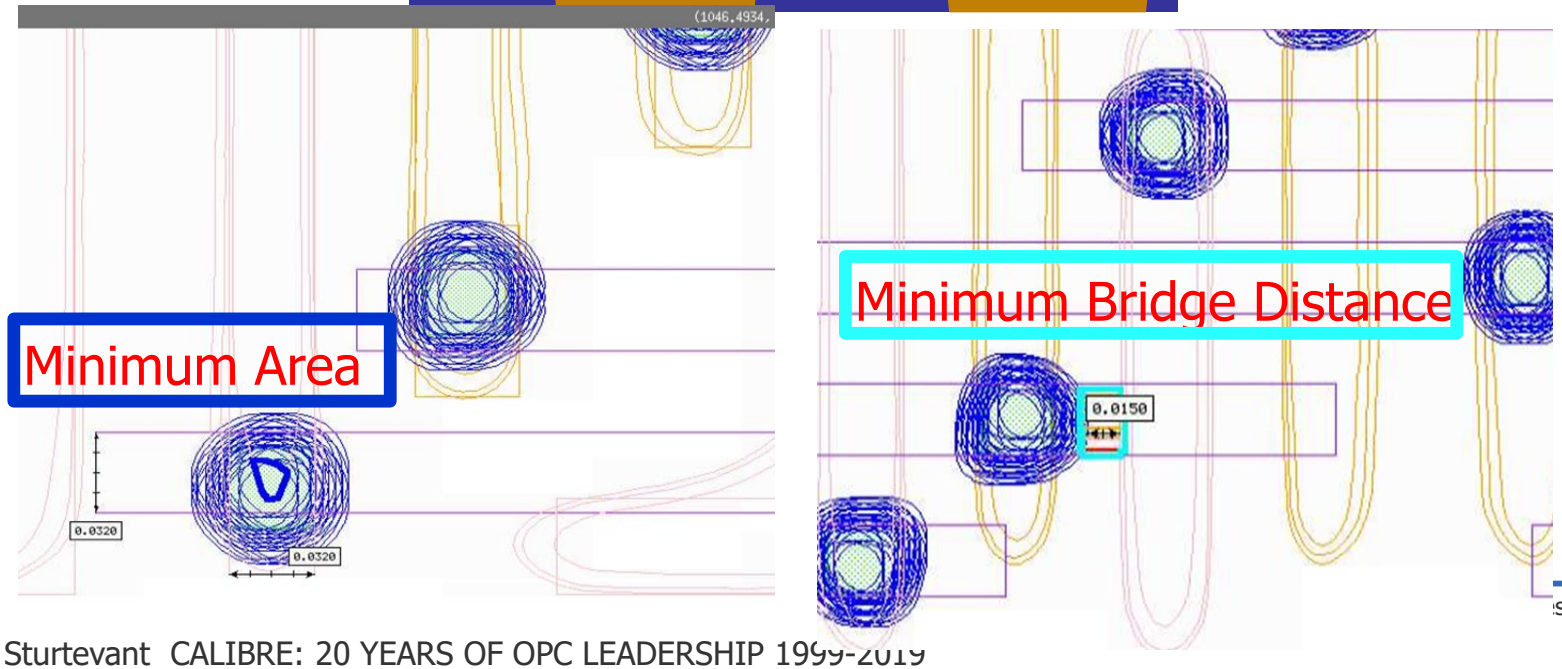
Billions of simulation-based measurements
Across full chip for each overlay error vector
Determine worst-case in-die location

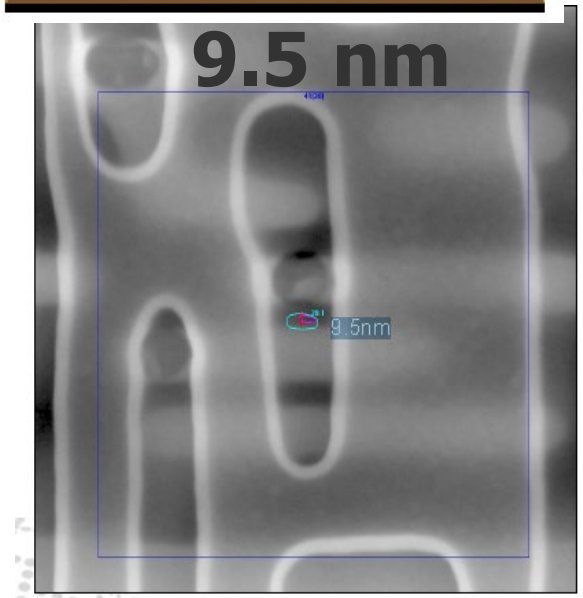
Key is that each limiting layout location per overlay vector is UNIQUE!

E-beam Overlay metrology increasingly important to validate simulated metrology analysis









Combine in-fab metrology data with design-specific virtual metrology to predict die fail rate per wafer.

Design-specific library: Offline

Models

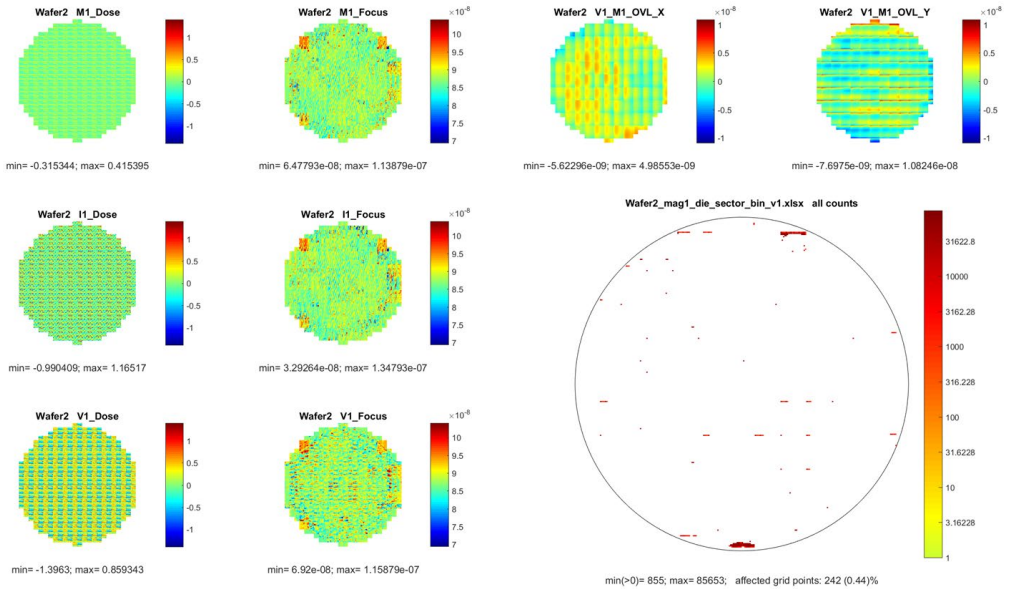
New chip_ post OPC.gds

PW conditions

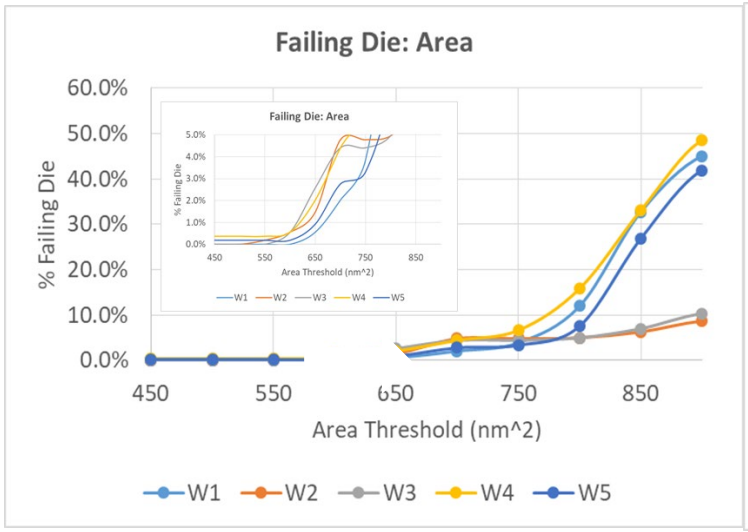
dbase of potential hotspots as f(focus, dose, overlay)

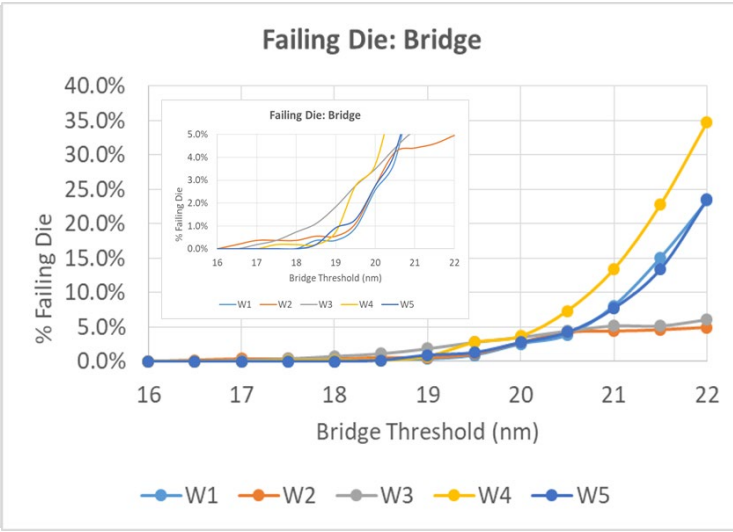
Design-specific library (~ 10^6 potential HS with CD, overlay metadata)

14 nm Chip: Metal/Via



Wafer data (E, z, overlay)





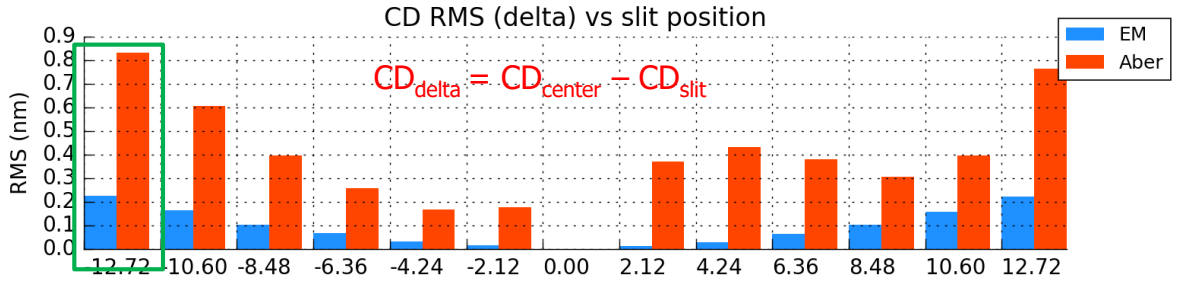
EUV Lithography Simulated Metrology Opportunities

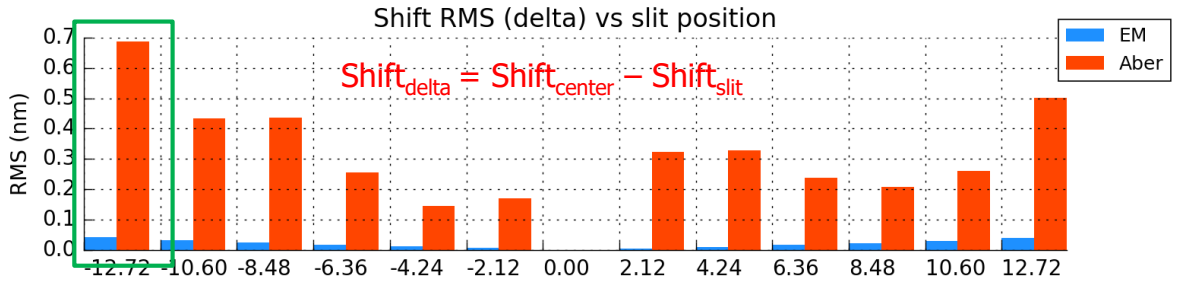
- Stochastic failure: Increased LER/LWR, which has typically been ignored in full-chip simulation for 193i. Stochastic model now makes full-chip consideration of this local effect possible.
- Aberration-driven CD and image shift control: Intra-layer and Inter-layer.
  - EUV aberration levels are ~ 10X higher than 193i, and tool to tool aberration signature differences leads to uncorrectable CD and pattern shift errors. These effects are pattern and illumination dependent.
  - Exceedingly painful / impossible to do such in-fab with real metrology

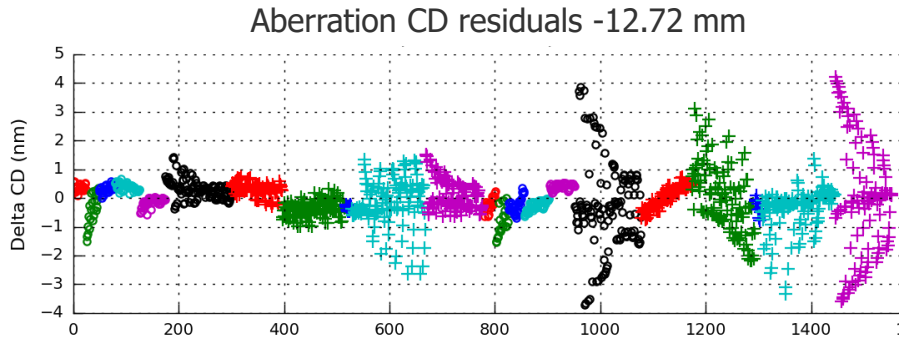
Impact of aberrations in EUV

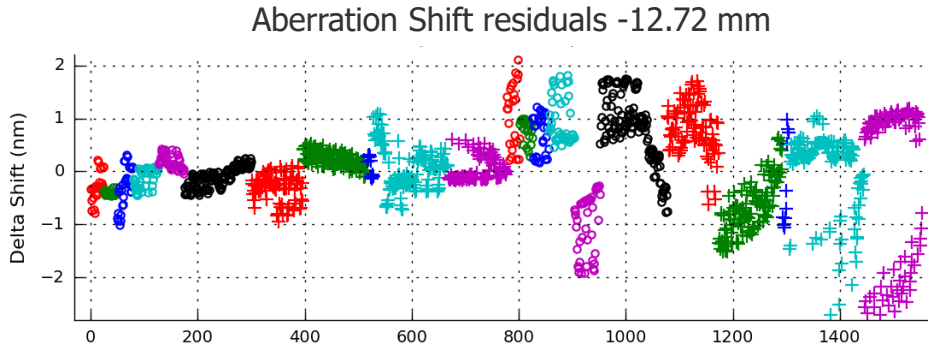
- 7 nm design with parametric test structures corrected with
  - Measured center slit aberration, verified using slit specific aberrations
  - Center slit 3D mask, verified using slit specific 3D mask

Measured aberrations at 13 slit locations from NXE3300







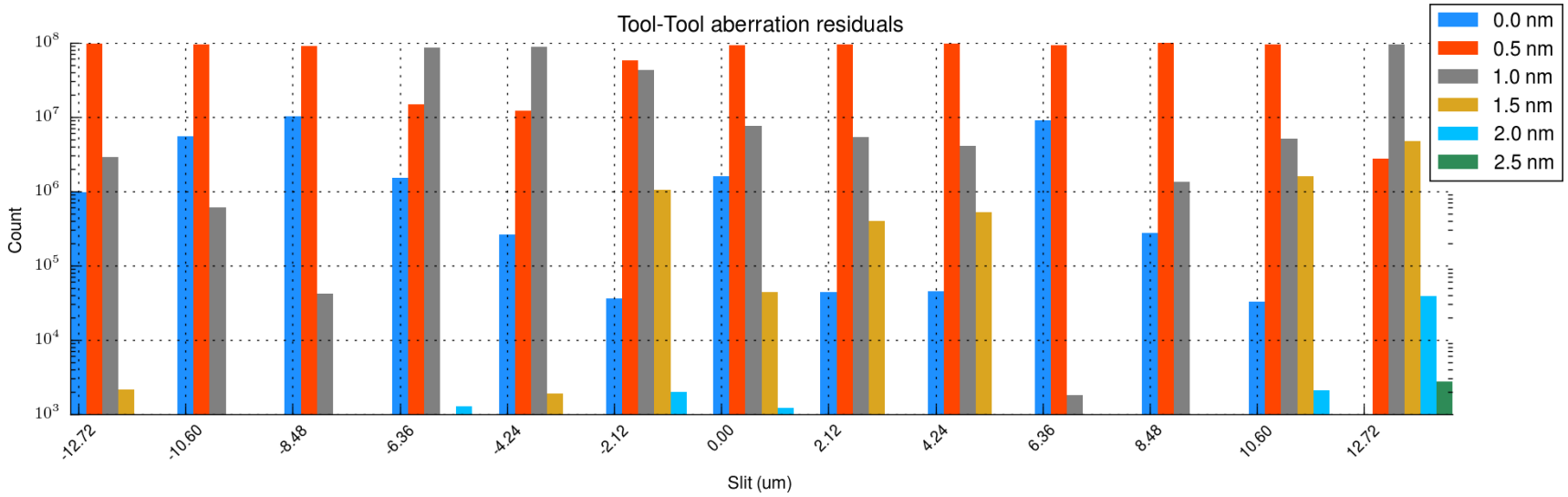


CD/Shift changes from aberrations much larger than EMF effects

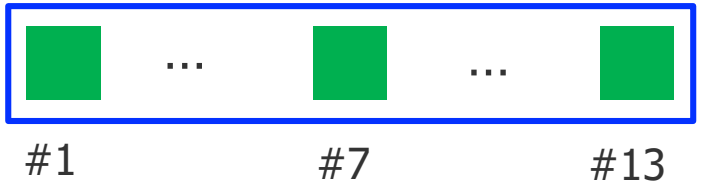
Tool to Tool Aberration Variability in EUVL

Tool to tool aberration variation is of the same order as across the slit variation

Max: 1.5nm 1.0nm 1.0nm 1.0nm 1.5nm 2.0nm 2.0nm 1.5nm 1.6nm 1.0nm 1.0nm 2.0nm 2.5nm



- 7 nm M1 chiplet 2mm x 2mm
- Placed at 13 different slit locations



- Design OPCed with Tool A measured aberrations and verified with Tool B measured aberrations
- Contour differences between Tool A nominal and Tool B nominal contours

Tool to tool variation is uncorrectable by OPC software

Characterizing tool – tool aberration variation impact through simulation-based metrology


#A Aberration A


#B Aberration B


#C Aberration C


#D Aberration D


#E Aberration E

EUV fleet of tools each with unique aberrations

Identify which tool in an 'N' tool fleet set guarantees best overall performance – 'Golden Tool' in the fleet

Correction – Verification results matrix

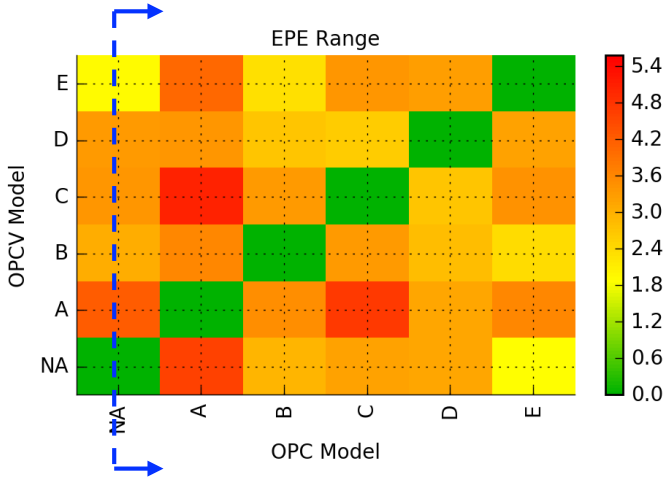
Verf \ OPC	NA	A	B	C	D	E
E						■
D					■	
C				■		
B			■			
A		■				
NA	■					

NA: No Aberrations

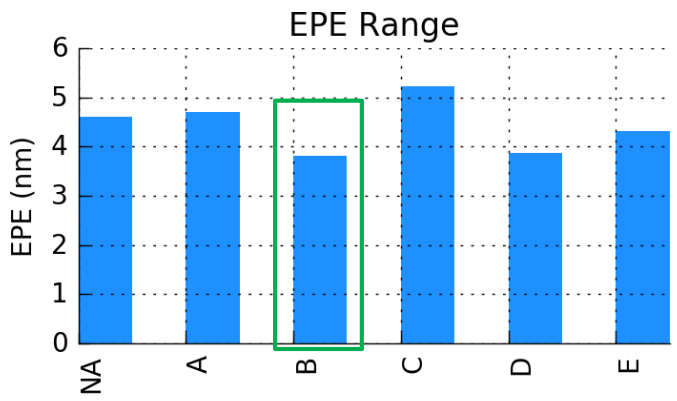
- Use every tool in the fleet for correction to get 'N' unique masks
- Verify each of these masks against every tool in the fleet
- Characterizing OPC mask performance in verification
  - EPE : max, range, 3 sigma
  - EPE Severity count
  - Image shift

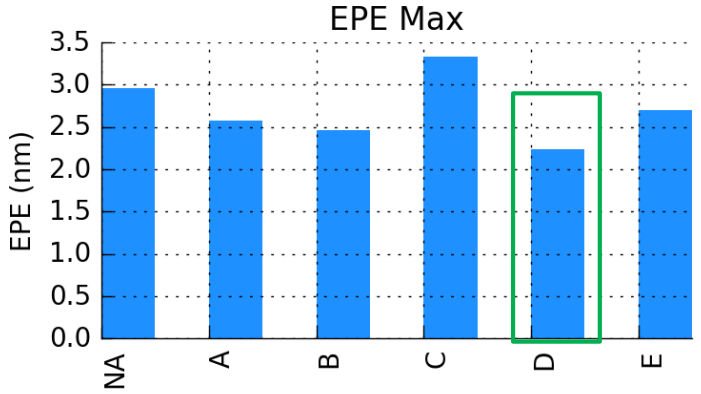
Impact of tool aberration diffs on Intra-layer EPE

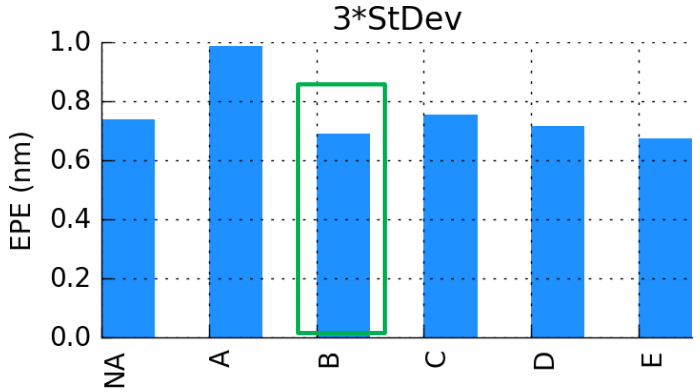
For each OPC mask, cumulative verification errors across each tool

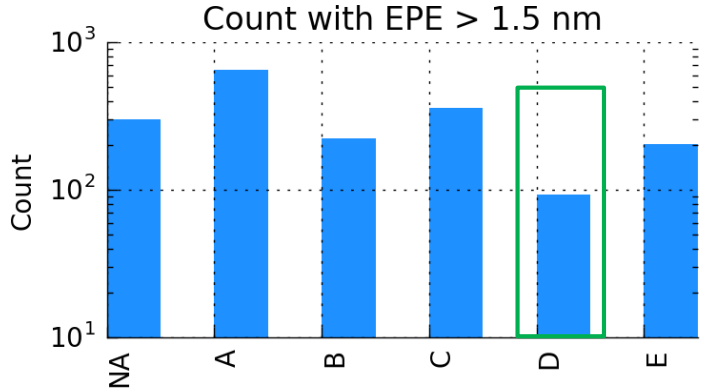


- Tool with the lowest aberration not necessarily the best tool
- Tool that *matches* the rest of the fleet most closely is the best tool





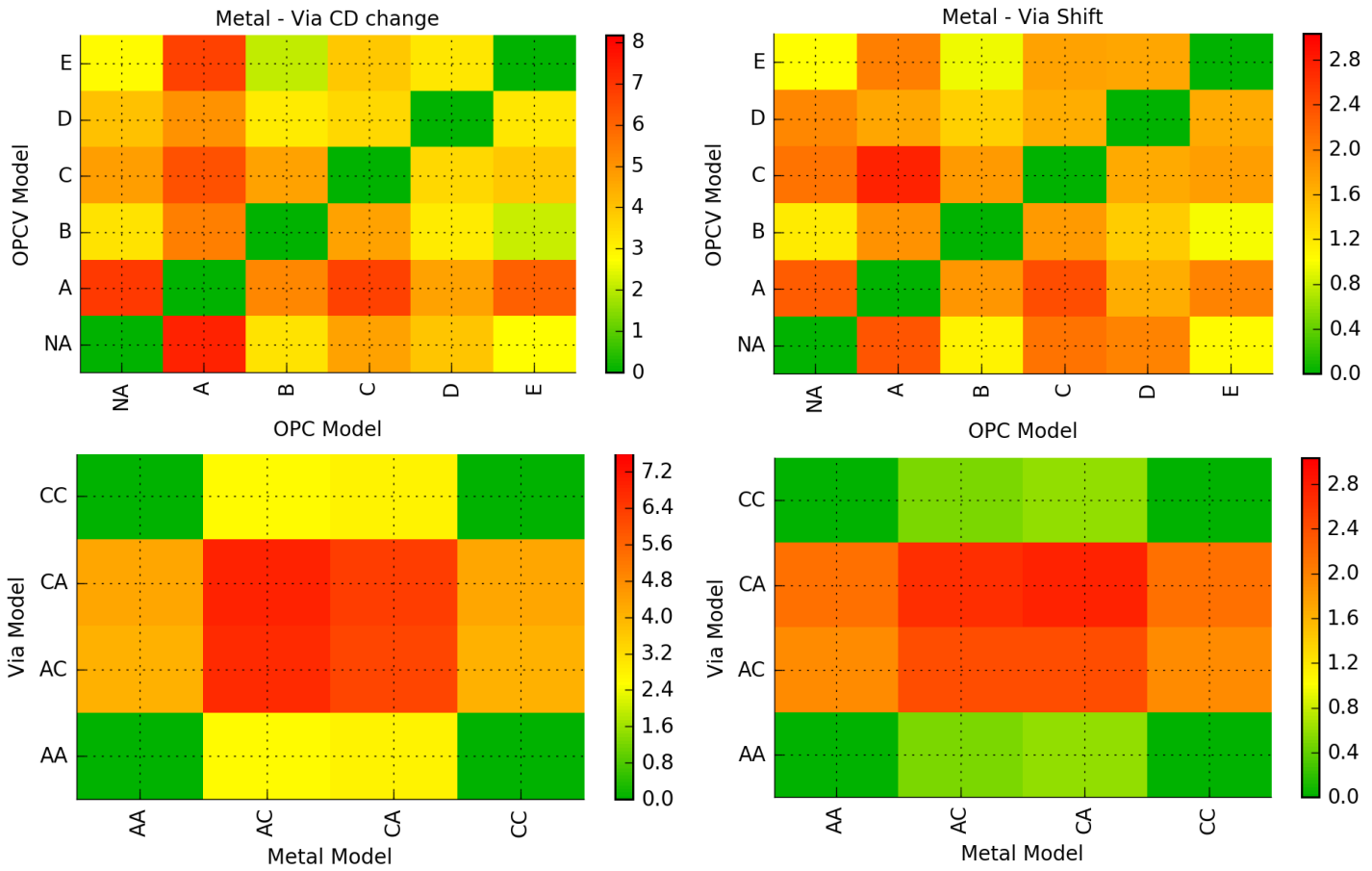




In this fleet Tool D would be the best candidate for model calibration / correction for this specific layer / source map

Inter-layer uncorrectable edge placement errors on test patterns (Metal / Via example)

- 5 scanners (3300, 3350) actual across slit aberration fingerprints
- Large variety of metal, via TPs across slit.
- All combinations of OPC model and exposure tool for metal and via layers.
- If no tool-specific OPC model and mask dedication, manifests worst case of ~ ***5nm max uncorrectable inter-layer edge to edge errors***.

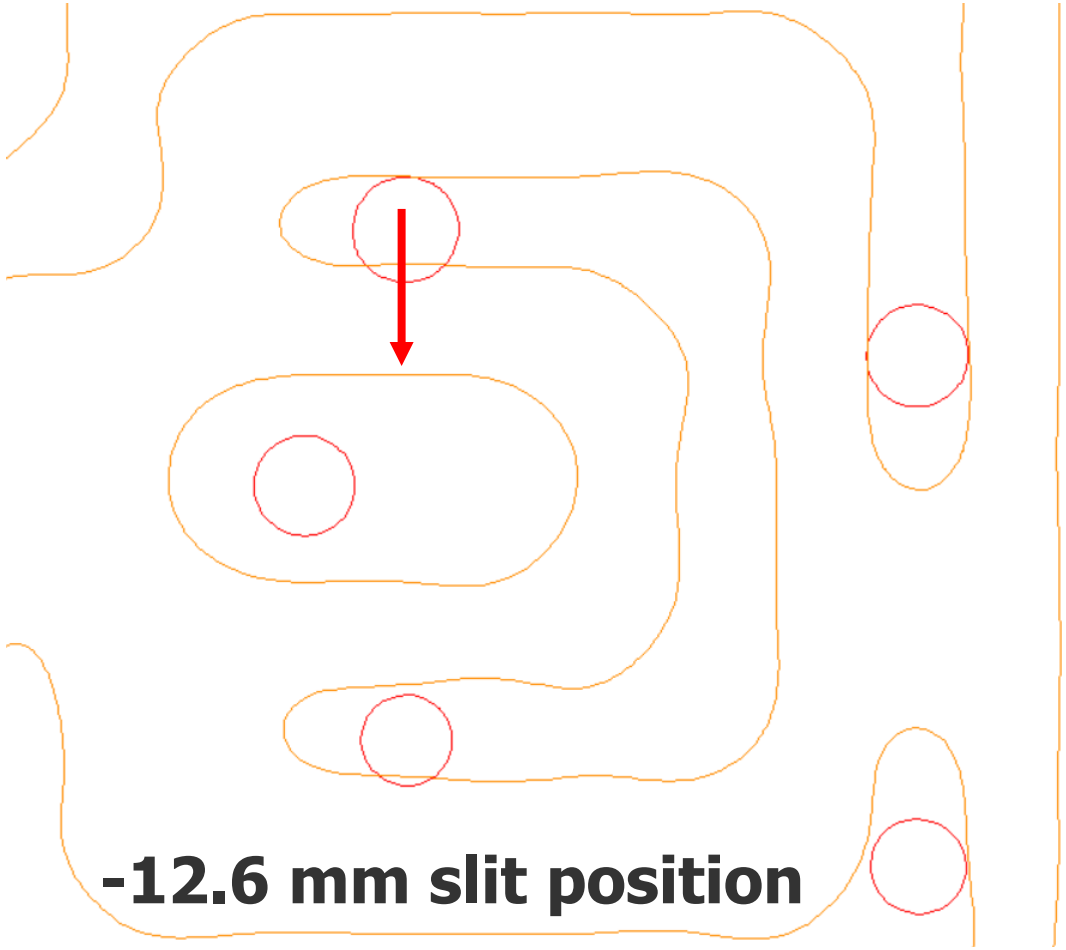


$$Max\ Edge\ to\ Edge\ Error = \left|\left\{\frac{dCD_{metal}}{2} - \frac{dCD_{via}}{2}\right\}\right| + \{|shiftmetal\ - shiftvia|\}$$

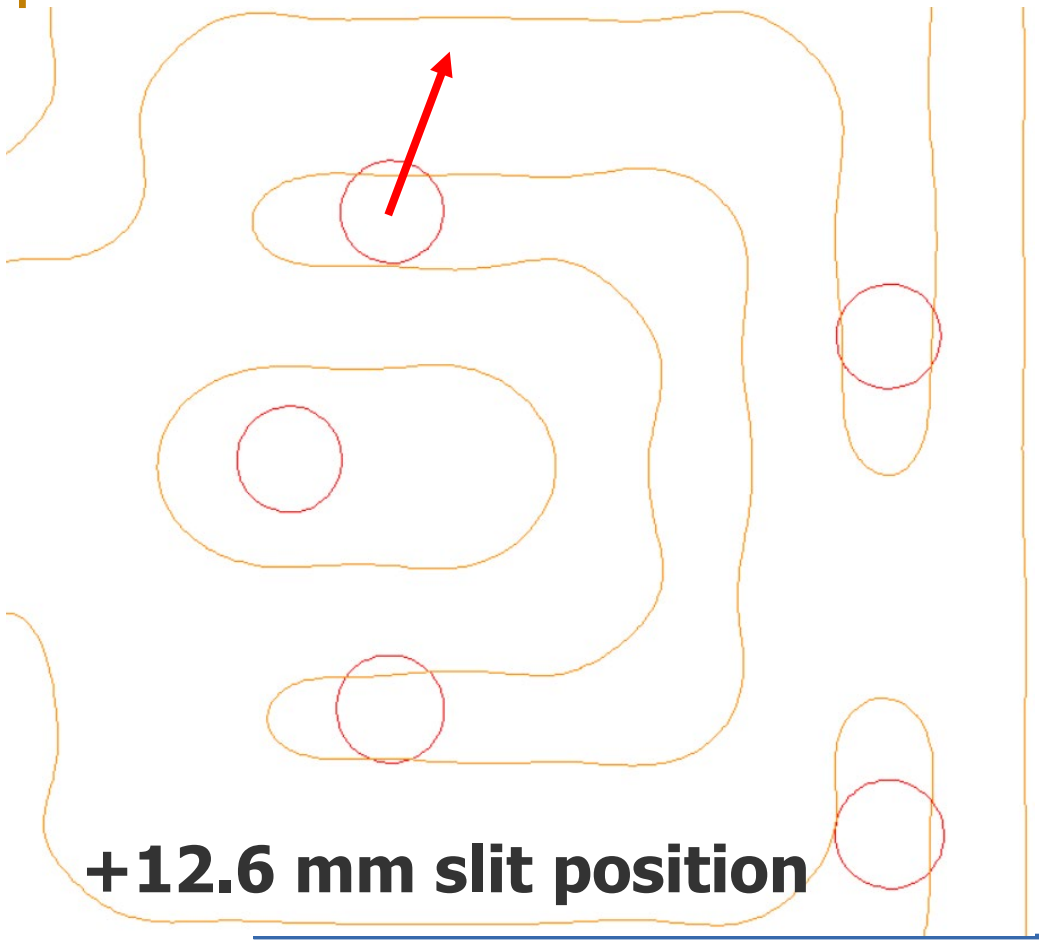
Example of uncorrectable CD and pattern shift across slit:

Via OPC Tool 3 Exposed Tool 1

Metal OPC Tool 1 Exposed Tool 3

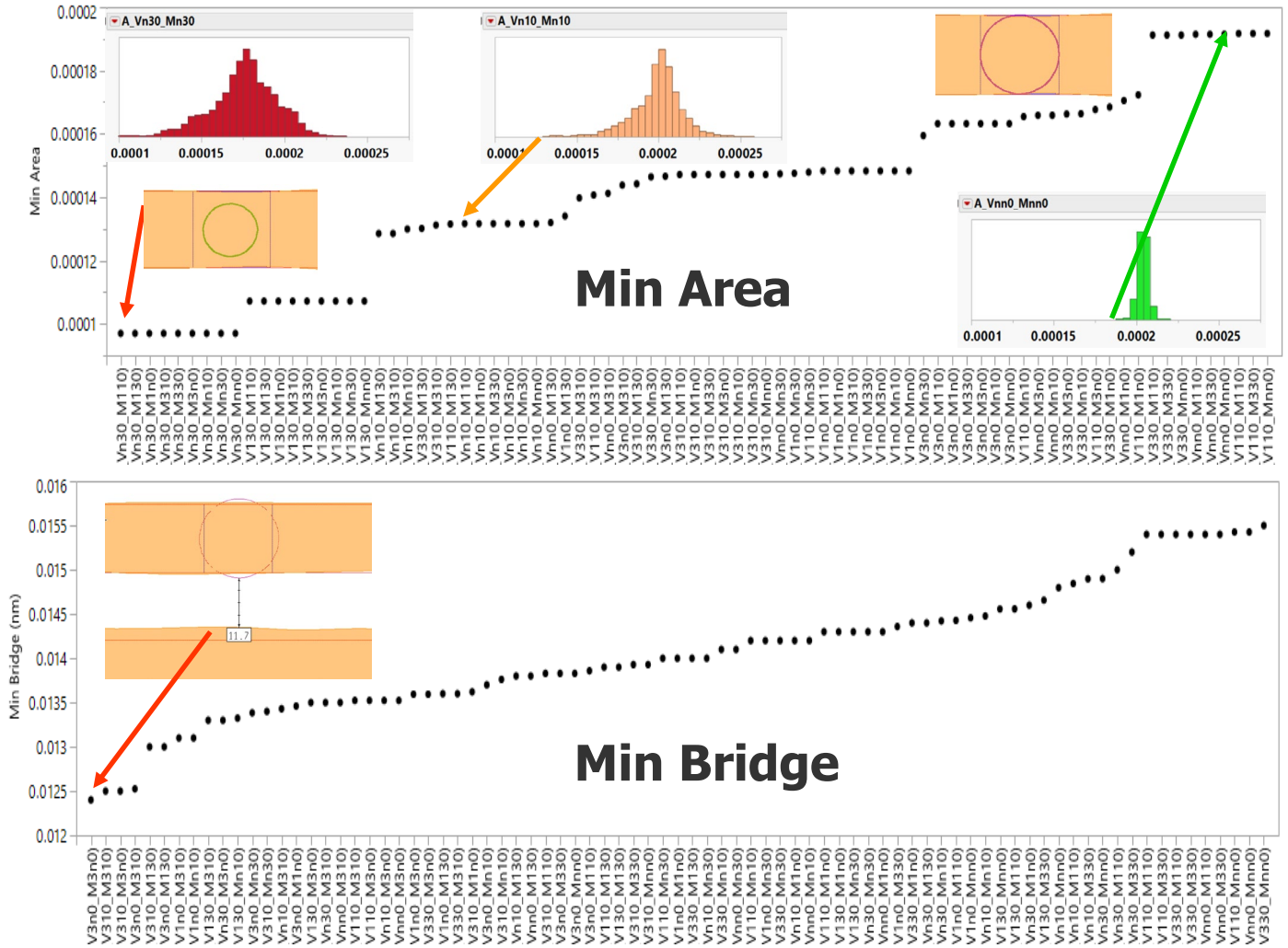


-12.6 mm slit position



+12.6 mm slit position

Manufacturing scanner fleet analysis



- 81 tool combinations for metal/via OPC tool in model: exposed tool
- All at Best Focus
- Largest min AREA for all cases where via and metal use same aberration set for OPC and verification

Summary

- Simulation-based metrology can be used to assess process window for intra- and inter-layer failure, and to guide specific metrology sampling for most effective use of in-fab tools.
- Analytical alternative to brute force MC method presented for prediction of failure probability for individual hotspots, and for full-chip yield estimation
- Designs will have particular locations where specific two-layer CD and overlay error vectors will manifest most severely from an inter-layer edge placement perspective.
- Simulation-based metrology can be used with actual in-fab wafer metrology to assess wafer-level die failure
- EUV will not necessarily solve all inter-layer edge placement control woes, simulation can be a powerful tool to elucidate.

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