Holistic Metrology Approaches For Improved Device Overlay And Edge Placement Error

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ASML
April 3, 2019

Outline

- The problem statements

- Holistic approach (involving lithography and beyond) taken towards dealing with the issue

- Conclusion

Problem statements

- In multi patterning processes, overlay is now entangled with CD including OPC and local placement error (stochastic)
  - This combined effect is Edge Placement Error (EPE) and it is the key metrics for patterning budget generation and holistic patterning control
  - EPE is a serious challenge for continued shrink (scaling)

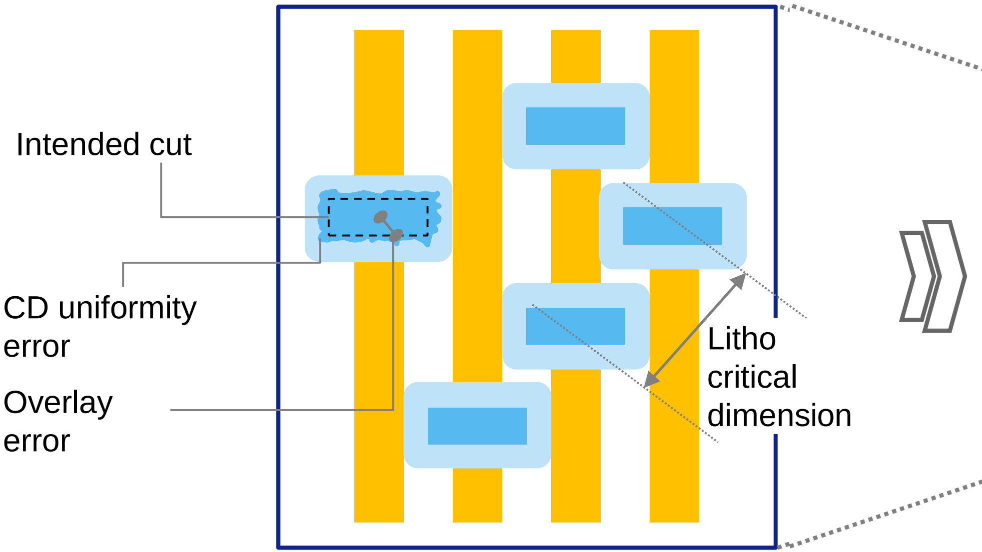
- Stochastic driving the need to move from mean to worst of the variabilities to avoid critical patterning defects
  - Driving down the allowed overlay margin to an unprecedented level
  - Need to do everything to improve device overlay

Edge placement error is the main challenge for continued shrink

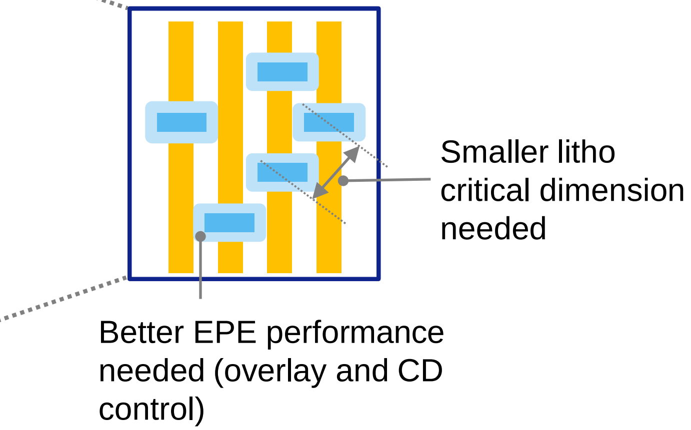
Edge placement error (EPE) and litho critical dimension (CD) main patterning parameters…

…and shrink requires ever tighter requirements

node x



node x+2

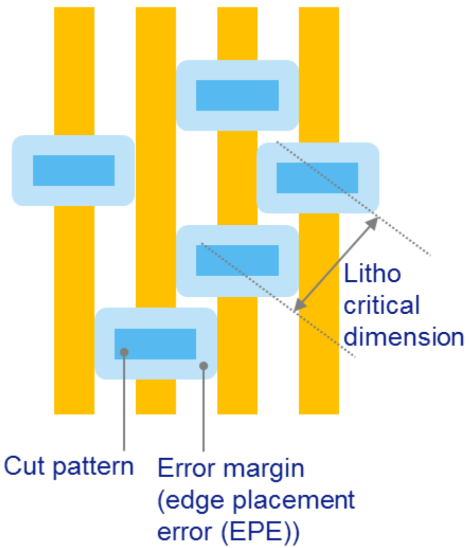


Edge placement error (EPE): combined error of overlay and CD uniformity (global CDU, local stochastic and OPC error)

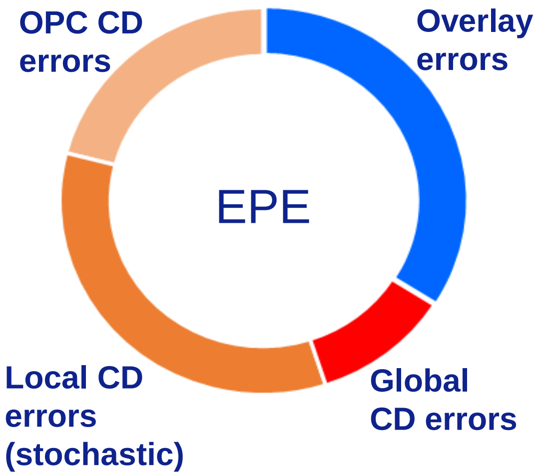
CD: Critical Dimension, OPC: Mask Optical Proximity Correction

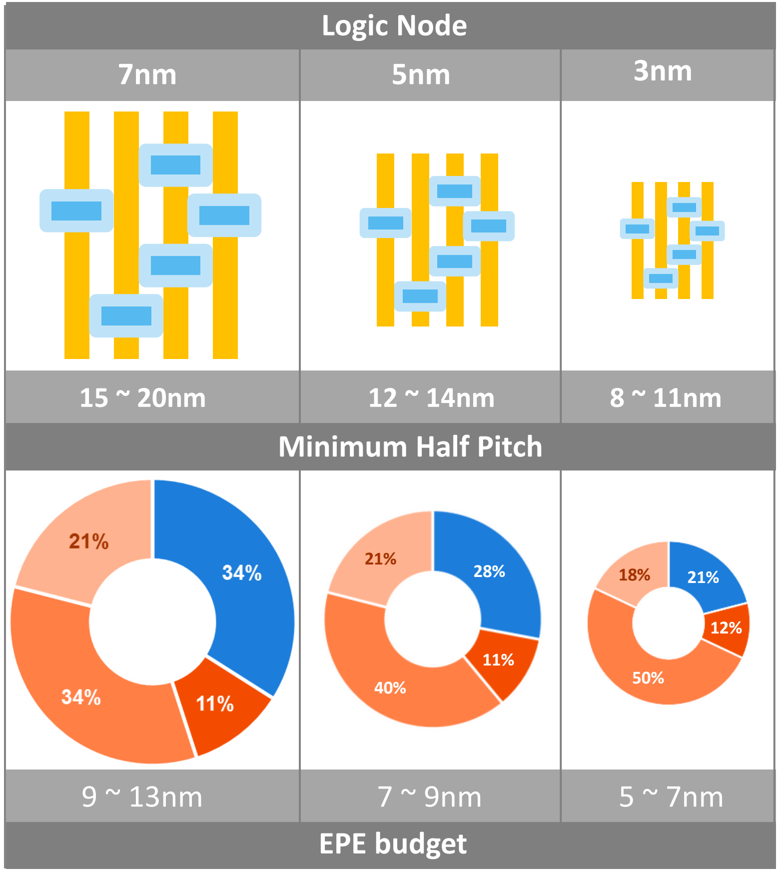
Scaling drives multiple patterning performance parameters to improve Edge Placement Error (EPE)

Typical Logic Pattern



Typical Logic EPE budget





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3 main points to address in device overlay and EPE

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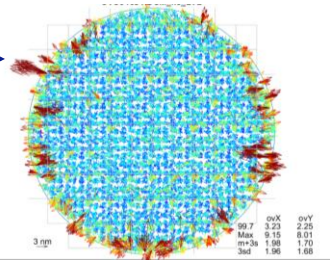
1. Address "local variation" that counts for the major part of the EPE
   - Maximizing process window with patterning processes, SMO and OPC address a large part of it, but it is important to quantify the remaining stochastic part so it can be compensated by tightening the other budget items

Global

2. Accurate measurement and control of wafer deformation
   - Decouple target asymmetry from wafer deformation (make overlay metrology immune to target asymmetry, so it can measure wafer deformation accurately)

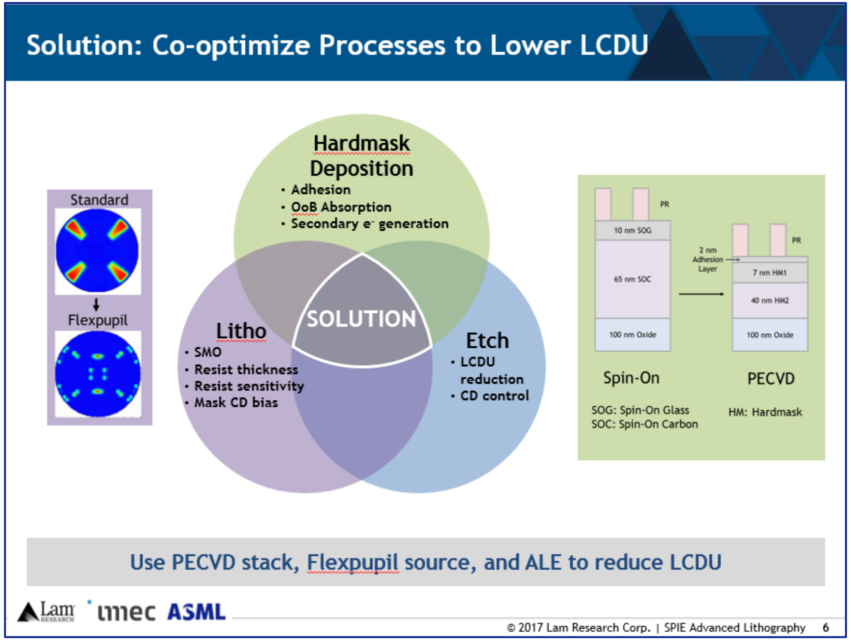
3. Control device overlay
   - Minimize device to target offset
   - On device overlay metrology

Are these accurate OV ?

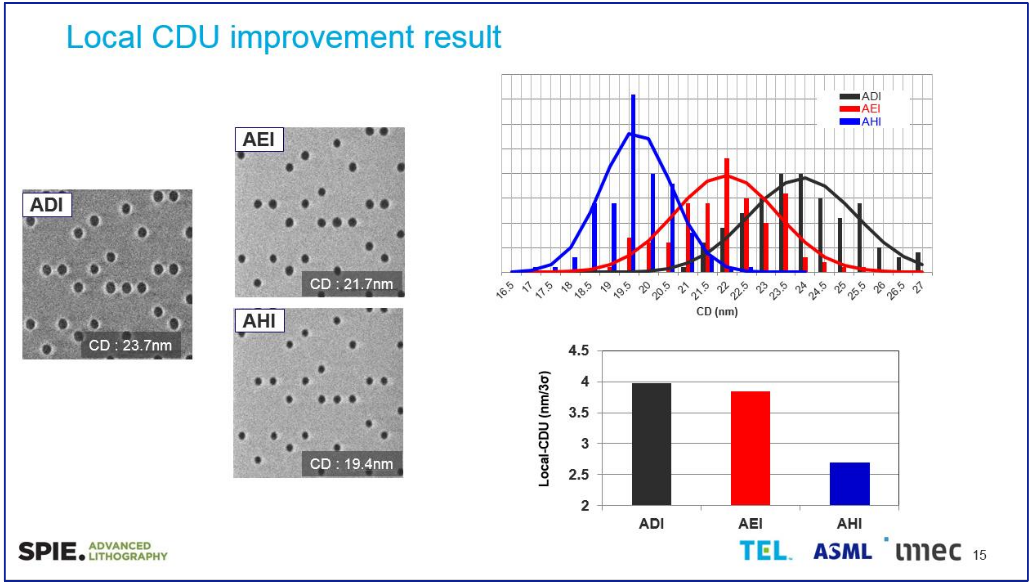


Much work is being done to reduce local variations with co-optimization of processes

Andrew Liang et. al., SPIE 2017



Hidetami Yaegashi et. al., SPIE 2017



keynote Mircea Dusa SPIE2019 paper 10963-1

Source Mask Optimization (SMO) minimizing global and local CD variation by superposing stochastics EPE band to cost function

15% reduction of local CDU without compromising other performance metrics

SMO (global) cost function through process variation:

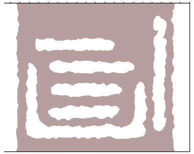
$$\mathrm{CF} = \sum_{\mathrm{pw,e}} w_{pw,e}(EPE^n + w\ PPE^n)$$

- **Edge Placement Error (EPE) and,**
- **Pattern Placement error (PPE)**

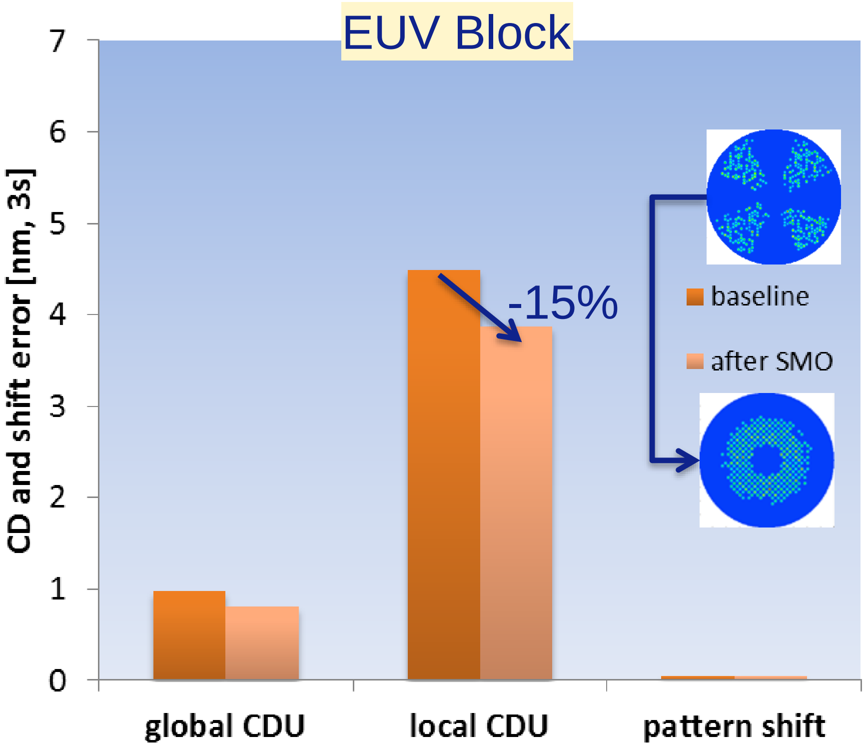
SMO superposes stochastics EPE band

- **Local CD variation**

$$\mathrm{sEPE} = \frac{a}{blur\_ILS^b}$$



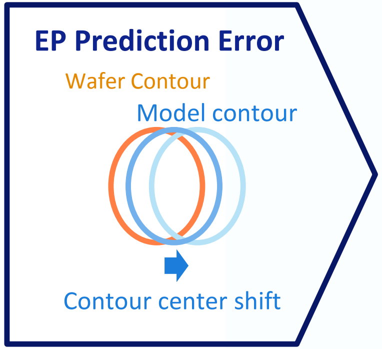
a and *b* calibrated to full stochastic resist model or wafer data



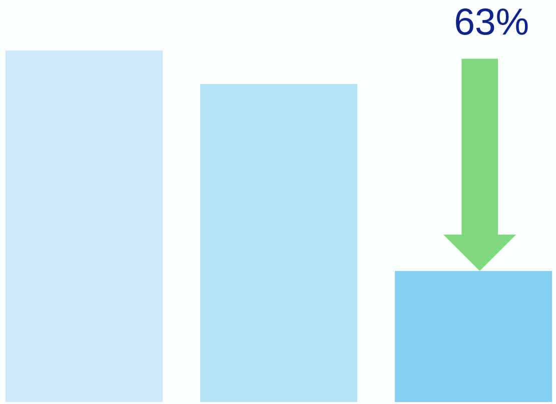
Stephen Hsu, et al, “EUV Resolution Enhancement Techniques (RET) for k1 0.4 and below”, SPIE 2015

Improving OPC accuracy with more pattern coverage by the use of massive metrology (fast eBeam system, accurate contour metrology) and deep learning models

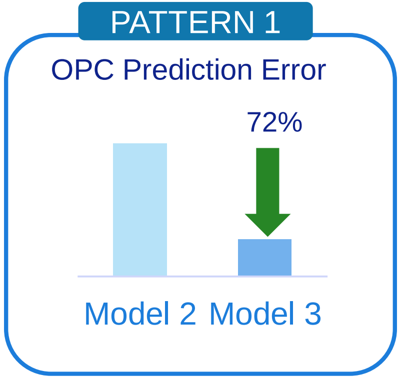
>60% OPC error reduction (~10% of EPE reduction)

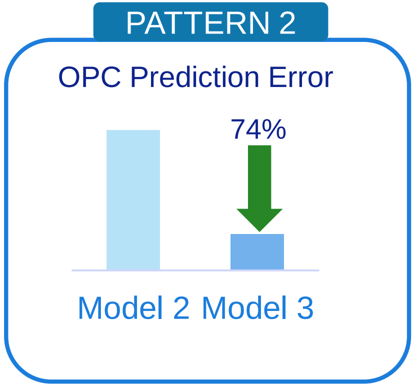


OPC prediction error reduction using MXP metrology & Newron model
(verified on >20,000 EP gauges)



1 CD Gauge only, FEM+ Model
2 CD Gauge only, Newron Model **(4x gauges)**
3 CD & EP Gauges, Newron Model **(9x gauges)**





Young-Seok Kim et. al.(SPIE 2019) Paper 10959-37

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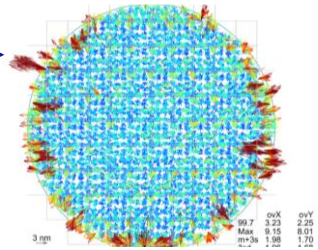
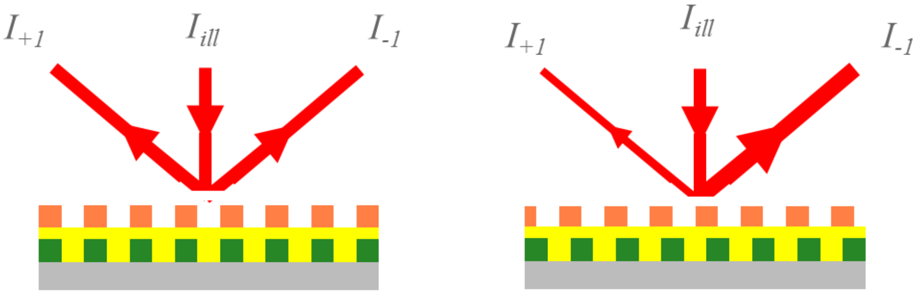


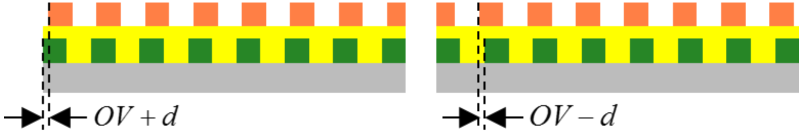
Concept of Diffraction-Based Overlay metrology (μDBO)



OV = 0: $A = I_{+1} - I_{-1} = 0$ OV ≠ 0: $A = I_{+1} - I_{-1} = K \times OV$

Overlay sensitivity K is stack-dependent and is eliminated with 2 "biased" gratings:

grating 1 grating 2



measured asymmetry

$$A_+ = K(OV + d)$$

measured asymmetry

$$A_- = K(OV - d)$$

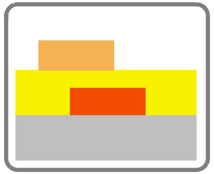
How to determine overlay OV:

$$\frac{A_+}{A_-} = \frac{K(OV + d)}{K(OV - d)}$$

$$A_+ = \left(\frac{OV + d}{OV - d}\right) A_-$$

A_+ as a function A_- is a straight line through 0.

Solve overlay from slope of this line:



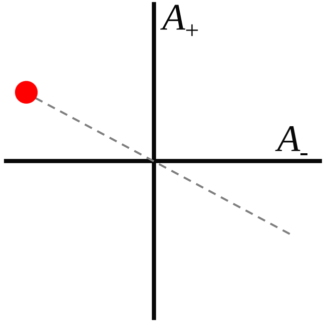
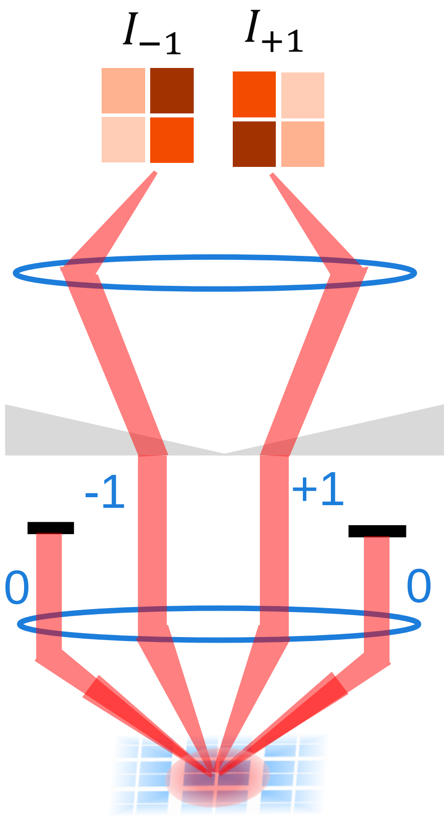


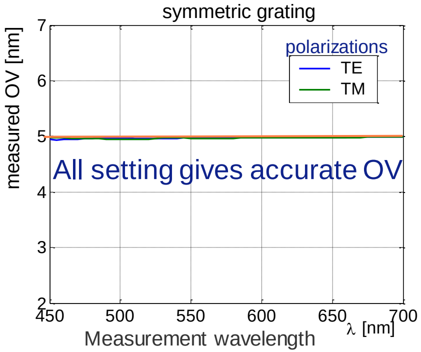
image-plane detection mode of YieldStar is used for μDBO



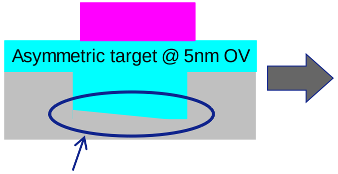
large spot illuminates the full target

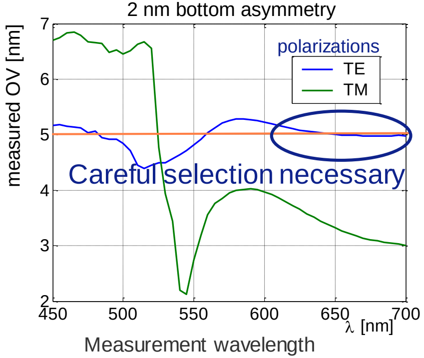
Target asymmetry is a challenge in overlay metrology

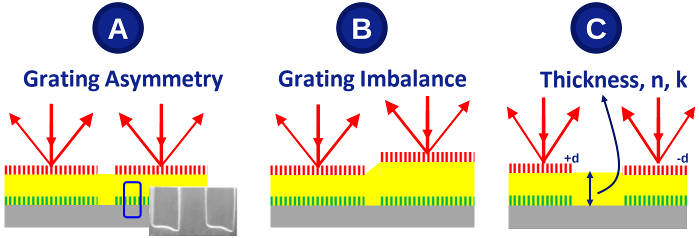
Presence of grating asymmetry, imbalance along with film variations trigger an overlay swing phenomena



Simulation using signal formation physics







In the absence of asymmetry → life is easier in OV metrology

But when **asymmetry is present**, each measurement site may be susceptible to an OV error

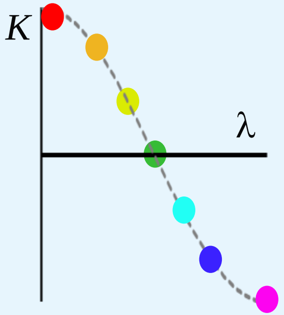
Multi wavelengths measurement was introduced to eliminate or minimize these errors

Multiple wavelengths are needed to deal with asymmetry

overlay sensitivity K also depends on wavelength

$$A_+(\lambda) = \boxed{K(\lambda)} \times (OV + d) + \Delta I$$

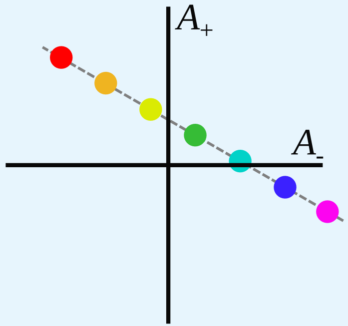
$$A_-(\lambda) = \boxed{K(\lambda)} \times (OV - d) + \Delta I$$

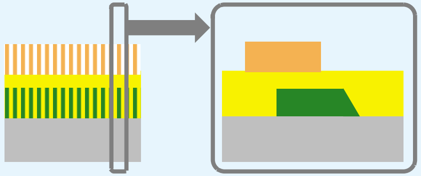


A plot of A_+ versus A_- for different wavelengths yields:

$$A_+(\lambda) = \left(\frac{OV+d}{OV-d}\right) A_-(\lambda) + C$$

Slope versus overlay

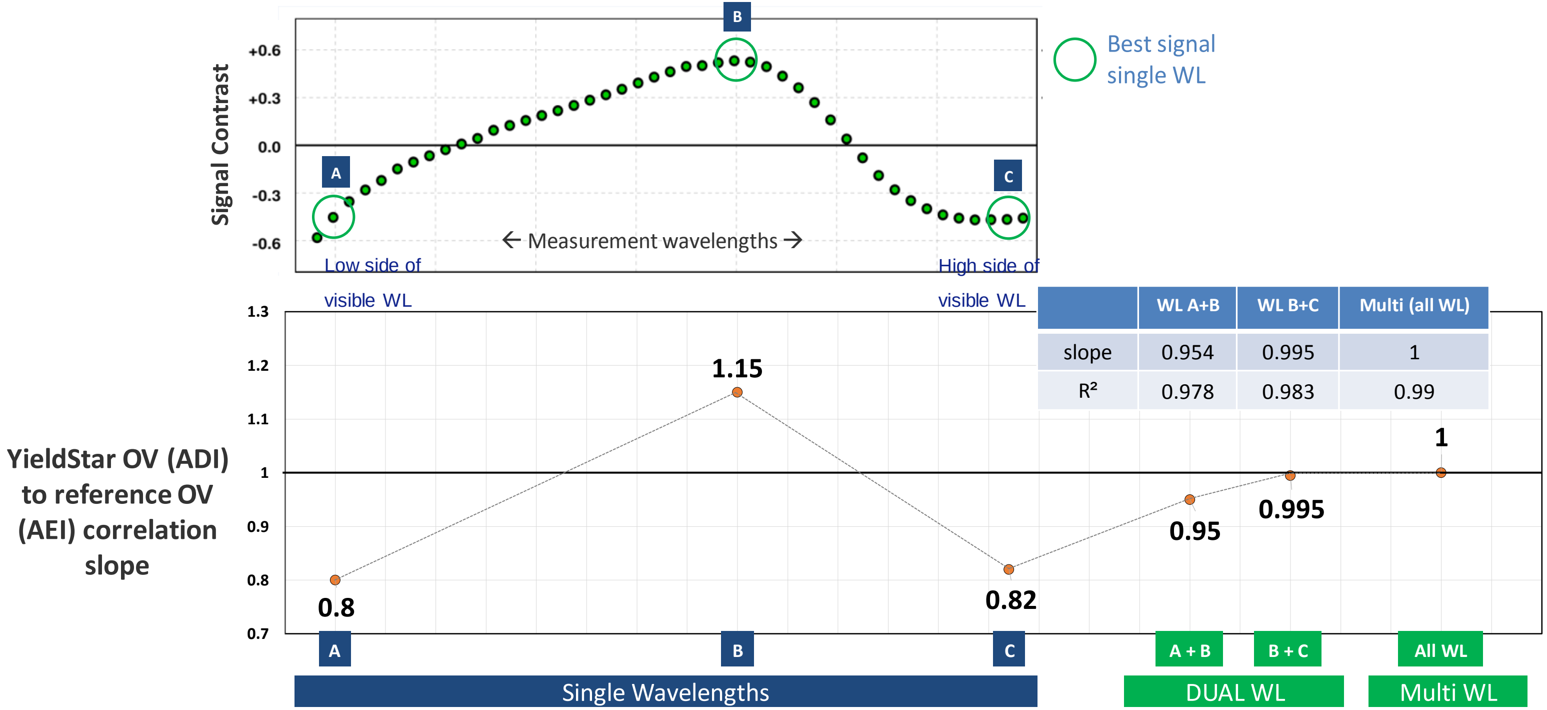




At least 2 wavelengths are needed to determine the slope (= OV)

Multi wavelength (WL) overlay providing better accuracy

Single WL OV (even @ signal peaks) do not match reference, but multi WL (and also dual WL) provide good match to reference OV

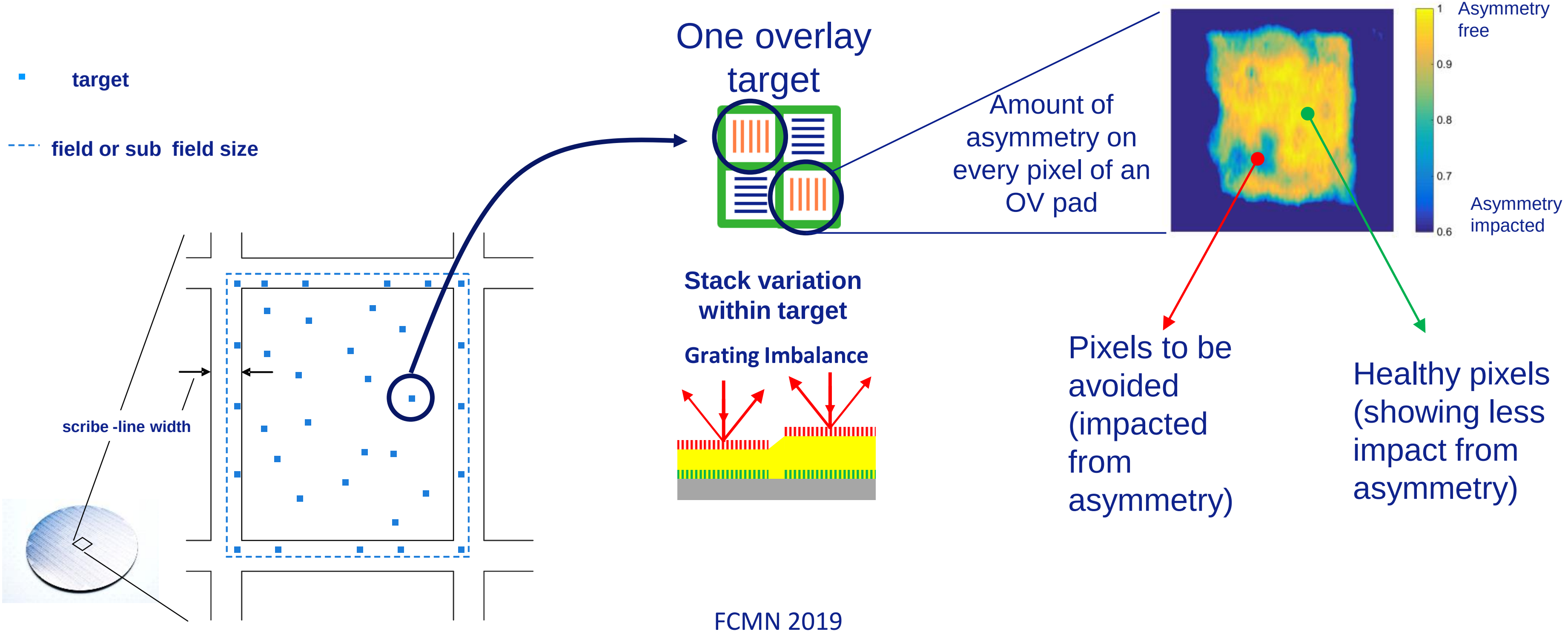


	WL A+B	WL B+C	Multi (all WL)
slope	0.954	0.995	1
R^2	0.978	0.983	0.99

These large asymmetries can exist at a very local target level

Stack variation between gratings (grating imbalance) can cause OV error

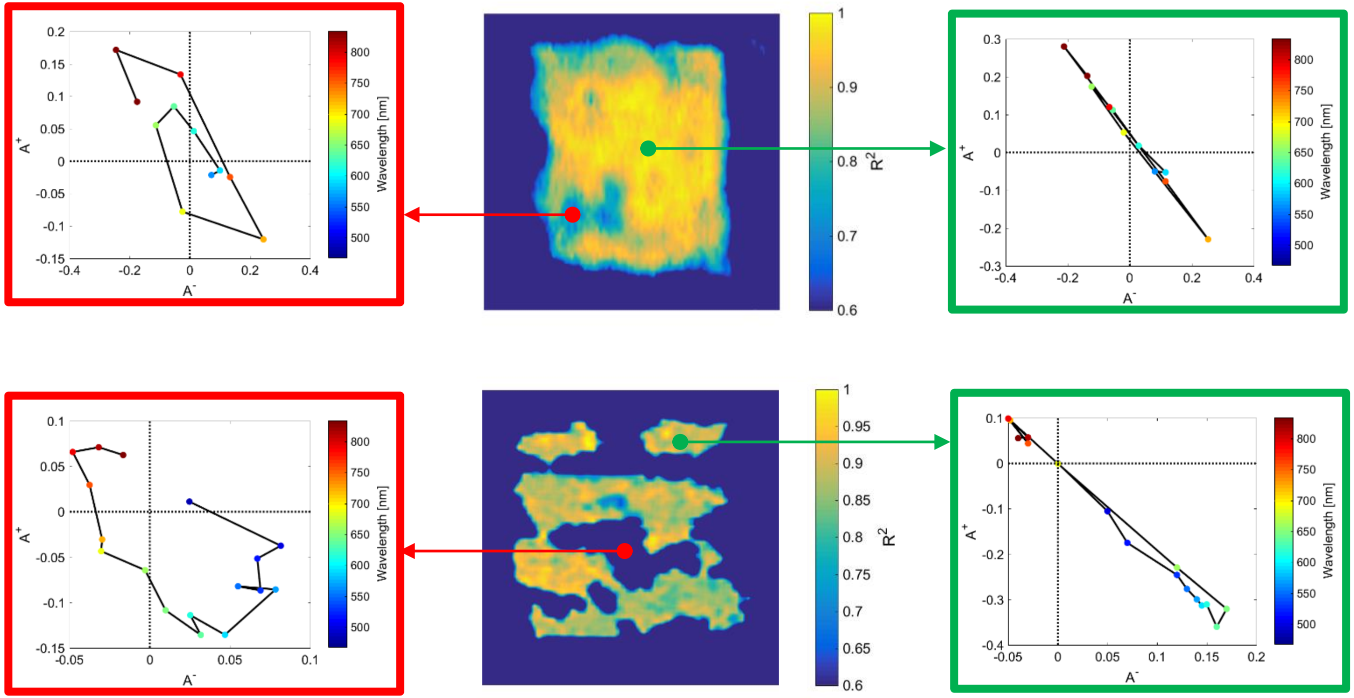
Even within a single grating of a target real-estate, not all pixels suffer from similar asymmetry



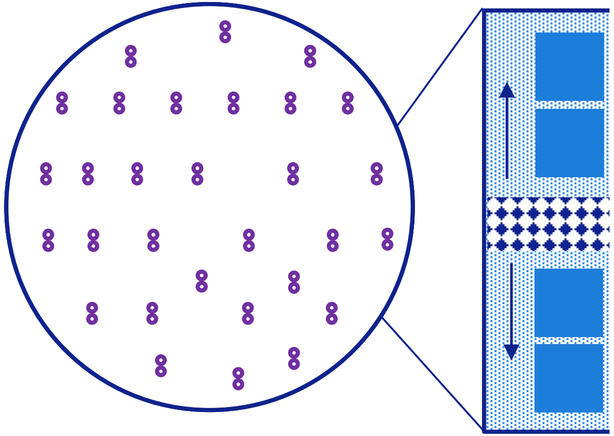
Intra-target variability of asymmetry observed on multiple product layers

R^2 of linear A+/A- fit on every pixel of OV pad clearly shows intra-target variability

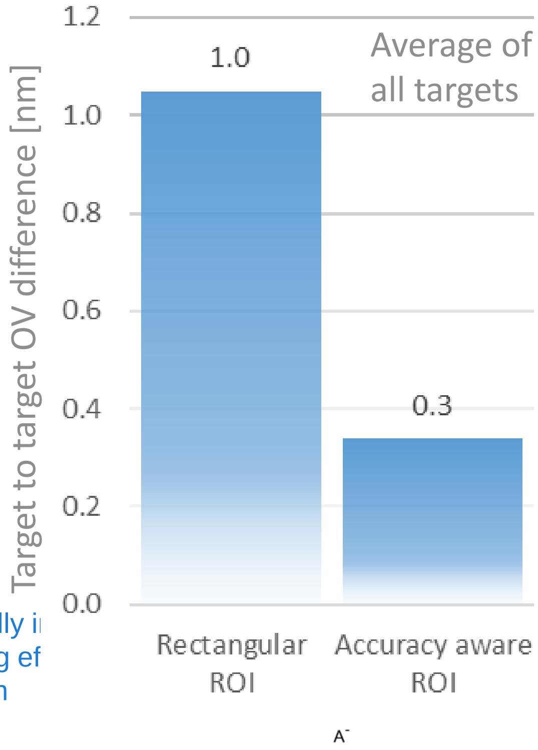
A “Pixel mapping” algorithm searches for “low-asymmetry” areas in a grating



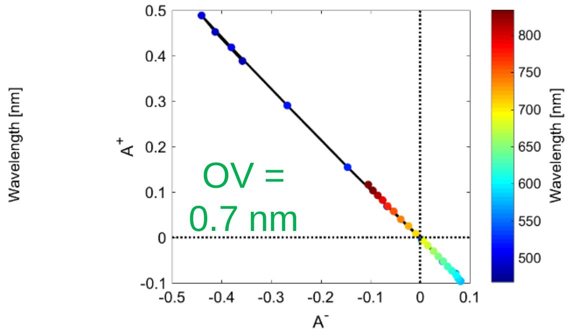
Pixel mapping improving accuracy on dedicated accuracy test wafer

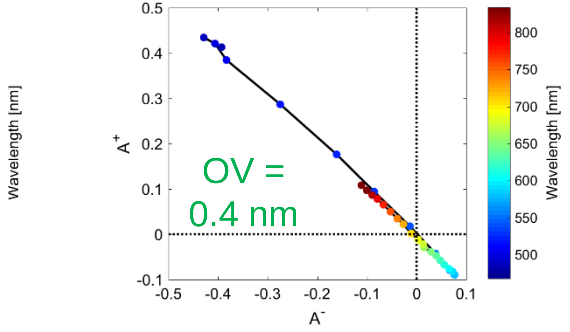


Intentionally i
processing ef
Y-direction



Accuracy aware ROI



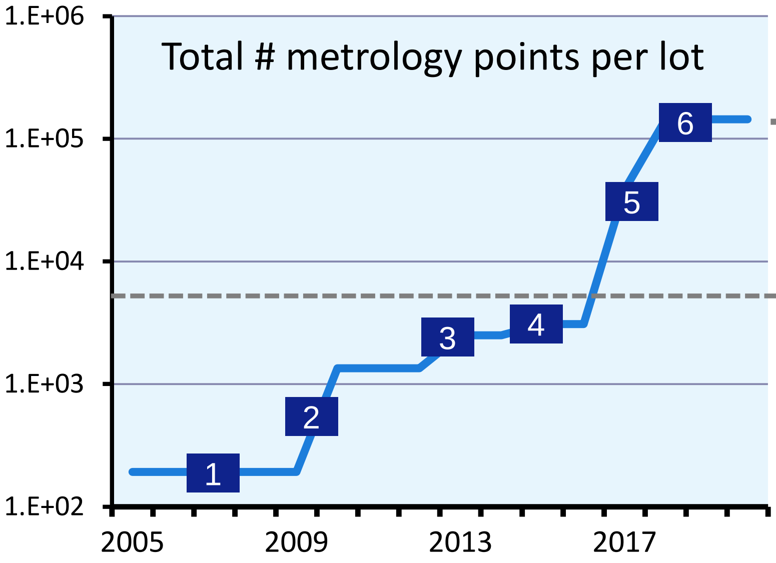


Pixel mapping effectively removes the target to target overlay delta between 2 neighboring targets

Now as we discussed the accuracy in overlay metrology, let’s move on to see how to use those accurate measurements in <u>process correction</u>

OV roadmap continues to drive the need for higher metro sampling (w/ high order correction)

Computational metrology to mitigate this increase in sampling



> 20× gap

Computational metrology

↑

Use process models and scanner knowledge to create dense wafer map

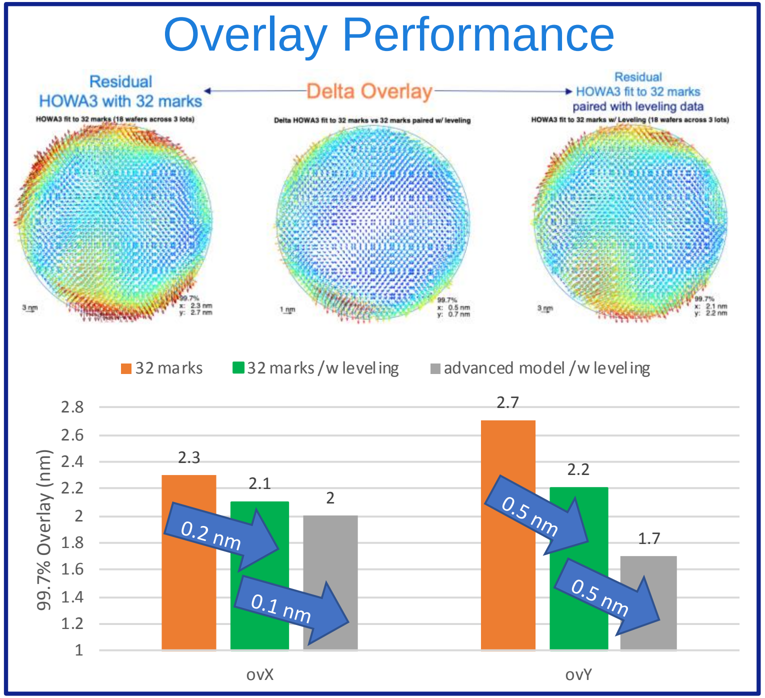
Practical # metro points per lot with high productivity metro tools

1	Inter-field control per scanner chuck
2	+ intra-field control with 6 parameters
3	Intra-field 6 parameters → 12 parameters
4	Intra-field 12 parameters → 19 parameters
5	+ wafer level control
6	Intra-field 19 parameters → 38 parameters

Combining Leveling and Alignment results in a dense overlay grid that can be used for better OV control

- Leveling paired with alignment metrology improves overlay performance of HOWA3 model

- Using of the spatial frequency between enhanced alignment and its corresponding measure overlay, we can realize additional improvements to performance



Emil Schmitt-Weaver et. al., SPIE 2019; Paper 10961-7

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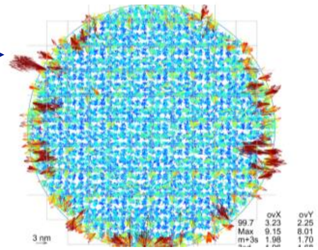
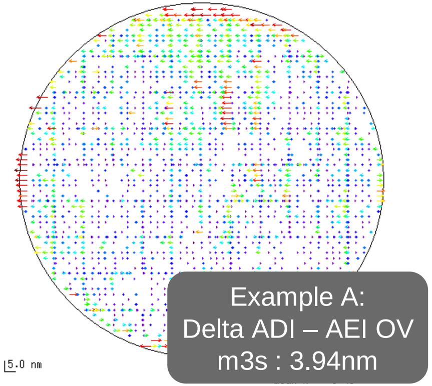


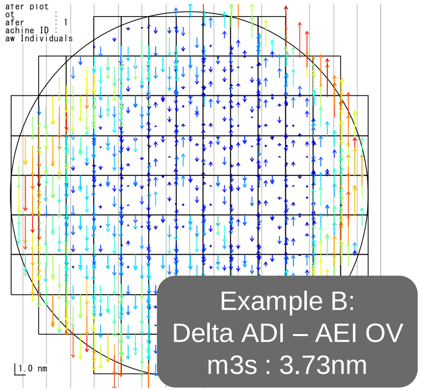
Device overlay after etch

Need to address the delta between after develop overlay (measured on OV targets) vs. after etch overlay (measured on device)

- Calibrating for the offset between ADI to AEI is necessary to take care of
  - Target to device offset
  - Etch bias (if any)
  - Stress release
  - …

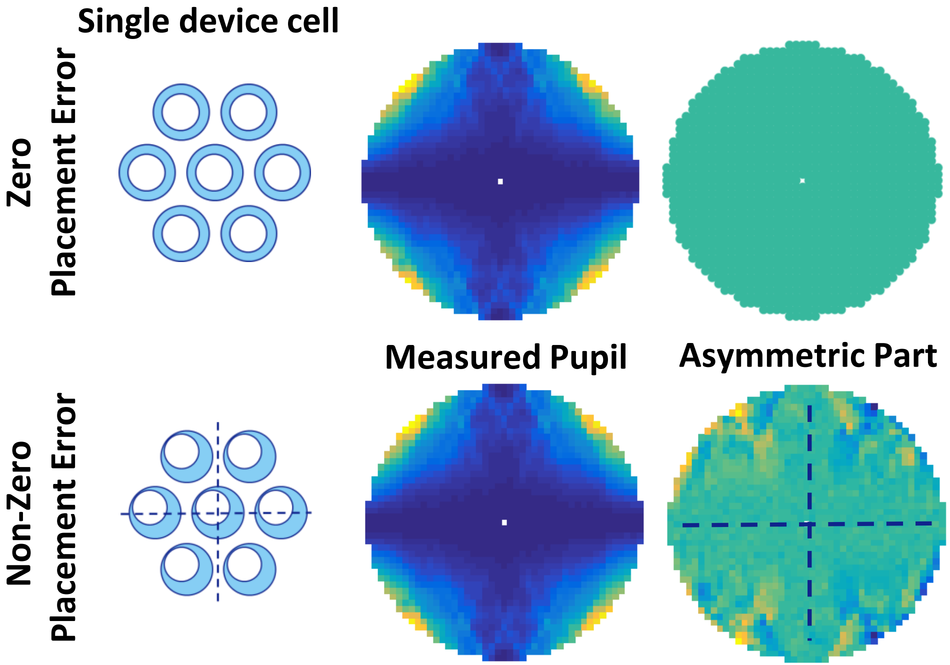


- Even though computational metrology can predict extreme dense overlay map at ADI, it still needs calibration / validation using real measured data on device after etch (AEI OV)
  - Needs hyper-dense AEI OV measurement to capture the true device OV fingerprint

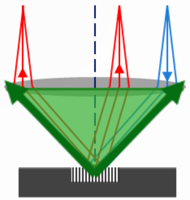


YieldStar In-Device Metrology (IDM) Overlay Concept for Angle-Resolved Scatterometry

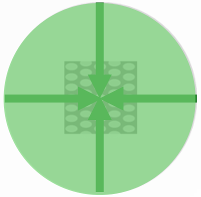
Overlay Principle



High 0.95 NA Continuous Angles



All Azimuthal Directions



Overlay asymmetry signal fully captured with YieldStar's unique design within one acquisition

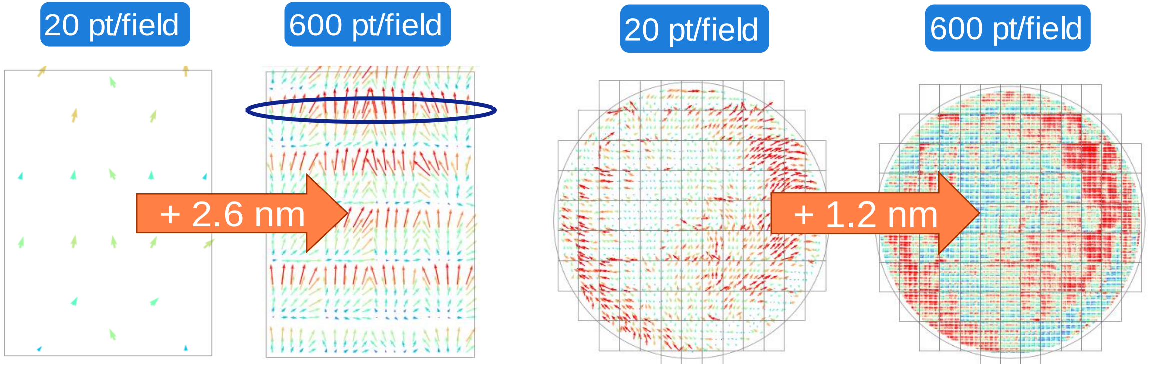
Overlay signal typically at the edge of the pupil

AEI measurement directly on device enables hyper-dense overlay information revealing more accurate picture of wafer and field fingerprint

- Measurement directly on device removes the limitation on the number of dedicated targets that needs to be placed on a product mask

Power of AEI optical metrology:

- Measurement directly on device shows the need for sampling density
- Sparse sampling misses high frequent intra-field behavior and misses much detail in wafer fingerprint



Average field overlay

Average wafer overlay

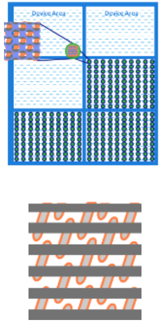
HG Lee, J. Karssenberg et. al. (SPIE 2019) Paper 10959-6

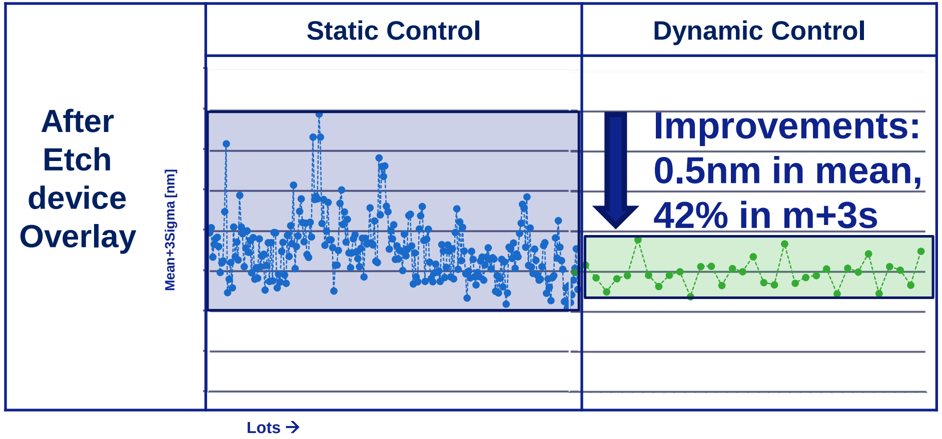
A dynamic control using after etch overlay (measured on device) showing benefit over static control; this means:

1. ADI vs. AEI overlay delta is varying run-time

2. Need a high speed after etch overlay metrology for this feedback control

Measured by optical scatterometry





Conclusions

- Main contributors to EPE are Local CD error (OPC error, stochastics) and Overlay

- With continued shrink (scaling) the local error starts to dominate
  - Co-optimization of processes (litho, etch, deposition) needs to be done to minimize this local error
  - Important to quantify the remaining stochastic part so it can be compensated by tightening the other budget items, such as overlay

- Need to do everything possible to improve overlay
  - Improve accuracy in overlay metrology by multi wavelength
  - High order process correction in overlay (using device overlay information):
    - Increase in sampling to be mitigated by computational metrology where scanner metro and OV metro are used in conjunction to create dense overlay maps at ADI (can be further boosted by incorporating pre-litho inputs)
    - Best overlay control obtained by OV metrology feedback coupled with scanner metrology feedforward
    - Device overlay is addressed by calibration / validation using dense measured data on device after etch (AEI OV)

- So tough road … yes, but a significant collaborative work is done and being done in the industry to effectively address the challenge in device overlay and EPE

Thank you !