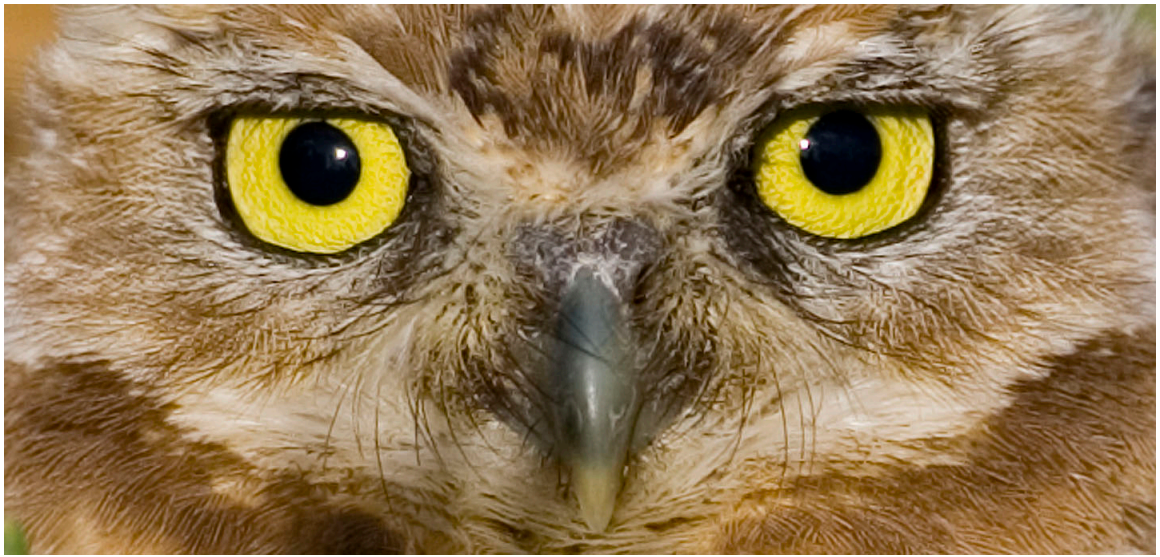
Moore's Law in a Neuromorphic World



g dan hutcheson

The 2nd inspection revolution

KLA 2020, Circa 1984

The tool that sparked **the yield management revolution**

KLA

KLA 2020 WAFER INSPECTOR

"The Measured Difference"

KLA's Revolutionary system takes you from human judgement to automated measurement.

Controlling a process is measuring the difference between a variable and a reference. The key words are *measured* and *difference*. A semiconductor process can approach a 100% yield by *"measuring the differences"* in the process and changing the parameters which control the fabrication system.

Today, people provide the information for controlling a semiconductor process. But is the accuracy and timeliness of the human "measured difference" good enough to control the fabrication of today's circuits? And what about tomorrow's circuit requirements?

Because of the need for a clean environment, are humans part of the process problem?

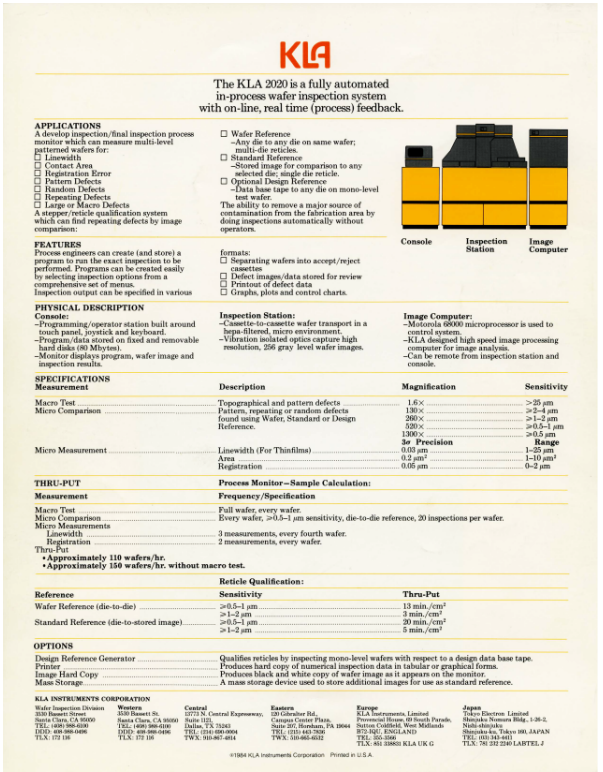
Now, the KLA 2020 Wafer Inspector provides solutions to these critical questions by allowing you to measure the differences in the most important lithographic process variables. This includes Critical Dimension—Linewidth, Registration and Area—and Defects—Random, Repeating and Pattern. And the system allows all of this without operator contamination.

Who would have thought that your best process engineer could be an inspector? With the multifunction KLA 2020, your best engineer can easily program the inspections to be executed—at the right location, the right frequency and to the correct specifications.

The KLA 2020 is not only fast and accurate, it can keep up with the output of several of your fastest steppers or printers. The results provided by the Wafer Inspector are statistically more precise, more consistent, and more timely than is possible with other methods in practice today.

There is much more that you should know about the "measured difference" from KLA Instruments Corporation. It could make a major difference to improving your process . . . and your profits.

Call or write today for our brochure which details information about the KLA 2020 Wafer Inspector.



KLA

The KLA 2020 is a fully automated in-process wafer inspection system with on-line, real time (process) feedback.

APPLICATIONS

A develop inspection/final inspection process monitor which can measure multi-level patterned wafers for:

- ☐ Linewidth
- ☐ Contact Area
- ☐ Registration Error
- ☐ Pattern Defects
- ☐ Random Defects
- ☐ Repeating Defects
- ☐ Large or Macro Defects

A stepper/reticle qualification system which can find repeating defects by image comparison:

- ☐ Wafer Reference
  –Any die to any die on same wafer; multi-die reticles.
- ☐ Standard Reference
  –Stored image for comparison to any selected die; single die reticle.
- ☐ Optional Design Reference
  –Data base tape to any die on mono-level test wafer.

The ability to remove a major source of contamination from the fabrication area by doing inspections automatically without operators.

Console | Inspection Station | Image Computer

FEATURES

Process engineers can create (and store) a program to run the exact inspection to be performed. Programs can be created easily by selecting inspection options from a comprehensive set of menus.

Inspection output can be specified in various formats:

- ☐ Separating wafers into accept/reject cassettes
- ☐ Defect images/data stored for review
- ☐ Printout of defect data
- ☐ Graphs, plots and control charts.

PHYSICAL DESCRIPTION

Console:
–Programming/operator station built around touch panel, joystick and keyboard.
–Program/data stored on fixed and removable hard disks (80 Mbytes).
–Monitor displays program, wafer image and inspection results.

Inspection Station:
–Cassette-to-cassette wafer transport in a hepa-filtered, micro environment.
–Vibration isolated optics capture high resolution, 256 gray level wafer images.

Image Computer:
–Motorola 68000 microprocessor is used to control system.
–KLA designed high speed image processing computer for image analysis.
–Can be remote from inspection station and console.

SPECIFICATIONS

Measurement	Description	Magnification	Sensitivity
Macro Test	Topographical and pattern defects	1.6×	>25 μm
Micro Comparison	Pattern, repeating or random defects found using Wafer, Standard or Design Reference.	130×	≥2–4 μm
		260×	≥1–2 μm
		520×	≥0.5–1 μm
		1300×	≥0.5 μm
		3σ Precision	**Range**
Micro Measurement	Linewidth (For Thinfilms)	0.03 μm	1–25 μm
	Area	0.2 μm²	1–10 μm²
	Registration	0.05 μm	0–2 μm

THRU-PUT

Process Monitor—Sample Calculation:

Measurement	Frequency/Specification
Macro Test	Full wafer, every wafer.
Micro Comparison	Every wafer, ≥0.5–1 μm sensitivity, die-to-die reference, 20 inspections per wafer.
Micro Measurements	
Linewidth	3 measurements, every fourth wafer.
Registration	2 measurements, every wafer.

Thru-Put
- **Approximately 110 wafers/hr.**
- **Approximately 150 wafers/hr. without macro test.**

Reticle Qualification:

Reference	Sensitivity	Thru-Put
Wafer Reference (die-to-die)	≥0.5–1 μm	13 min./cm²
	≥1–2 μm	3 min./cm²
Standard Reference (die-to-stored image)	≥0.5–1 μm	20 min./cm²
	≥1–2 μm	5 min./cm²

OPTIONS

Design Reference Generator	Qualifies reticles by inspecting mono-level wafers with respect to a design data base tape.
Printer	Produces hard copy of numerical inspection data in tabular or graphical forms.
Image Hard Copy	Produces black and white copy of wafer image as it appears on the monitor.
Mass Storage	A mass storage device used to store additional images for use as standard reference.

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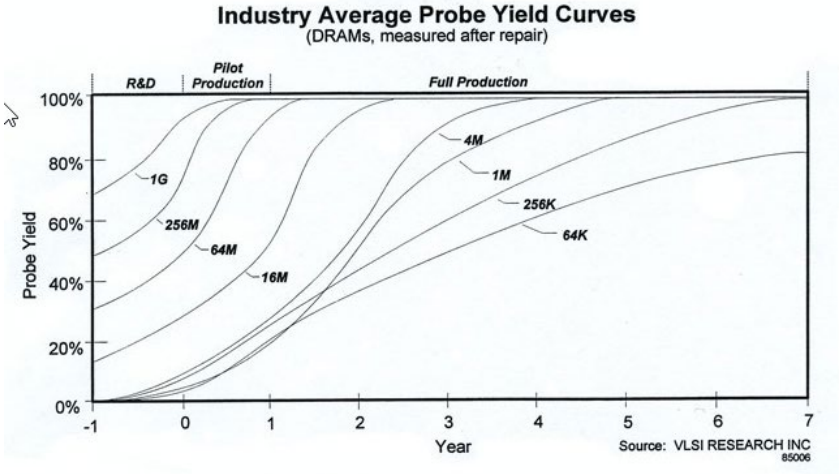
Early 90s: The Birth of Yield Management

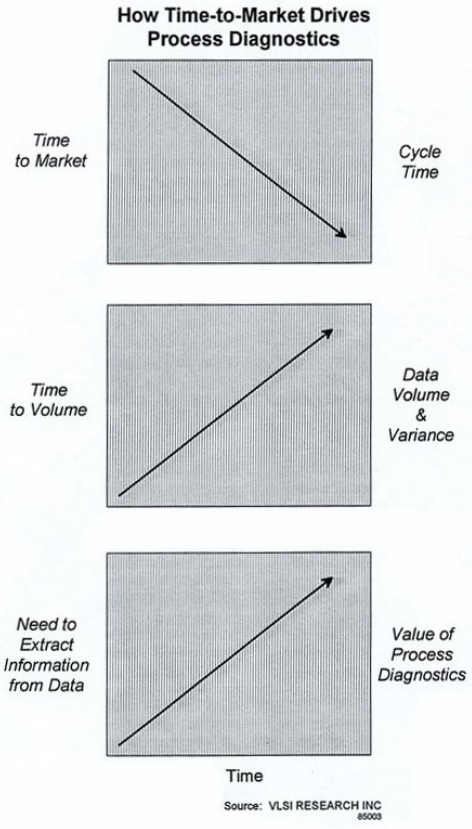


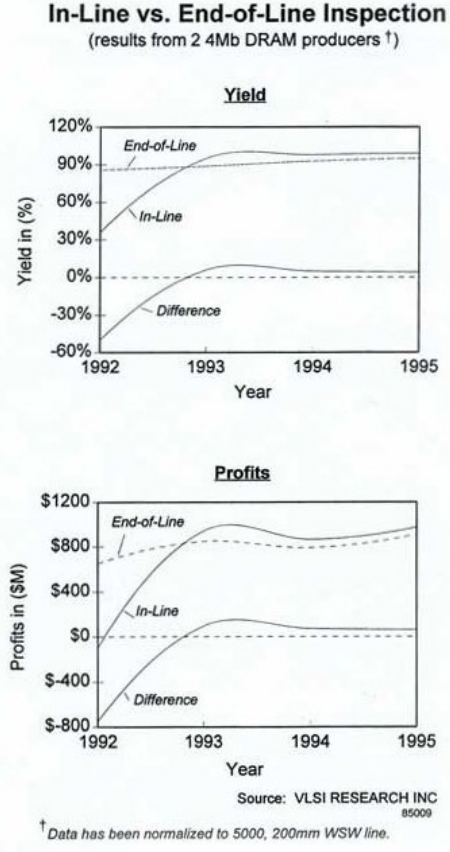
Process Diagnostics Helps Speed . . . Which . . .

- Time-to-Results
- Time-to-Market
- Time-to-Value
- Time-to-Money

- Raises Yields
- Raises Profits
- Raises Return-on-Assets
- Raises Your Companies Stock Price

Source: VLSI RESEARCH INC
85011





Source: https://www.chiphistory.org/109-change-in-chip-making-and-how-it-is-driving-process-diagnostics

Metrology Time Machine: *As the 1990s close,*

*you still see it as **humans clustered around a tool …***

but it's data not images that are being looked at

We learned that Process Control increases the value of wafers out

Engineering Analysis

Problem Solving:
- Quickly find and fix sources of yield loss
- Systematically improve yield
- Characterize new process
- Yield ramp

Facilitate faster yield ramp

Identify systematic defects

Perform high sampling rates

Inline Monitoring

Yield Learning:
- Find all defect sources in a process flow
- Reduce baseline defectivity
- Identify process excursions quickly

Sensitivity to capture all defect types

Productivity to produce the data necessary to identify process issues

Flexibility to identify the process layer that is the source of defects (yield correlation)

Process & Tool Monitoring

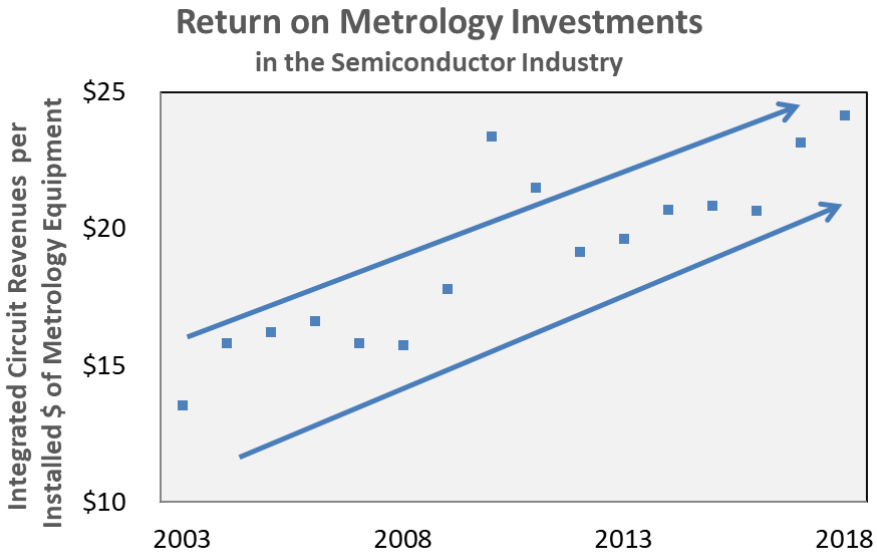
Productivity:
- Catch specific process tool, cell, or module excursions
- Identify good/bad tools
- Disposition of good/bad wafers

Identify bad process, bad tool, bad chamber in production

Inspector Requirements
- Sensitivity and selectivity
- High throughput
- Easy to use
- Low cost of ownership

Yield Management's ROI is Enormous

- $24 of IC sales returned for every $1 of installed Process Diagnostic equipment in 2018
  - Up 73% since 2003
- This was critical part of enabling Moore's Law to continue



Moore's Law and its Allies

Component density **doubles**
every two years

due to

geometry shrinks

for roughly the

same areal cost

Gordon Moore - 1975

Gordon Moore in 1975 Source: Intel

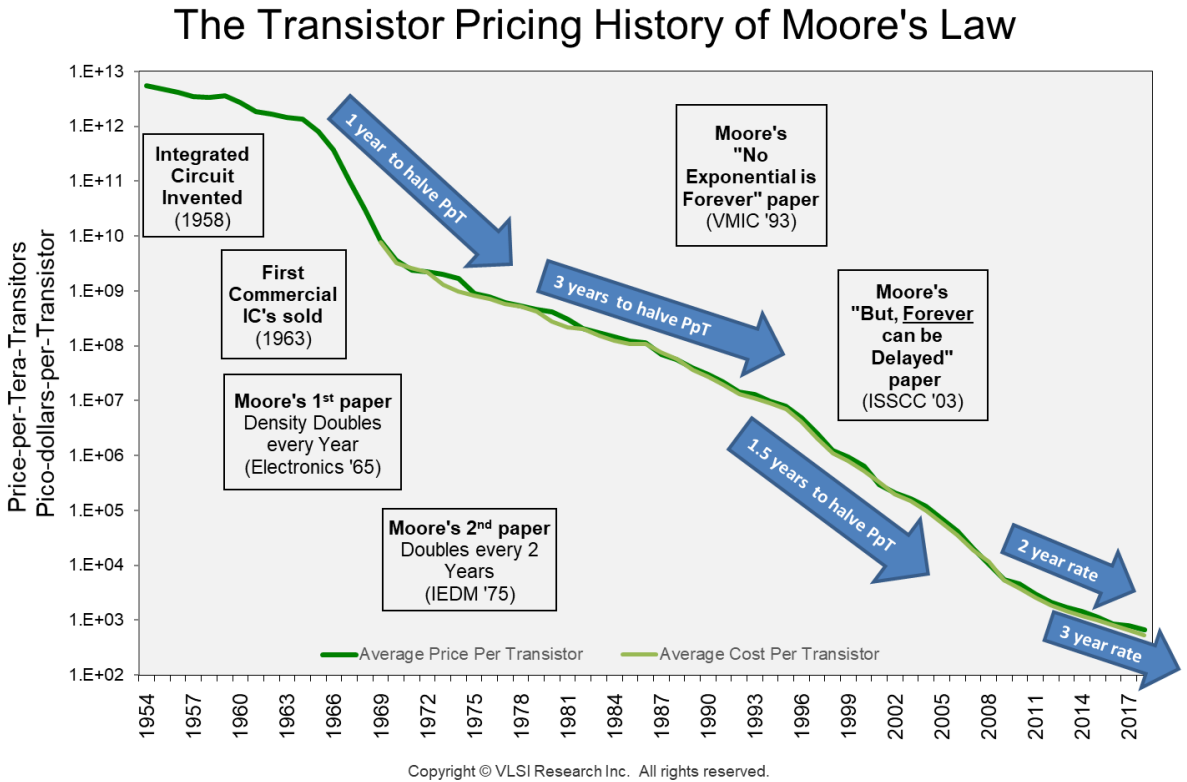
Value Growth in Semiconductors is created through **FIVE** mechanisms:

- Moore's Law: Economic Performance
- Dennard's Law: Device Performance
- Koomey's Law: System Performance
- Metcalfe's Law: More Users
- Emergent Behavior: Innovation

Is it time for a new revolution?

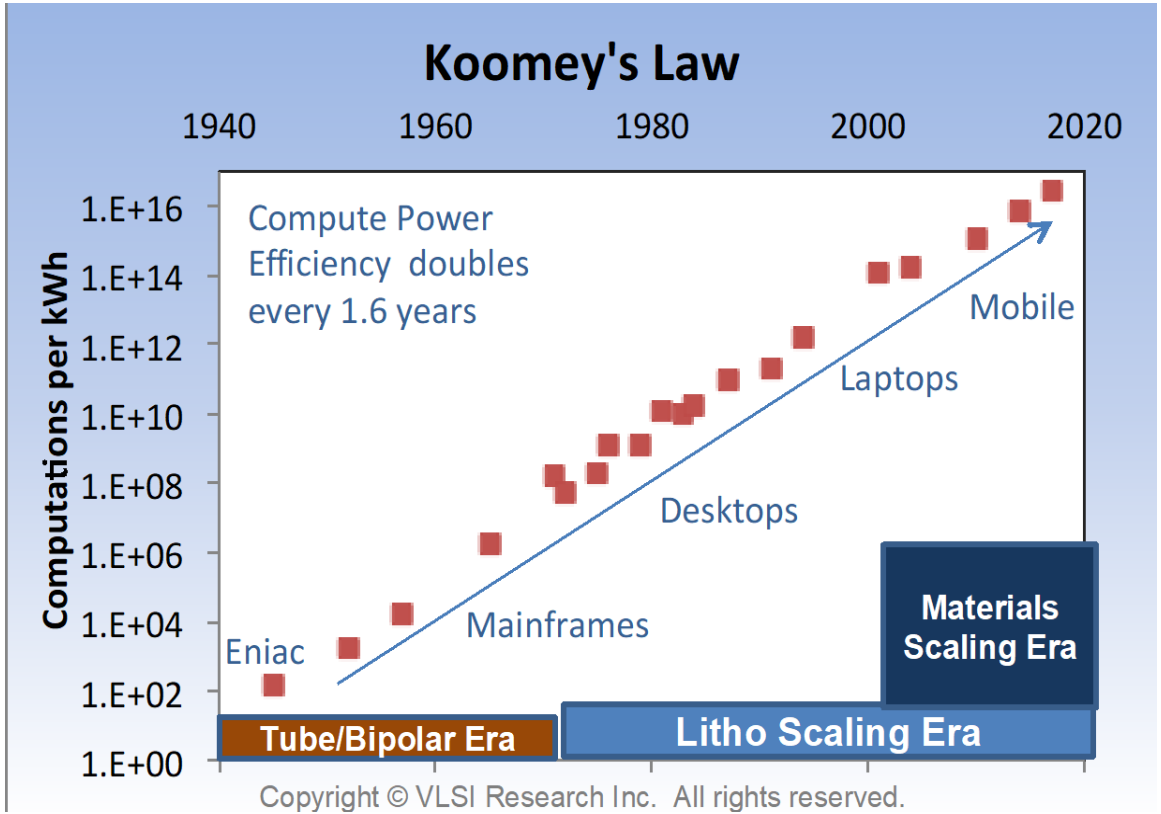
- Moore's Law accelerated after the introduction of yield Management
- It is slowing again

What do we do if it stops?



We can't stop

- Koomey's Law: Compute Power Efficiency Doubles
- Made possible by …
  - Better architectures
  - Faster & more power stingy transistors and interconnect
- We need this to solve even bigger problems
- Leads us to new compute architectures
  - neuromorphic
    - even quantum



Compute Architecture 101

- **von Neuman Architecture**
  - John von Neuman created in 1945
  - Any stored-program computer
    - Processing unit:
      - ALU + registers
    - Control unit:
      - Instruction resister + program counter
    - Memory unit
      - For data & instructions
    - Instruction and data fetch cannot occur simultaneously…"**bottleneck**"
      - Because both share the same bus

Compute Architecture 101

- **Neuromorphic Architectures**
  - Carver Mead coined NM in 1990
  - Biologically inspired networks or …
    - Mostly still deep in research
    - Holy grail is a memory-centric architecture
      - But Analog
      - Not Digital
    - "Think outside the von Neuman box"
  - Artificial networks that run on a von Neuman Architecture
    - Most commercial AI systems are in this class
      - Don't be fooled, a GPU is still a von Neuman Architecture

AI Drivers: **Data & Memory** are the **Food & Water** of AI systems

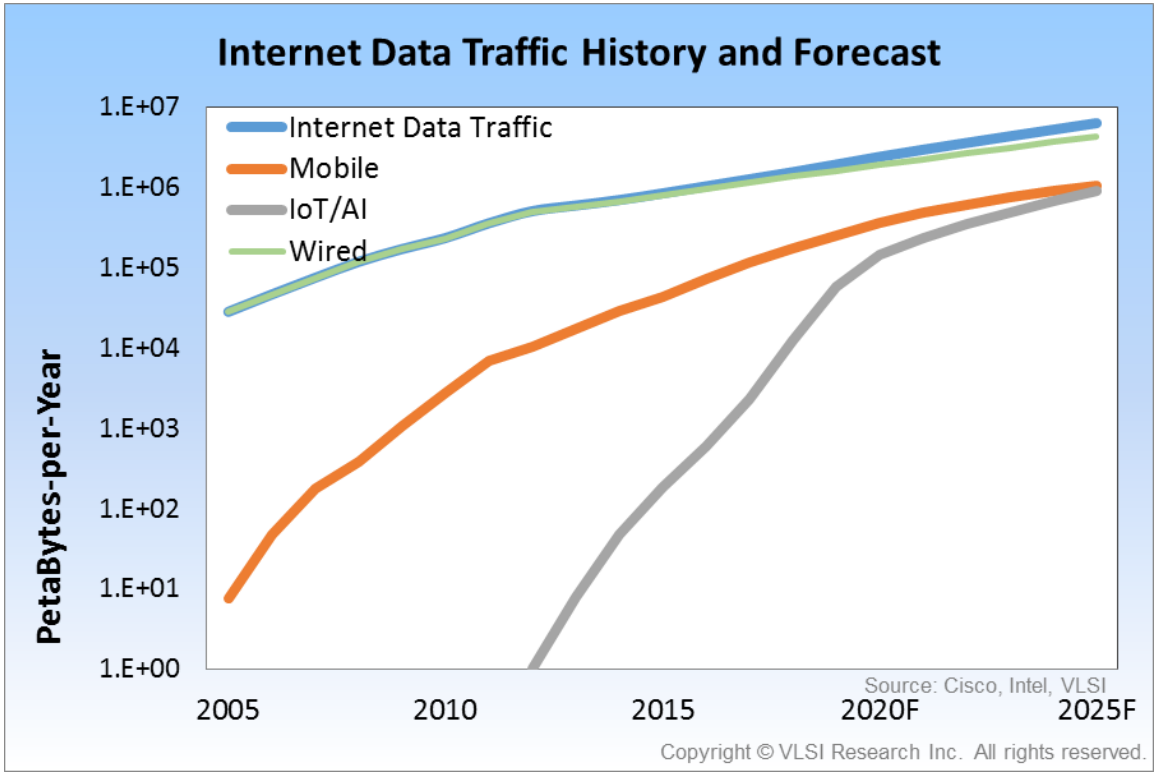
Data growth is exponential

Why it will continue?

The

History of Progress is all about Information Storage and Retrieval

Self-Driving cars have to crash into trees a thousand times before they learn that it's a bad idea

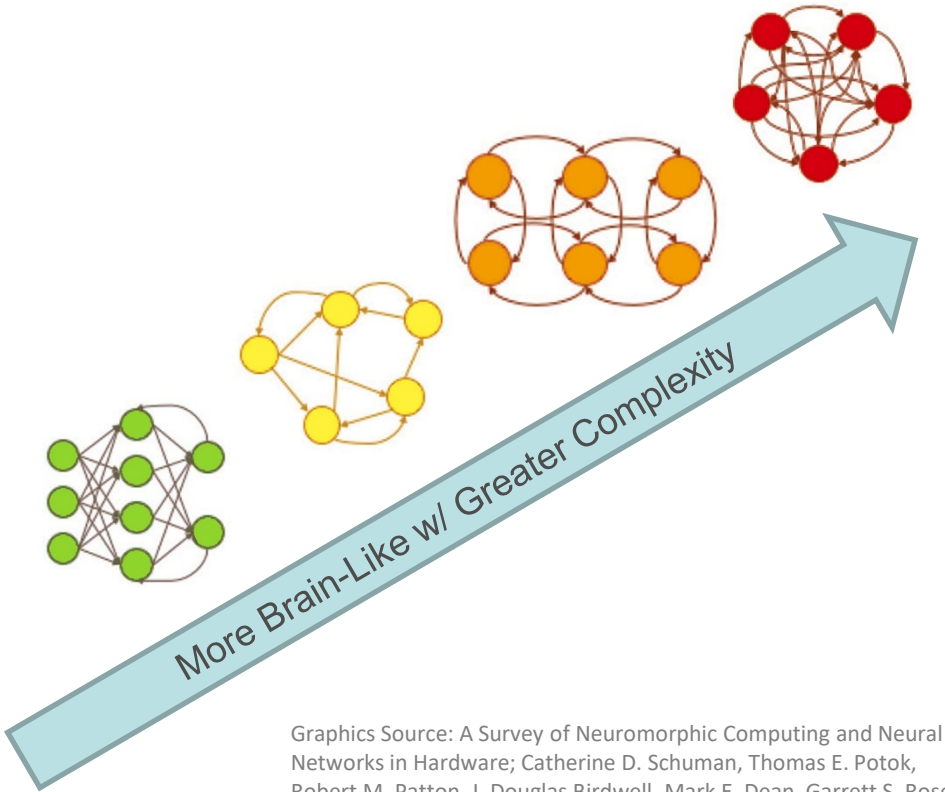


AI: Cognitive … or why Smart is the new dumb

- What's changed:
  - Smart is simply a different interface
  - Cognitive is when hardware understands borderline cases
- For example
  - Smart is asking, ‘play “I can’t get no satisfaction”’
    - Uber deep learning AZ accident
    - Google cats vs. dogs
  - Cognitive is asking, “tell me if Julie comes back after curfew”[2]
    - That change is a revolution in what needs to be done with silicon

CA 101: **Deep-Learning Network Models**

- Fully-Connected Recurrent
- Locally-Connected Recurrent
- Sparsely-Connected Recurrent
- Feed-Forward with some Recurrence
- **Feed-Forward**
  - Most common in the wild



Graphics Source: A Survey of Neuromorphic Computing and Neural Networks in Hardware; Catherine D. Schuman, Thomas E. Potok, Robert M. Patton, J. Douglas Birdwell, Mark E. Dean, Garrett S. Rose, James S. Plank, arXiv:1705.06963v1

AI 101: Semiconductor Needs

Training:

- Super Computers
- GPUs
  - Massively parallel
  - Ideal for matrix math
- Needs heterogeneous integration
  - With lots of HBM
- FPGAs
  - For testing various algos, models, and network topologies

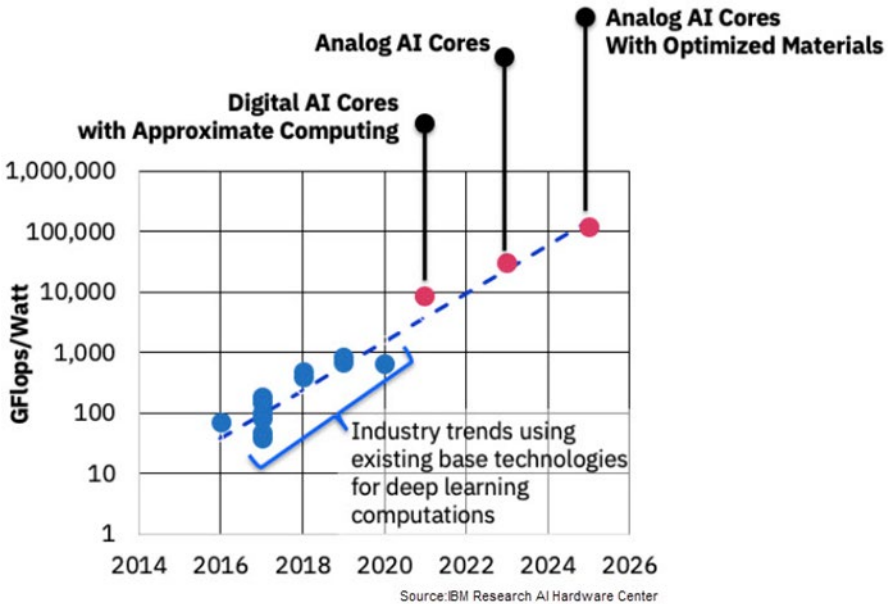
AI 101: Semiconductor Needs

Deployment:

- Custom ASICs
  - Needs heterogeneous integration
  - Needs lots of volume to justify cost
  - Or when system-level profits or subsidies can offset the costs
    - APT's SpiNNaker
    - IBM's TrueNorth
    - Google's Tensor TPU
    - HP's Memristor
- FPGAs
  - Quick solution when volumes are low
  - But expensive and high power needs

The AI Roadmap needs manufacturing innovation

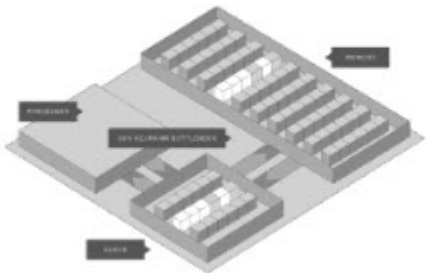
- AI moves from today's GPU/CPU architectures through …
- Digital AI cores and onto …
- Analog AI Cores
  - AKA in Memory Computing (iMC)



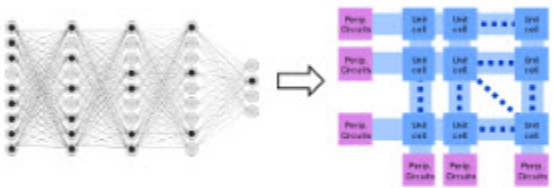
Analog in-Memory Computing

The von Neumann Bottleneck is real: Google's AlphaGo needed >10,000X the power of Lee Sedol's brain to beat him at Go. iMC helps solve this, but new materials and in-process inspection methods will be needed.

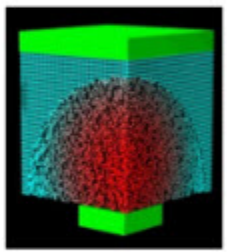
Eliminate the Von-Neumann Bottleneck



Map DNNs to analog cross-point arrays



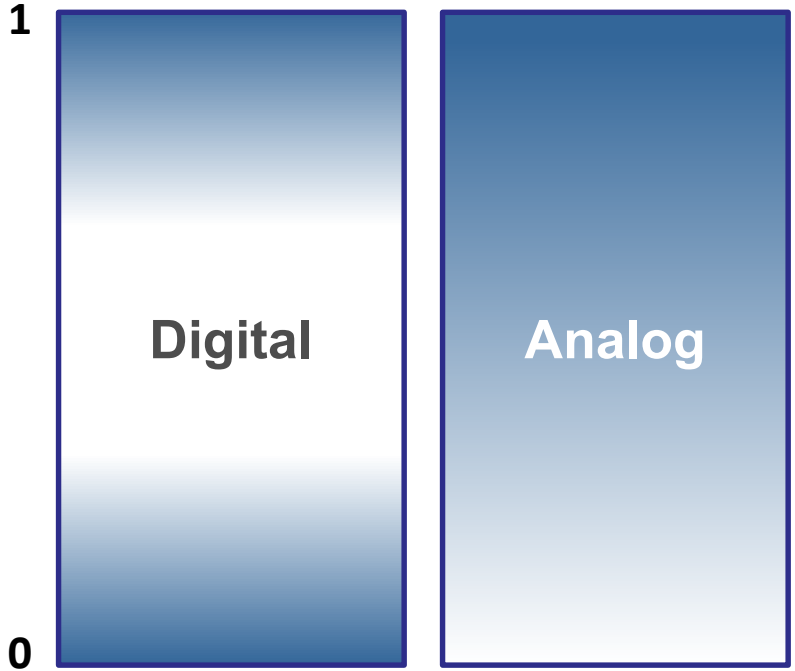
NVM materials in array crosspoints to store weights



Source:IBM Research AI Hardware Center

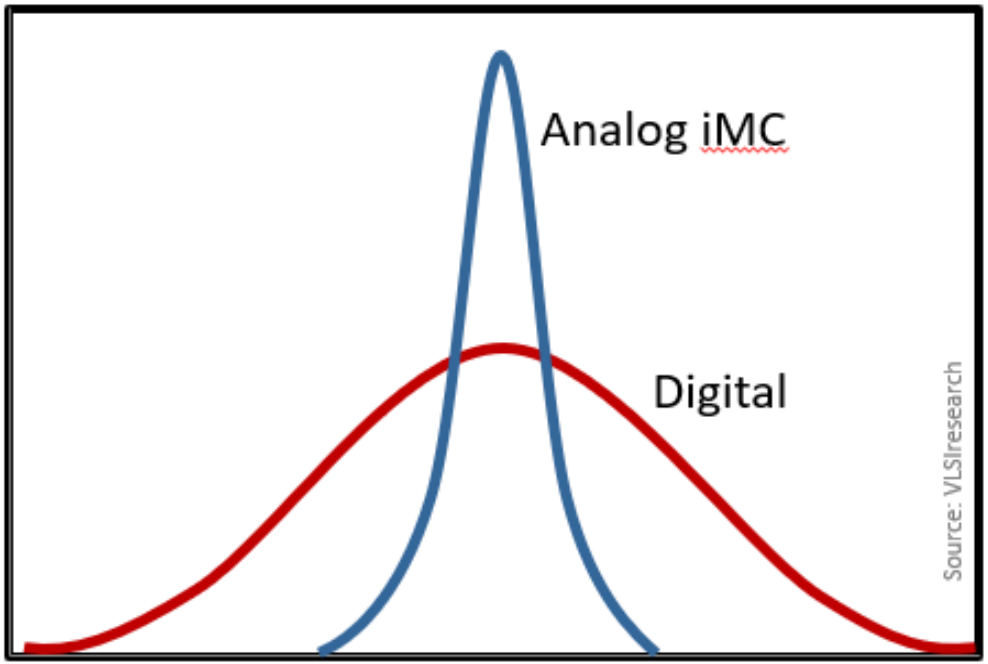
The iMC neuromorphic quality challenge

- Moore's law was about more transistors, all of which only have 2 states
  - Digital Transistors can work with sloppy controls, as long as an 'eye' can be made out
- Analog memory virtually has an infinite number of states, but
  - All cells need to closely match
  - Need a linear and symmetric conductance curve



Finding Defects is not enough anymore
Variability will be key

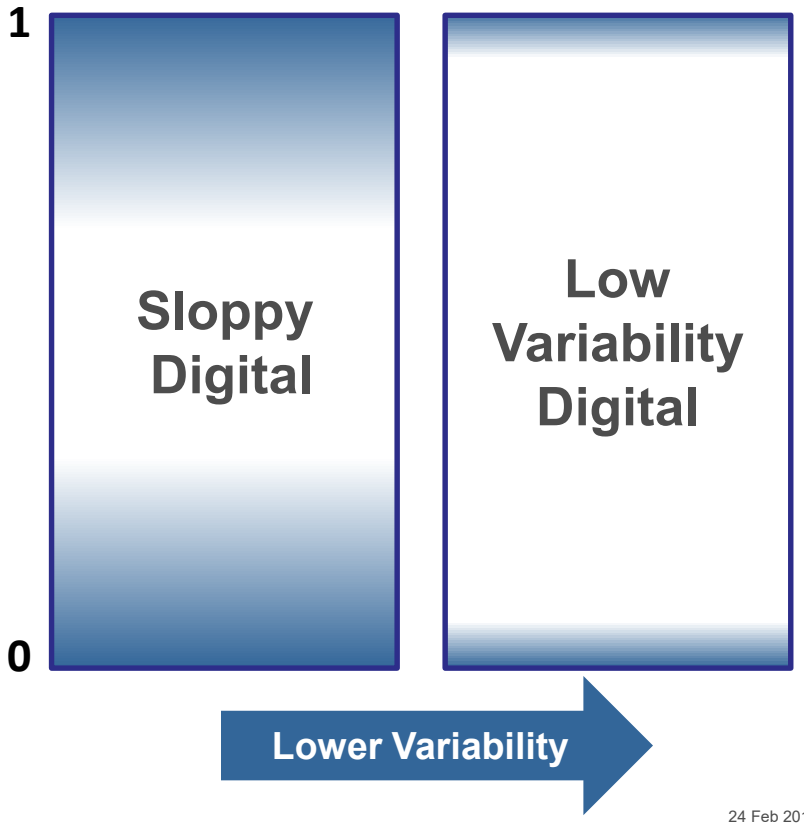
- Analog iMC needs much tighter variability control than digital
- The move from error component parts to Edge Placement Error (EPE) is the right direction
- Need materials uniformity and repeatability as well



Chip Variability Distribution Needs

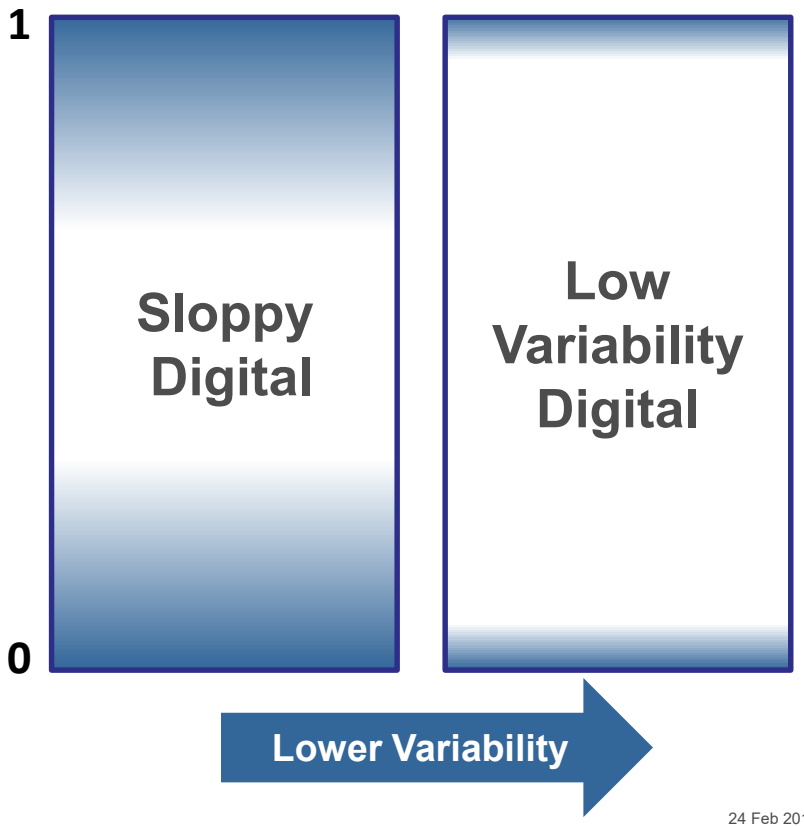
The good news: We're already on the way

- Solving Power and Performance issues means lowering variability in manufacturing
- While putting manufacturing on the road to neuromorphic Analog iMC



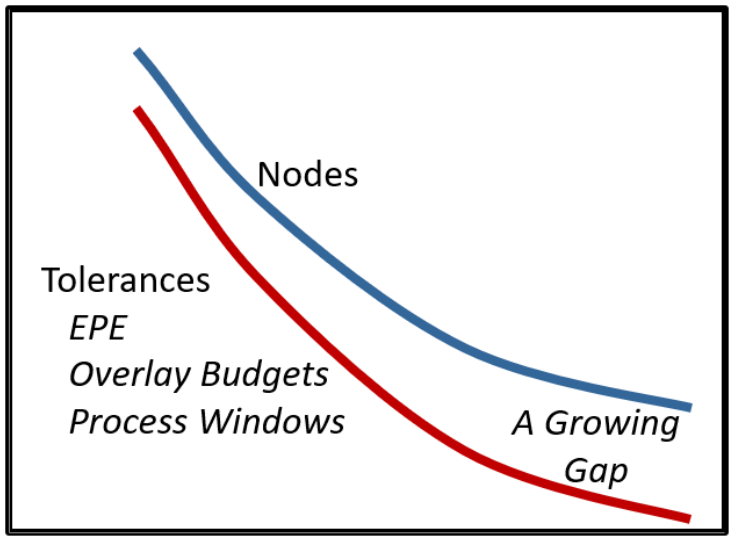
Lower Variability = Greater Reliability

- A critical need for automotive
  - Used to be solved by being 3 generations behind
  - Compute needs have pushed them to the leading edge
- While putting manufacturing on the road to neuromorphic Analog iMC

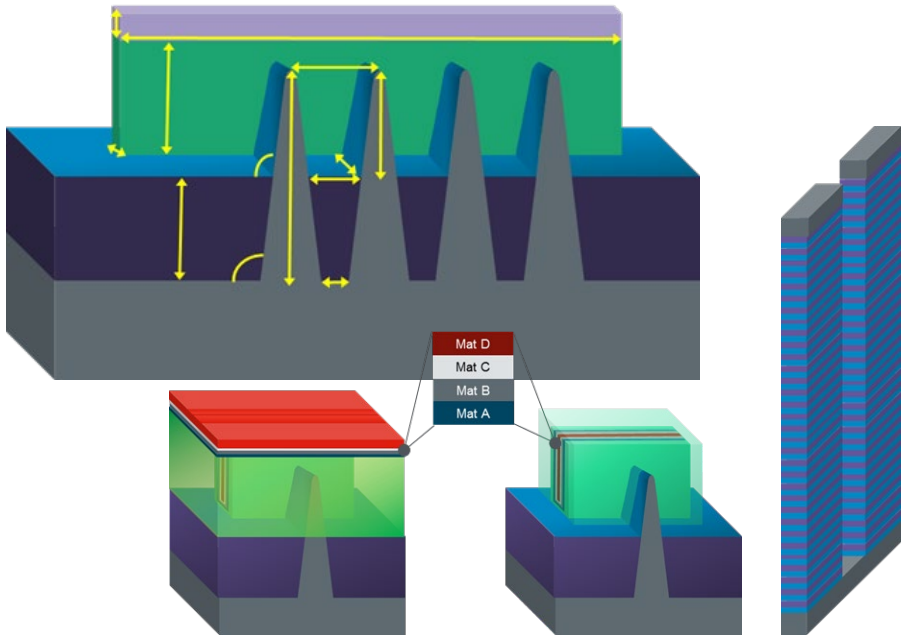


Single-Digit-nm Process Control Challenge

every nanometer matters in 3D processing



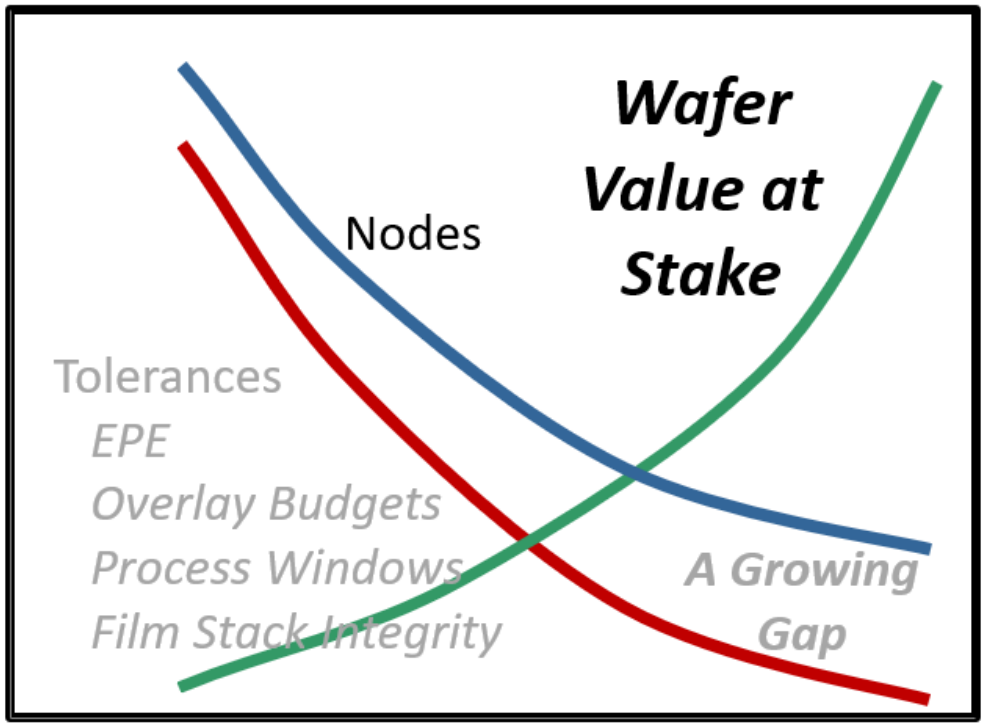
Moore's Law may be slowing …
Tolerance Requirements are not



Source: KLA

You can't fix what you can't find … You can't control what you can't measure

More is at stake than ever before



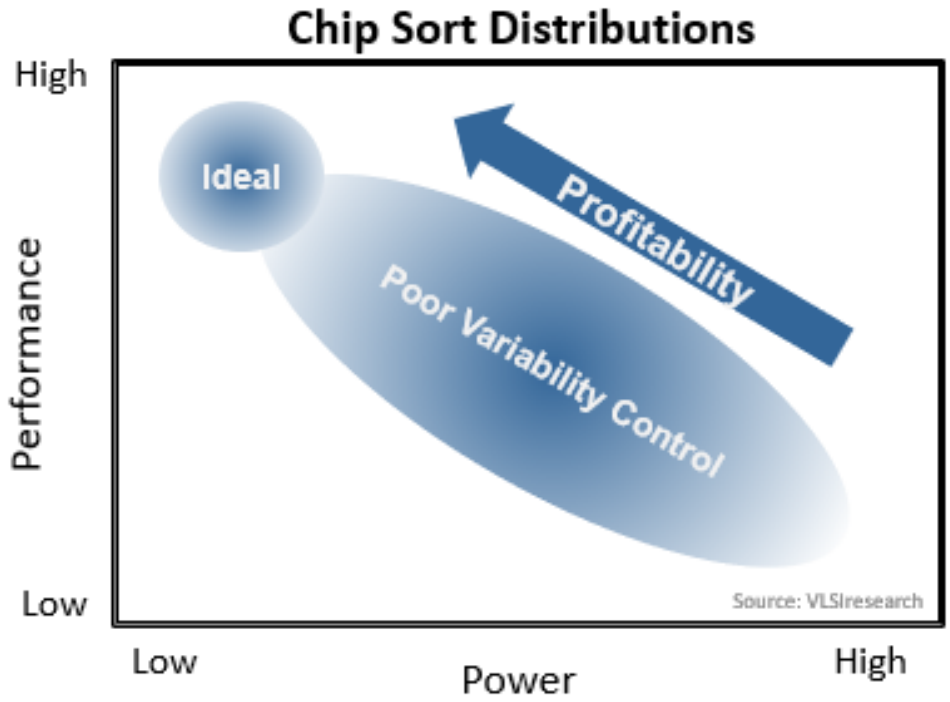
Source: VLSIresearch

Moore's Law may be slowing …

Tolerance Requirements are not

Variability Control Directly Affects Profits

- Poor variability control is expensive
  - Costs in Power, Performance, and Reliability …
  - Things we can't afford to leave on the table
- The best chips sell for more
- But they cost the same to make
- Hence, they are far more profitable
- Variability control must be in-line
  - Lots of knobs to control

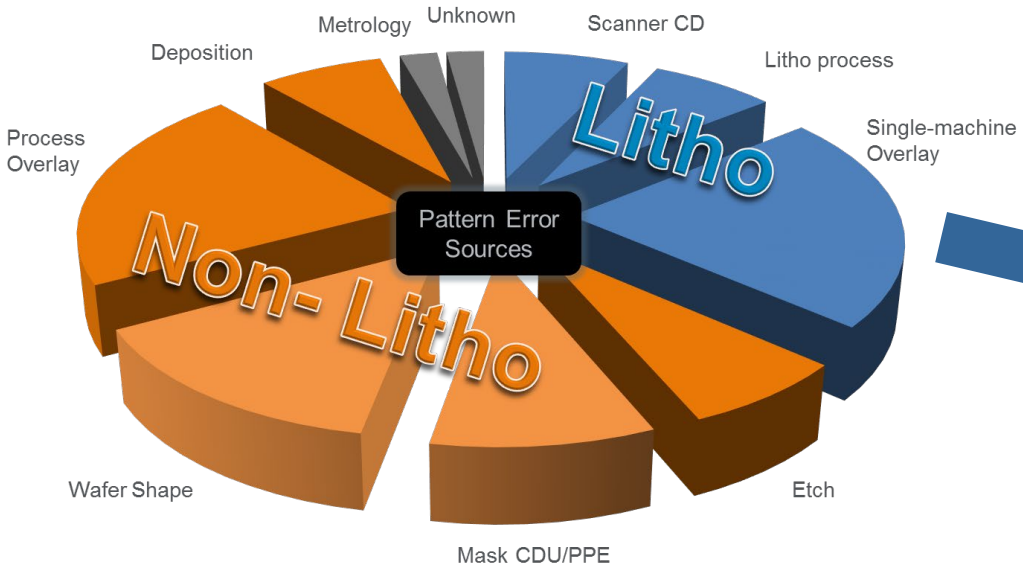


The need for a new inspection revolution

- Finding Defects is not enough anymore
  - Controlling variability will be key to ensuring that all cells and interconnect are structurally right as designed
- The implementation of AI in Automotive makes this a much more important imperative
- Hence, manufacturing will have to go through a dramatic change that we haven't seen since KLA introduced yield management concepts in the early nineties
  - There are powerful forces taking us to **Variability Management**

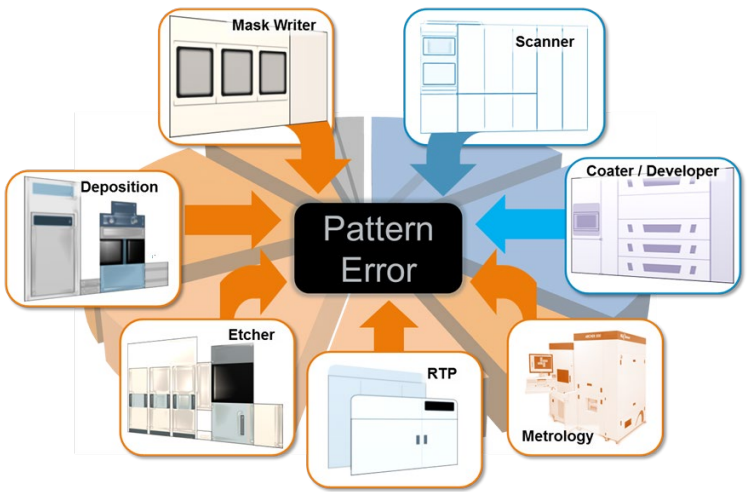
Non-Litho Errors Dominate

Rising non-Litho errors means more complex process control



CDU = Critical Dimension Uniformity
PPE = Pattern Placement Error

Process control inside and outside the litho cell is critical for meeting variability requirements

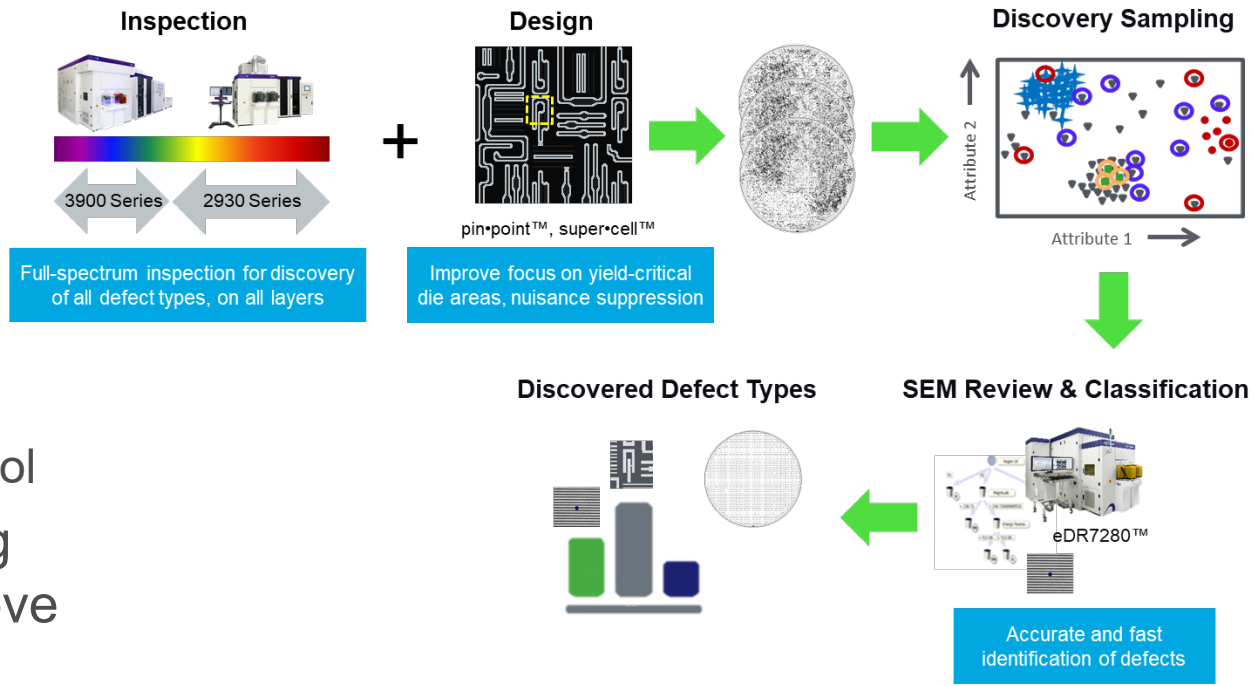


Source: KLA

Design Aware Inspection:

What being done for defects needs to be done for variability

- For faster and better inspection recipes
- Improved Paretos
- Focus on what's important
- Pass on what's not
  - For better cost control
- Systematically debug processes and improve yield

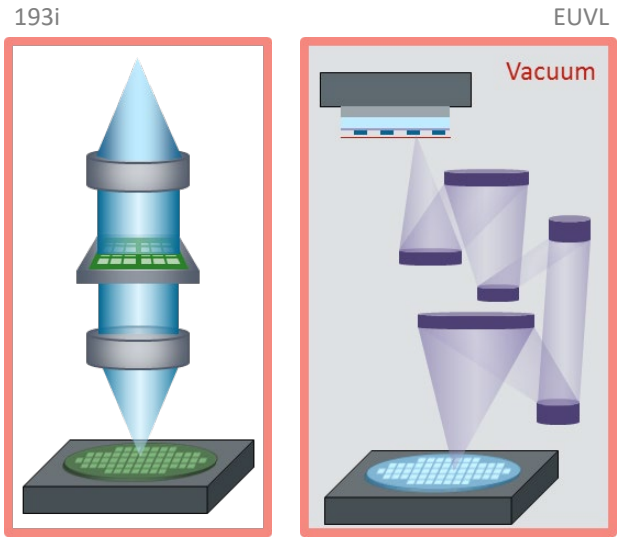


Source: KLA

EUV implementation accelerates trend for more Process Control

- Value of inspection increases with lithography
- The cost of lithography scan is increasing substantially with EUV
  - Lower throughput
  - Higher system value
  - Higher adjacent costs
    - Resist
    - Metrology
    - Reticles
    - Consumables
- Higher need for inspection and increasing sampling

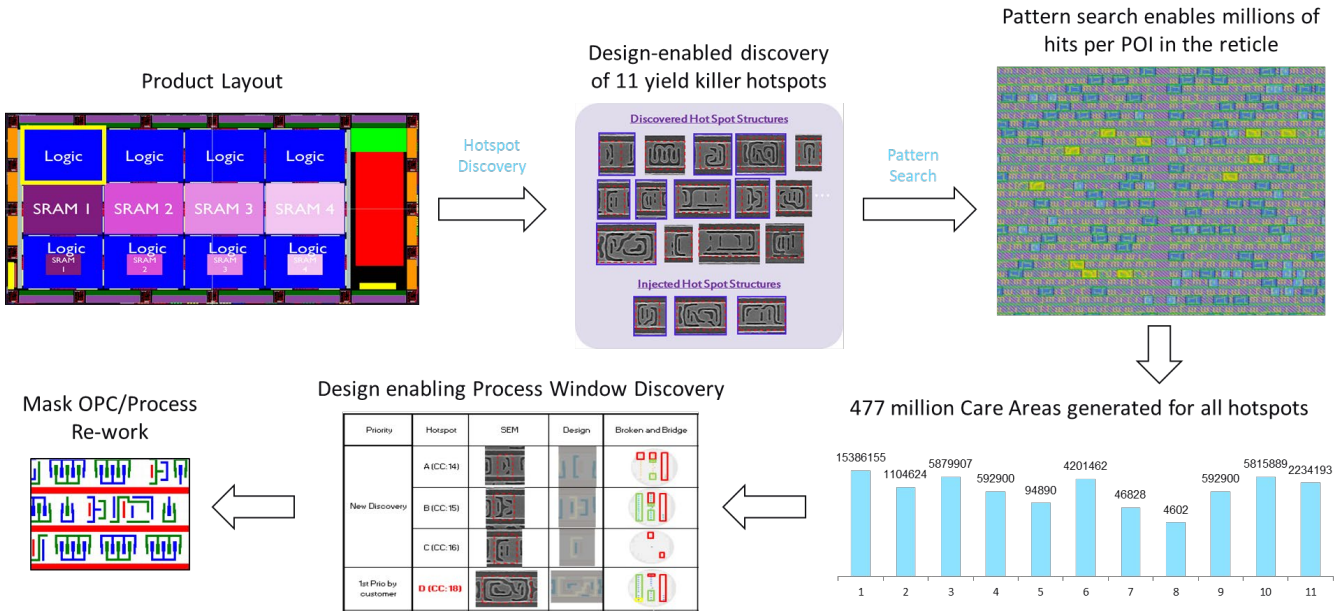
193i to EUV Lithography



- Cost per scan increasing with EUV
- Integration costs
- New materials

Design-Integrated Inspection for PWD

- Broadband optical inspection + design enables hotspot discovery for efficient process window discovery



Source: DOI: 10.1109/ASMC.2016.7491105 (imec) and DOI: 10.1109/ASMC.2017.7969272 (imec)

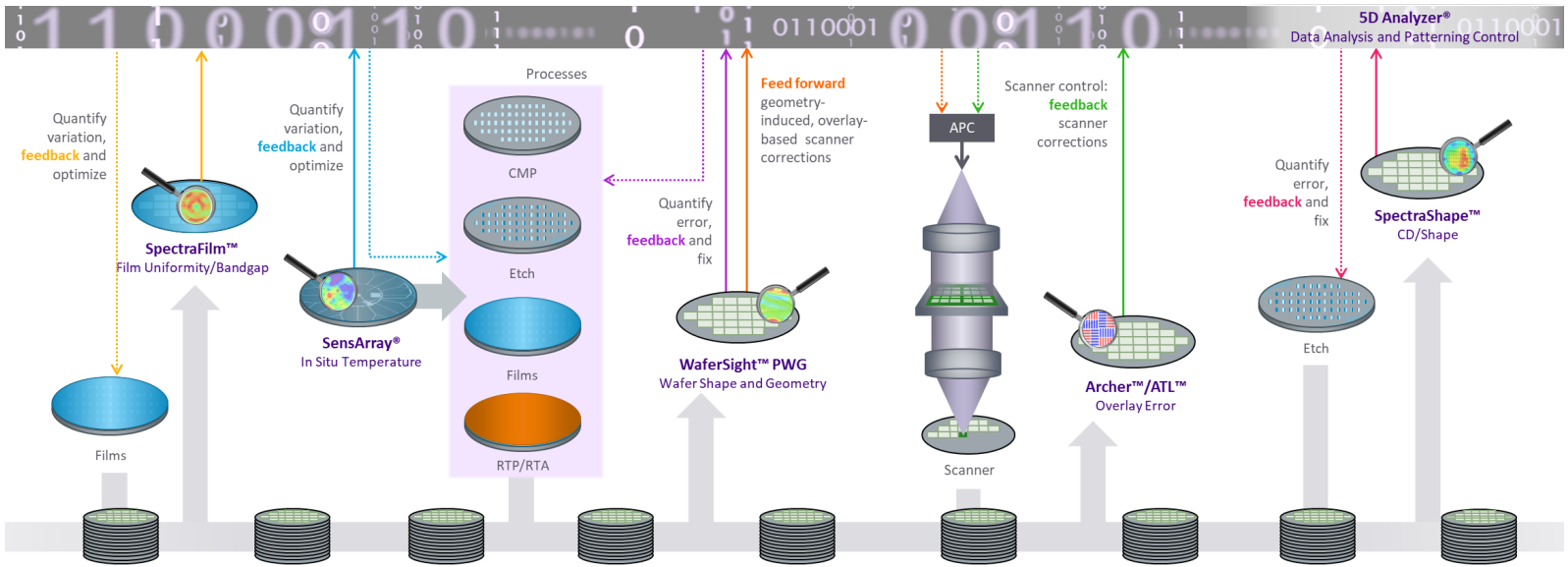
Fab-Wide Process Control

Big data analytics for feed-back and feed-forward control loops

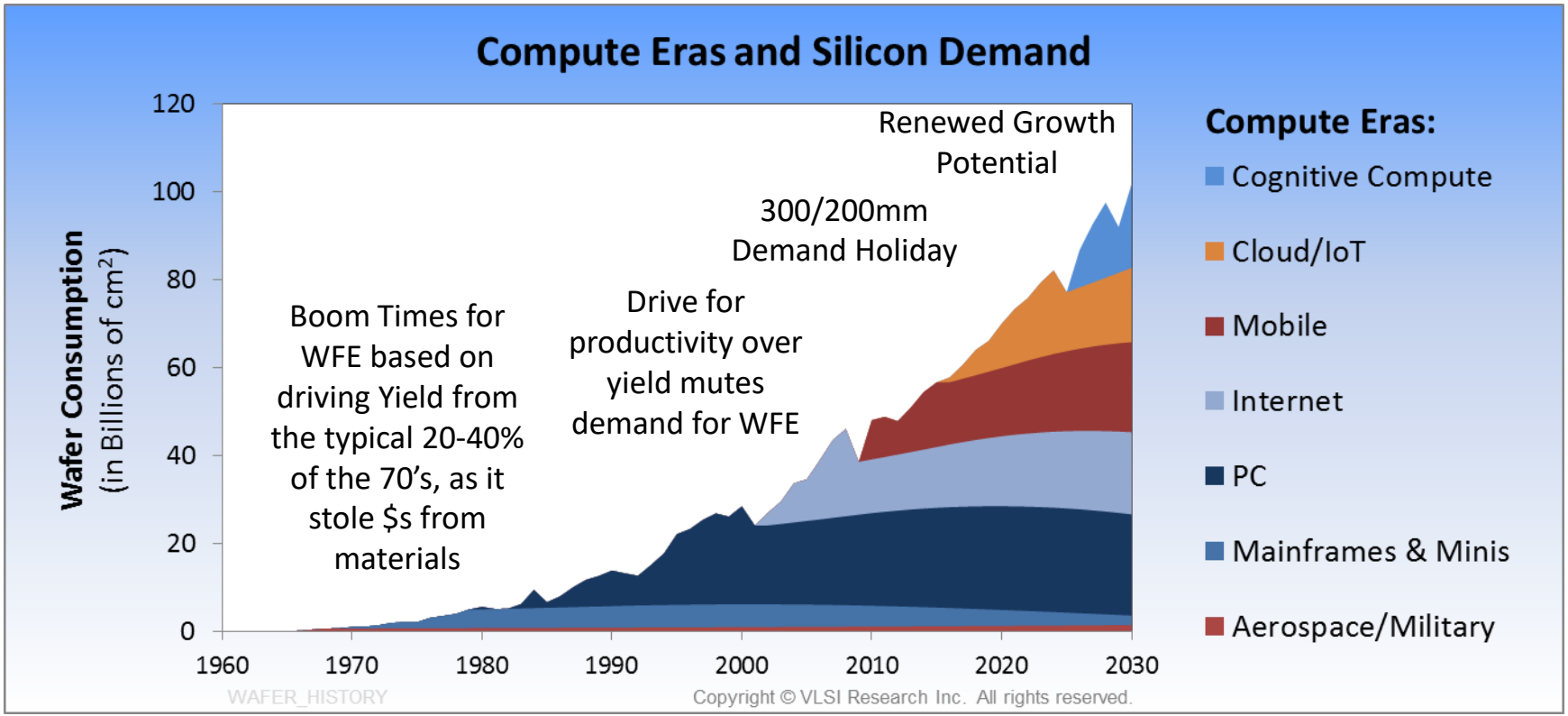
Address fab-wide sources of variation

- Optimize processes
- Augment information available for tool corrections

Source: KLA



If you build it … they will come



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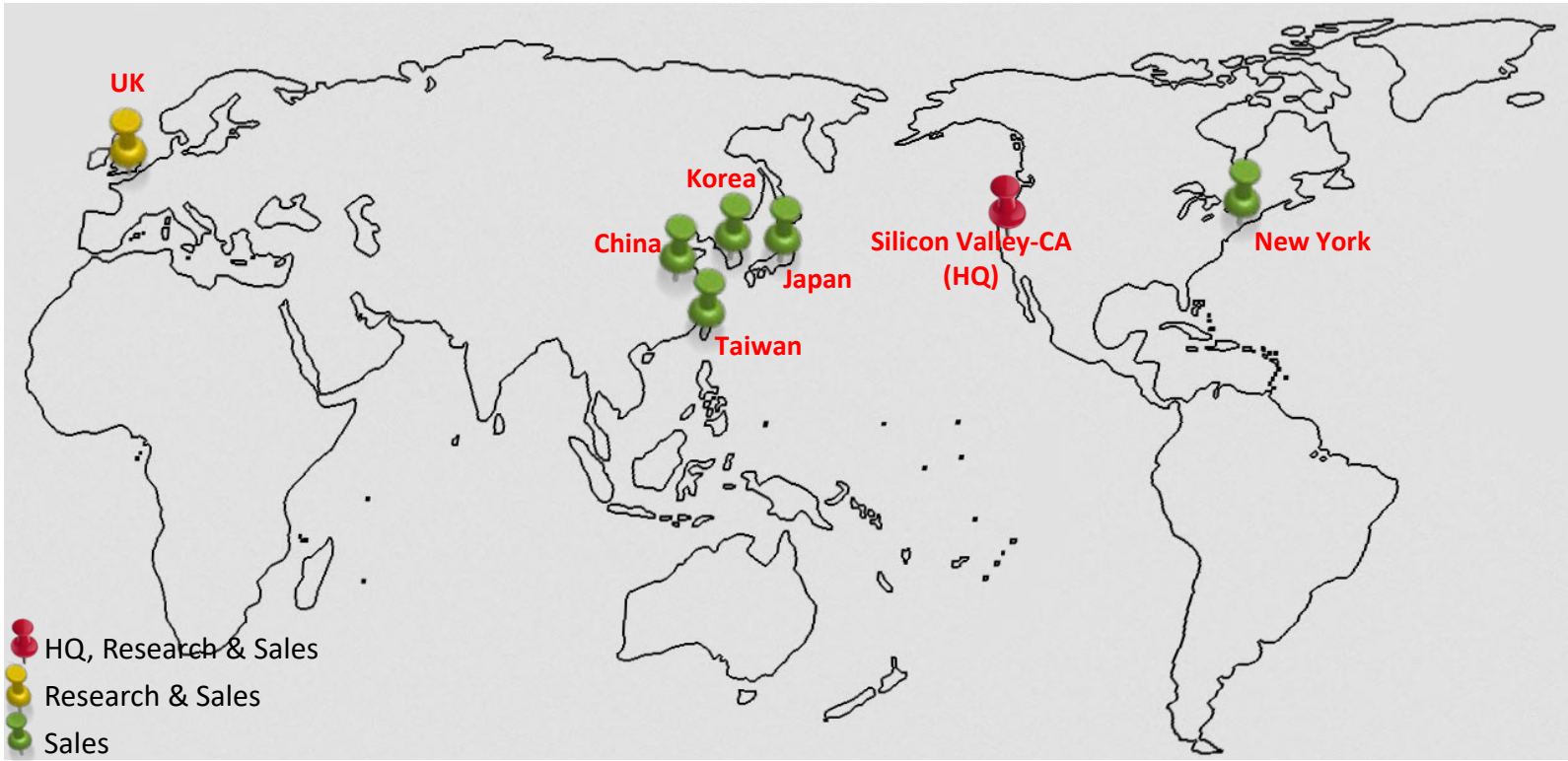
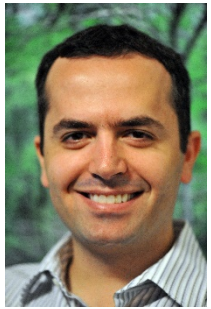


Meet the Team

G. Dan Hutcheson
CEO and Chairman of the Board

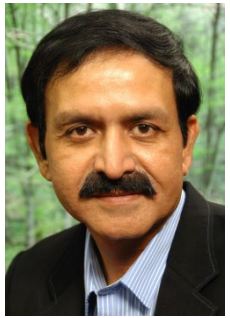
Risto Puhakka
President

John West
Managing Director, VLSIresearch Europe



Andrea Lati
Director, Market Research

Lisa M. Steele
Vice President



Manjesh Singh
CIO

Affiliates

Kaz Hayashi, Managing Director, Japan

Steve Huang, Managing Director, China Mainland

Young Soo (YS) Im, Managing Director, Korea

Philip Wang, Managing Director, Taiwan

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