Advanced Metrology for Nanoelectronics at the National Institute for Standards and Technology

Stephen Knight
Robert Celotta
David G. Seiler

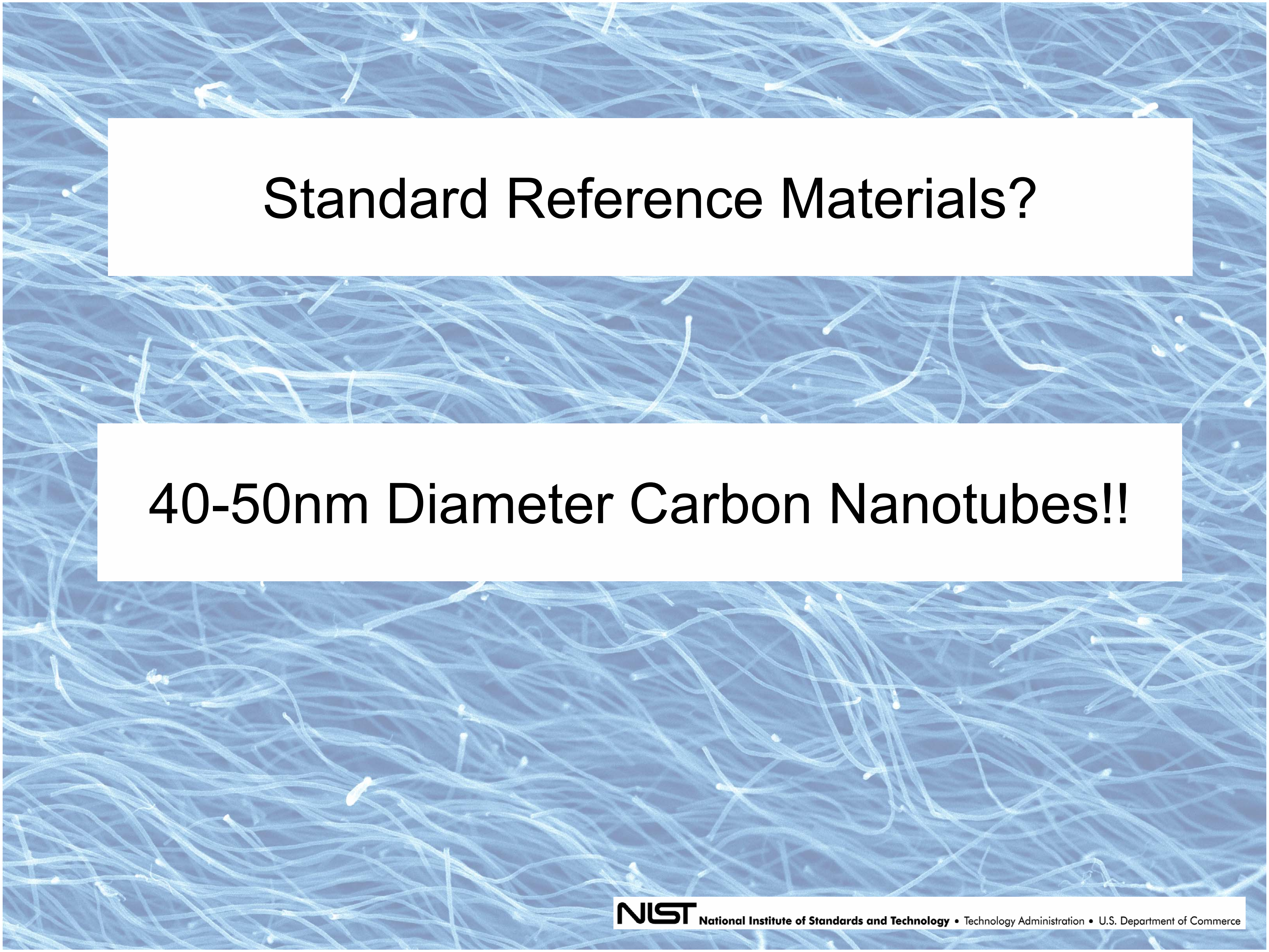
Outline

- A few more words about NIST…
  - Office of Microelectronics Programs
  - Center for Nanoscale Science and Technology
  - Semiconductor Electronics Division
- Emerging Devices and Materials
- Conclusions

Office of Microelectronics Programs

Critical Dimension and Overlay Projects

- Precision Engineering Division
- SEMATECH/ISMI
  - Member Companies
- Semiconductor Electronics Division
- Statistical Engineering Division
- Polymers Division
- Surface and Microanalysis Science Division
- Optical Technology Division
- University of Edinburgh
- VLSI Standards
- Other National Metrology Institutes



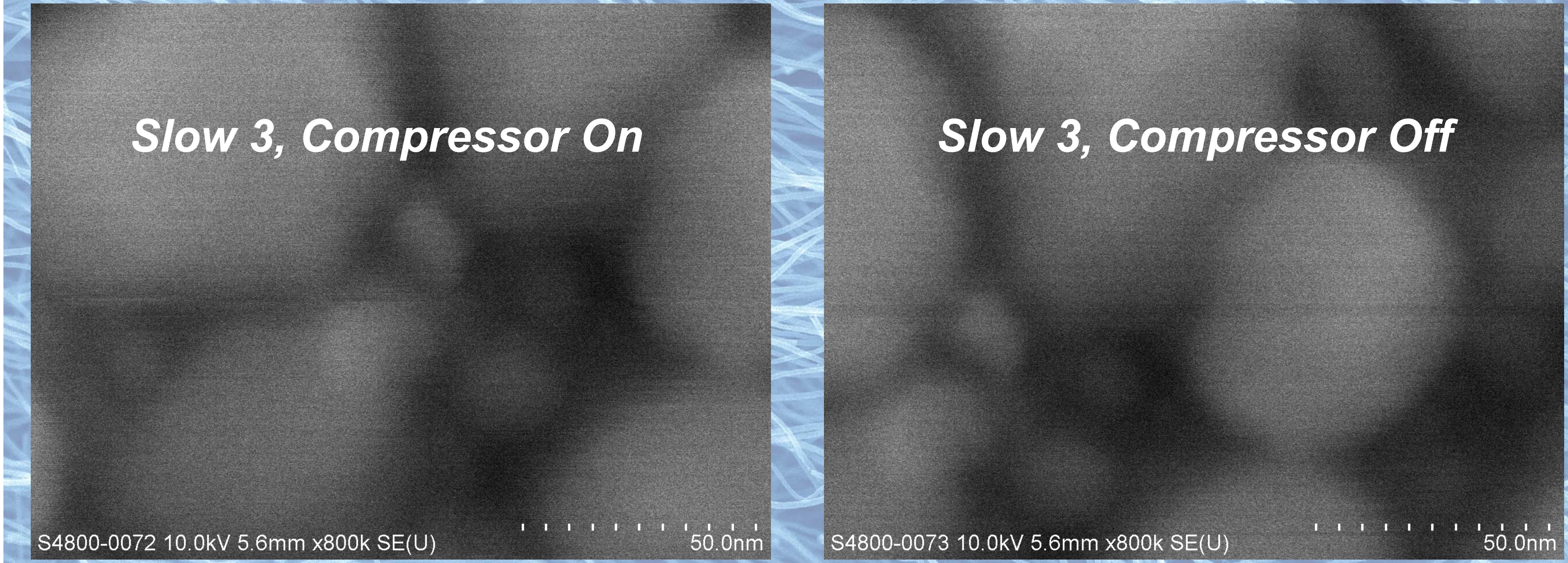
Standard Reference Materials?

40-50nm Diameter Carbon Nanotubes!!

Refrigerator installed at STAR

Cryogen-free 100 mK refrigerator installed on Hitachi field-emission SEM at STAR Cryoelectronics

SEM Operation at 800 Kx



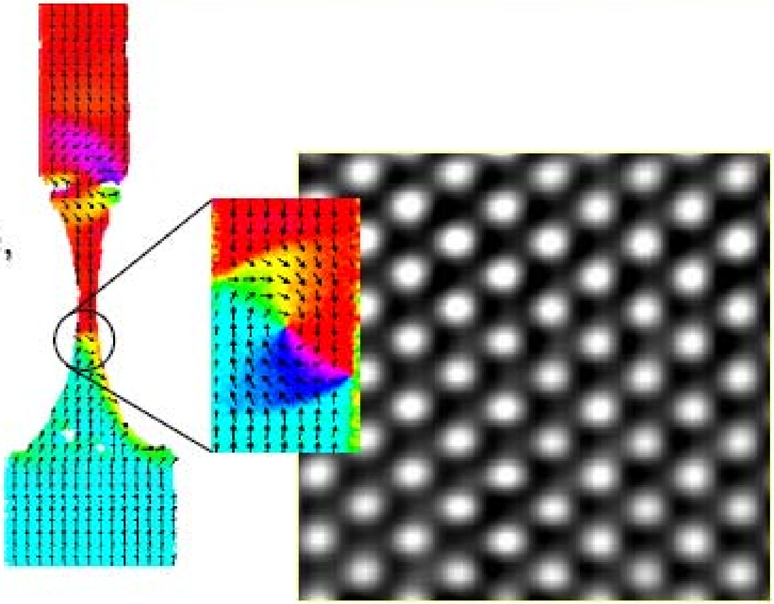
Slow 3, Compressor On

Slow 3, Compressor Off

SEM images with and without cryocooler in operation; negligible degradation. If this configuration is repeatable, vibration issue is solved.

Center for Nanoscale Science and Technology (CNST)

- New multidisciplinary center aimed at converting nanotechnology discoveries to products
- Mission: develop the necessary measurement science and instrumentation to meet emerging needs
- Establish the materials and process characterization to enable scaled-up, reliable, cost effective manufacturing of nanoscale materials, structures, devices, and systems
- Partner with industry, academia, and government to turn the potential of nanotechnology into reality



POC: Dr. Robert Celotta, (301)-975-3710 robert.celotta@nist.gov

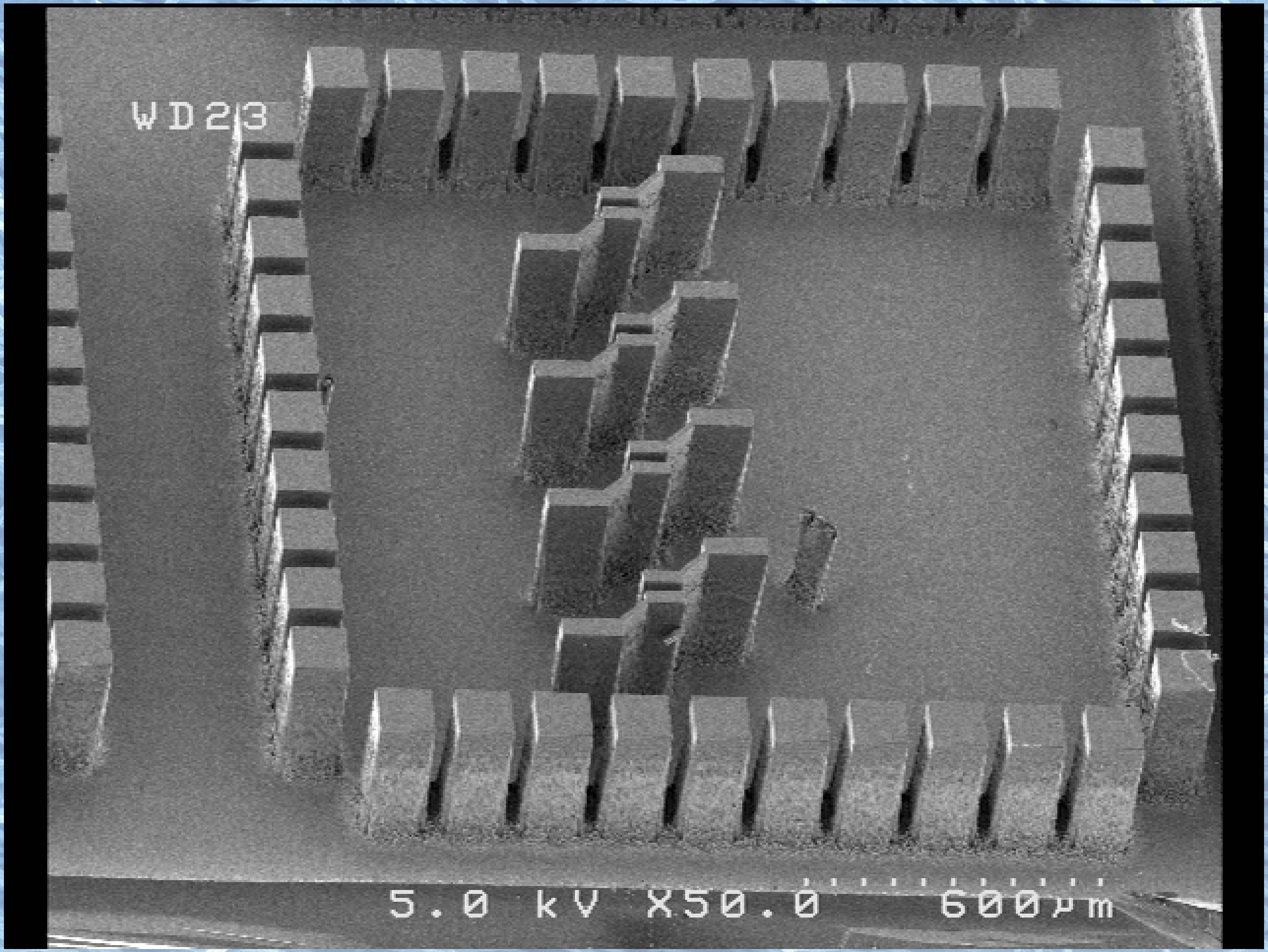
Center for Nanoscale Science and Technology

The Center enables science and industry by providing essential measurement methods, instrumentation, and standards to support all phases of nanotechnology development, from discovery to production.

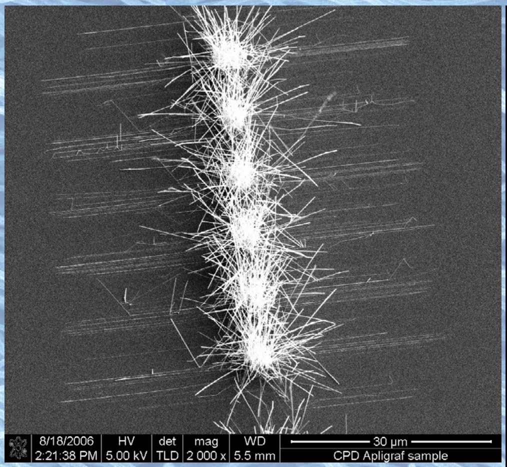
Nano-Imprint Lithography Tool: Nanonex NX-2000

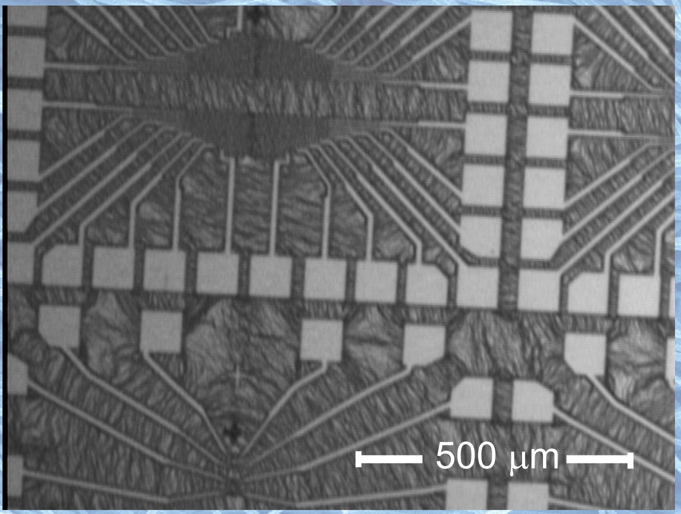
E-beam Lithography System: Leica VB300 (projected availability April 2007)

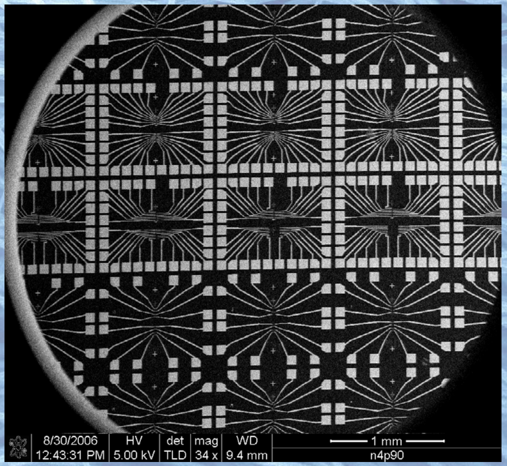
Deep RIE Etch

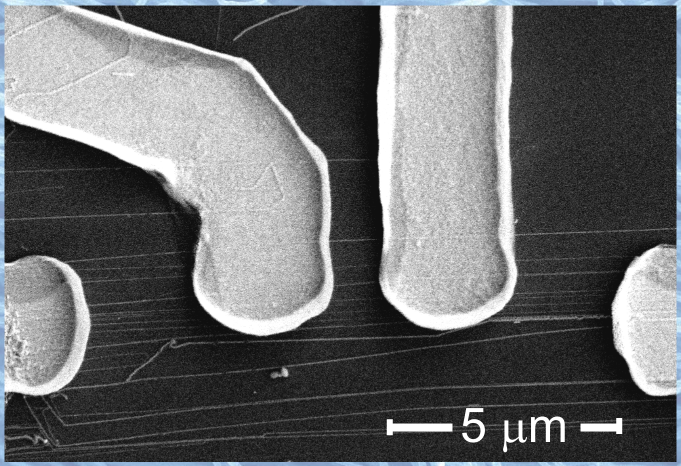


Nano-Manhattan?

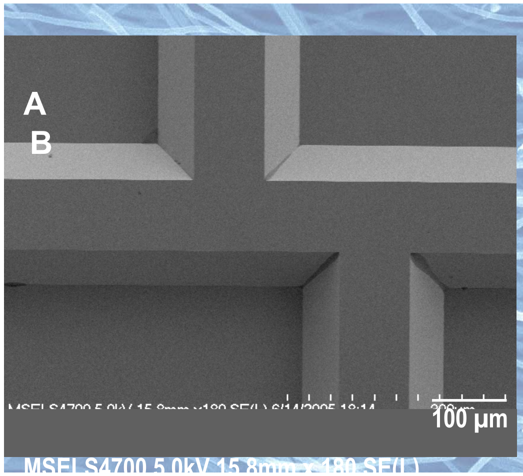




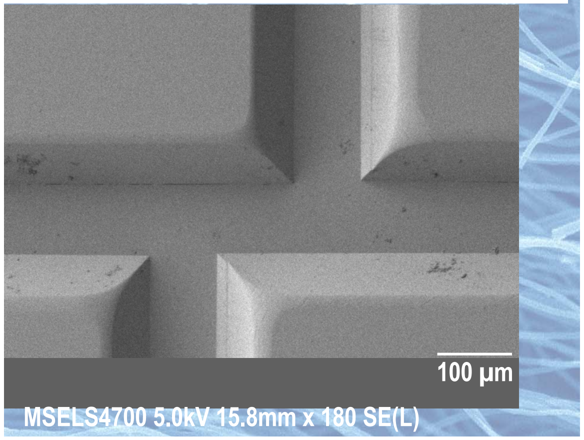




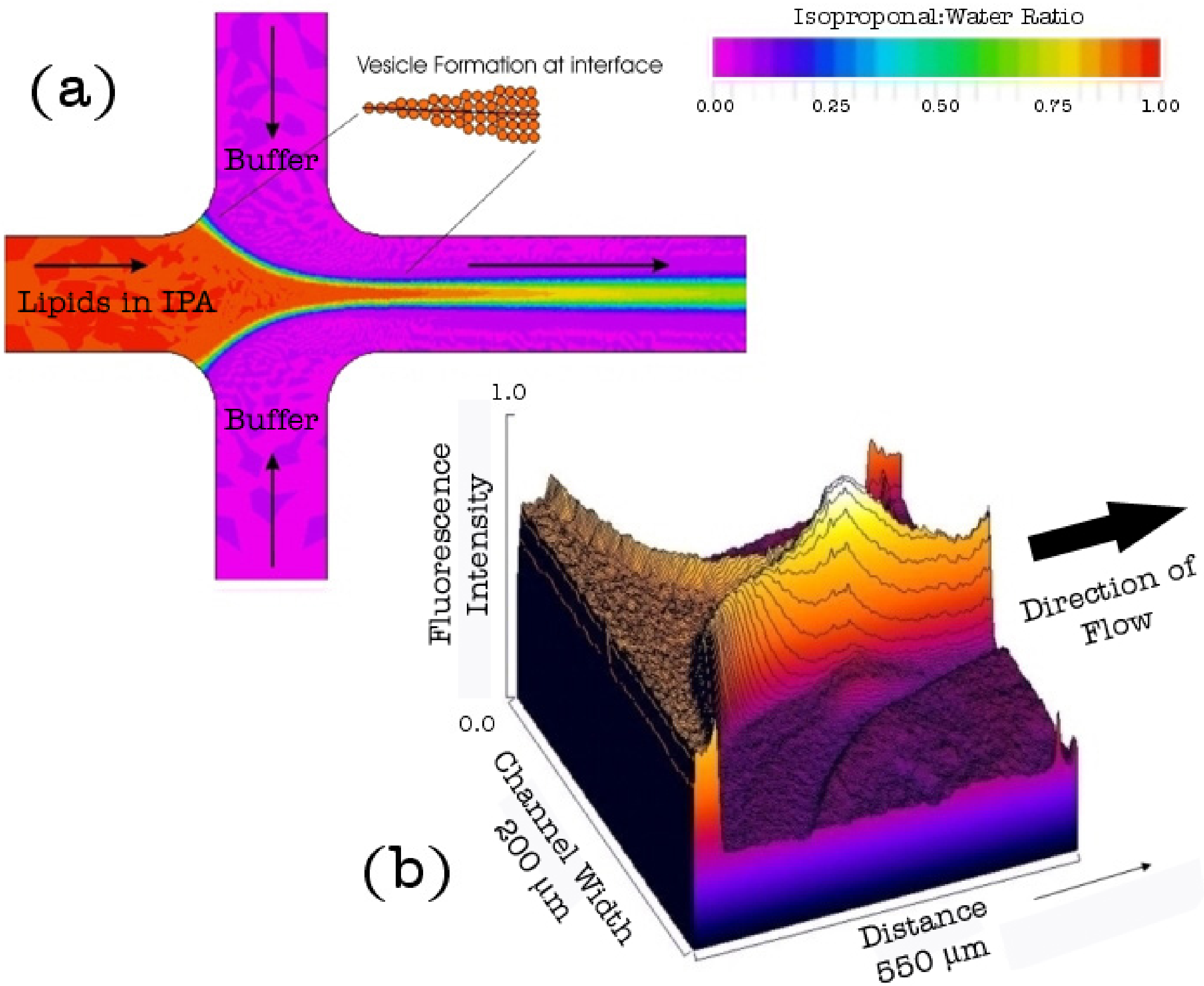
Large Scale Fabrication of Nanowire-Based Devices Using Optical Photolithography

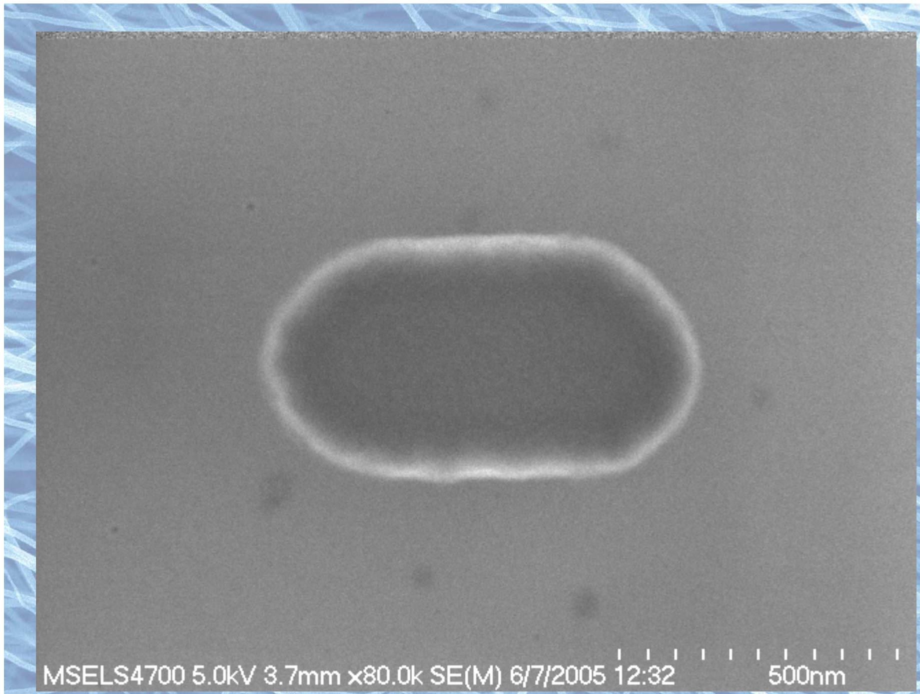


Scanning Electron Micrograph (SEM) of a photo-lithographically patterned and wet etched Si template prepared for polymer hot embossing.

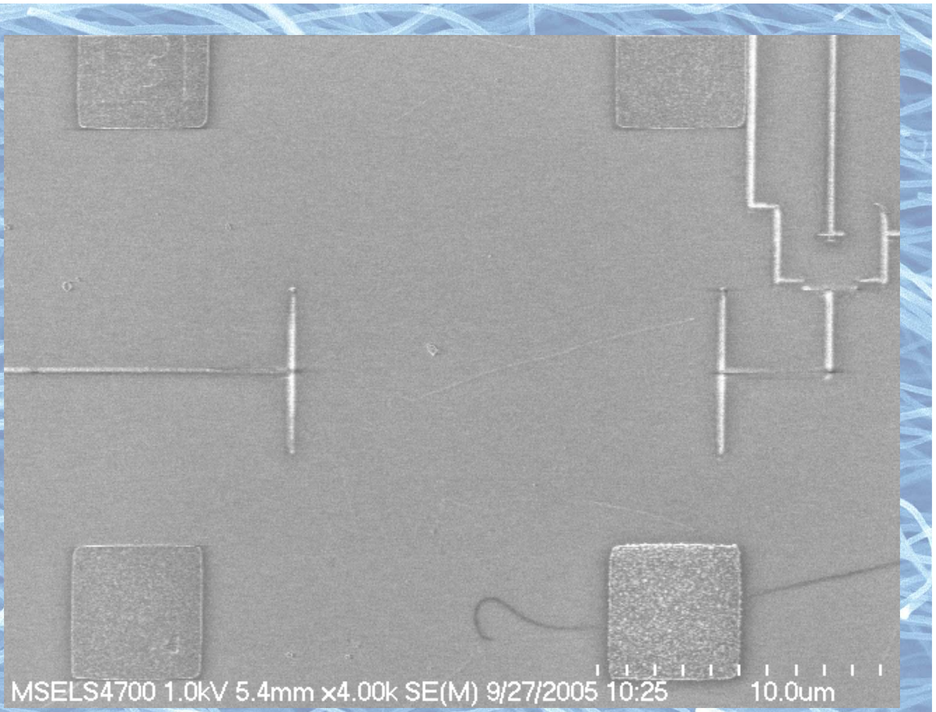


SEM of a microfluidic channel fabricated by hot embossing pattern shown in A into poly(methyl methacrylate) (PMMA) substrate at 105 °C, 5.5 MPa for 30 min; Images acquired by Monica Edelstein and Jayna Shah.





Magnetic dot in well: magnetic metal (Co) deposited inside a SiO_2 well, for spintronics measurements. The well and the metal dot are both deliberately designed to be oval in shape, in order to avoid magnetic shape anisotropy. Note the very small gap between the inner edge of the well and the outer edge of the metal dot, and the excellent overlay. Fabricated at NIST; Emmanouel Hourdakis, Cindi Dennis, Bill Egelhoff, Neil Zimmerman.



Coulomb blockade transistor and carbon nanotube: the bright vertical and horizontal lines are Al leads fanning out from the tunnel junctions that produce the Coulomb blockade. The faint white line running roughly horizontally between the two bright vertical lines in the center of the micrograph is a carbon nanotube. We are attempting to measure electrostatic charge transfer in the nanotube. Fabricated at NIST and University of Maryland; Emmanouel Hourdakis, Neil Zimmerman.

Resolution vs Throughput

Transistor cost = cost of one letter in *NY Times*
(P. Silverman, Intel, EIPBN (2005))

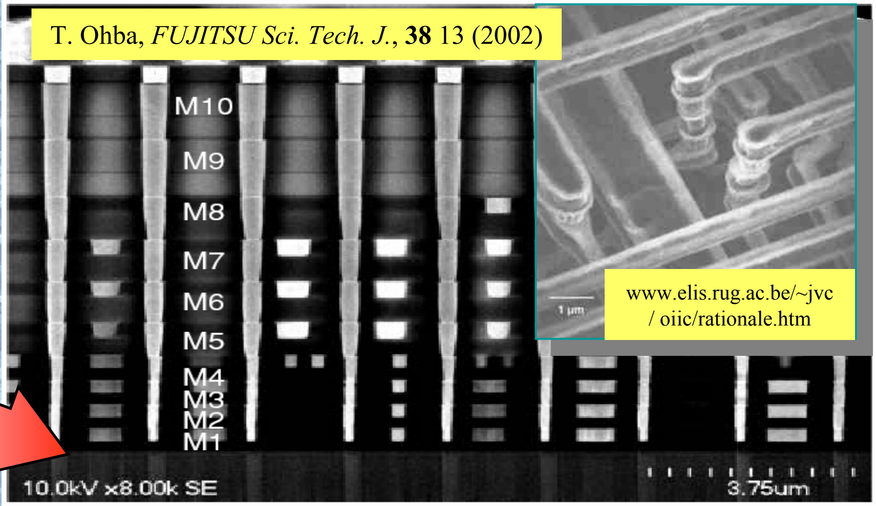
Need transistor-sized features on *NY Times*-sized areas

After D.M. Tennant and C.R. Marrian, *J. Vac. Sci. Technol.* (2003)

Lithographically-Directed Self-Assembly

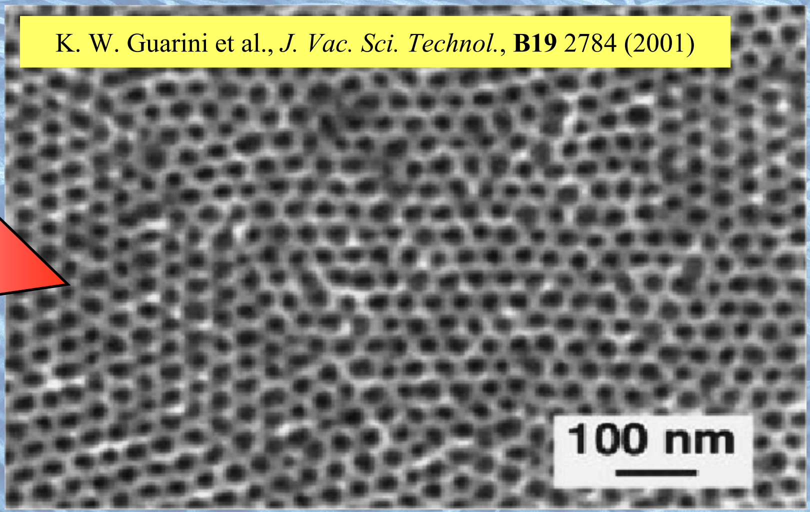
- Lithography: creates arbitrary shapes and complex hierarchies, but limited to 40 nm pitch, 5-10 nm size features

- Self-assembly: massively parallel, works with nanoscale objects, but generates only simple arrays without long-range order or hierarchy


T. Ohba, *FUJITSU Sci. Tech. J.*, **38** 13 (2002)

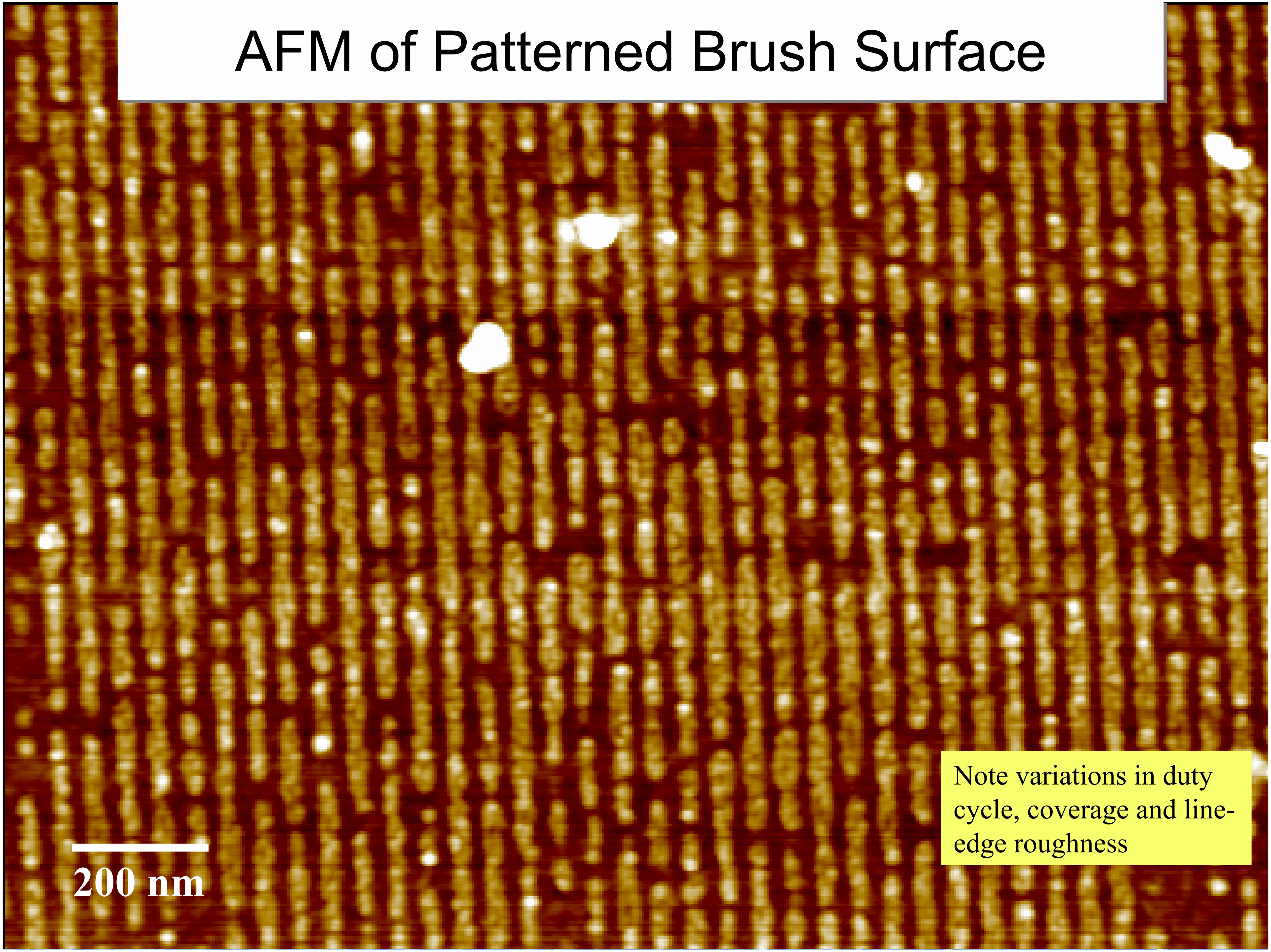
www.elis.rug.ac.be/~jvc / oiic/rationale.htm

IC multilevel interconnect structure


K. W. Guarini et al., *J. Vac. Sci. Technol.*, **B19** 2784 (2001)

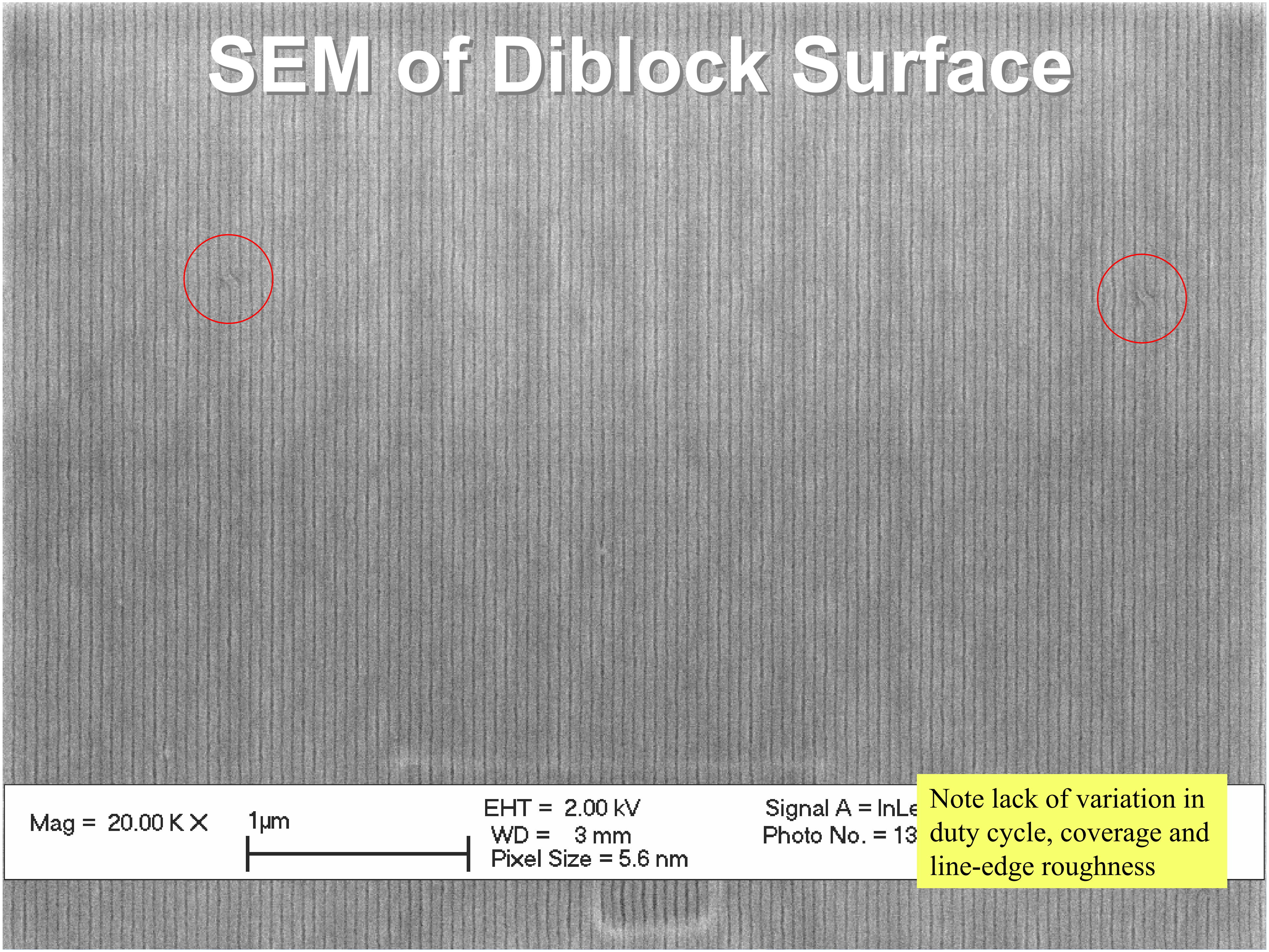
Polystyrene/PMMA diblock copolymer template

AFM of Patterned Brush Surface



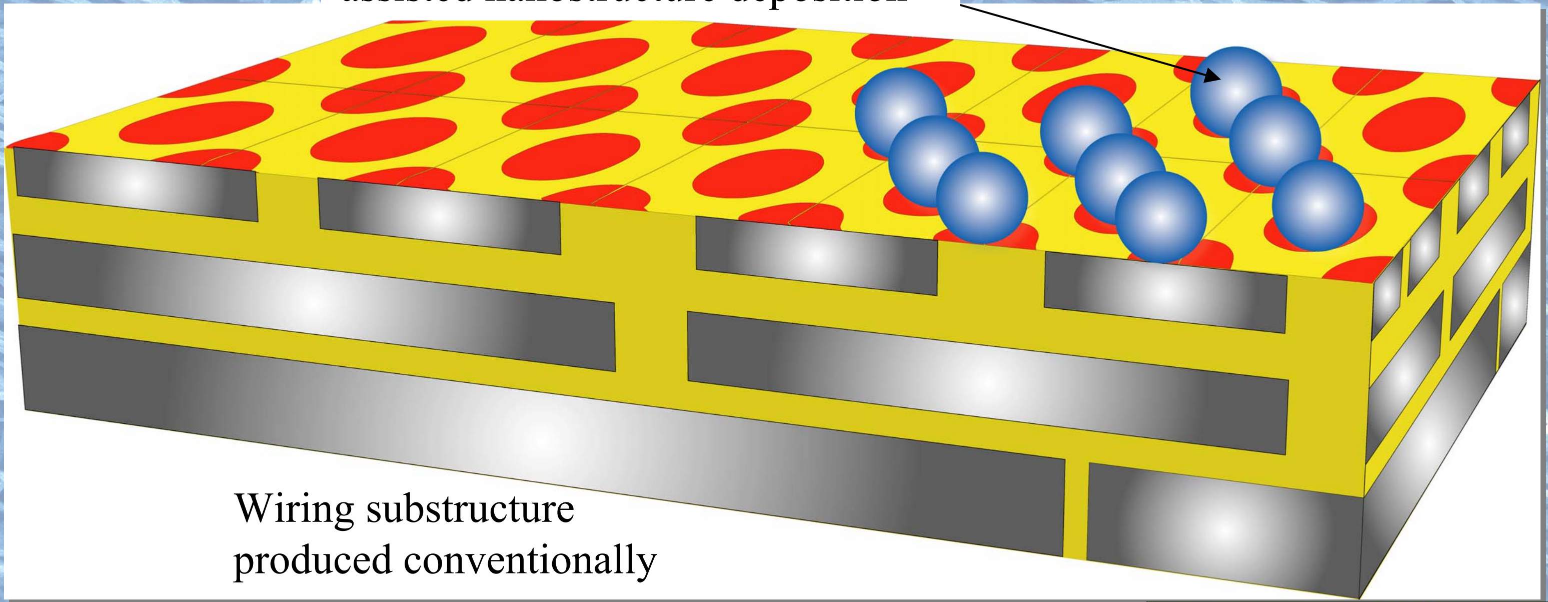
Note variations in duty cycle, coverage and line-edge roughness

SEM of Diblock Surface



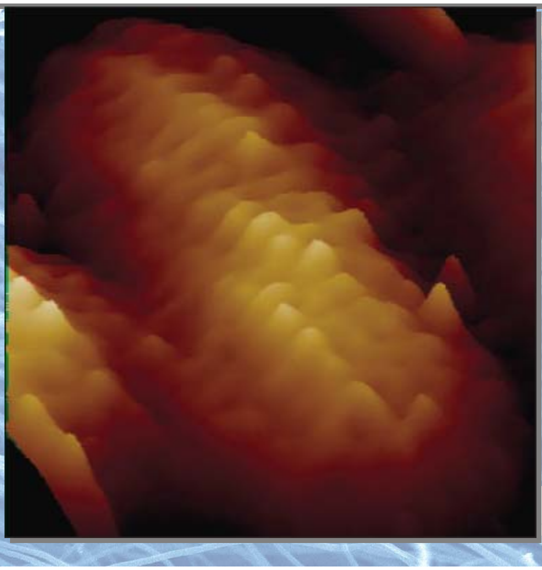
Note lack of variation in duty cycle, coverage and line-edge roughness

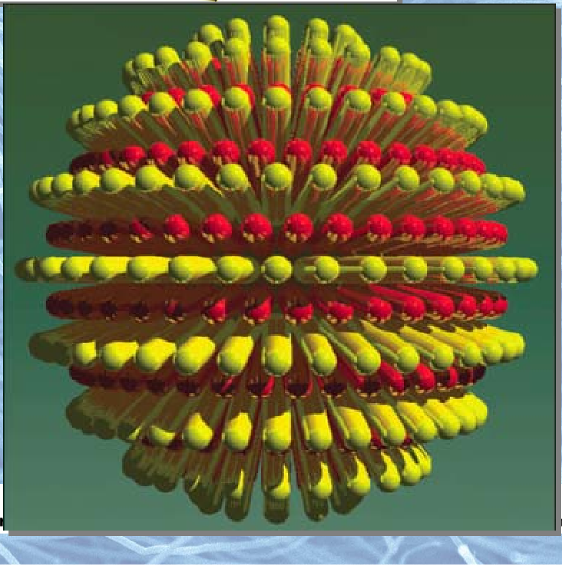
Self-Assembly and Sub-Lithographic Patterning



Field or chemical-recognition assisted nanostructure deposition

Wiring substructure produced conventionally

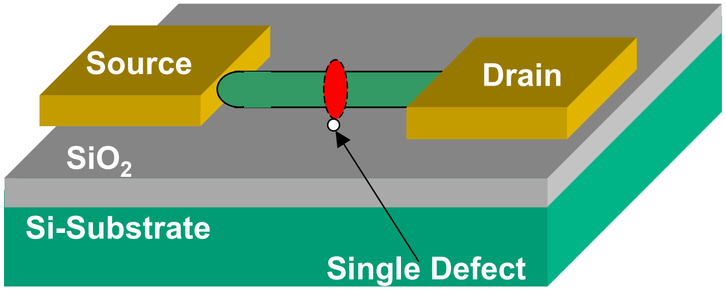


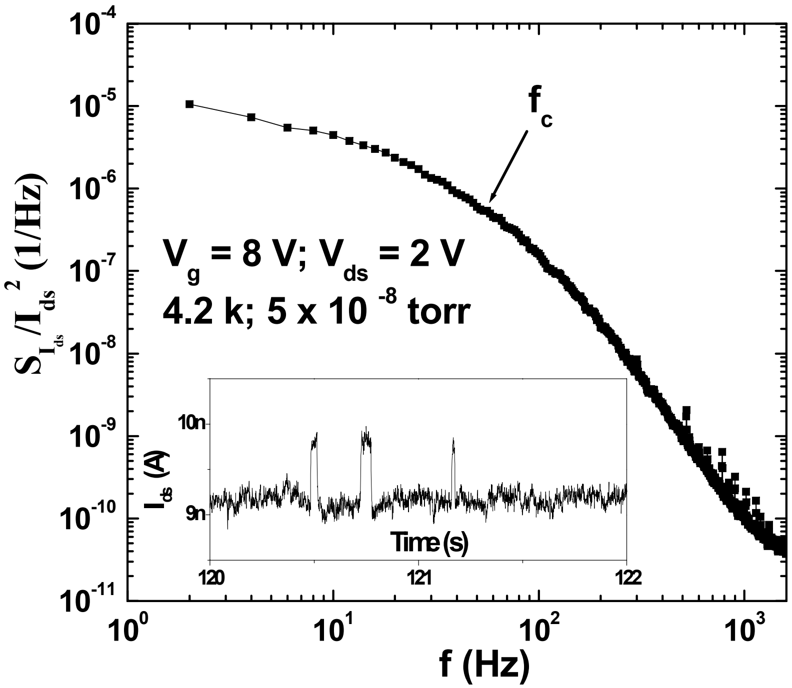


"Spontaneous assembly of subnanometre ordered domains in the ligand shell of monolayer-protected nanoparticles", A.M. Jackson, J.W. Myerson and F. Stellacci, *Nature Materials*, **3** 330 (2004)

Semiconductor Electronics Division

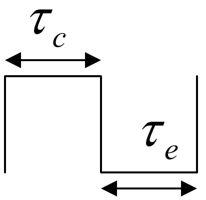
Random Telegraph Signal (RTS): a probe for single electronic defects





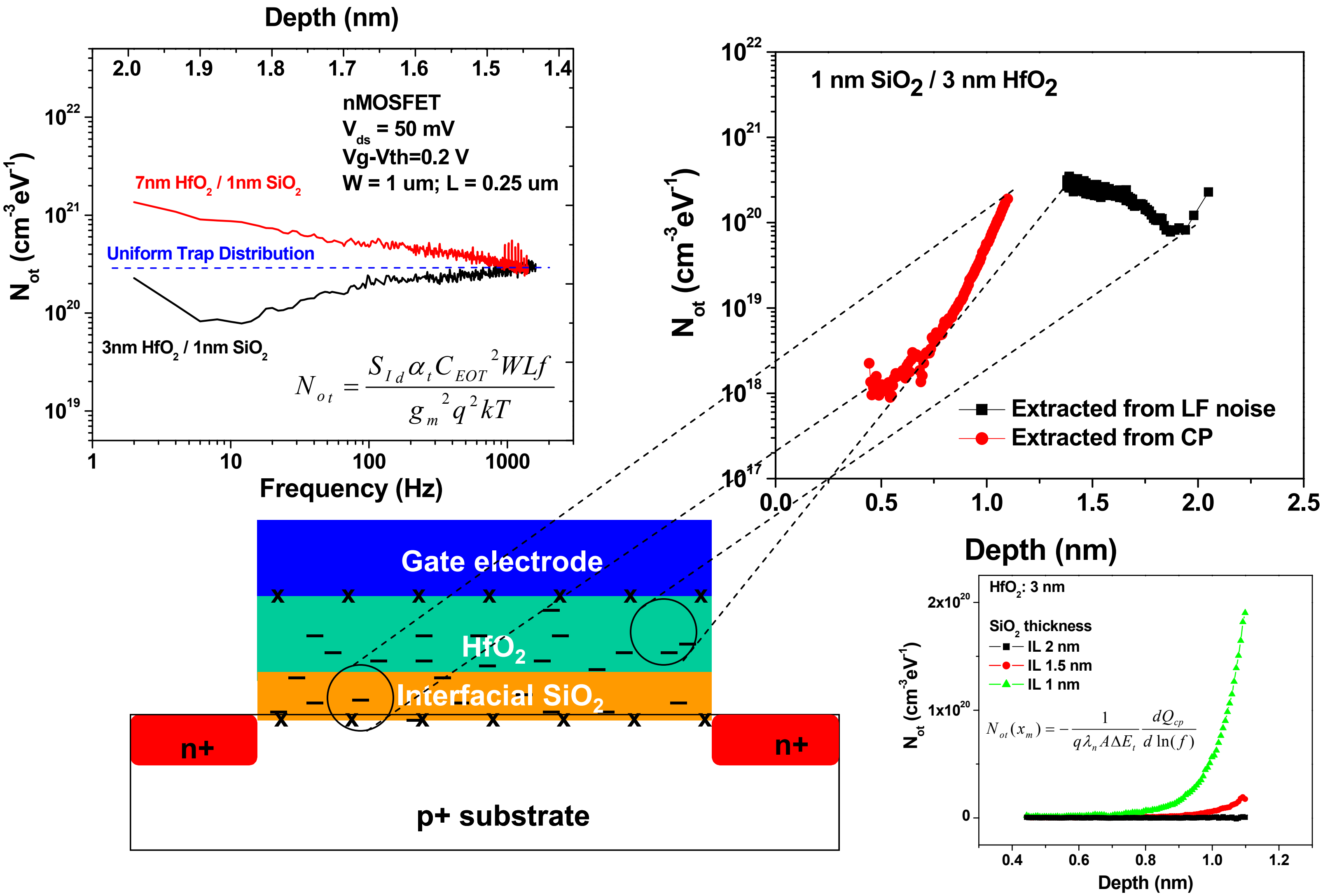
$$S_I(f) = \frac{k}{1+(f/f_0)^2}; \quad f_0 = \frac{1}{2\pi\tau_0};$$

$$\frac{1}{\tau_0} = \frac{1}{\tau_c} + \frac{1}{\tau_e};$$



The bias-voltage/temperature dependence of the capture and emission times allow one to determine the type, location, and barrier energy of the defects.

Combining techniques to extend profiling range

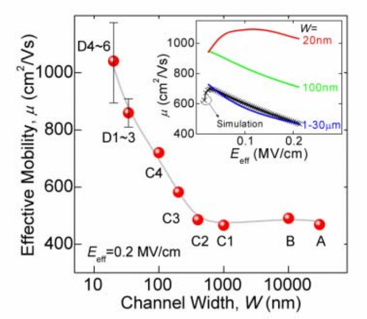


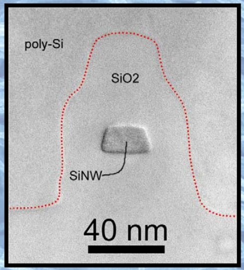
Defining and developing metrology for future silicon nanotechnology

NIST is developing the advanced metrology required for Si-based nanoelectronics

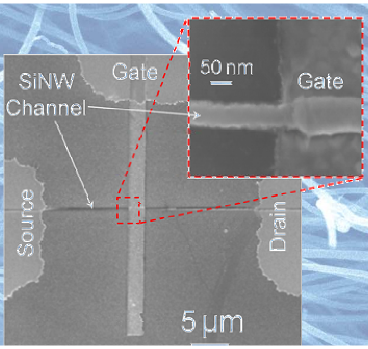
Focus: Electrical and physical metrology of the *basic building blocks* of confined-silicon devices (e.g., quantum layers, wires, and quantum-dots).

Top Down





Extrapolation of existing CMOS fabrication technology…



Top Down

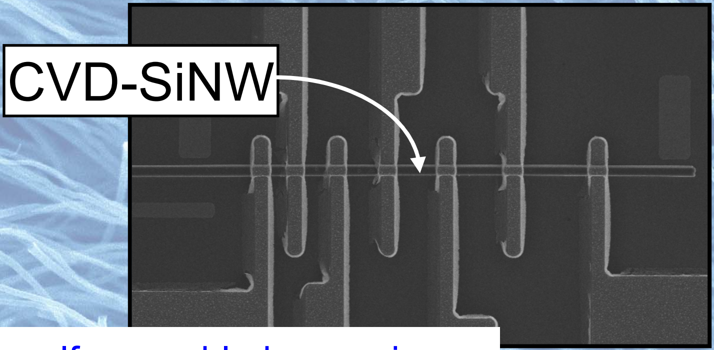
- Mobility enhancement observed

Sang-Mo Koo, et al. Nano Lett. 2004

- New Test Structures Developed

S-M Koo, et al., Nano Letters, 2005. & Nanotechnology, 2005.

Bottom Up



Latest results in
Poster 010
2007 FCMN

- Sophisticated Test Structures for self-assembled nanowires

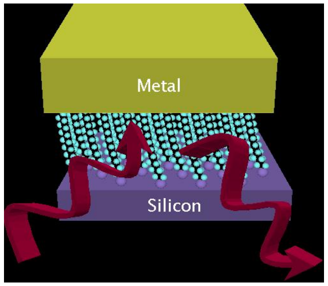
Qiliang Li, et al., IEEE Trans on Nanotech. March 2007.

Hybrid Si/molecular-electronic Devices

NIST is developing the measurement infrastructure necessary to enable the integration of molecular electronics with CMOS

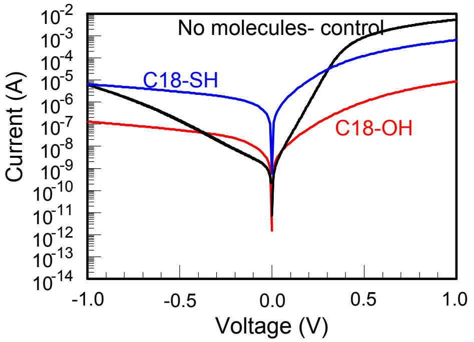
Organic Layer Formation and Characterization

(FTIR, pb-RAIRS, IETS, SE, CA, XPS, UPS, AFM, STM …)



Electrical Device Characterization

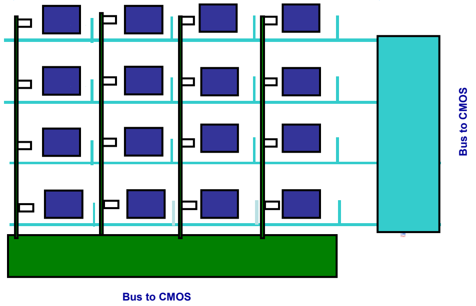
(Suite of electrical test structures & measurements)



CA Hacker et al.,
J. Phys. Chem. (2007-submitted)
CA Richter, et al.
J.Phys Chem (2006).
CA Hacker et al., Langmuir (2005).

Technology Implementation

(CMOS-based on-chip test bed)



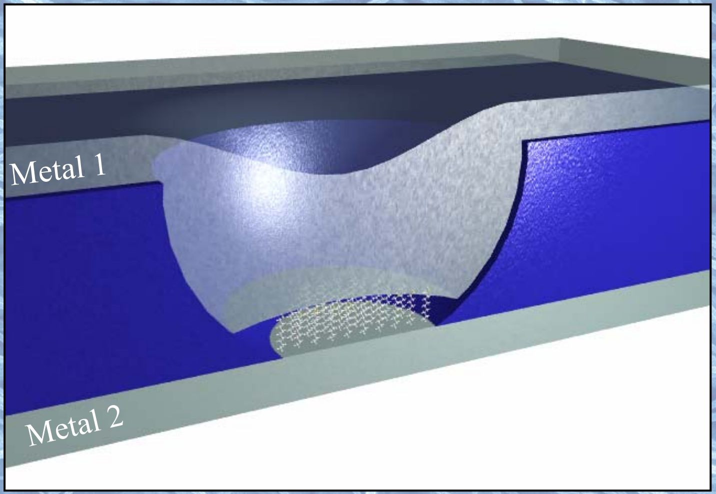
CA Richter, et al., Solid State Elec. (2006).

Latest results in
Poster 015
2007 FCMN

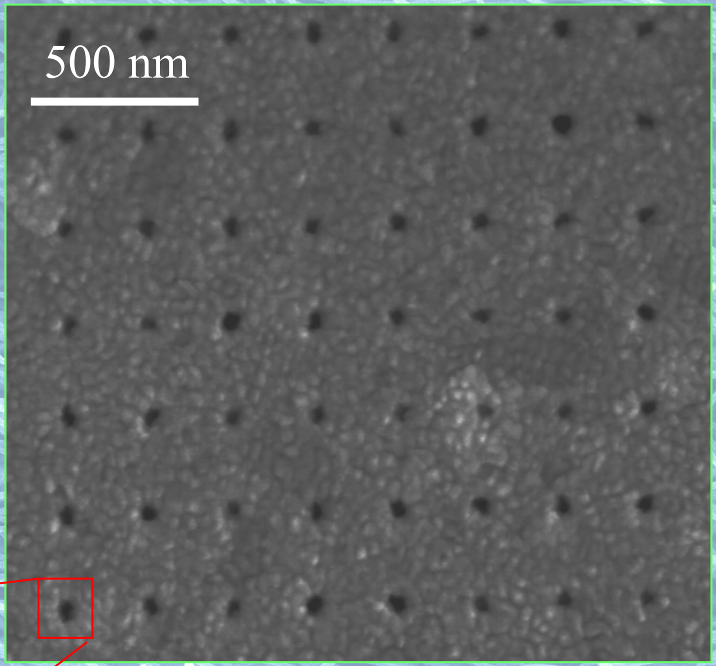
Nadine Gergel-Hackett, et al., Proc of the ACM/IEEE GLS-VLSI (2007)

Developing critical metrology necessary to support industrial innovation

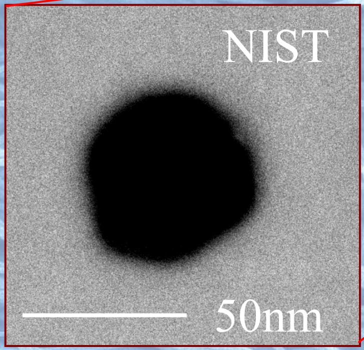
Nanopore device for molecular transport measurement



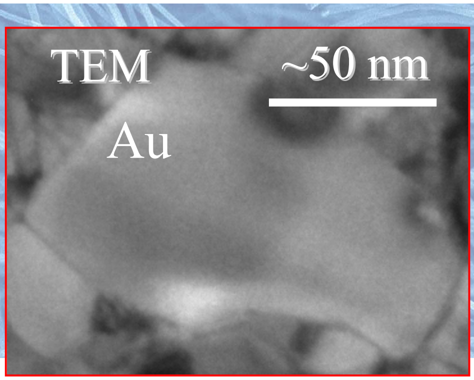
Wang et al., Appl. Phys. Lett. 89, 153105 (2006)



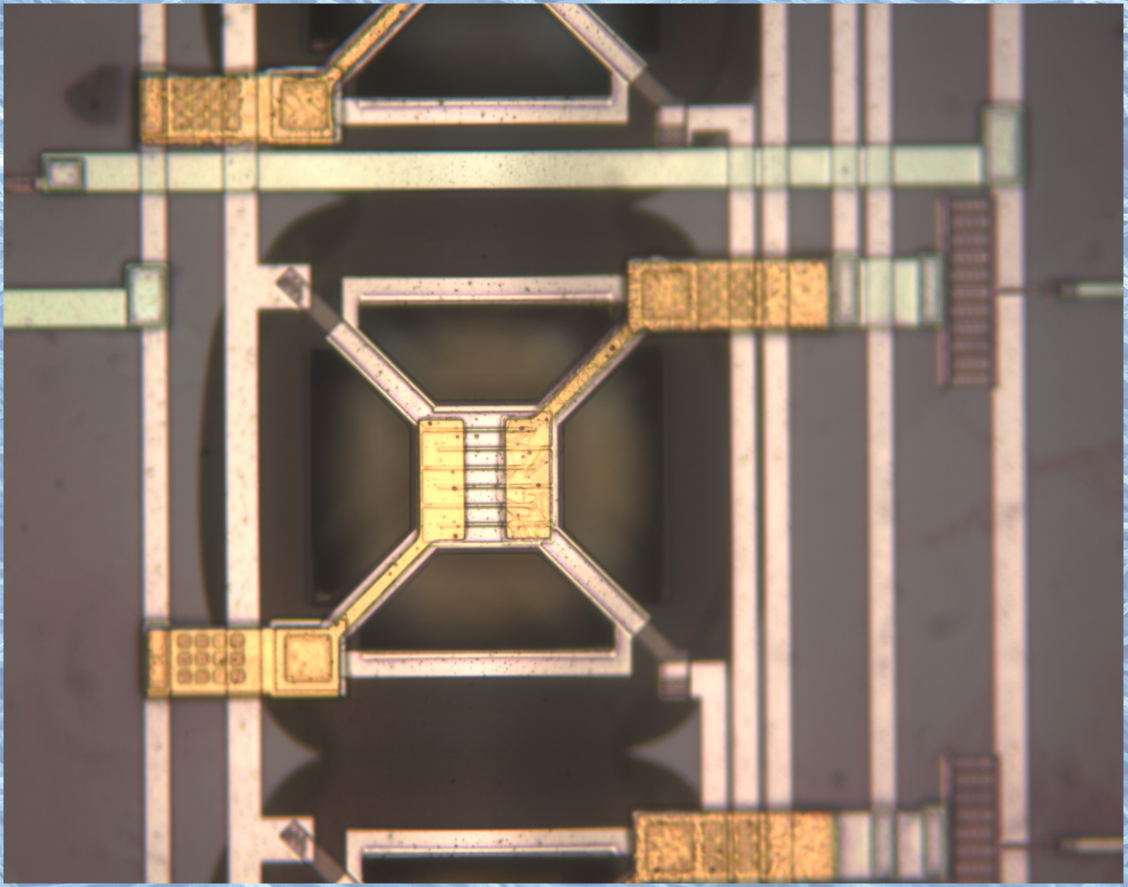
SEM image of the test pattern



TEM image of a nanopore



Micro Hot Plate Gas Sensor

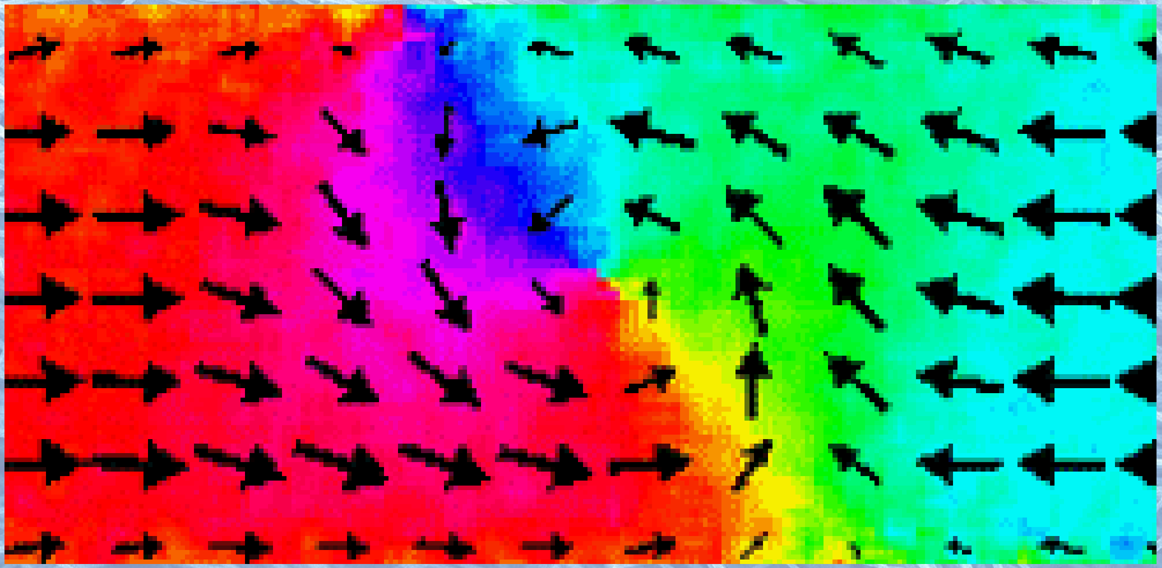


Emerging Devices and Materials

- Islands of research activity
- As efforts grow, increasing collaboration
- Coordinated programs

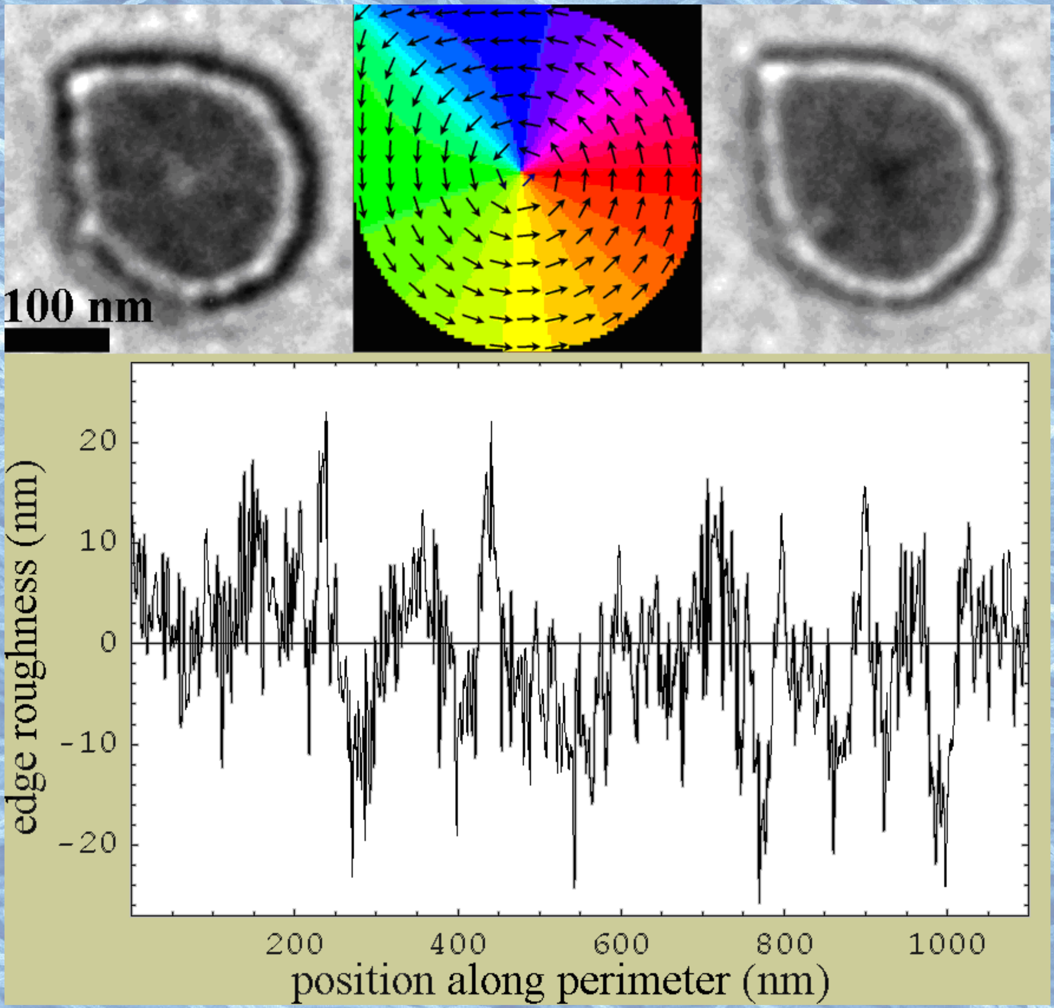
Nano-Magnetics

Scanning Electron Microscope Polarization Analysis

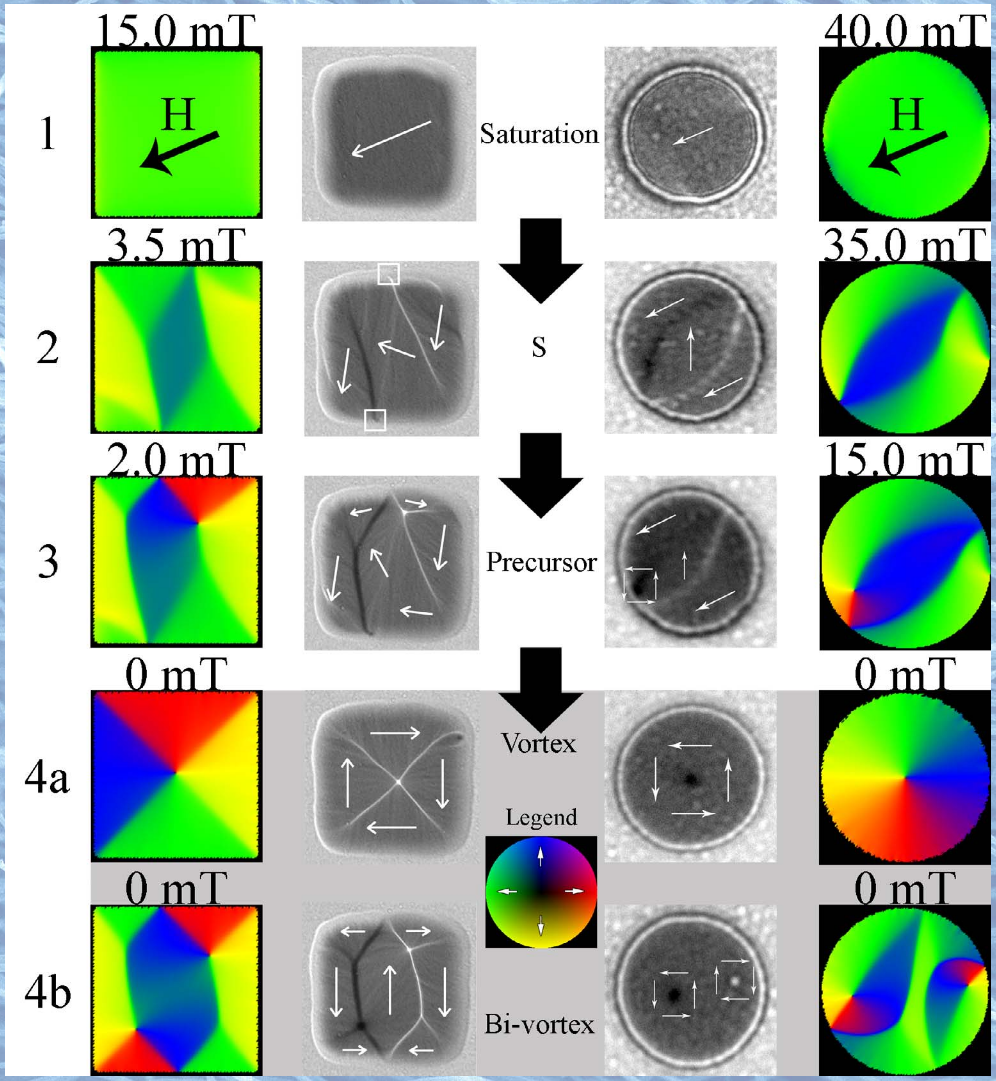


CNST, John Unguris

Nano Magnetics, TEM and Modeling



Metallurgy Division, June Lau



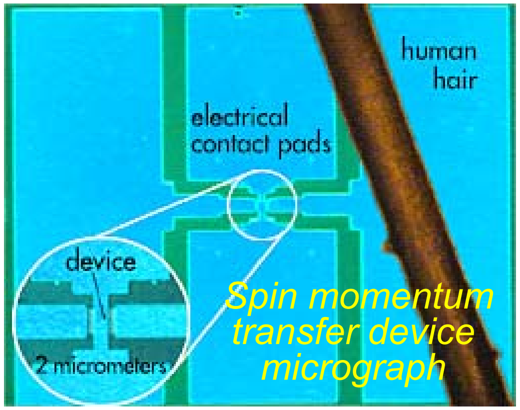
Metallurgy Division, June Lau

Spin-Transfer Microwave Nano-Oscillators

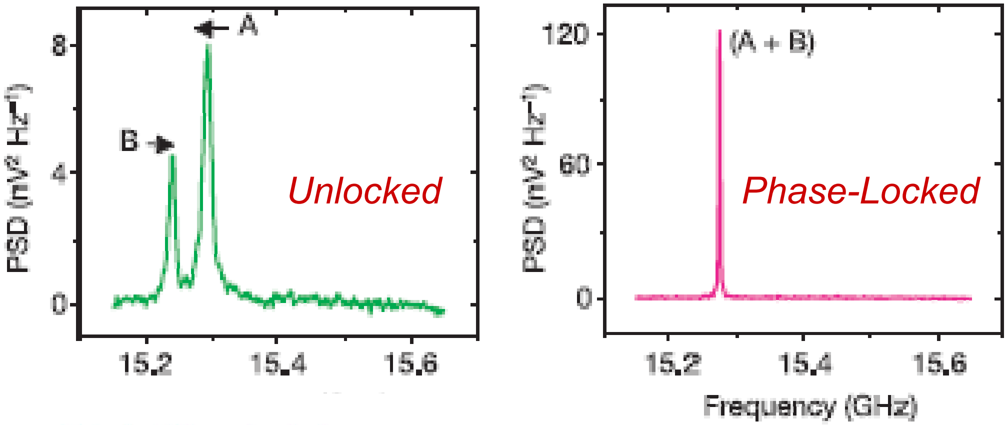
Bill Rippard, Matt Pufall, Shehzaad Kaka, Stephen Russek, and Tom Silva

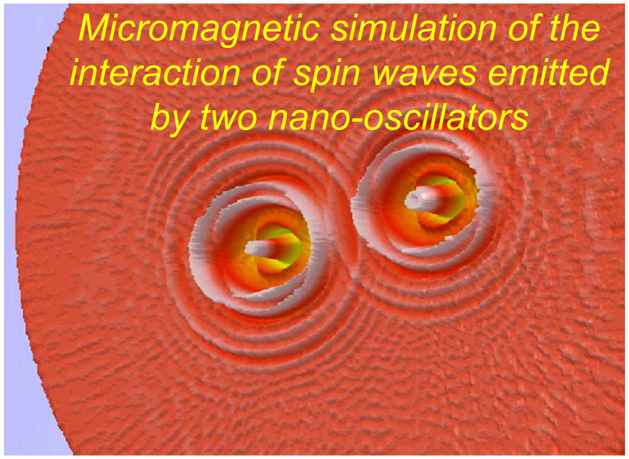
Electronics and Electrical Engineering Laboratory, NIST-Boulder

Spin-transfer oscillators use electron spin to induce coherent precession of magnetization; tunable from 5 to over 40 gigahertz depending on dc current and magnetic field; 50 nanometers in diameter. They have very narrow spectral linewidths.



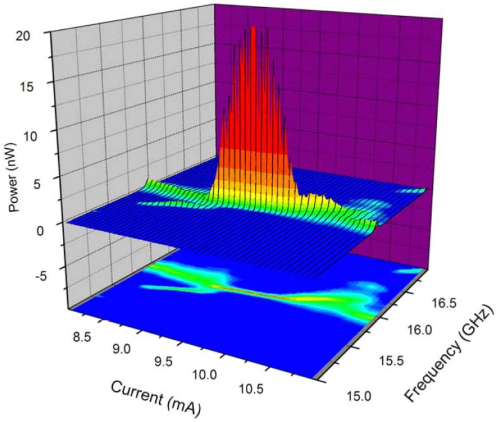
Spin momentum transfer device micrograph





Micromagnetic simulation of the interaction of spin waves emitted by two nano-oscillators

Power Output of Phase-Locked Spin-Transfer Oscillators



Phase-locking of the dynamic magnetic properties of two spin-transfer oscillators located 500 nanometers apart

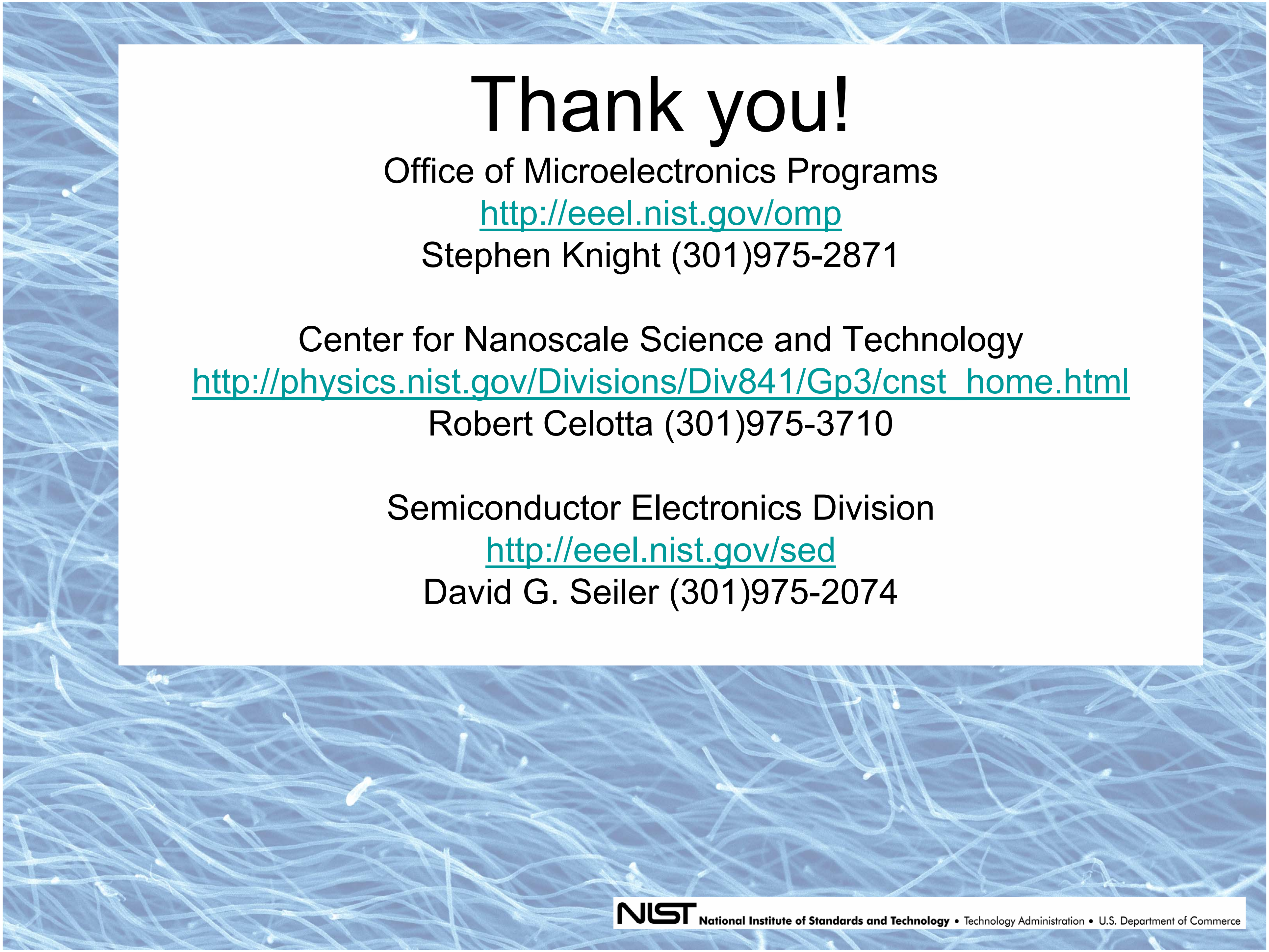
> *Perhaps as magnetics makes its way into the common semiconductor world, this will provide a useful system reference clock.*
> *— Michael Brown, Intel*

Future applications :

- Reference oscillators
- Directional transmitters and receivers in cell phones and radar systems
- Nano-wireless communications within or between chips
- High-frequency signal processors
- On-chip microwave spectroscopy
- Switching of magnetic random access memory (MRAM)

Conclusions

- Robust programs supporting Nanoelectronics metrology at NIST
- Internal and external collaborations are essential for success!



Thank you!

Office of Microelectronics Programs
http://eeel.nist.gov/omp
Stephen Knight (301)975-2871

Center for Nanoscale Science and Technology
http://physics.nist.gov/Divisions/Div841/Gp3/cnst_home.html
Robert Celotta (301)975-3710

Semiconductor Electronics Division
http://eeel.nist.gov/sed
David G. Seiler (301)975-2074