Inelastic Electron Tunneling Spectroscopy (IETS) of Ultra-thin Gate Dielectrics

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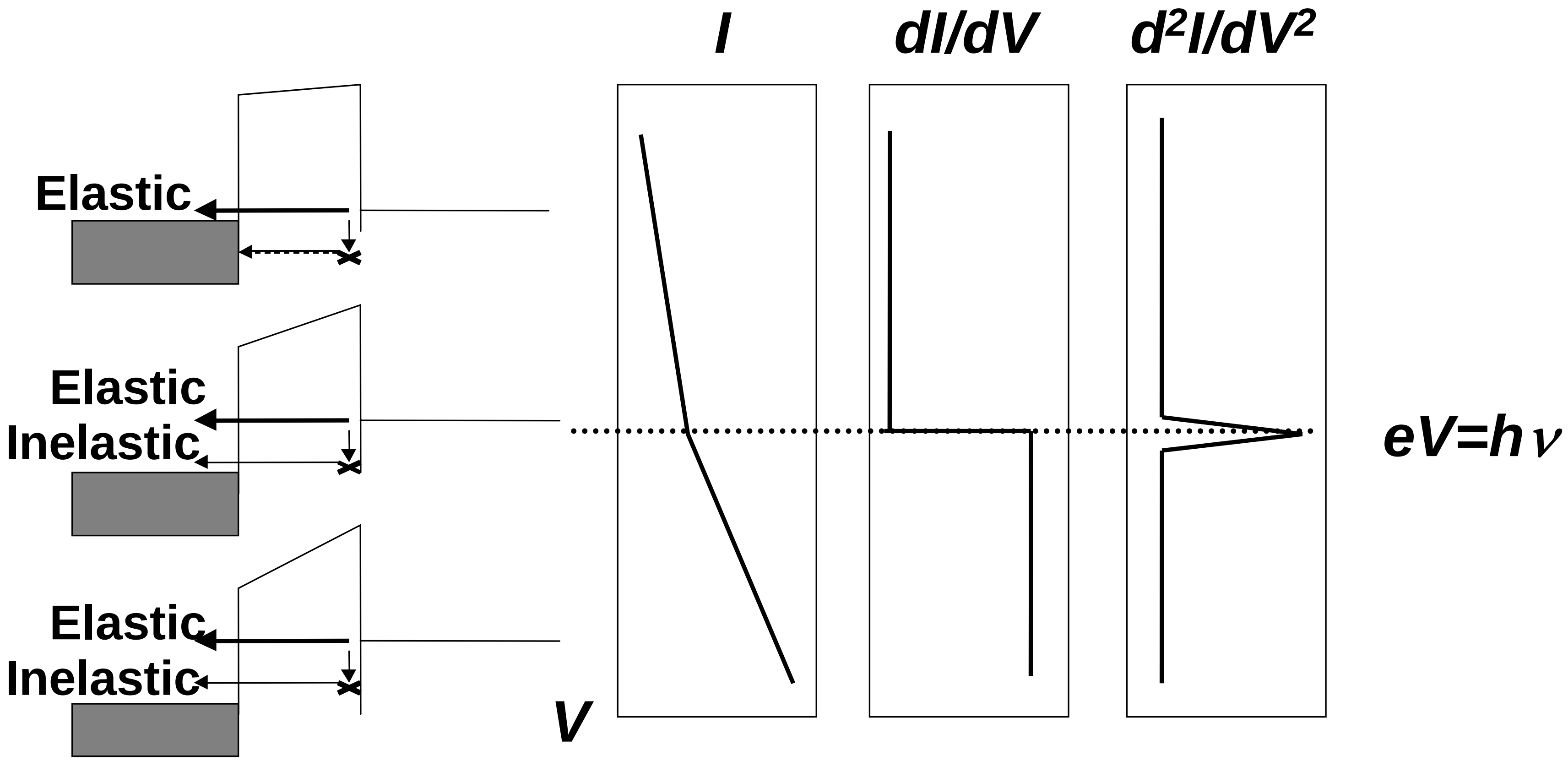
Inelastic Electron Tunneling Spectroscopy

An Inelastic Tunneling Event at $E=eV=h\nu$ Causes

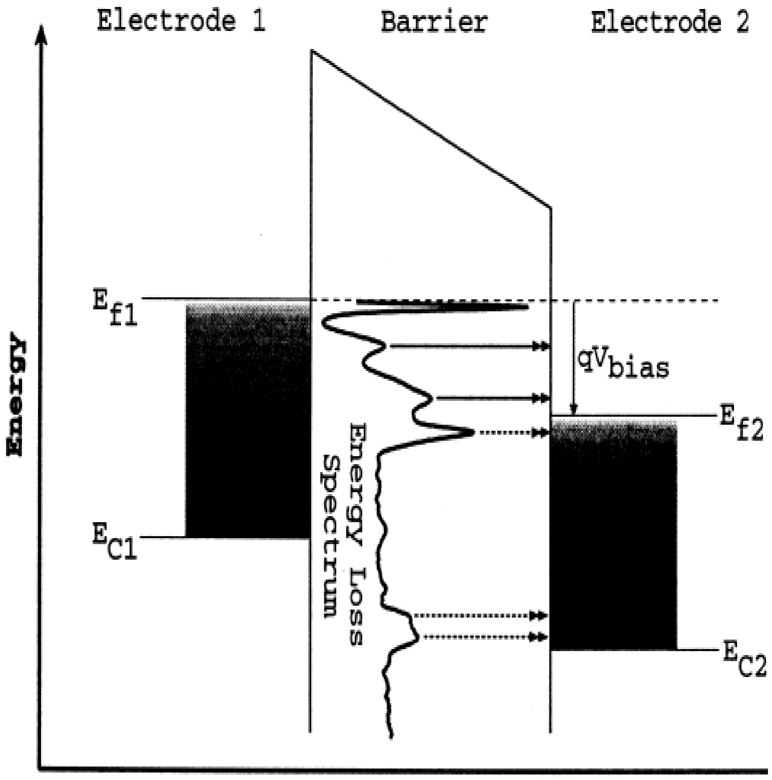
(a) *I-V* to increase slope;

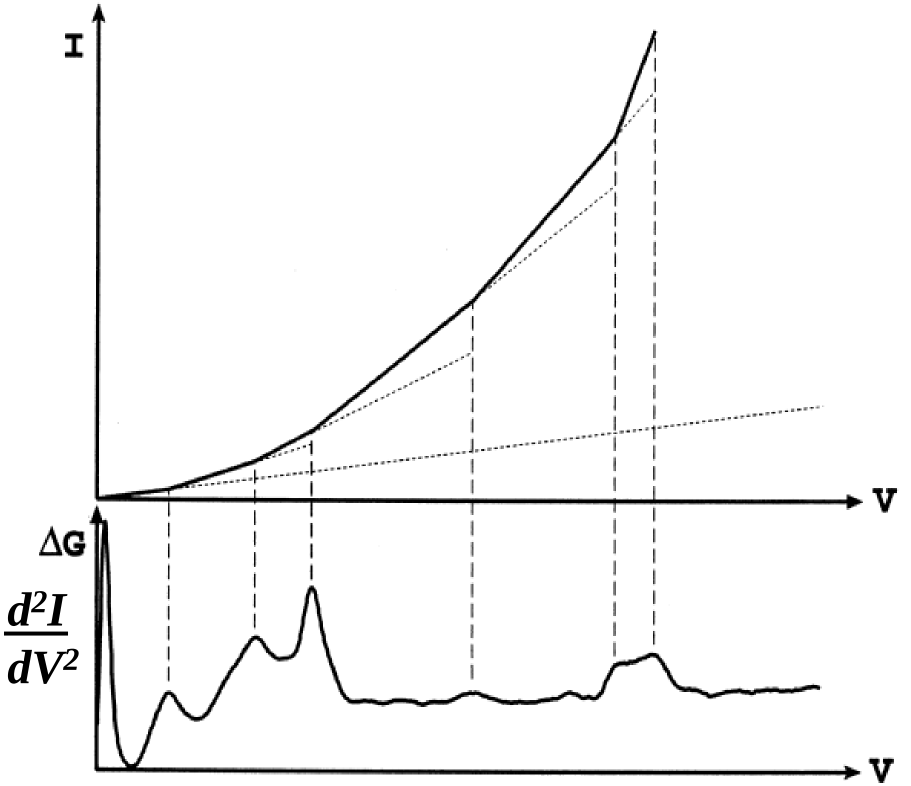
(b) a step in *dI/dV;*

(c) a peak in d^2I/dV^2



Various Inelastic Modes in the Barrier (Left) May Be Reflected in IETS (Bottom Right)





IETS probes phonons, bonding vibrations, impurities, and Traps

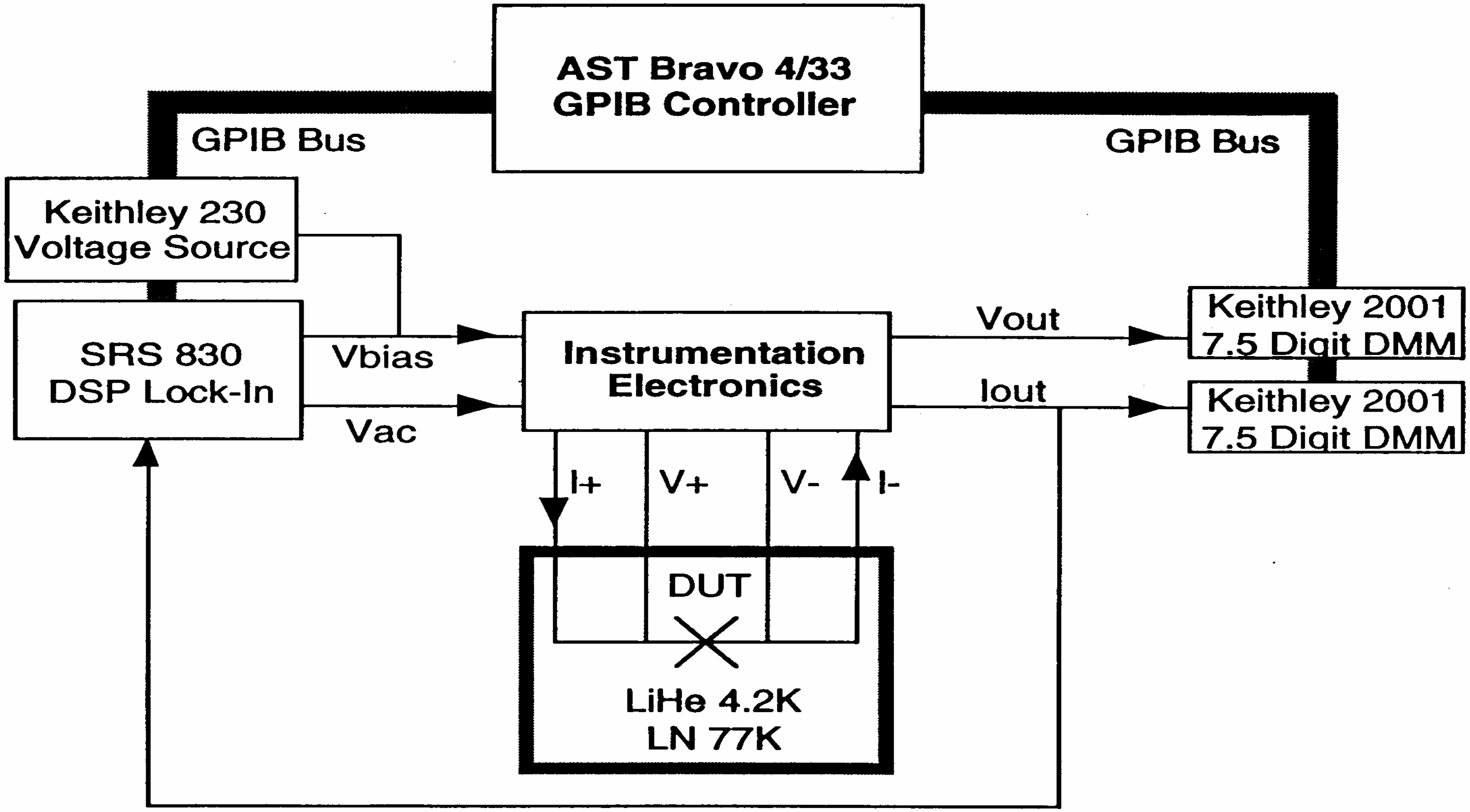
Interactions Detectable by IETS

- Substrate Silicon Phonons
- Gate Electrode Phonons
- Dielectric Vibrations (Phonons)
- Impurity Bonding Vibrations
- Trap States

Measurement Setup
based on standard lock-in measurement

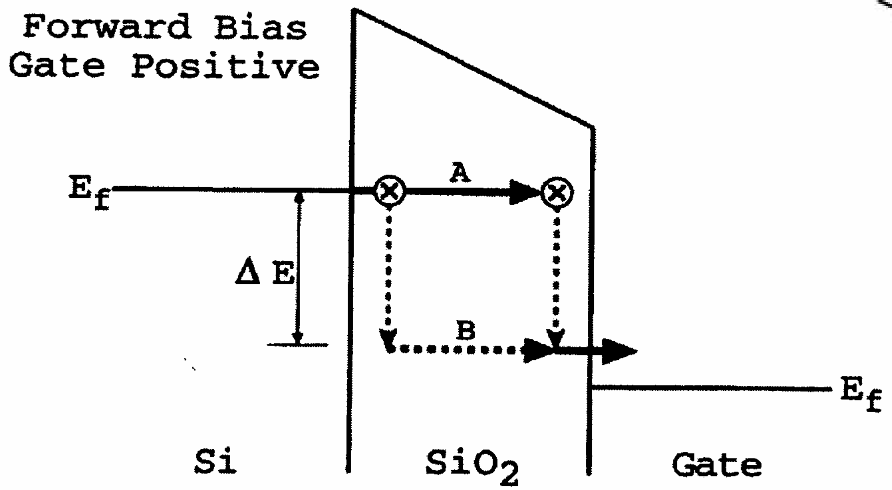
Second derivative of I-V is proportional to second harmonic signal from device under test.

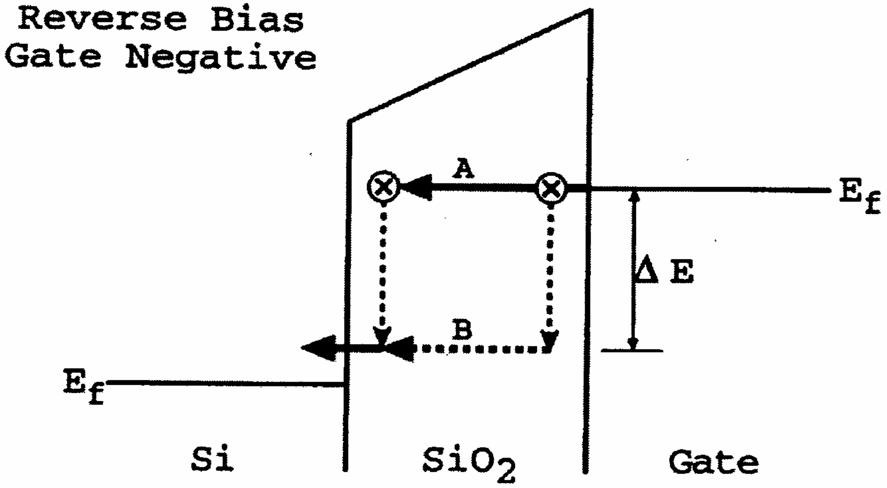
$$I(V + v\cos\omega t) = I(V) + \frac{dI}{dV} v\cos\omega t + \frac{1}{4}\frac{d^2I}{dV^2} v^2 (1+\cos 2\omega t) + \ldots$$



Bias Polarity Dependence

Electrons have higher probability to interact with a vibration located near the positively biased electrode.





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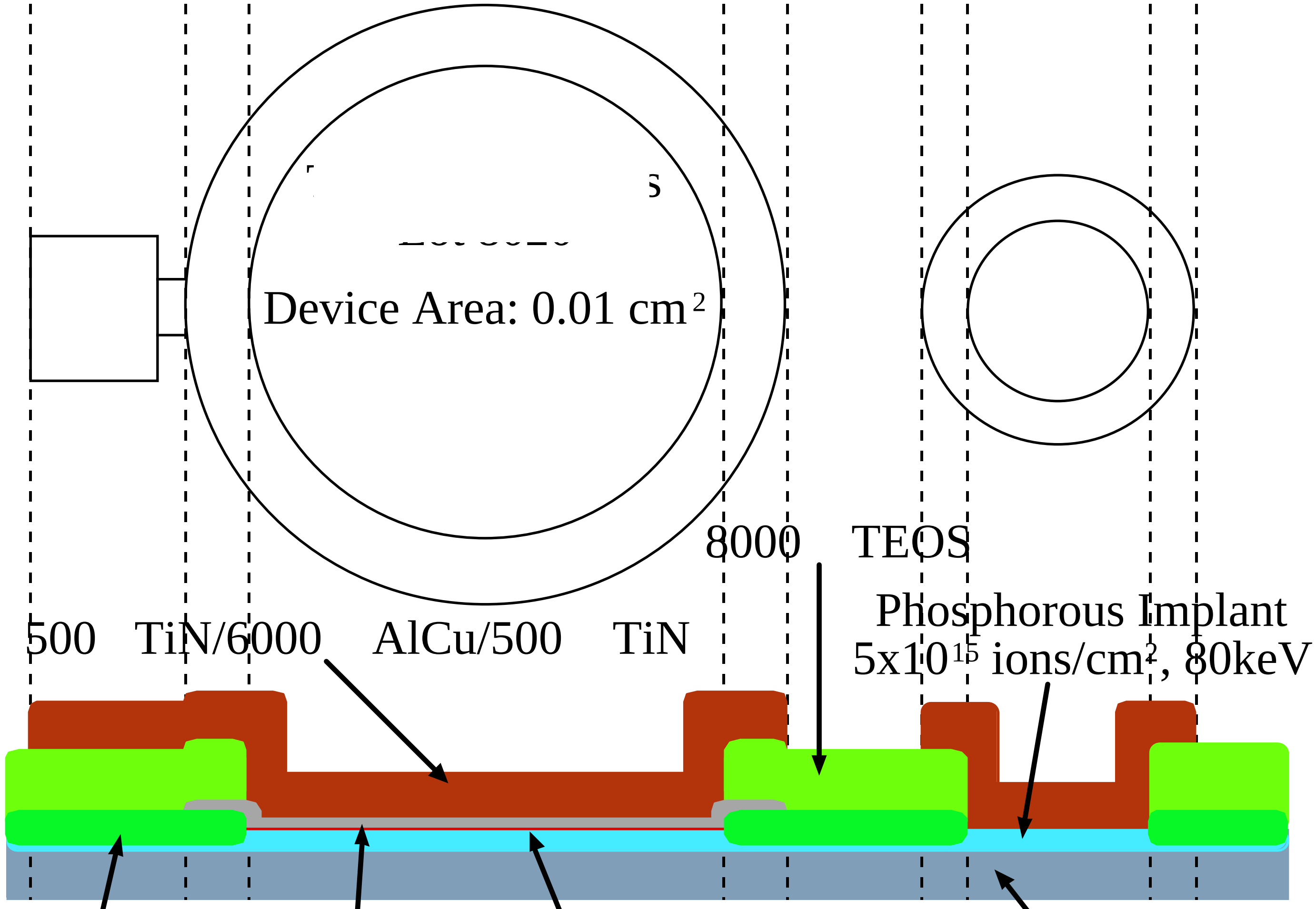
SAMPLES



Device Area: 0.01 cm²

8000 TEOS

Phosphorous Implant
5x10^{15} ions/cm^{2}, 80keV

500 TiN/6000 AlCu/500 TiN

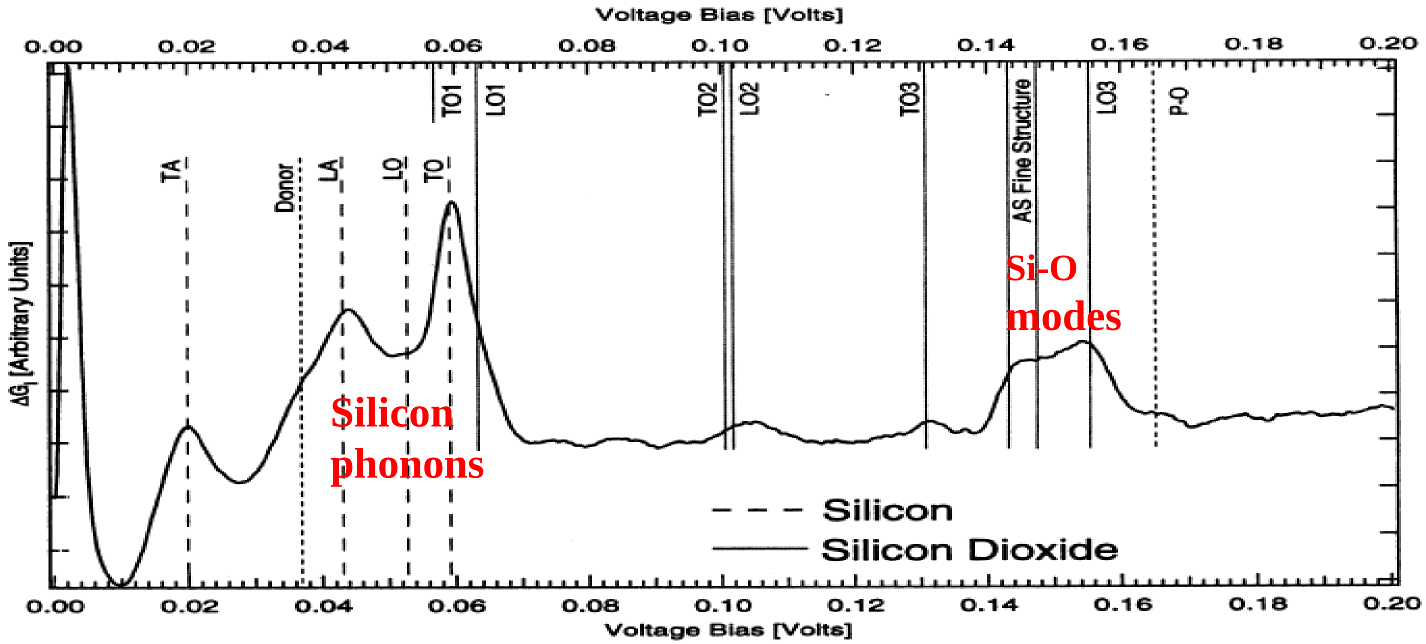
4500
LOCOS

2500 ISD
Polysilicon

15 to 18
Tunnel Oxide

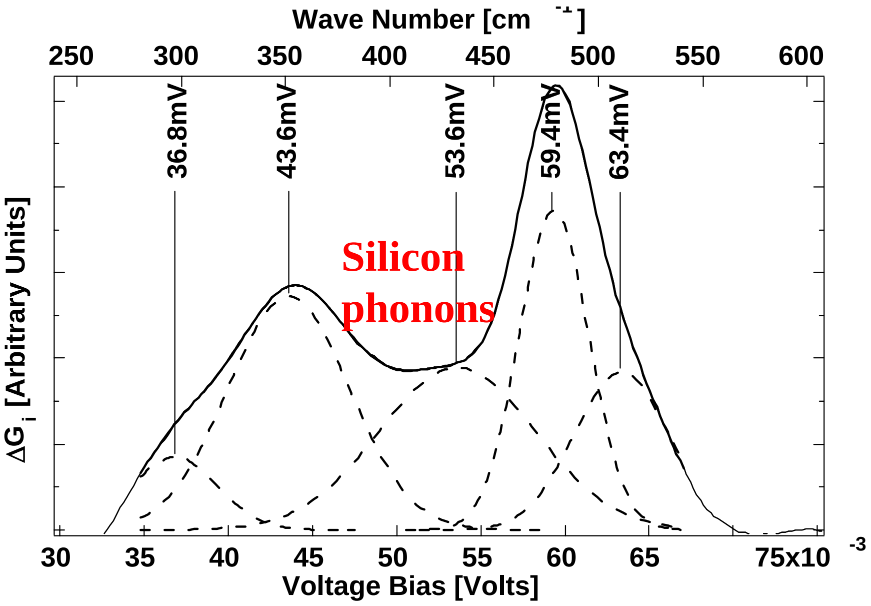
n-type (100),
1½cm-10½cm

IETS Spectrum of SiO_2/Si

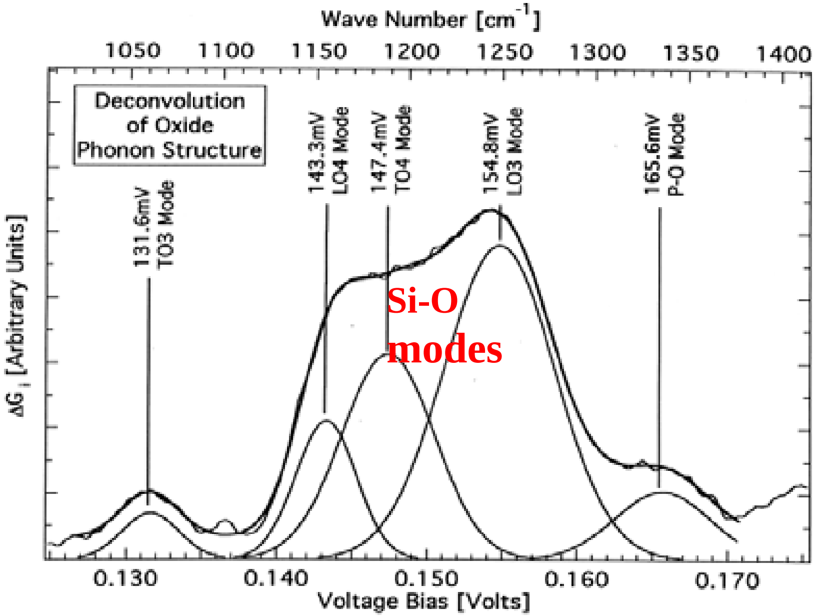


Si-O modes

Silicon phonons



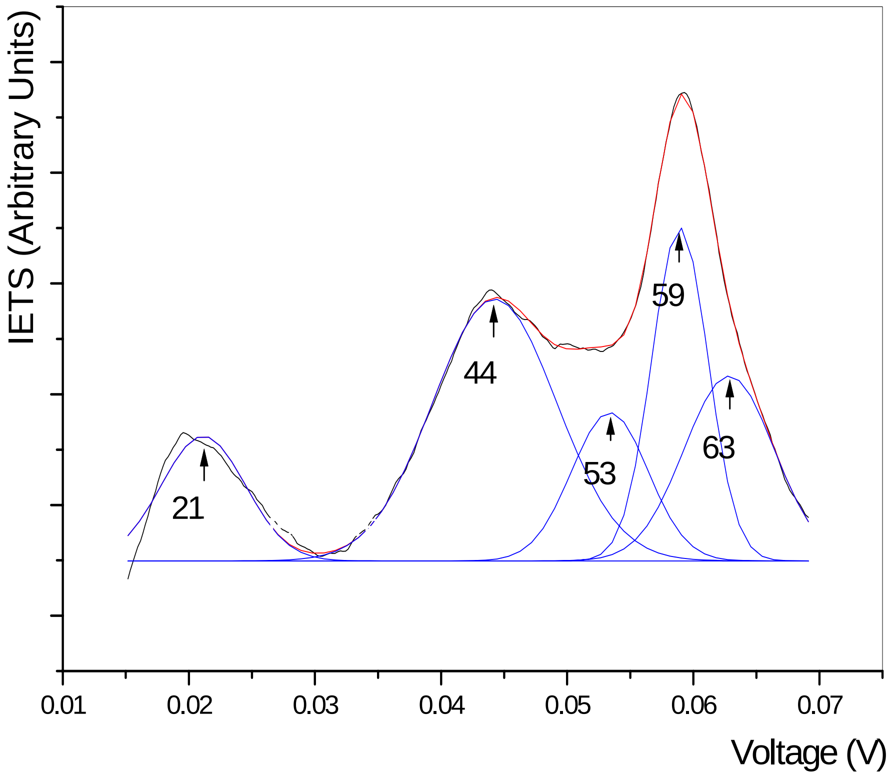
Silicon phonons



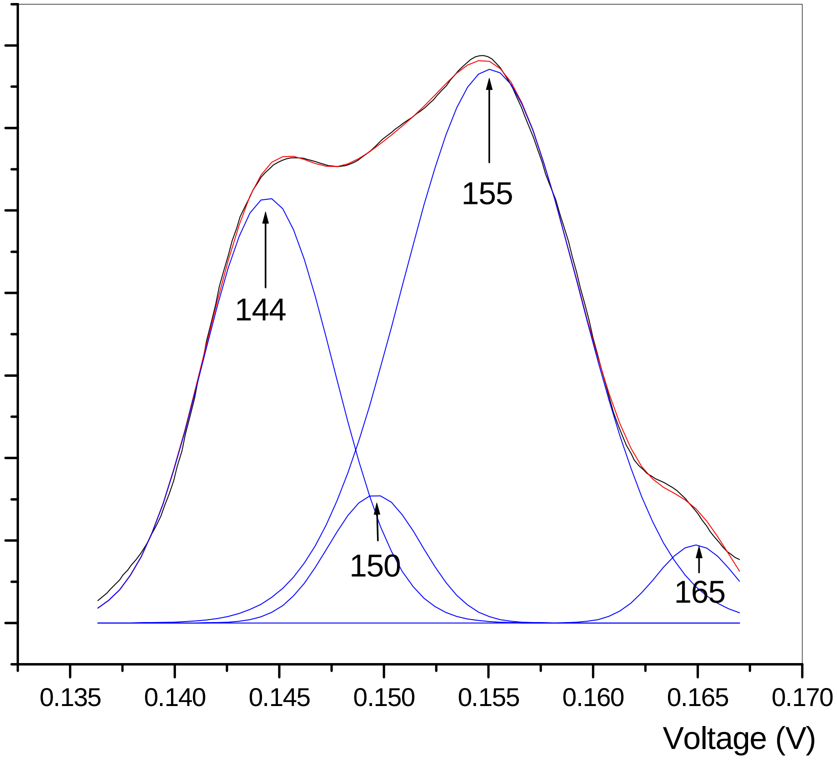
Si-O modes

Si phonons and SiO_2 vibration modes

Si phonons

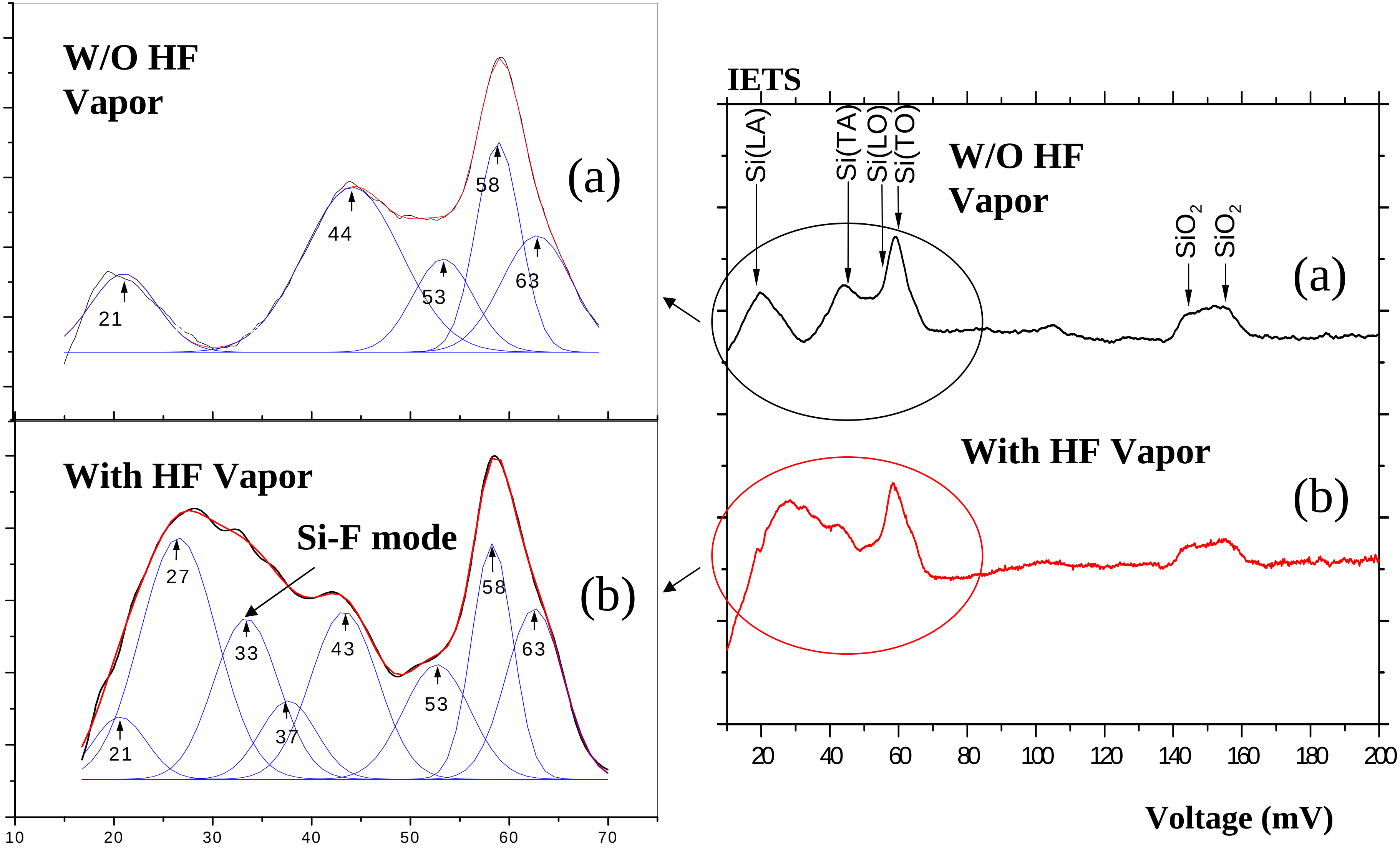


SiO_2 vibrations



21 mV: Si TA mode
44 mV: Si LA mode
53 mV: Si LO mode
59 mV: Si TO mode

63 mV: Si-O LO1 mode (Rocking)
144 mV: Si-O AS1 mode (Asymmetric Stretch)
150 mV: Si-O AS2 mode (Asymmetric Stretch)
155 mV: Si-O LO3 mode (Symmetrric Stretch)
165 mV: P-O mode

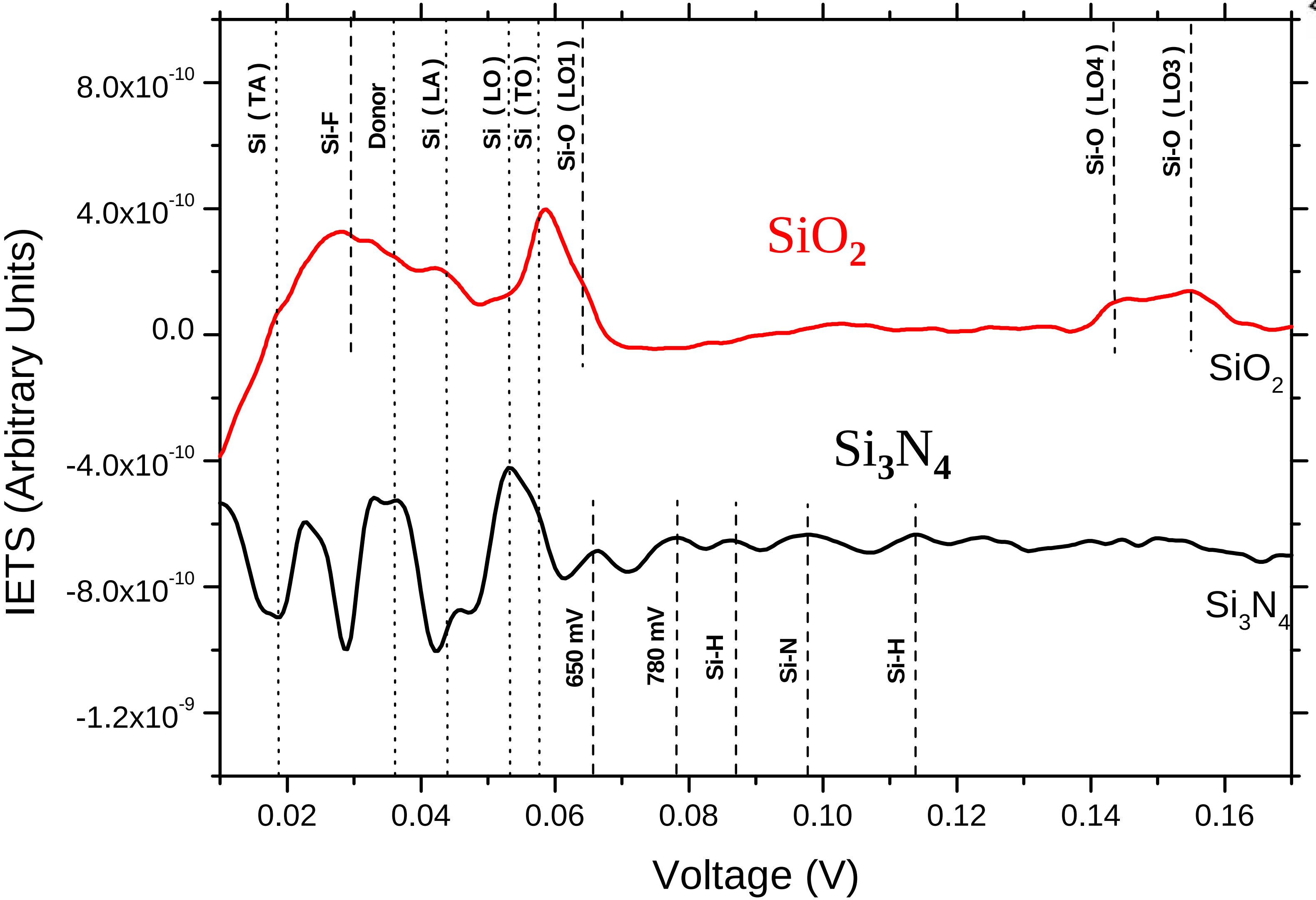


IETS can detect structure changes caused by different processing conditions.

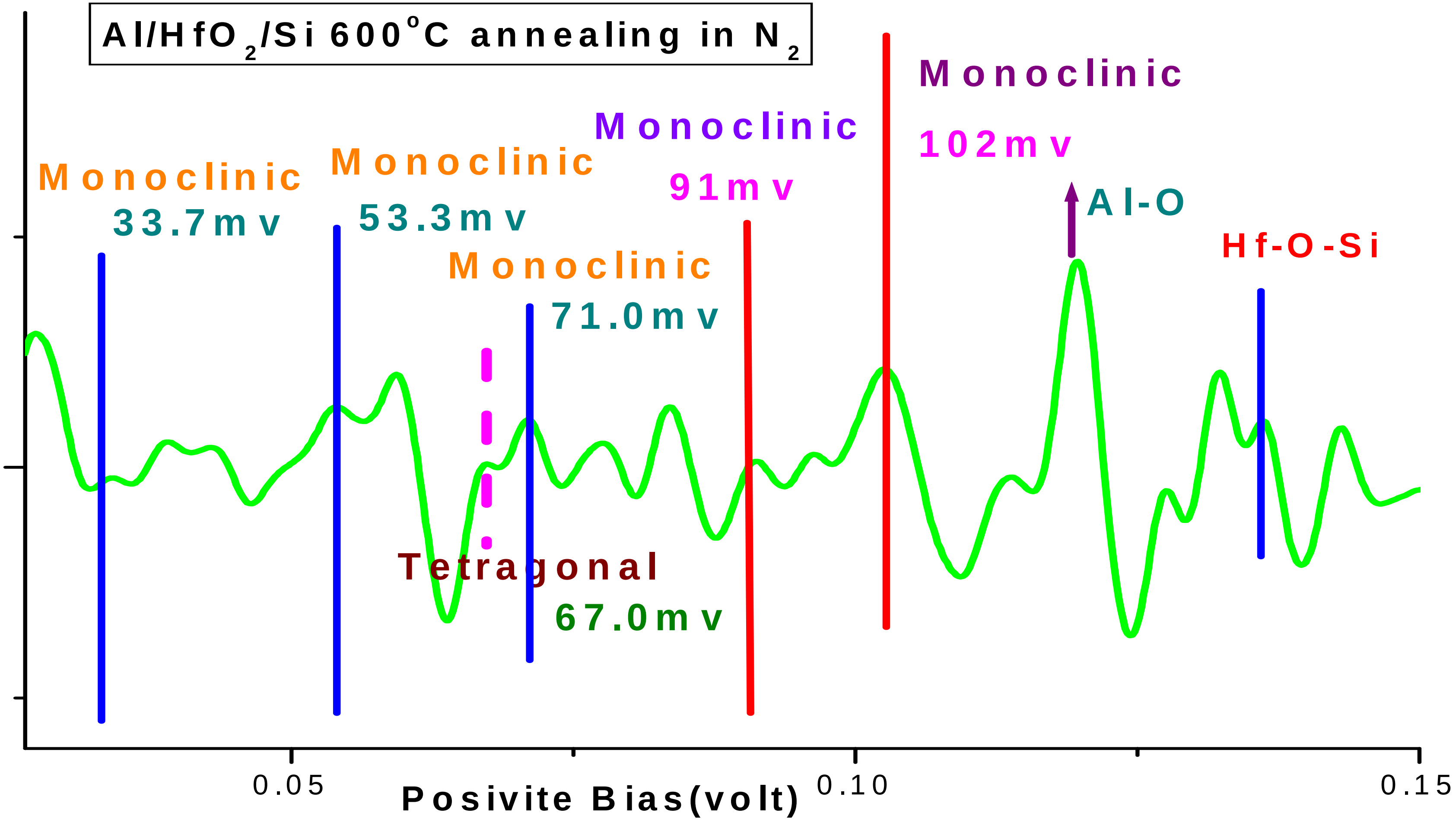
(a) SiO_2/Si without HF vapor pre oxidation cleaning

(b) SiO_2/Si with the HF vapor pre oxidation cleaning

IETS of Thermal SiO_2/Si and CVD Si_3N_4/Si



IETS of Al/HfO$_2$/Si

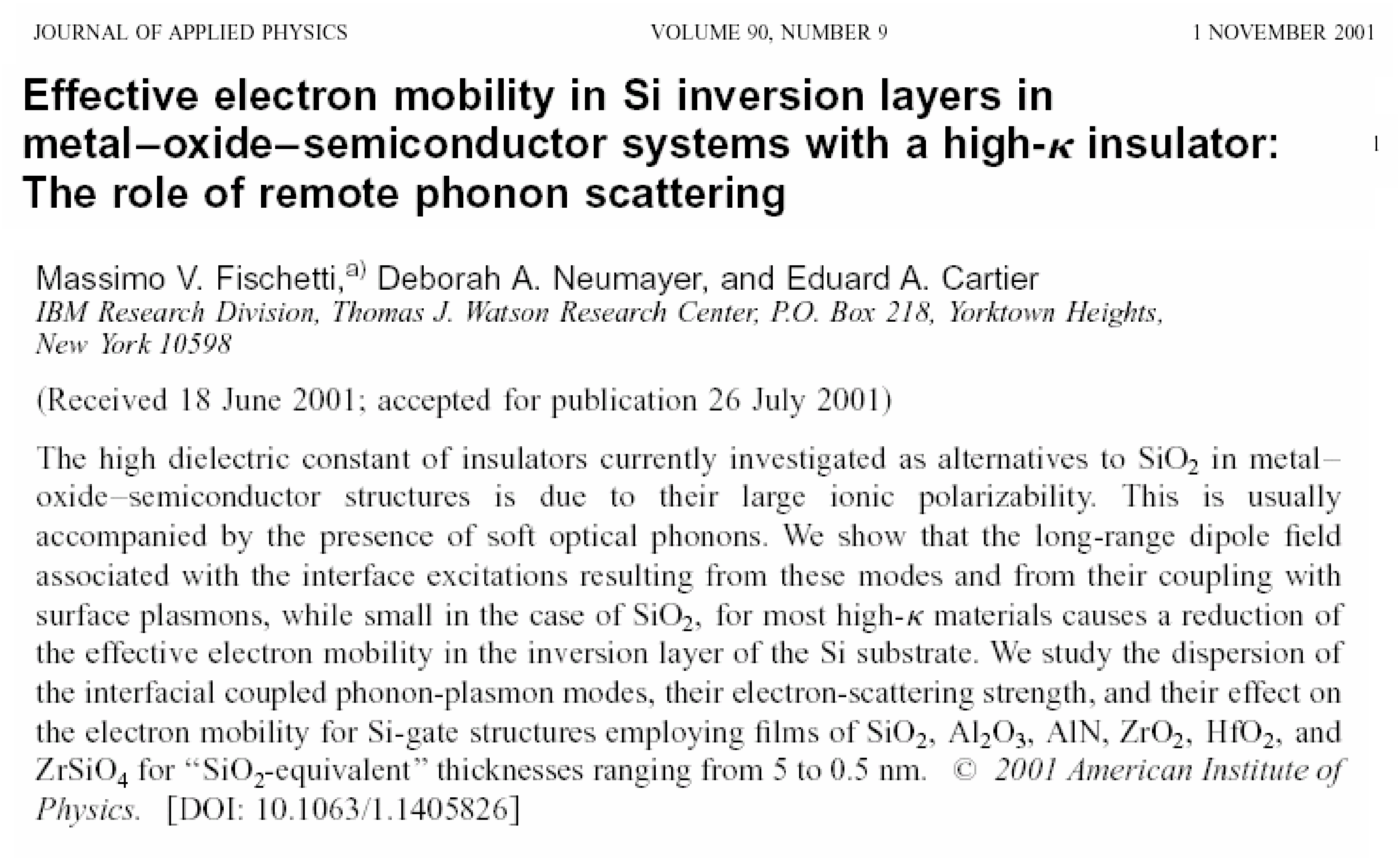


Theoretical (LDA and GGA) and experimental (Raman and IETS) of phonon modes in HfO_2

Modes (cm-1)	Monoclinic Bu	Monoclinic Ag,Bg	Monoclinic Bg	Monoclinic Ag	Monoclinic Bg	Moniclinic Bg	Tetragonal
LDA	261	423,424	570	738	821	667	536
GGA	252	382,385	529	640	716	627	
Raman	256	382,398	551	672	773	640	
IETS	270 (33.7mv)	411 (51mV)	572 (71mv)	725 (91mv)	822 (109mv)	637 (79mv)	536 (66.4mv)

---Xinyuan Zhao and David Vanderbit, Physical Review B,vol. 65, 2002

Remote Phonon Scattering



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Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-κ insulator: The role of remote phonon scattering

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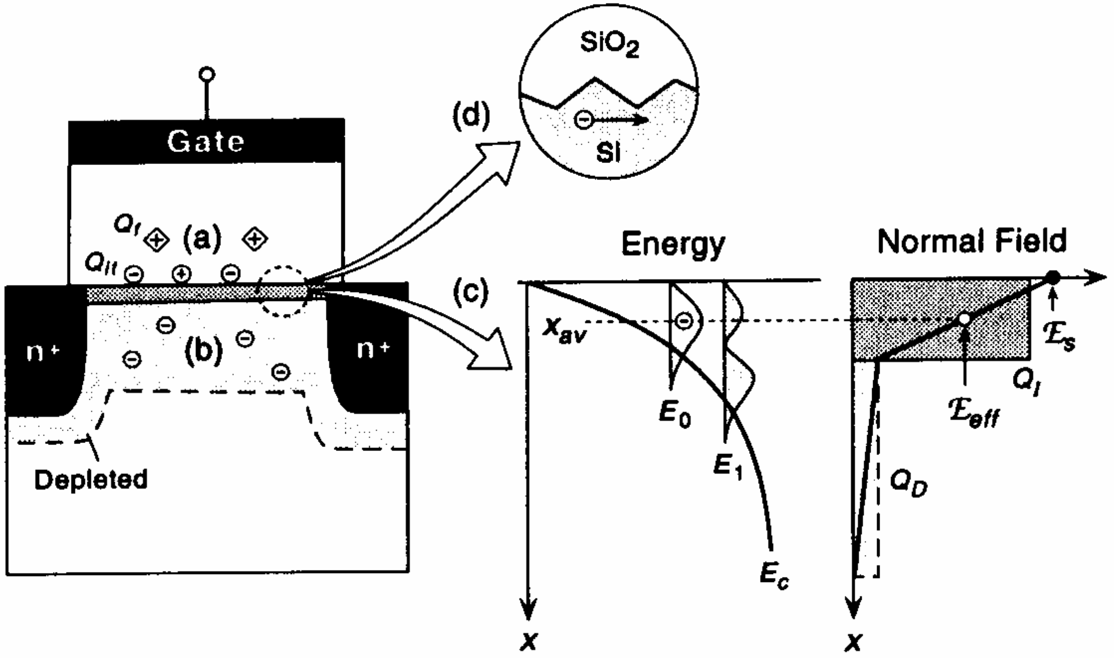
(Received 18 June 2001; accepted for publication 26 July 2001)

The high dielectric constant of insulators currently investigated as alternatives to SiO_2 in metal–oxide–semiconductor structures is due to their large ionic polarizability. This is usually accompanied by the presence of soft optical phonons. We show that the long-range dipole field associated with the interface excitations resulting from these modes and from their coupling with surface plasmons, while small in the case of SiO_2, for most high-κ materials causes a reduction of the effective electron mobility in the inversion layer of the Si substrate. We study the dispersion of the interfacial coupled phonon-plasmon modes, their electron-scattering strength, and their effect on the electron mobility for Si-gate structures employing films of SiO_2, Al_2O_3, AlN, ZrO_2, HfO_2, and $ZrSiO_4$ for "SiO_2-equivalent" thicknesses ranging from 5 to 0.5 nm. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1405826]

Scattering mechanisms



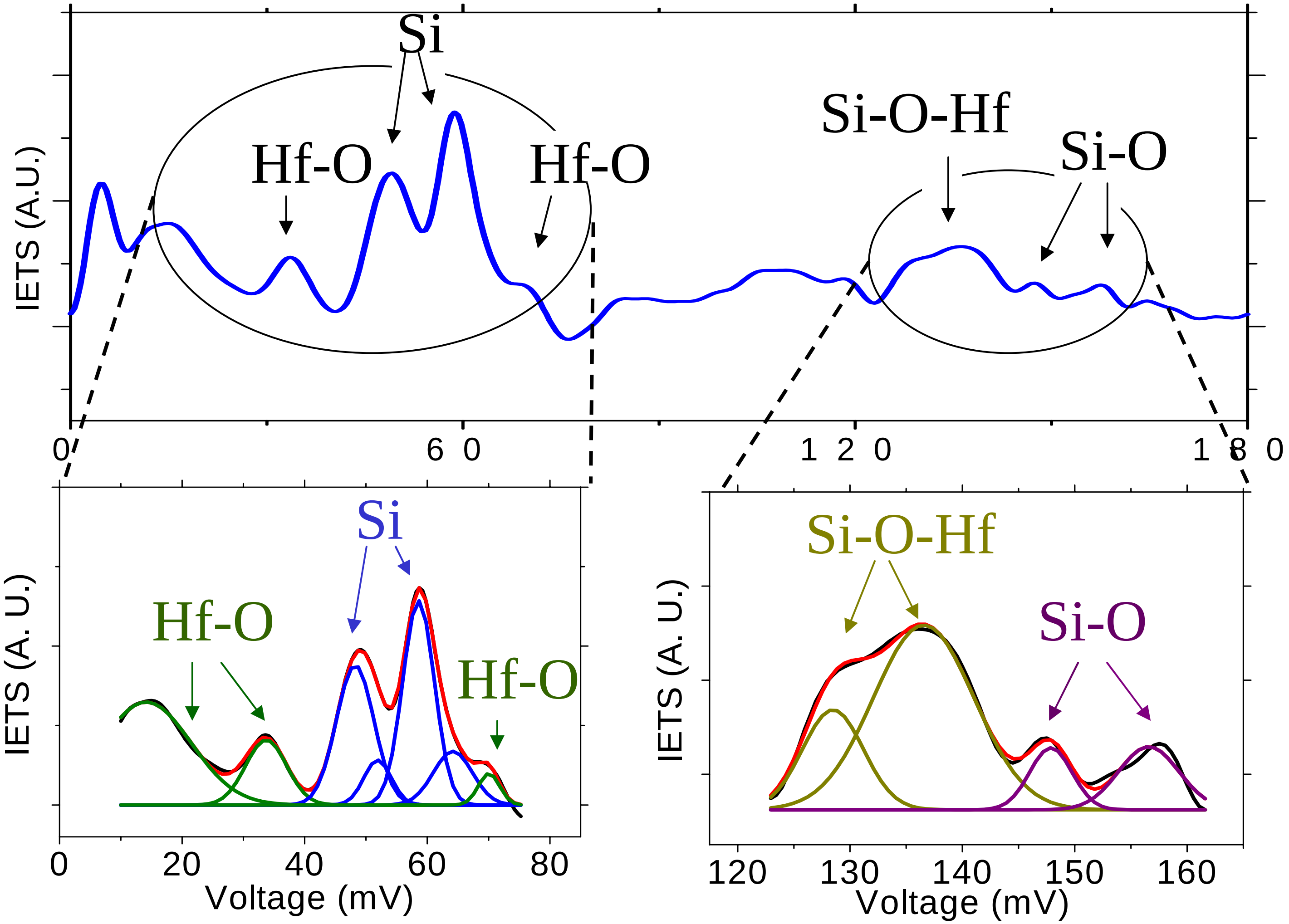
(a) Coulomb scattering due to trapped charge in dielectrics

(b) Coulomb scattering due to ionized impurities in depletion layer

(d) Surface roughness scattering

(e) Phonon scattering due to lattice vibration

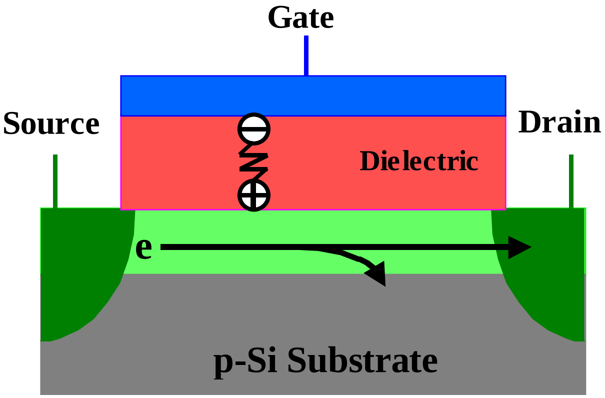
IETS Signals for HfO_2/Si



Lower energy peaks are Si and HfO_2 phonons; Higher energy peaks are Si-O and SiO-Hf phonons

Mobility Reduction due to Soft Phonon Scattering

Gate Dielectric	SiO_2	HfO_2
Bond strength	Strong Si-O bond	Weak Hf-O bond
Optical phonon energy (meV)	138	34, 48, 70
Rate of emission/absorption phonon	Low	High
Static permittivity $\varepsilon_{ox}^{0}/\varepsilon_o$	3.9	22.0
Optical permittivity $\varepsilon_{ox}^{\infty}/\varepsilon_o$	2.5	5.03
Electron phonon coupling strength	Low	High
Mobility limited by remote phonon scattering	High	Low



HfO_2 gated MOSFET might have reduced mobility due to soft phonon scattering.

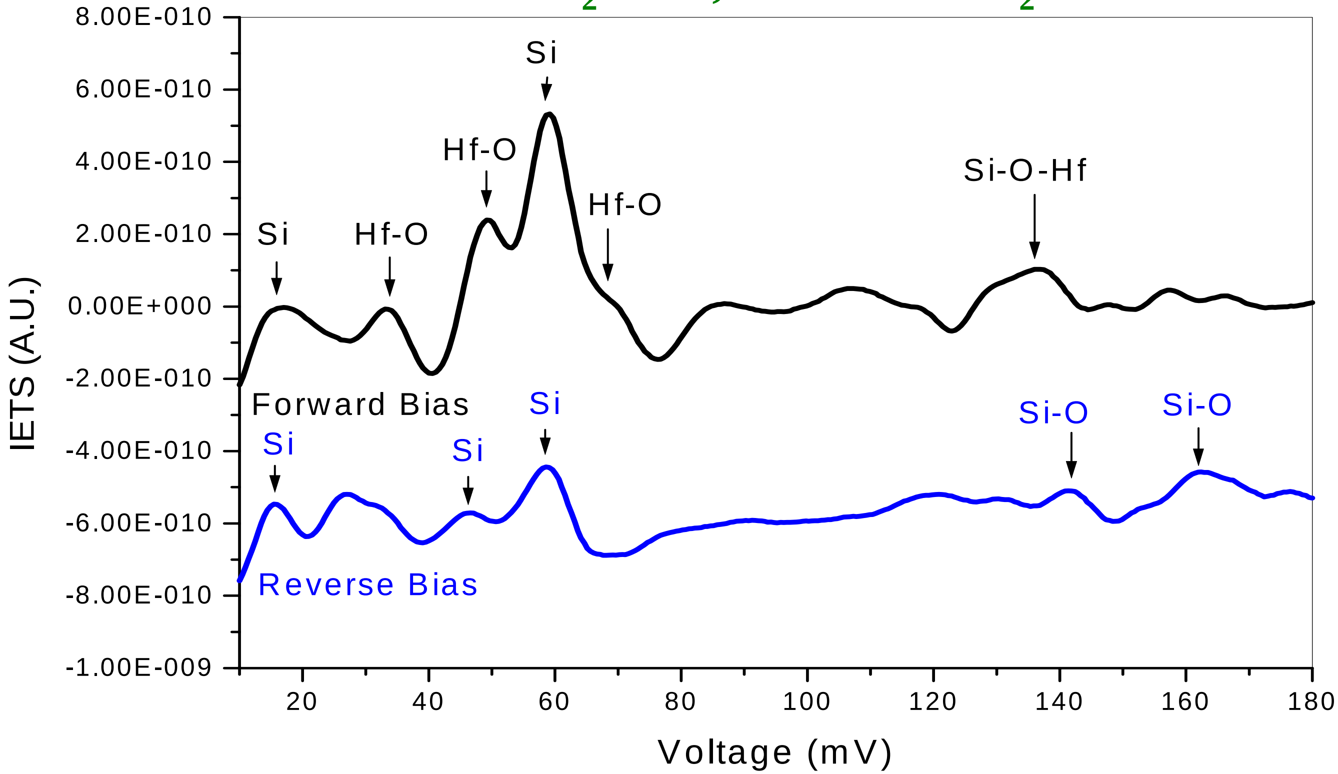
A) Phonon energies close to *kT* at room temp.

B) Scattering strength $\propto \dfrac{\varepsilon_{ox}^{0} - \varepsilon_{ox}^{\infty}}{(\varepsilon_{si}^{\infty} + \varepsilon_{ox}^{\infty})(\varepsilon_{si}^{\infty} + \varepsilon_{ox}^{0})}$

[M. Fischetti, et.al, J. Appl. Phys.,Vol.90, p4587, 2001]

Bias Polarity Dependence of IETS for Al/HfO_2/Si

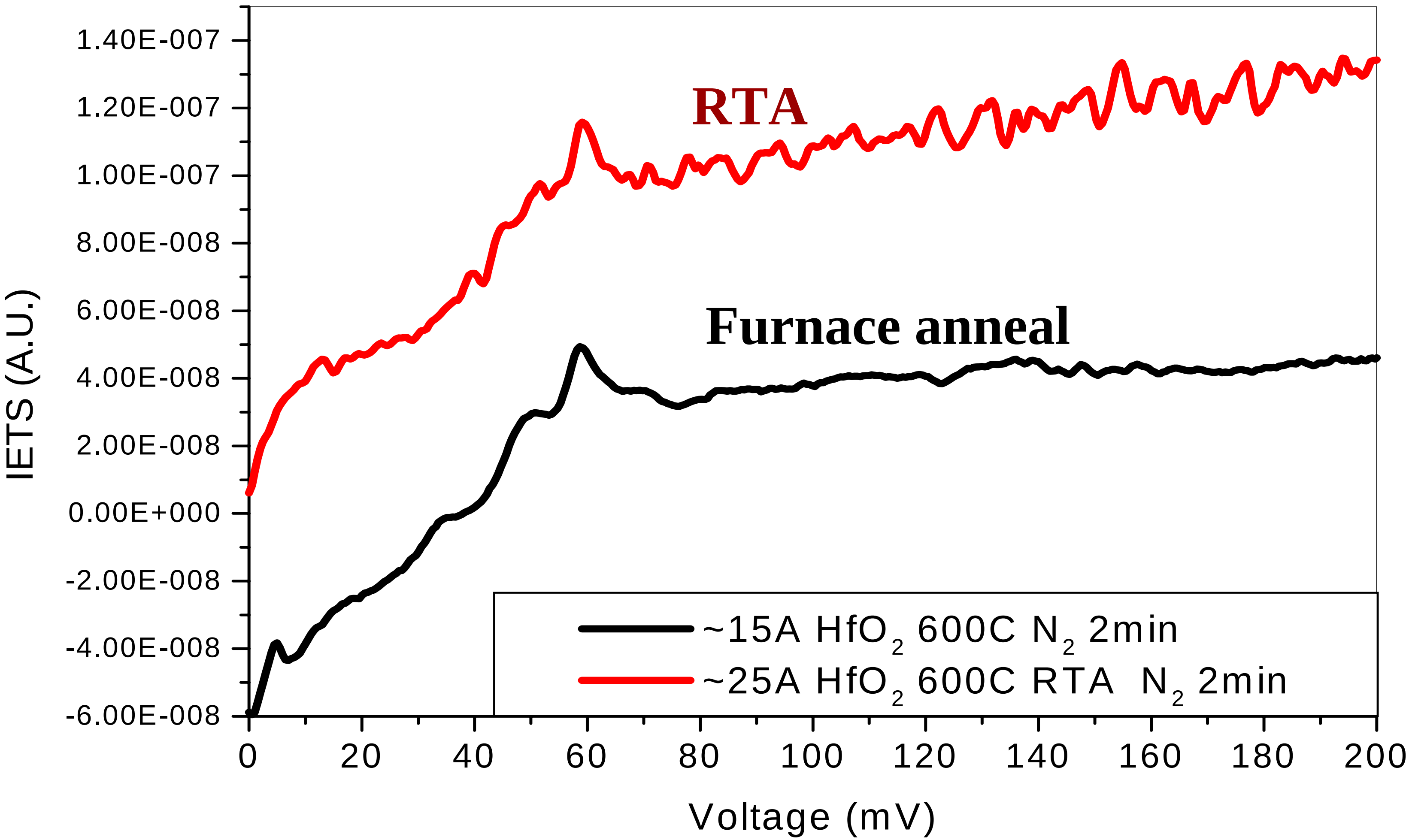
- Results suggest significantly different microstructures near Al-HfO_2 interface and Si-HfO_2 interface.
- HfO_2/Si interface is more SiO_2-like.
- HfO_2/Al interface is more HfO_2-like.



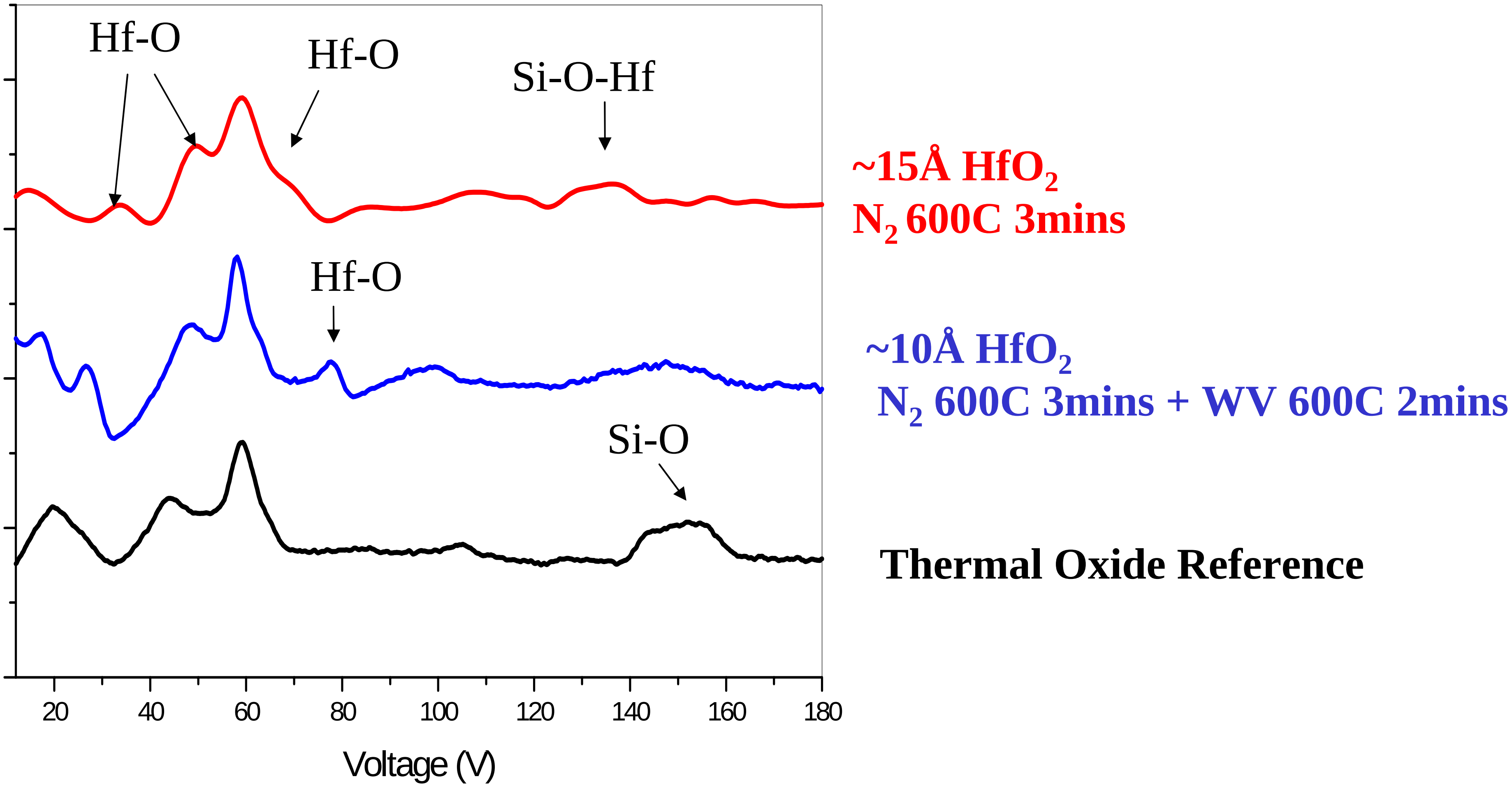
~15A JVD HfO_2 on Si, annealed in N_2 600C 3min

IETS sensitive to process variations for Al/HfO$_2$/Si structure (1)

Post-deposition annealing: Furnace vs. RTA

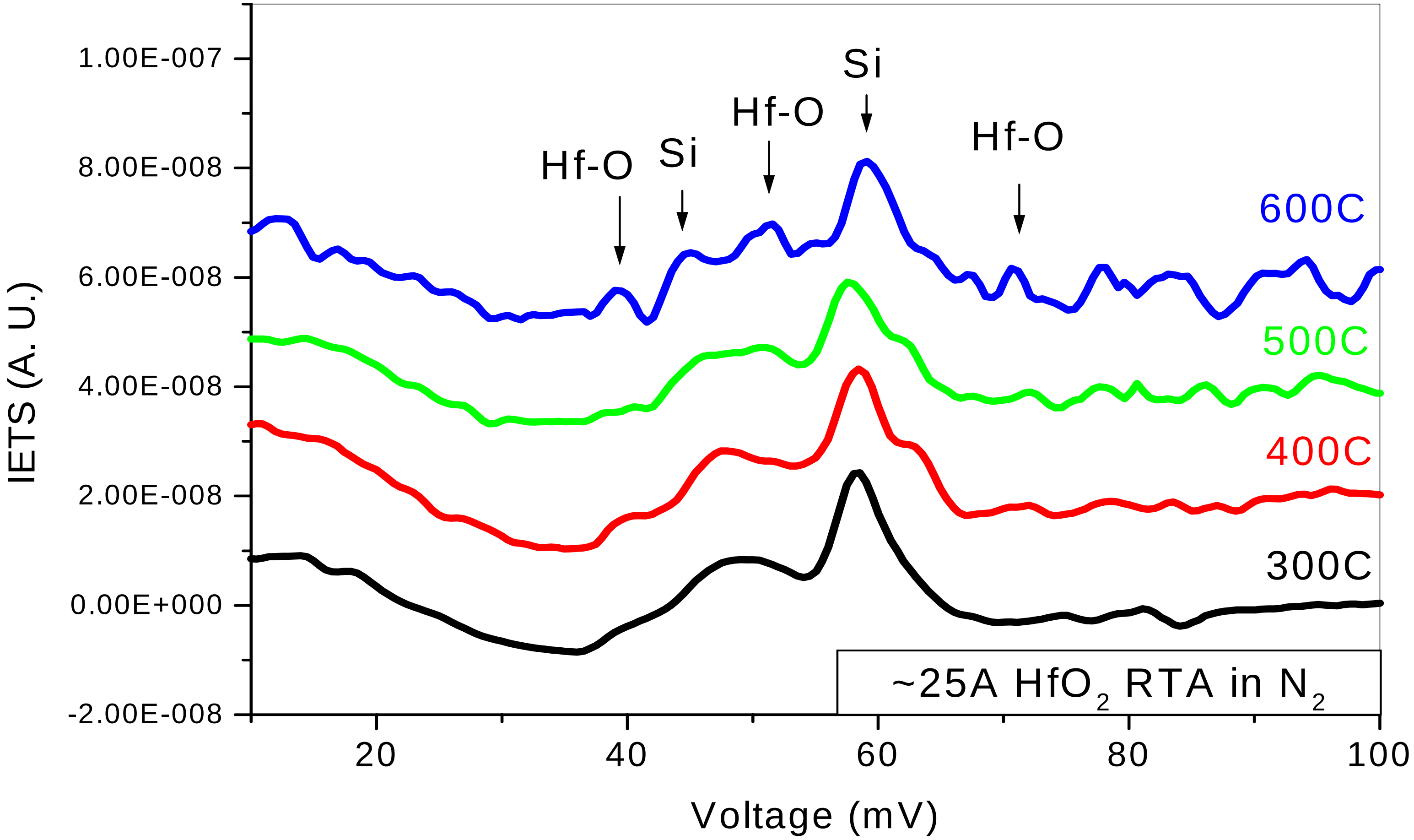


IETS sensitive to process variations for Al/HfO_2/Si structure (2)



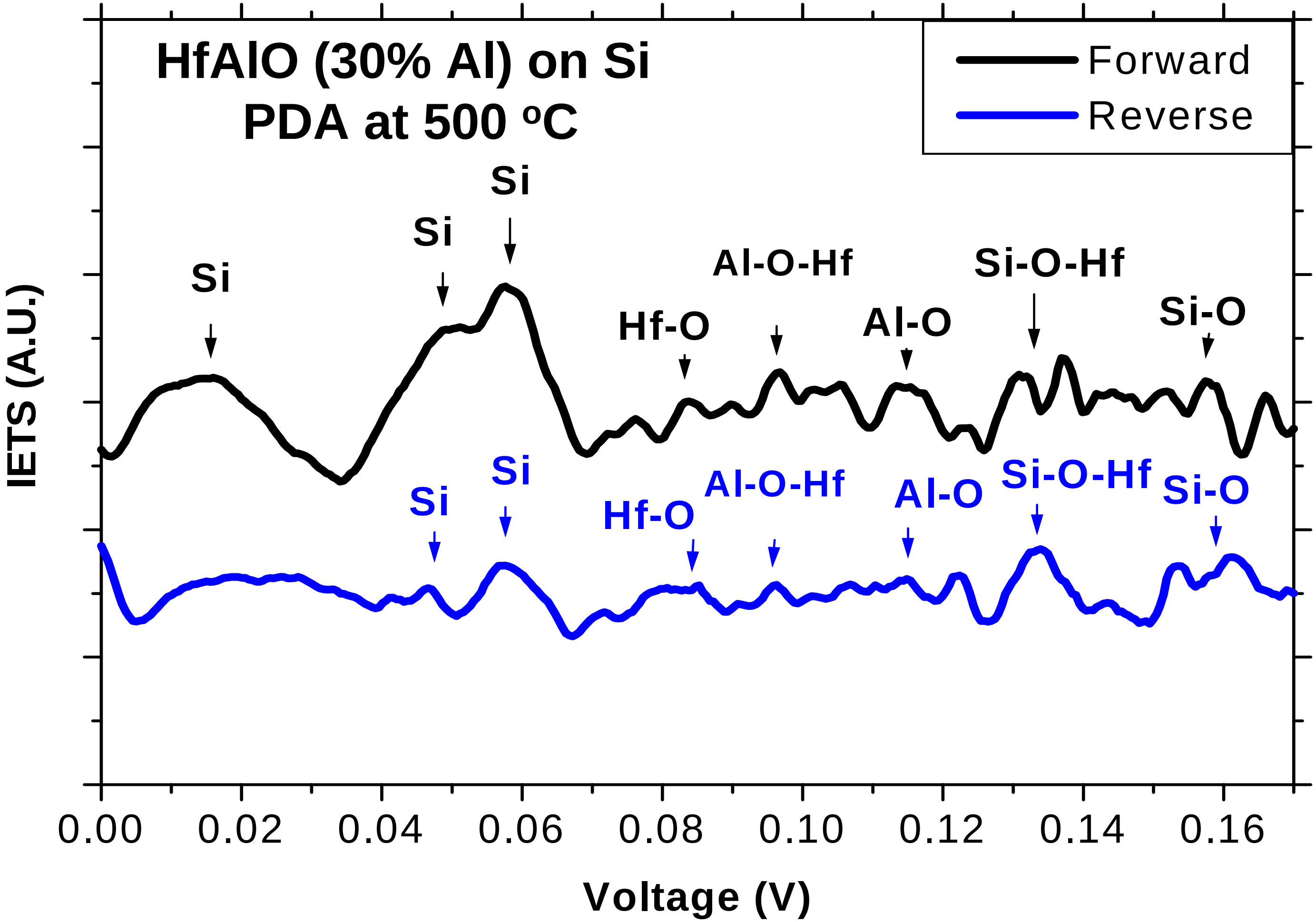
IETS sensitive to process variations for Al/HfO_2/Si structure (3)

- Hf-O peaks stronger with increasing PDA temperature
- Linked to more HfO_2 crystallization at higher temperatures.



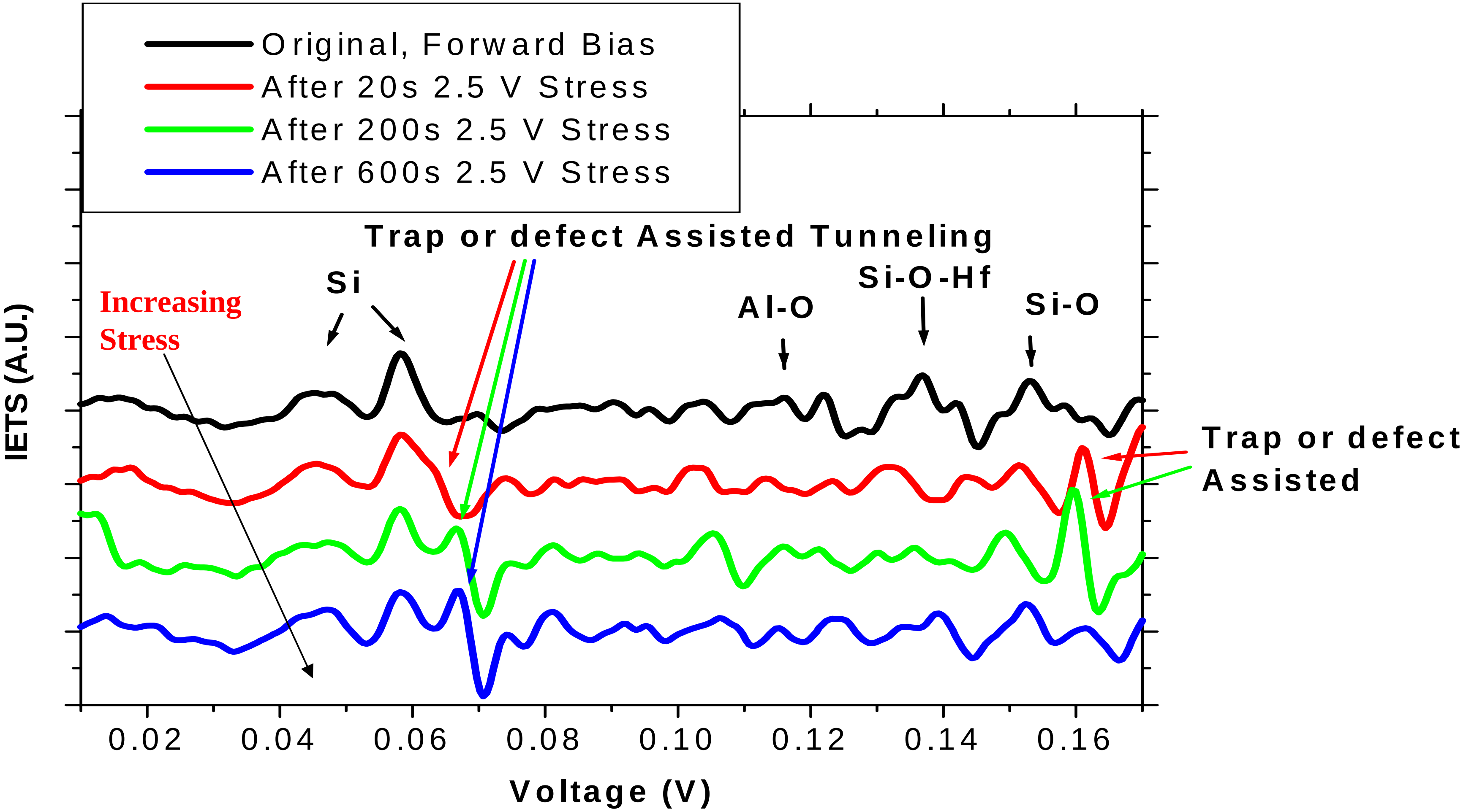
IETS of HfAlO on Si

- Al-O peak appears in both forward and reverse-bias spectra, suggesting that Al-O bonds exist throughout both interfaces
- Possible Al-O-Hf vibration is identified at 0.095V.

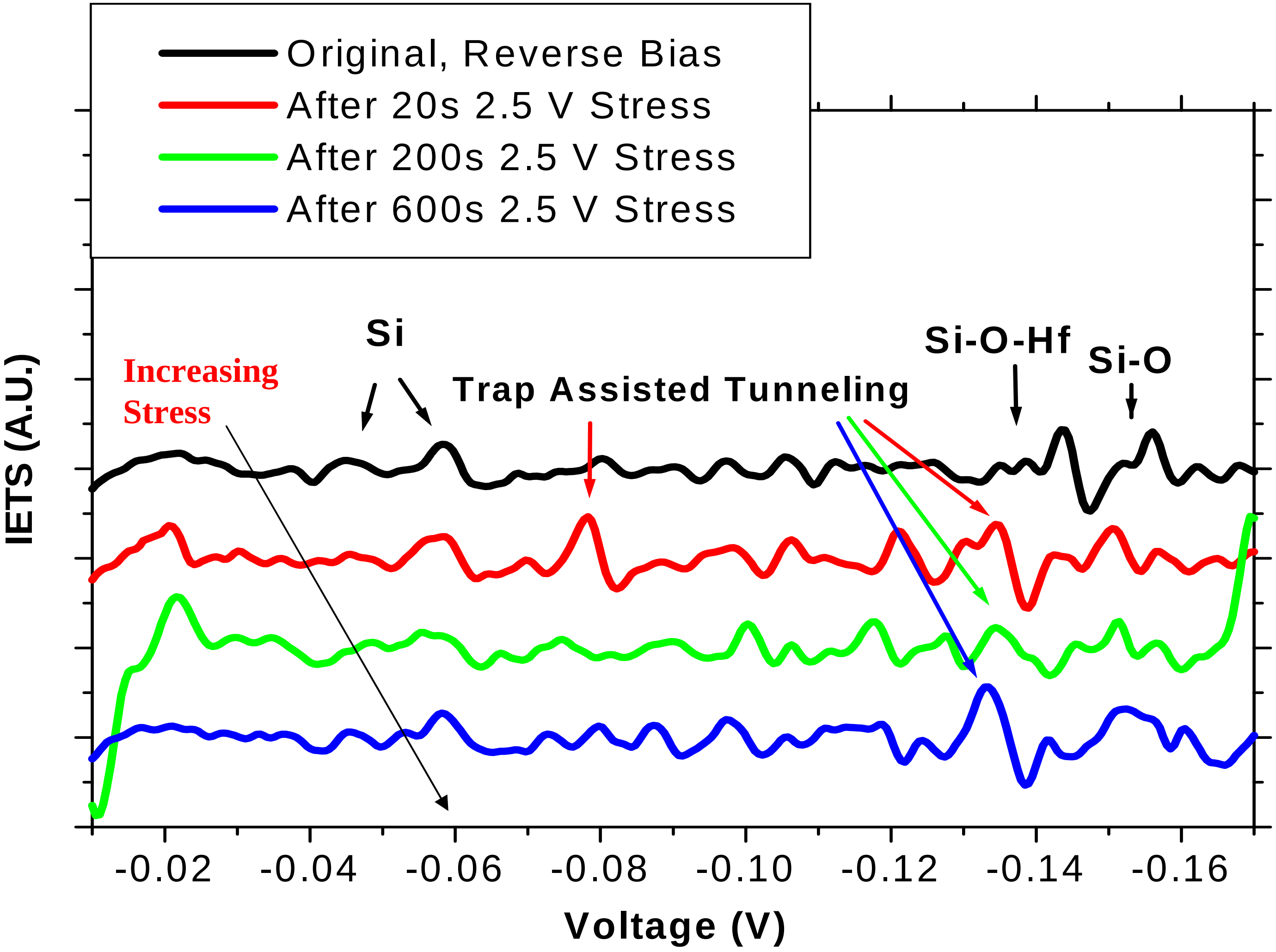


Voltage Stress Induced Effect

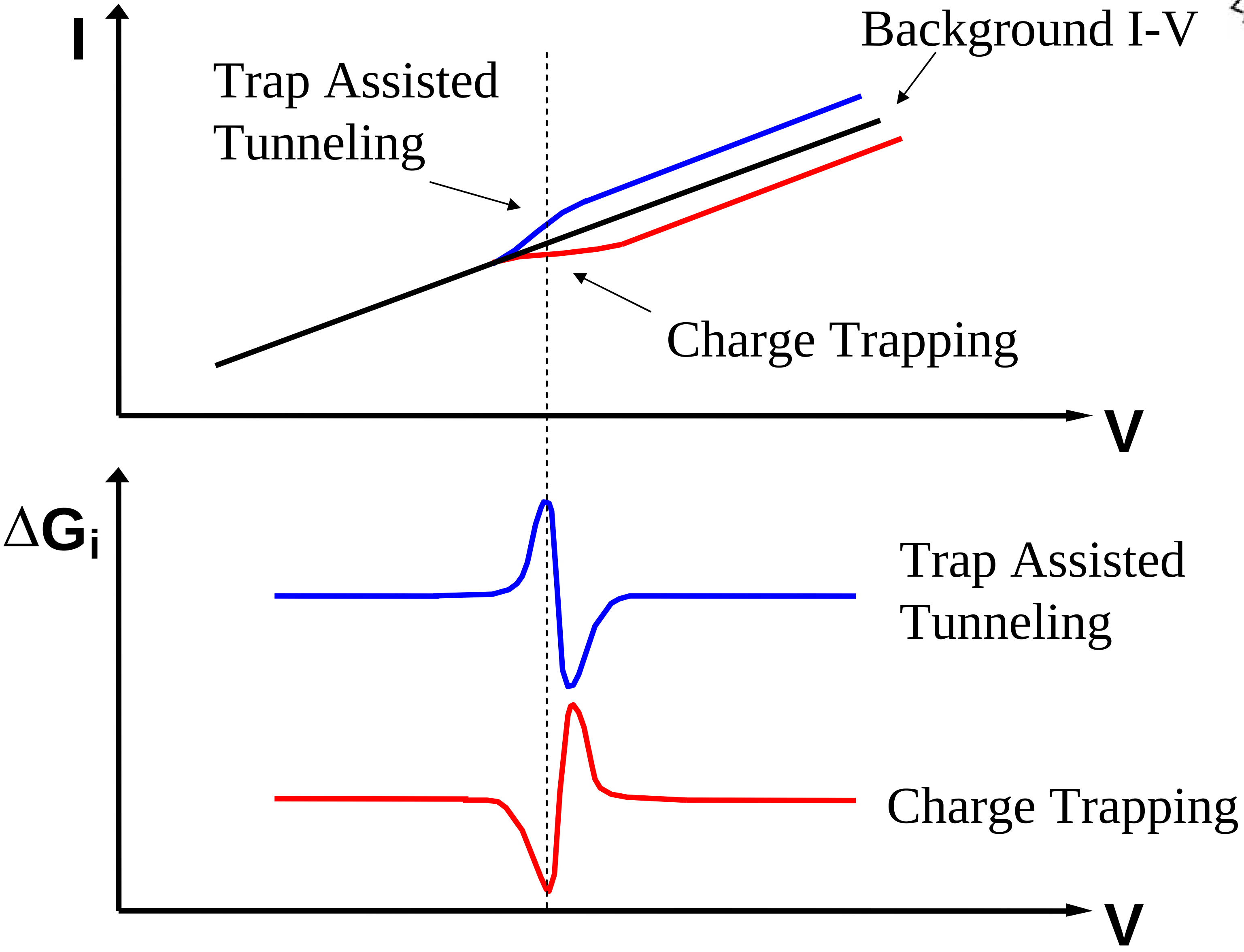
Features at 0.07V and 0.16V indicate trap assisted tunneling.



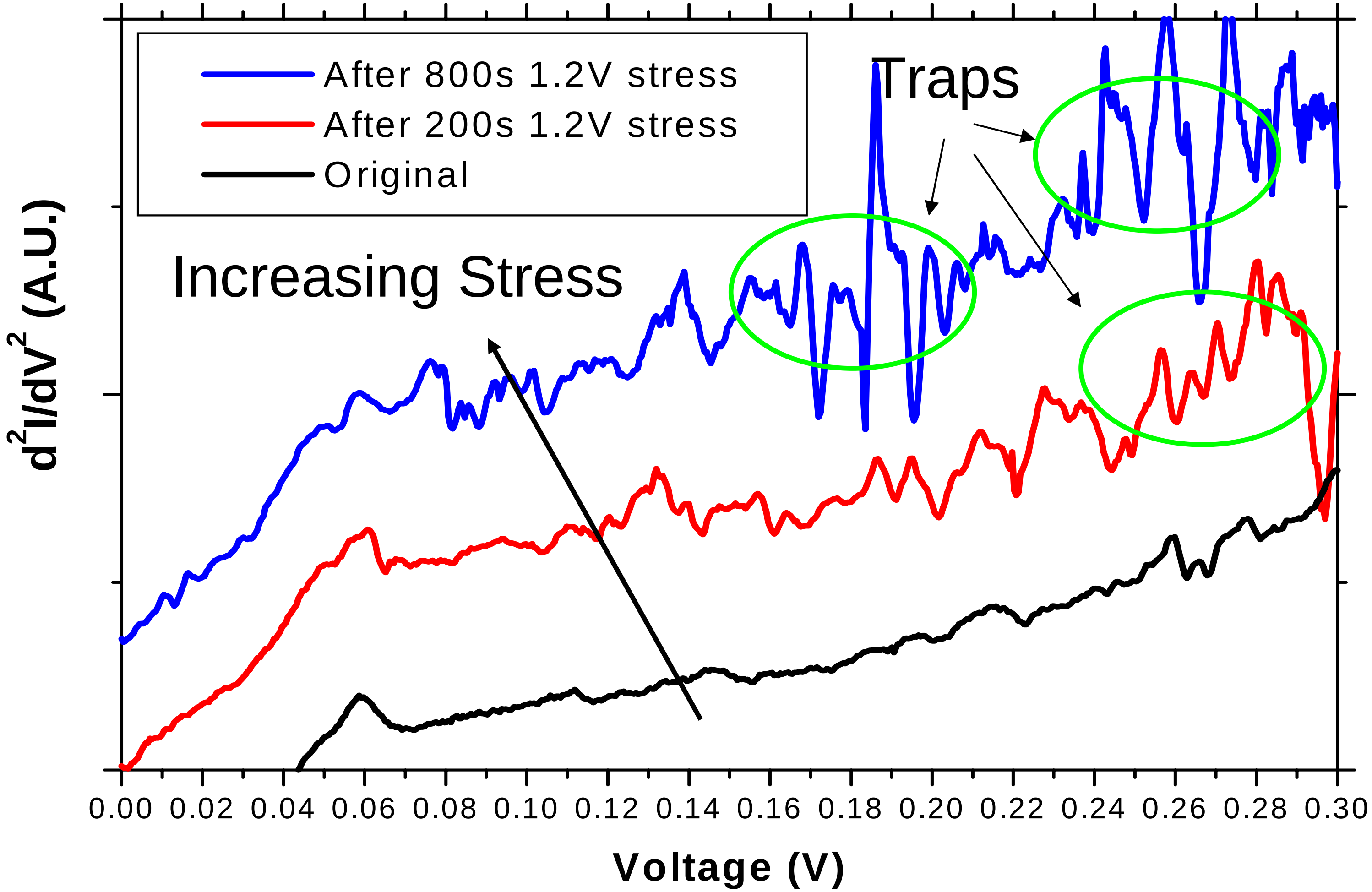
Voltage Stress Induced Effect (Reverse Bias)



Trap Related Effect from IETS

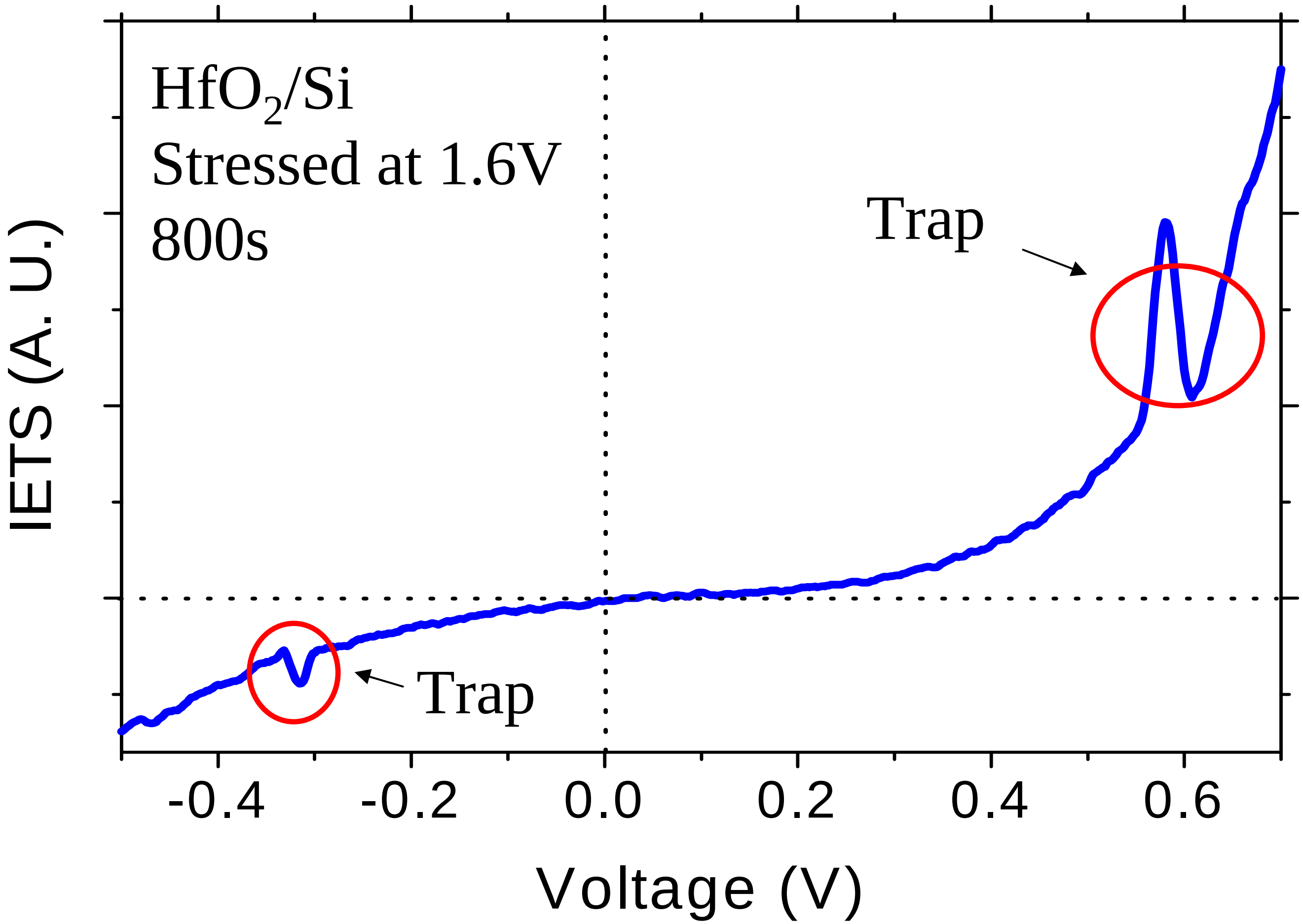


IETS Reveals Stress-Induced Traps



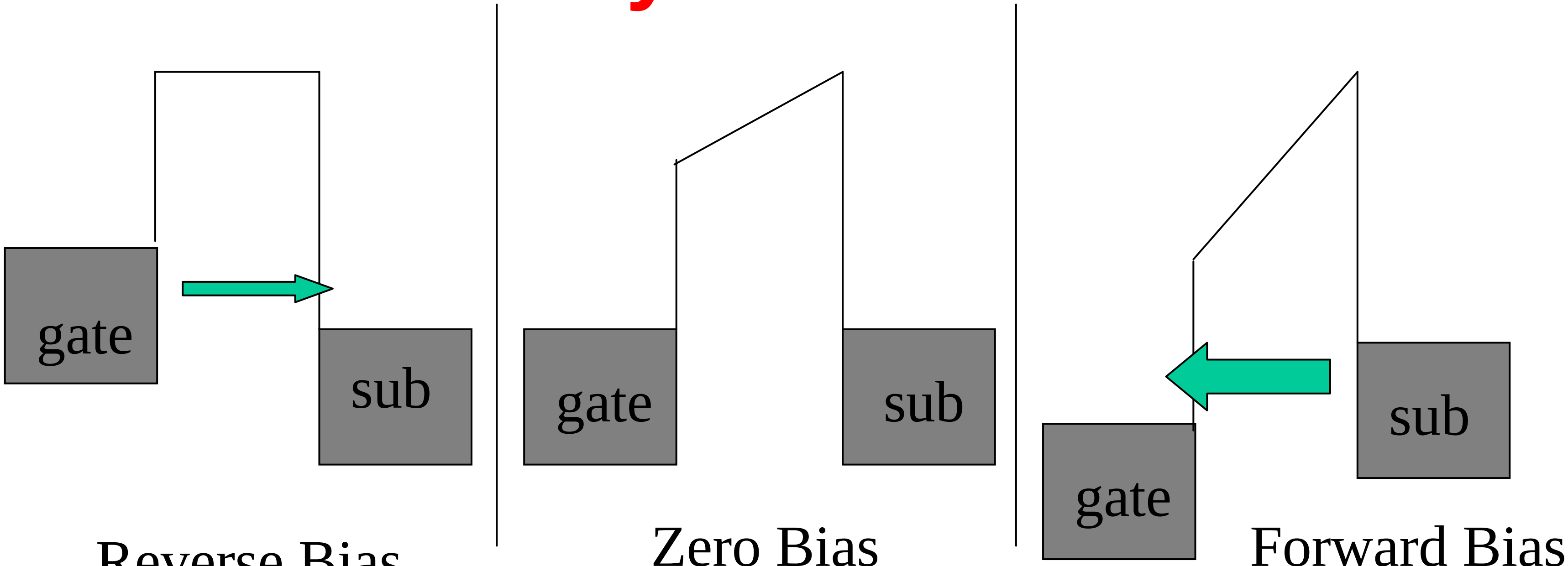
IETS has high sensitivity in detecting traps.

Strong Trap Assisted Tunneling Effect Revealed by IETS



Forward-bias trap features stronger than reverse-bias ones, due to asymmetry of the barrier.

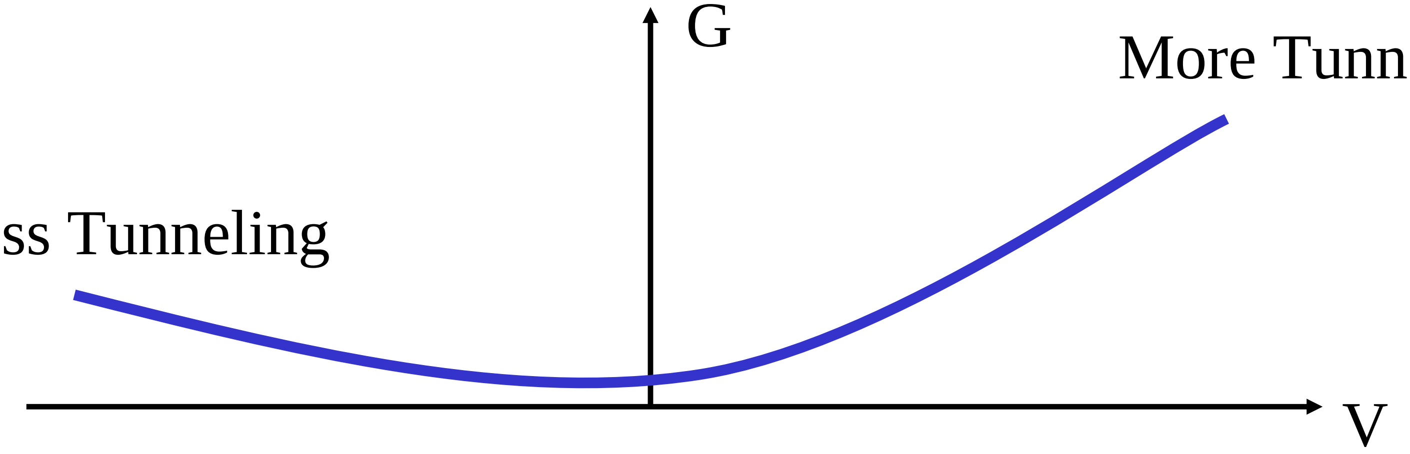
Polarity Dependence of Conductance Due to Asymmetric Barrier



Reverse Bias

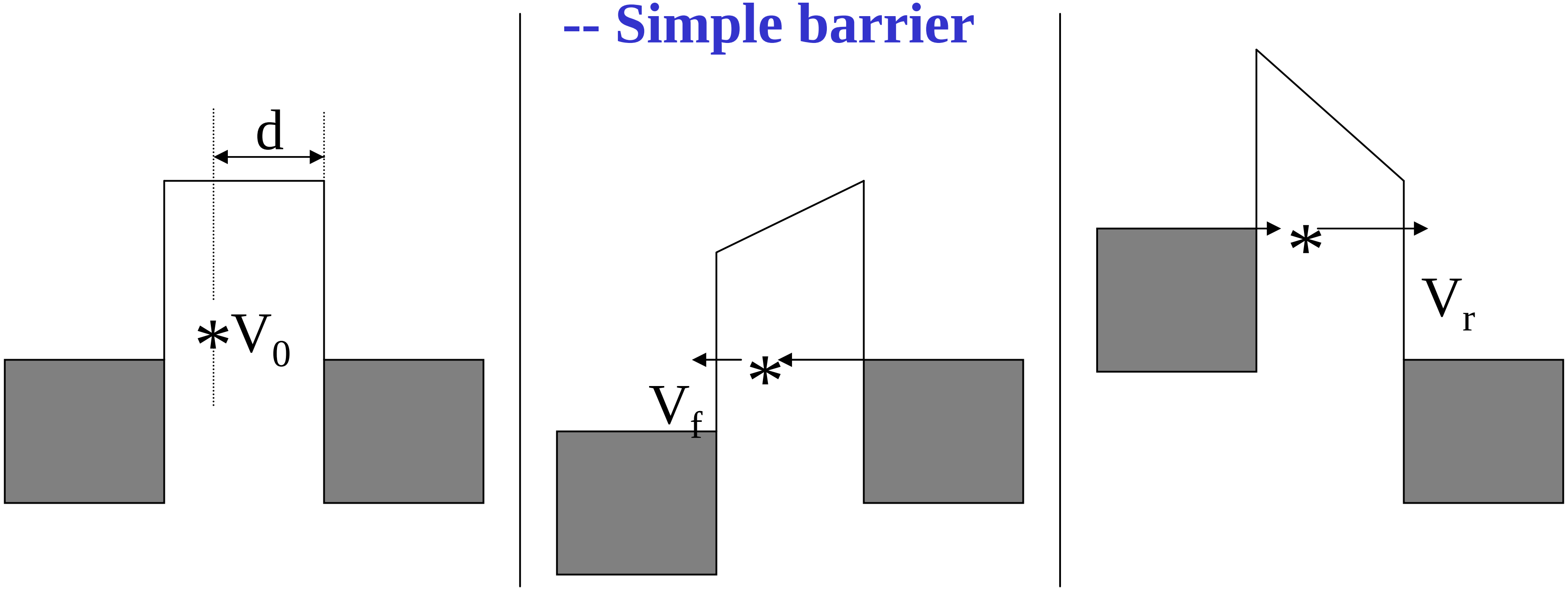
Zero Bias

Forward Bias



Determining Trap Energy and its Physical Location from forward and reverse data

-- Simple barrier



d is the physical location of the trap (assume total thickness is d_0).

eV_0 is the trap energy above the Fermi level (at zero bias).

V_f is the forward bias voltage required for the Fermi level to reach the trap.

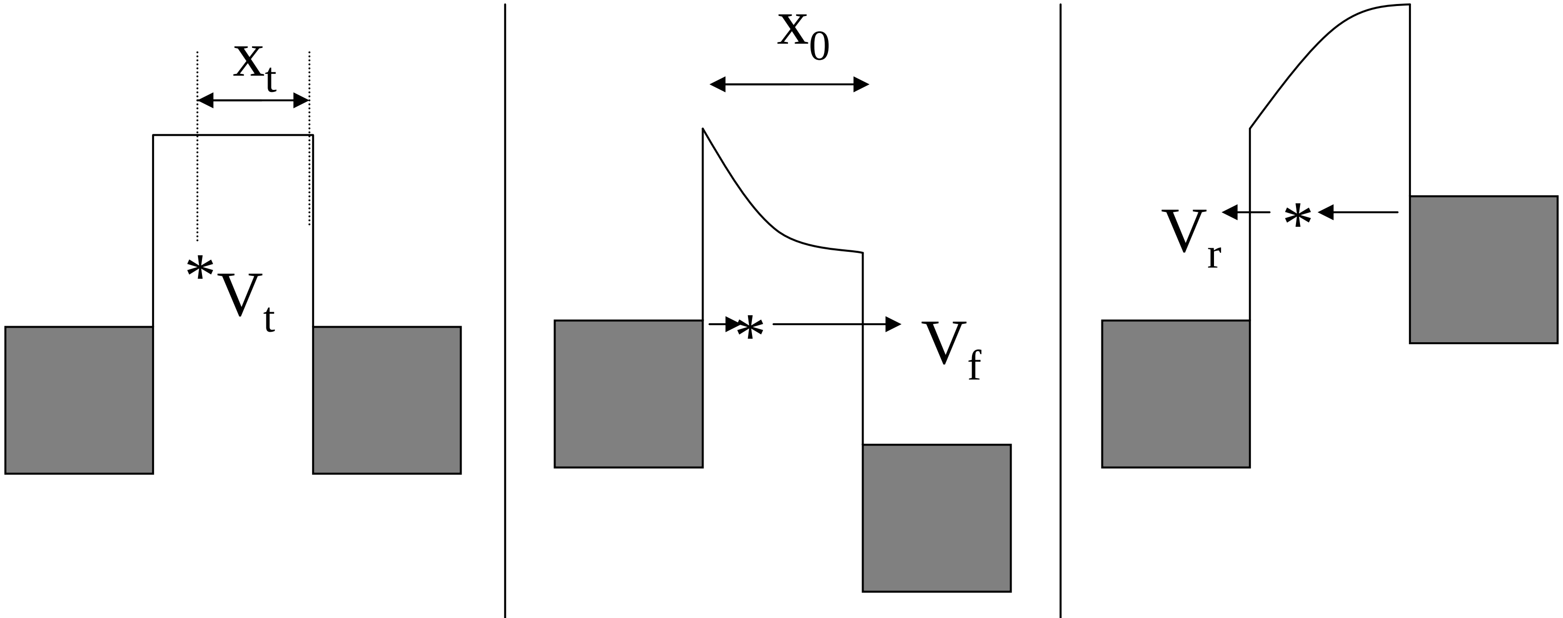
V_r is the reverse bias voltage required for the Fermi level to reach the trap.

Then,

$$\boxed{\begin{aligned} V_0 &= V_f V_r / (V_f+V_r) \\ d &= d_0 V_r / (V_f+V_r) \end{aligned}}$$

Determining Trap Energy and Location

-- Non-uniform dielectric constant



x_t: physical location of trap (with total physical thickness of x_0).

eV_t: trap energy above the Fermi level (at zero bias).

V_f : forward bias voltage required for Fermi level to reach trap energy.

V_r : reverse bias voltage required for Fermi level to reach trap energy.

Assume non-uniform dielectric constant: ε=ε(x). Then,

$$\boxed{\begin{aligned} V_t &= V_f V_r / (V_f + V_r) \\ d_t &= d_0 V_r / (V_f + V_r) \end{aligned}}$$

where $d_0 = \int_0^{x0} dx/\varepsilon(x)$, $d_t = \int_0^{xt} dx/\varepsilon(x)$

Determining Trap Energy and its Physical Location from Forward and Reverse data

Forward Bias: $$V_f - V_t = \int_0^{xt} dx\, D_f / \varepsilon(x) \qquad \text{——} \quad \text{(a)}$$

$$V_f = \int_0^{x_0} dx\, D_f / \varepsilon(x) \qquad \text{——} \quad \text{(b)}$$

Reverse Bias: $$V_t = \int_0^{xt} dx\, D_r / \varepsilon(x) \qquad \text{——} \quad \text{(c)}$$

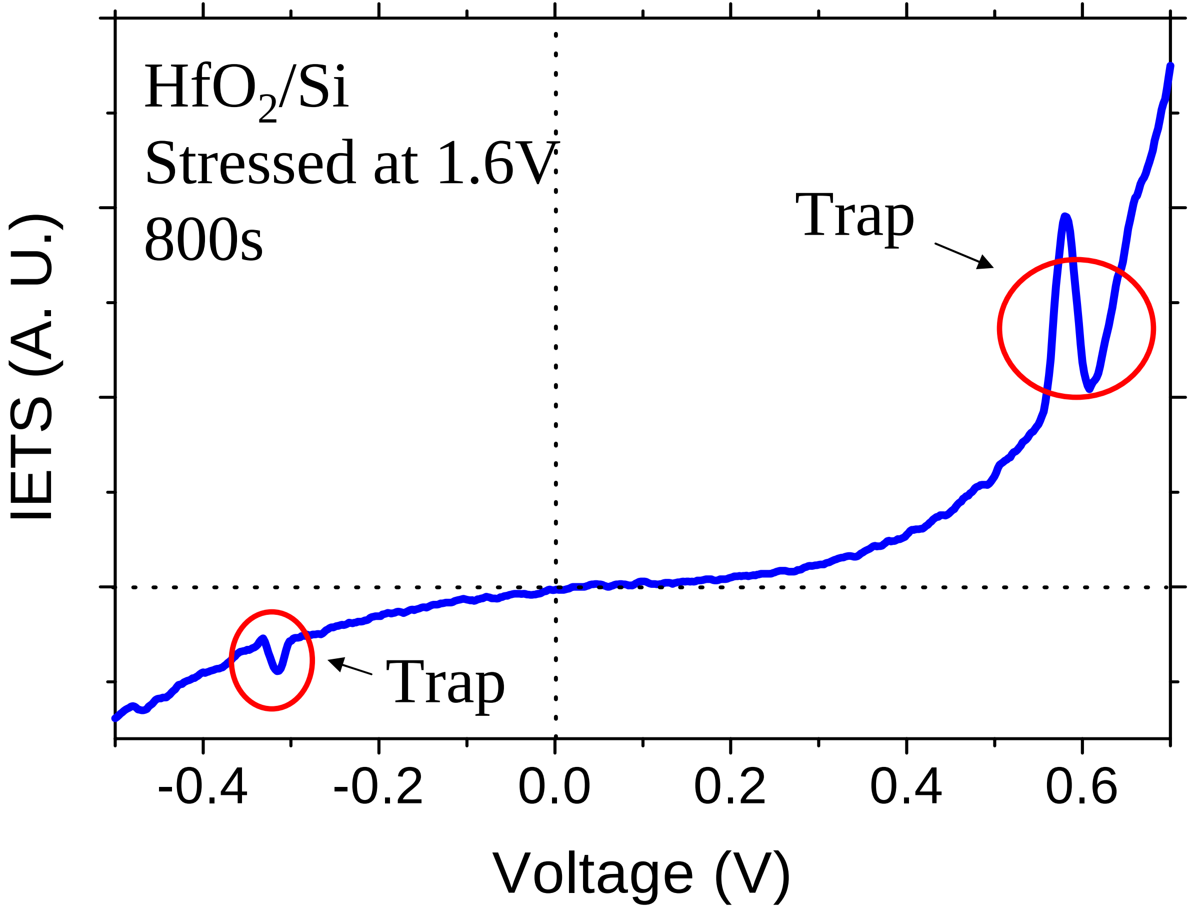
$$V_r = \int_0^{x_0} dx\, D_r / \varepsilon(x) \qquad \text{——} \quad \text{(d)}$$

From Eqs. (a)-(d), we get:

$$\boxed{\begin{aligned} V_t &= V_f V_r / (V_f + V_r) \\ d_t &= d_0 V_r / (V_f + V_r) \end{aligned}}$$

where $d_0 = \int_0^{x_0} dx/\varepsilon(x)$, $d_t = \int_0^{xt} dx/\varepsilon(x)$

Trap Energy and its Physical Location for a Particular Trap



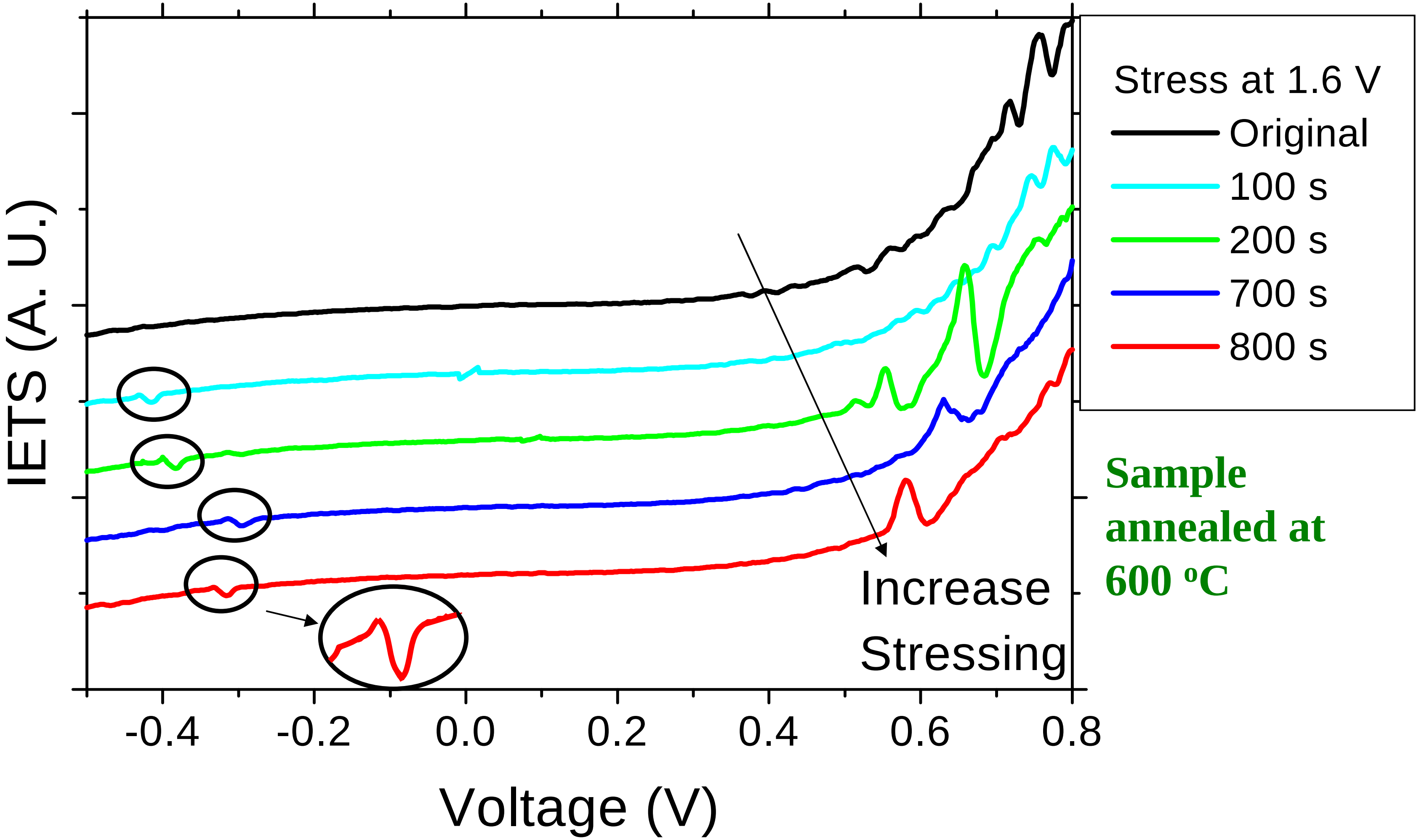
V_f = 0.58 V
V_b = 0.32 V

⬇

V_0 = 0.21 V
d = 0.36

The EOT of the dielectric is ~2.5 nm. ➡ The trap is located ~ 0.9 nm from the dielectric/Si interface

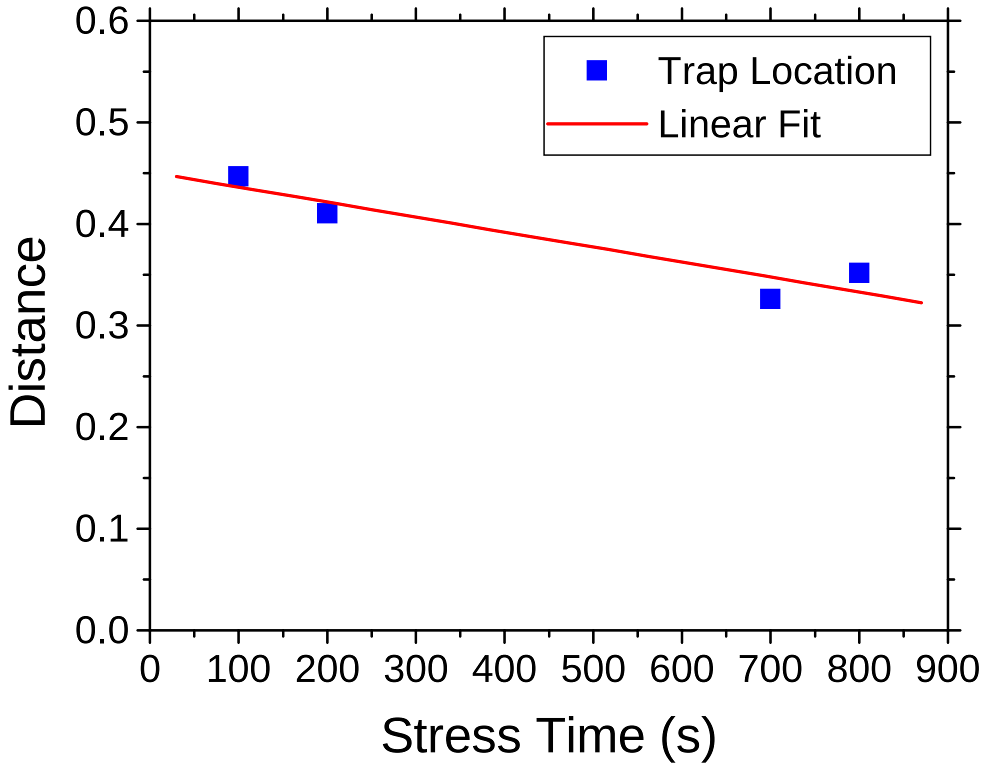
Evolution of Voltage Stress-Induced Traps in HfO_2/Si MOS Structure

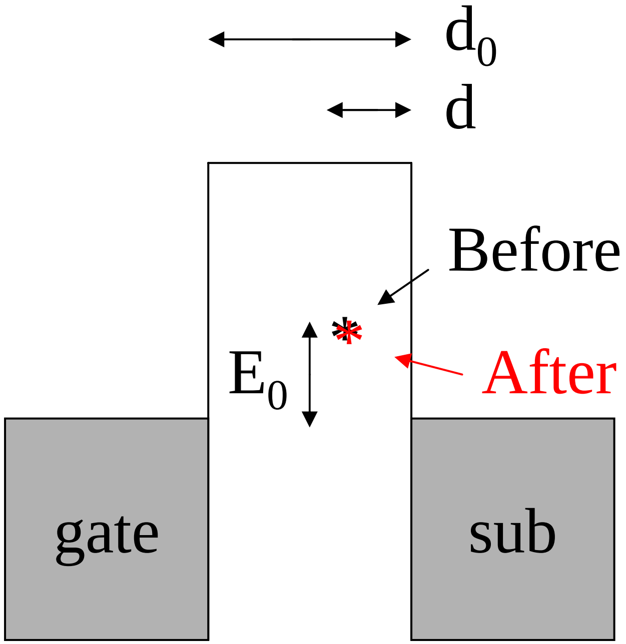


Sample annealed at 600 °C

- **Forward-bias and reverse-bias features arise from the same trap.**

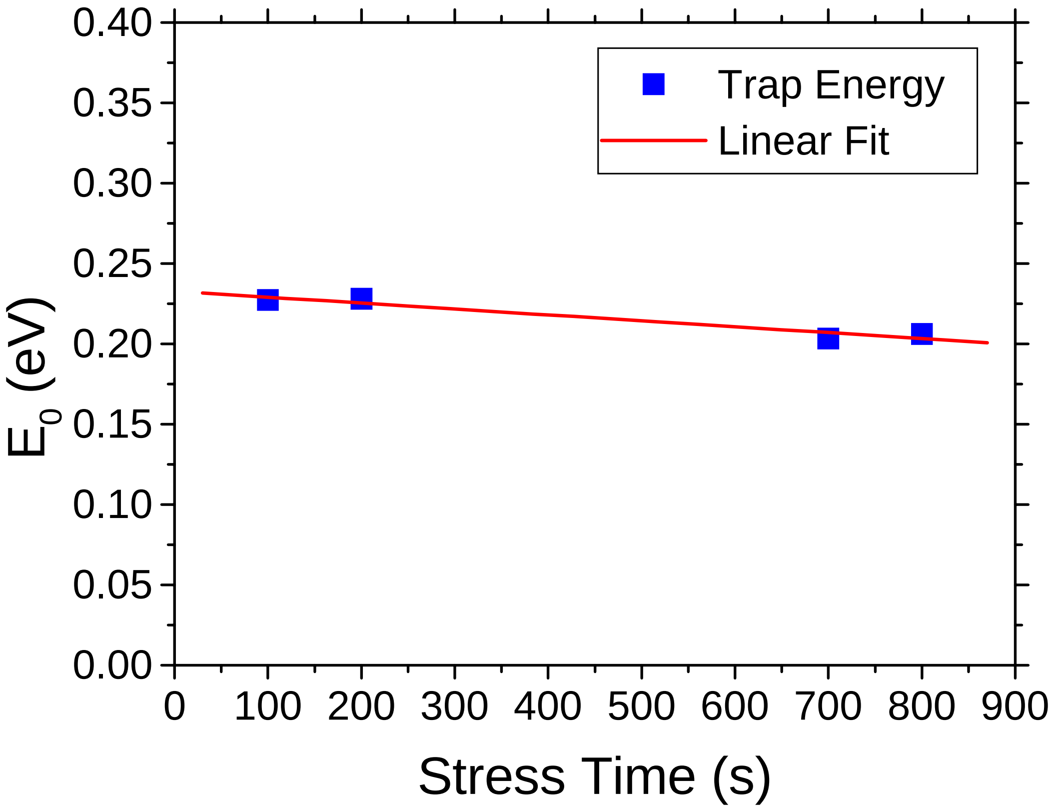
Trap Location as a Function of Stress Time

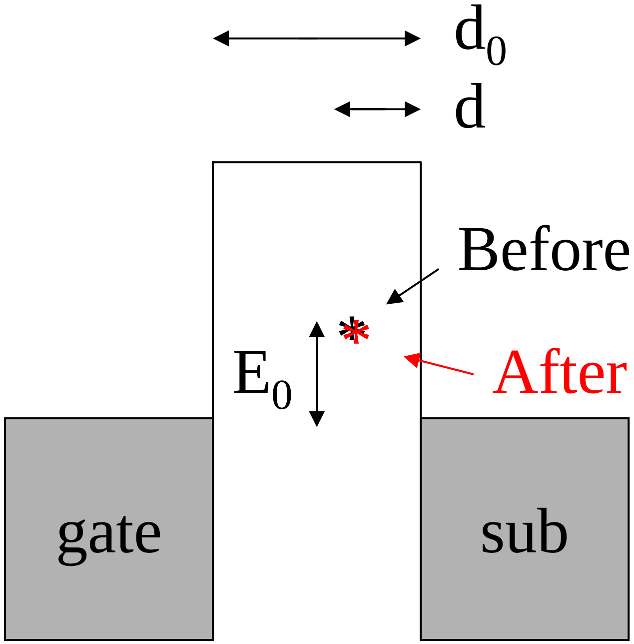




Trap seems to move closer to the substrate.

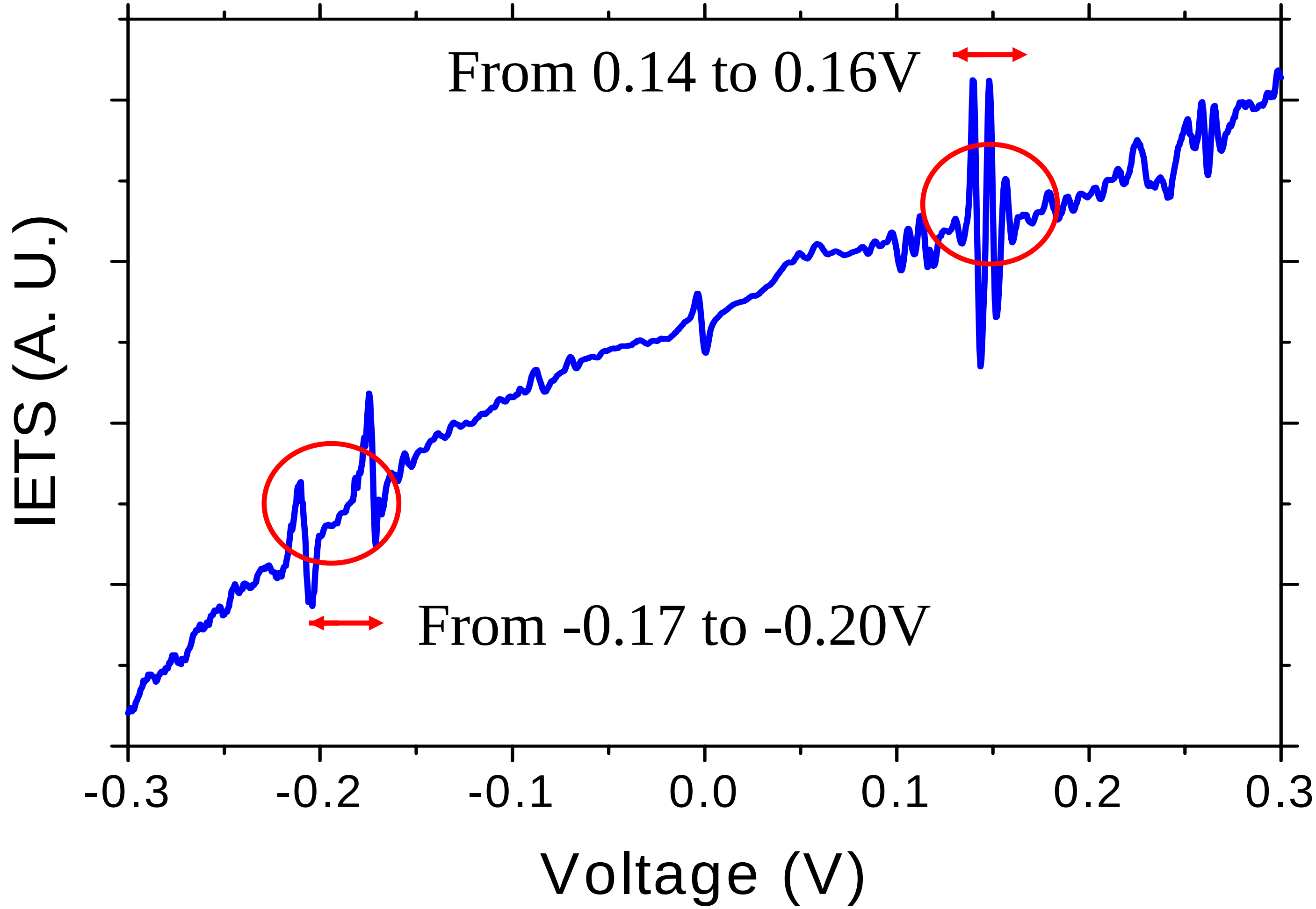
Trap Energy as a Function of Stress Time





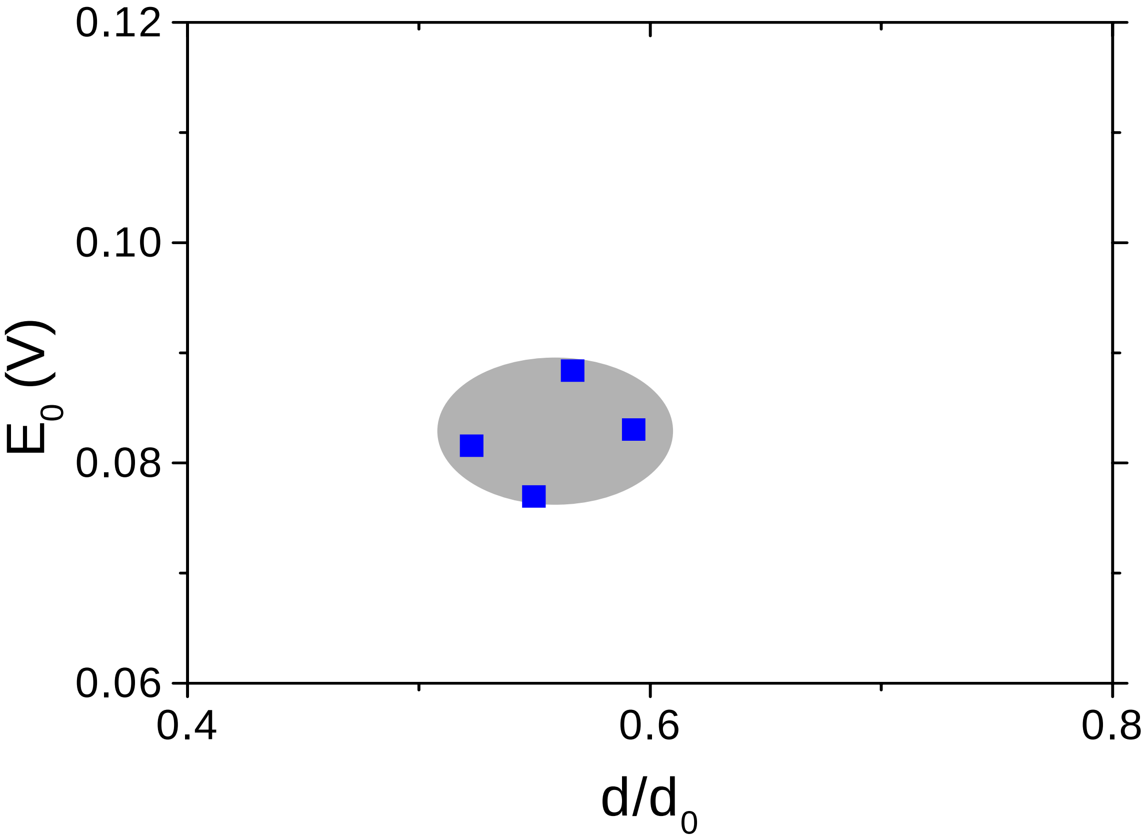
Trap seems to lower its energy very slightly

IETS Reveals Trap-related Feature of As-Deposited HfO_2/Si MOS



Two Prominent Traps are Revealed

Possible Trap Energies and Physical Locations in Previous Sample



- Trap energies estimated to be in the range 75 - 85 meV.
- Trap locations estimated to be 1.2 to 1.5 nm away from interface.

Summary

- **IETS reveals phonons, bonding vibrations, and defects in ultra-thin SiO_2/Si, HfO_2/Si and HfAlO/Si**
- **Soft phonons in HfO_2 have energies very close to Si phonons, which may scatter off channel carriers and cause mobility degradation.**
- **IETS reveals trap features in HfO_2/Si MOS structure.**
- **Trap energy and its physical location can be determined from the voltage locations of forward and reverse-biased IETS spectrum.**