The Nanotechnology Xccelerator

Project Descriptions in brief

For more information contact NanotechnologyXccelerator@nist.gov

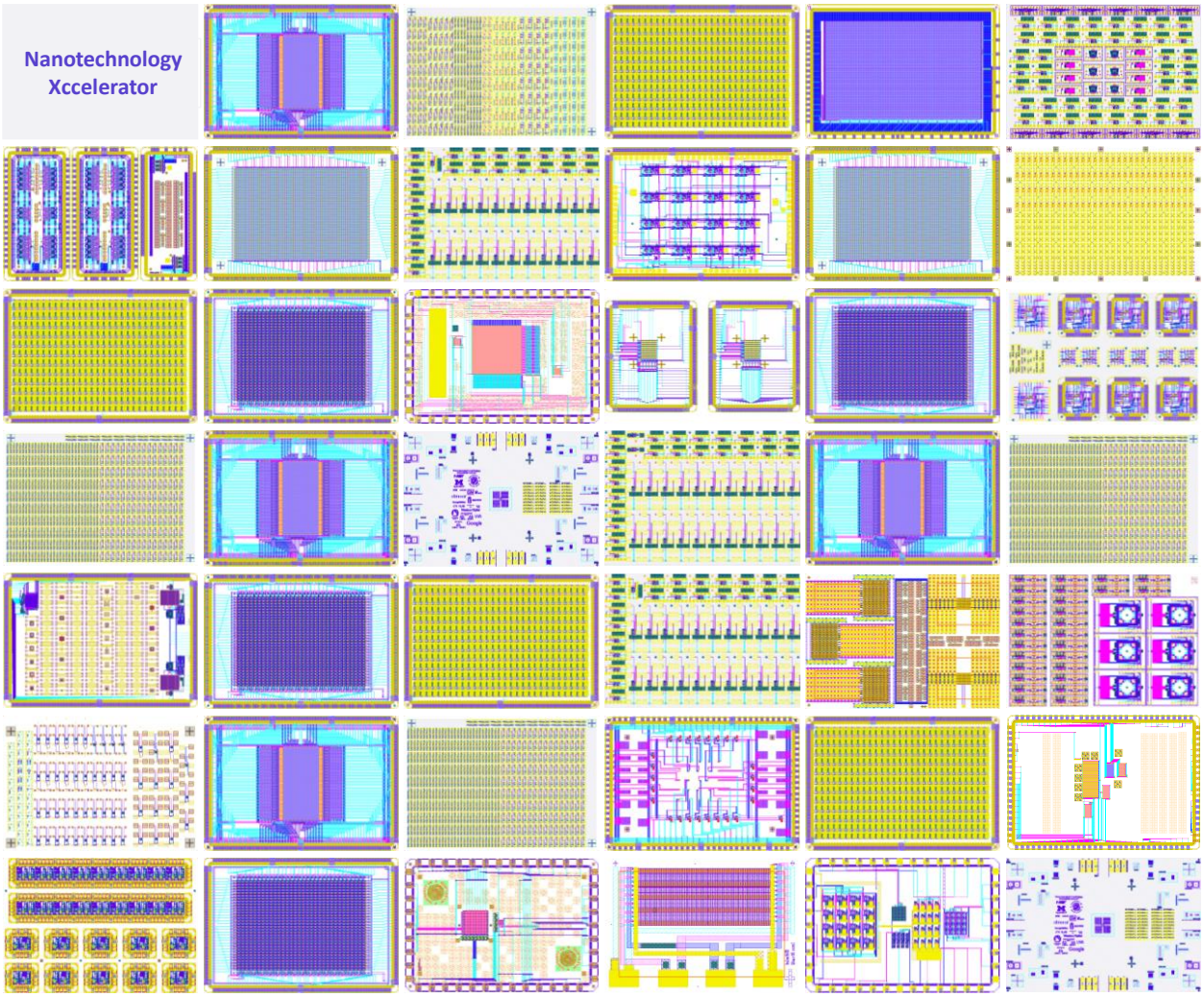

Figure 1 Overview of the entire 7 by 6 reticle composed of 30 unique tiles with several duplicates.

List of Tiles (excluding variants):

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1 Tile Title: Alignment Mark Tile

Team: George Washington University + NIST

PI(s): Gina Adam

Contact: ginaadam@gwu.edu

Description: This tile contains a diversity of alignment marks to achieve compatibility with diverse nanofabrication facilities. Marks include ASML PAS500 marks, GCA AutoStep 200, Canon FPA-2000, Nikon, MLA150, as well as contact alignment. Additional test structures are present to ensure basic connectivity of contacts, such as known resistor values and isolated transistors. The tile is split into quadrature so that dicing a wafer through the tile would place marks in all four corners of a coupon.

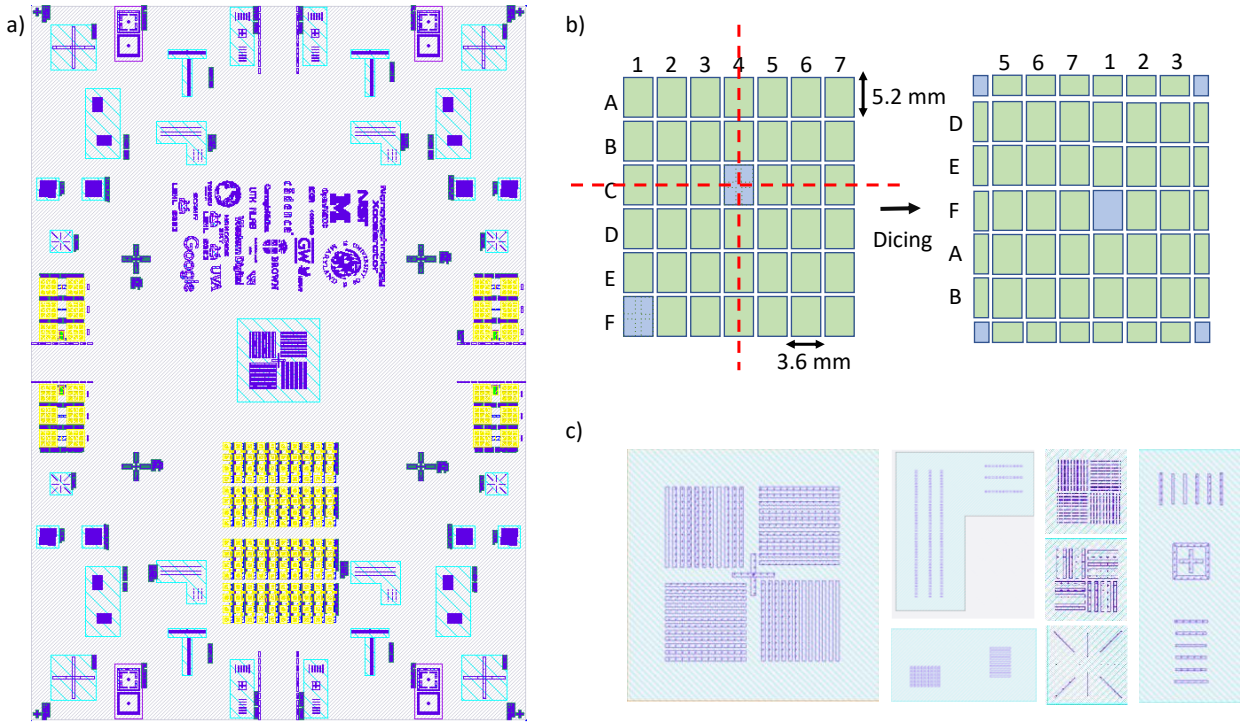

Figure 2 a) tile overview - note the duplicate of alignment marks in quadrature. b) Recommended dicing strategy for repeated reticle areas across a wafer to center a preferred target die for contact lithography. c) selection of alignment marks on the tile

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2 Tile Title: High Frequency TIA

Team: Austrian Institute of High Energy Physics

PI(s): Simon Waid

Contact: simon.waid@oeaw.ac.at

Description: This tile contains an array of 1GHz bandwidth differential transimpedance amplifiers designed to be directly integrated with nanoelectronic devices for high-speed detector applications. The integration feature size is 10 microns. The amplifier output drives a 50-ohm output load and can be used for both AC and DC measurements.

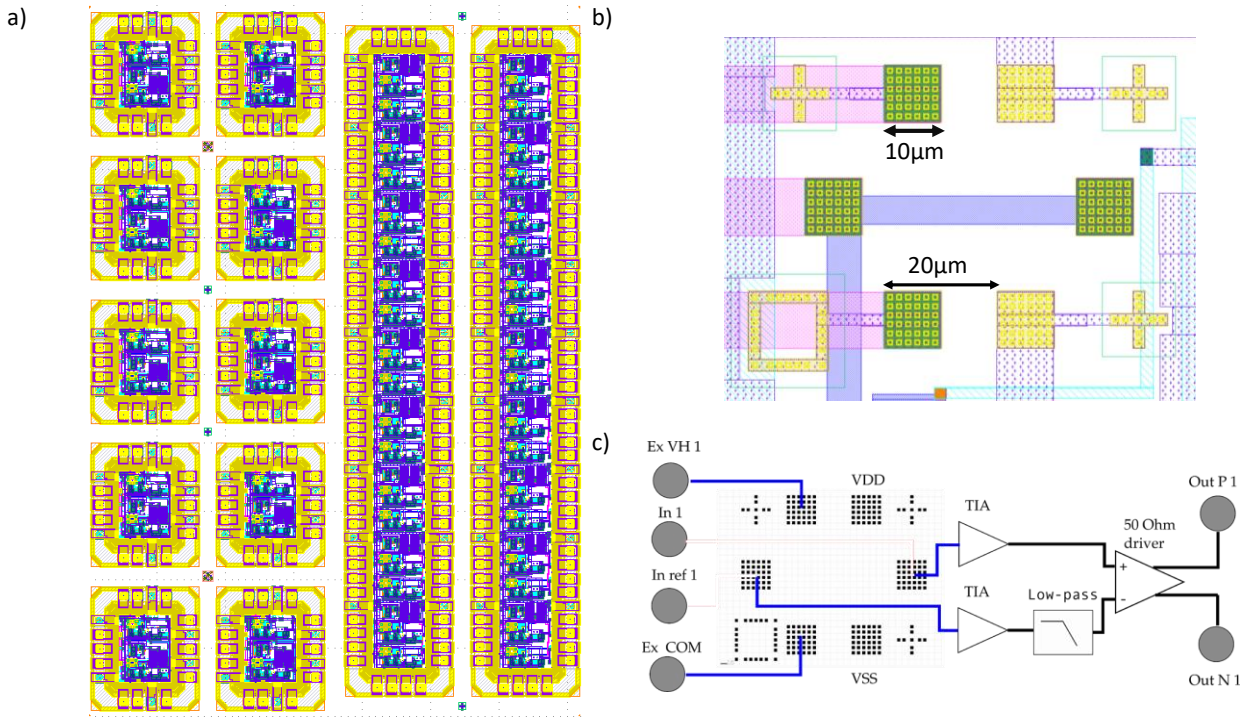

Figure 3 a) over view of the tile with multiple amplifier chips, b) select view of the nanofabrication region where devices can be added c) high level circuit description of the high frequency amplifier integrated with nanodevices.

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3 Tile Title: Cryogenic Test Vehicle Tile for Magnetic Sensors and Other Quantum Sensors

Team: Brown University

PI(s): Alex Zaslavsky and William Patterson

Contact: alex_zaslavsky@brown.edu and william_patterson_iii@brown.edu

Description: These circuits are aimed at cryogenic operation with low power consumption and low bandwidth and consist of the following:

1) A parametrized set of current mirrors intended to provide DC-biasing to pairs of adjacent nano-devices, with currents ranging from 0.5 to 350 uA. Each mirror has a fabrication area for its two nanodevices with preplaced contact vias.

2) A few of the same sensor pair sites with the lowest value current mirrors are combined with varactors in parallel with the sensors for voltage noise filtering. The intent is to limit the noise bandwidth of a nanodevice sensor operating at a few kilohertz.

3) A similar three-varactor test structure with 14 pF varactors, potentially useful for setting the frequency of a voltage-controlled oscillator as might be done in a PLL.

4) Two types of two-stage compensated operational amplifiers with RC feedback. The first stage has very low input capacitance for circuits requiring very light loading from nanodevices. There is a fabrication area for sensors or other post-processed devices with each amplifier. Some amplifiers have e-beam alignment marks for experimental device circuit fabrication with high resolution.

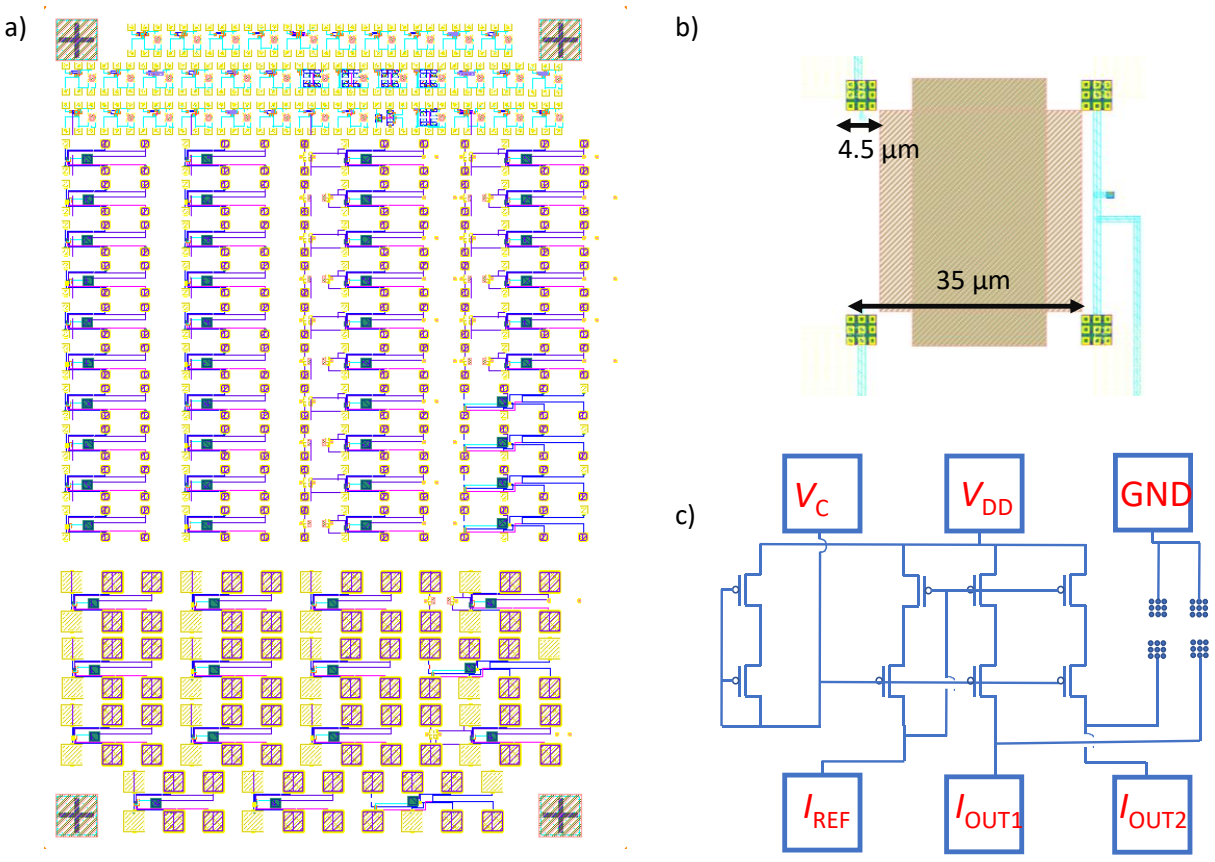

Figure 4 a) Overview of the tile with individual test points. b) close up of a selected nanofabrication region with exposed vias d) high level view of one of the cascoded current mirrors on the tile which can be used to bias a nanodevice.

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4 Tile Title: Test Tile for RF characterization of Nanodevices and measurement of Ferromagnetic Resonance of Nanodevices

Team: Carnegie Mellon University

PI(s): Rick Carley

Contact: lrc@andrew.cmu.edu

Description: This tile contains 3 elements geared toward the RF characterization of nanoelectronic devices including:

1) An array of inductors that can be used to a) characterize the Sky130 CMOs inductors and b) measure the magnetic permeability of lithographically patterned magnetic thin films.

2) An array of individual transistors which can be patterned with waveguides for high frequency measurements of nanoelectronic devices in series with a Sky130 transistor

3) A test on-chip Ferromagnetic Resonance test vehicle which can be used to measure the ferromagnetic response (from 1 to 10 GHz) of a magnetic thin film, 2D material, or spintronic devices.

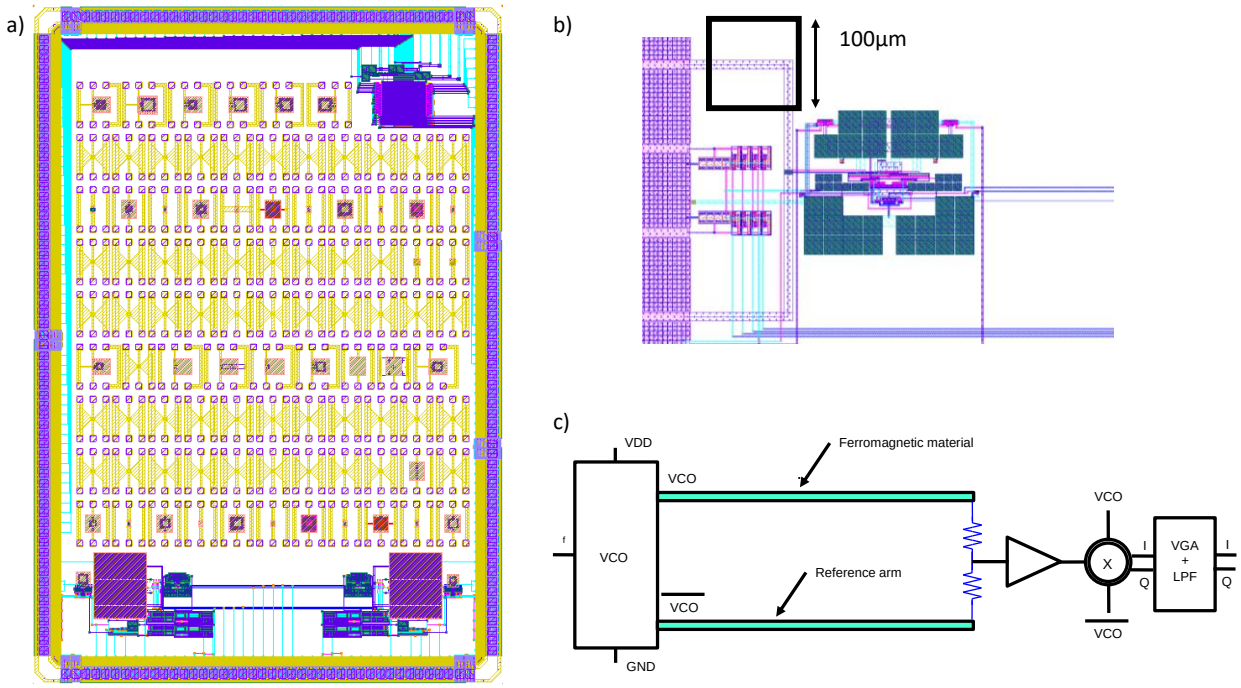

Figure 5 a) high level view of the tile b) close up of the region where a ferromagnetic film could be locally patterned. c) high level view of the circuit for doing on chip ferromagnetic resonance by observing the mismatch in impedance.

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5 Tile Title: Analog Gate Array Educational Tile

Team: Carnegie Mellon University

PI(s): Rick Carley

Contact: lrc@andrew.cmu.edu

Description: This tile is geared towards providing university students with a novel capability to tapeout an analog circuit design in less than 1 week. It can also be used as a first pass prototype of any novel

computing primitive with emerging technology. The chip consists of approximately 6000 transistors (along with resistors and capacitors) which can be electrically connected in any topology using a single metal layer. The novel routing is aided by special routing ties distributed through the chip. The feature size (2 microns) is designed to be compatible with modern high speed laser writers commonly found in university nanofabs.

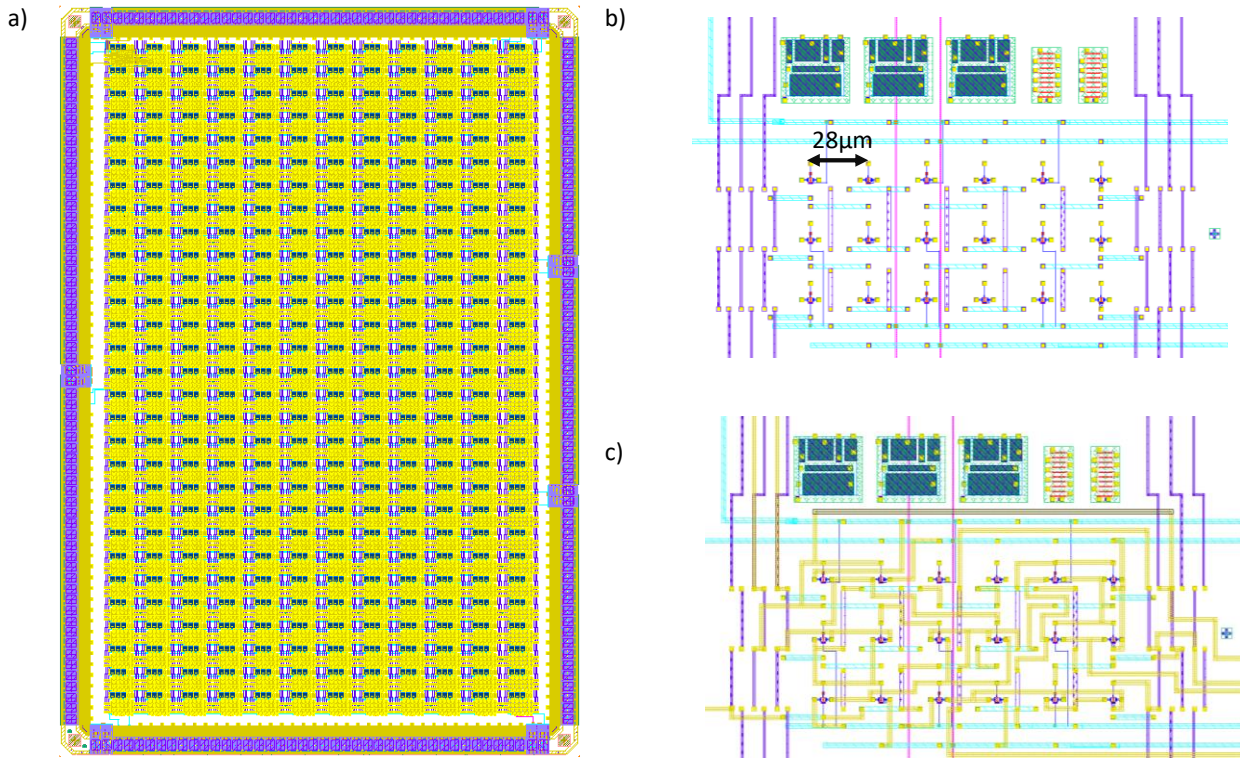

Figure 6 high level view of the tile which features 348 unit cells. b) local unit cell features transistors, capacitors, and resistors, c) example Miller amplifier created by a single lithography step.

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6 Tile Title: MEM-ID: A Reference Resistance Comparator Test Vehicle for Memory Devices

Team: George Washington University

PI(s): Gina Adam

Contact: ginaadam@gwu.edu

Description: The MEM-ID tile proposes several design variants of a leaf chip for a spatially distributed decision tree architecture. The design variants include some chips with padframe with ESD protection and some without, as well as sub-blocks for testing. Each chip processes an input by comparing it to a predefined boundary stored in up to three add-on two-terminal non-volatile multi-bit memory devices, which can be added by fabrication in an academic cleanroom. The add-on device can vary in terms of material stack, design and performance, depending on the research carried out by the scientific group utilizing the chip for monolithic integration. This approach facilitates the investigation of device-system

co-design. It also supports the prototyping with known good dies, overcoming the non-idealities challenge prevalent in emerging device technologies.

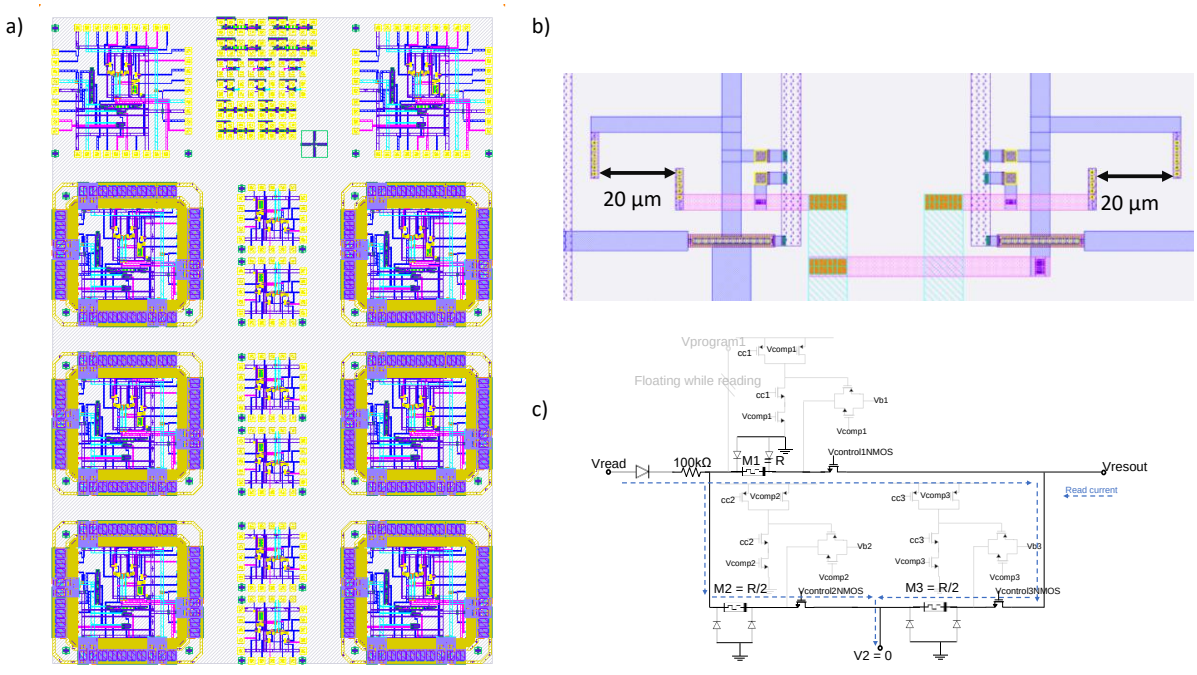

Figure 7 a) High level view of the tile which features multiple computing chiplets. b) Close up of the nanofabrication region to build a 2-terminal memory device. c) high level view of the local circuit which uses the memory device to send a signal.

7 Tile Title: Transistor Tile

Team: George Washington University

PI(s): Gina Adam

Contact: ginaadam@gwu.edu

Description: The transistor tile contains arrays of NMOS transistors in various sizes designed for both contact and e-beam lithography. These structures are ideal for 1T-1R measurements of integrated memory devices. The structures are designed for high density parametric measurements.

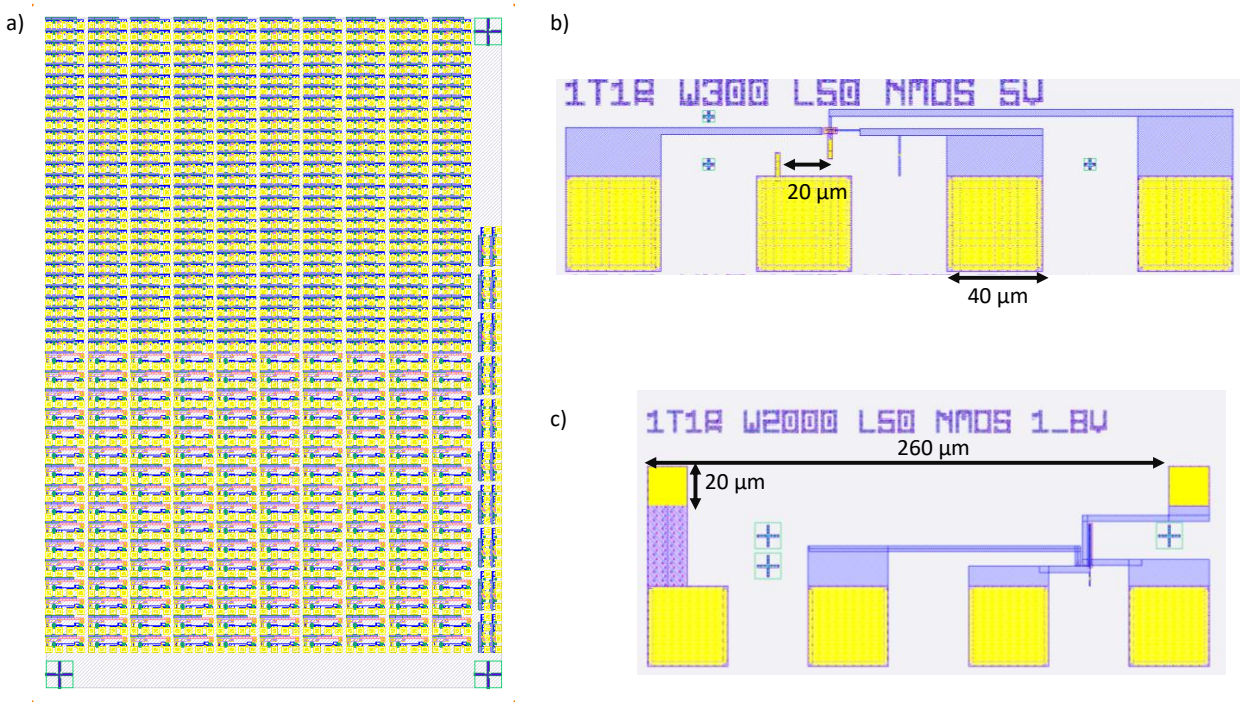

Figure 8 a) A high level view of the tile which contains many test sites, b) close up view of a transistor designed to be attached to a device with ebeam lithography, c) an additional transistor designed to be easily used with contact lithography.

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8 Tile Title: Nanotech Accelerator (NTA) Tile

Team: George Washington University

PI(s): Gina Adam

Contact: ginaadam@gwu.edu

Description: The NTA tile is similar to the transistor tile but includes additional structures including PMOS transistors, 2T-1R transistor configurations with both P- and NMOS devices, as well as passgate configurations consistent with the 3-Terminal array devices from the UVA team. Like the other tile, it has structures designed for both contact and e-beam lithography.

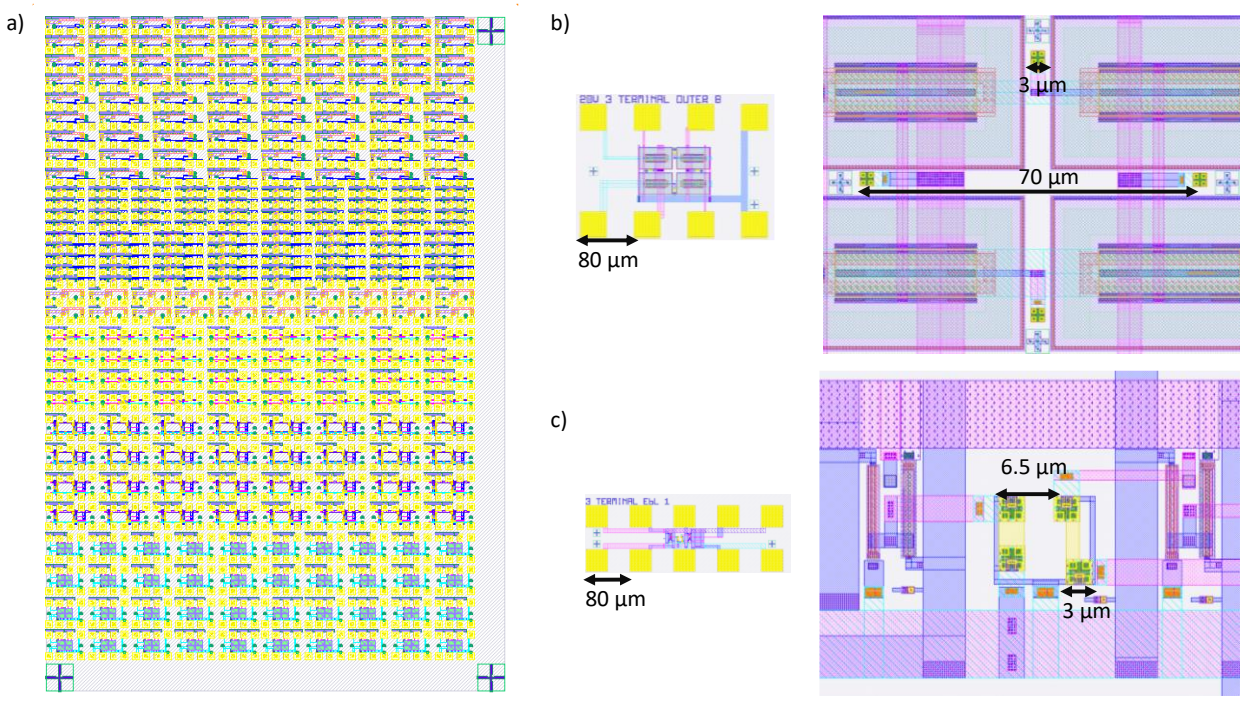

Figure 9 a) high level view of the tile, b) a close up of a high voltage transistor pass gate test structure, c) close up of a 5V transistor pass gate test structure.

9 Tile Title: Endurance Test Vehicle for Memory Devices

Team: University of Michigan

PI(s): Mehdi Saligane

Contact: mehdi@umich.edu

Description: The endurance test vehicle is designed to measure a 10x10 array of 2-terminal nanodevices. It is designed for devices with a 10-micron feature size. The system allows devices to be read through either external voltages or through the use of an on-chip programmable sense amplifier. Using external triggers provided by an FPGA, the chip can run through alternating set and reset pulses at 100s of Megahertz to allow the high-speed measurement of novel device bit error rates and endurance.

The chip comes in 2-variants which utilize two different high speed readout methods through the on-chip amplifier.

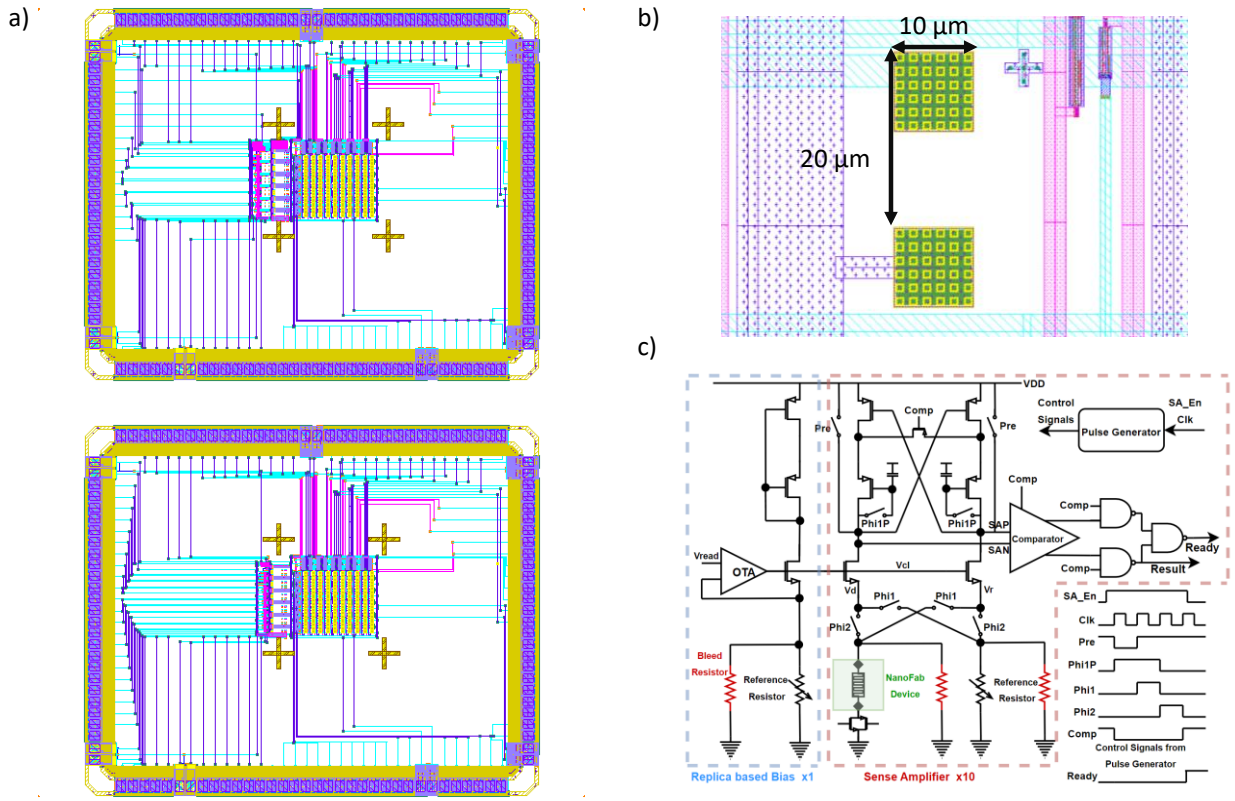

Figure 10 a) high level view of the tile which includes 2 variant chips, b) view of the local nanofabrication region for 2-terminal memory device and c) circuit level depiction of the on-chip triggered pulse and sense capability.

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10 Tile Title: NanoCMOS Passive Tile

Team: LBNL/UCB

PI(s): Maurice Garcia-Sciveres

Contact: mgarcia-sciveres@lbl.gov

Description: This tile contains a backing array of metal layers designed to efficiently route voltage and current for BEOL integrated 3-terminal devices for sensing and actuation tiled in arrays. No active elements such as transistors are present in the tile. The routing allows arrays of, for example, 100 nm length individual CNTs, to be routed to gate, source, and drain macroscopic probe pads. This will enable, for example, the development of frequency-resolving single photon sensors using functionalized nanodevice active receivers.

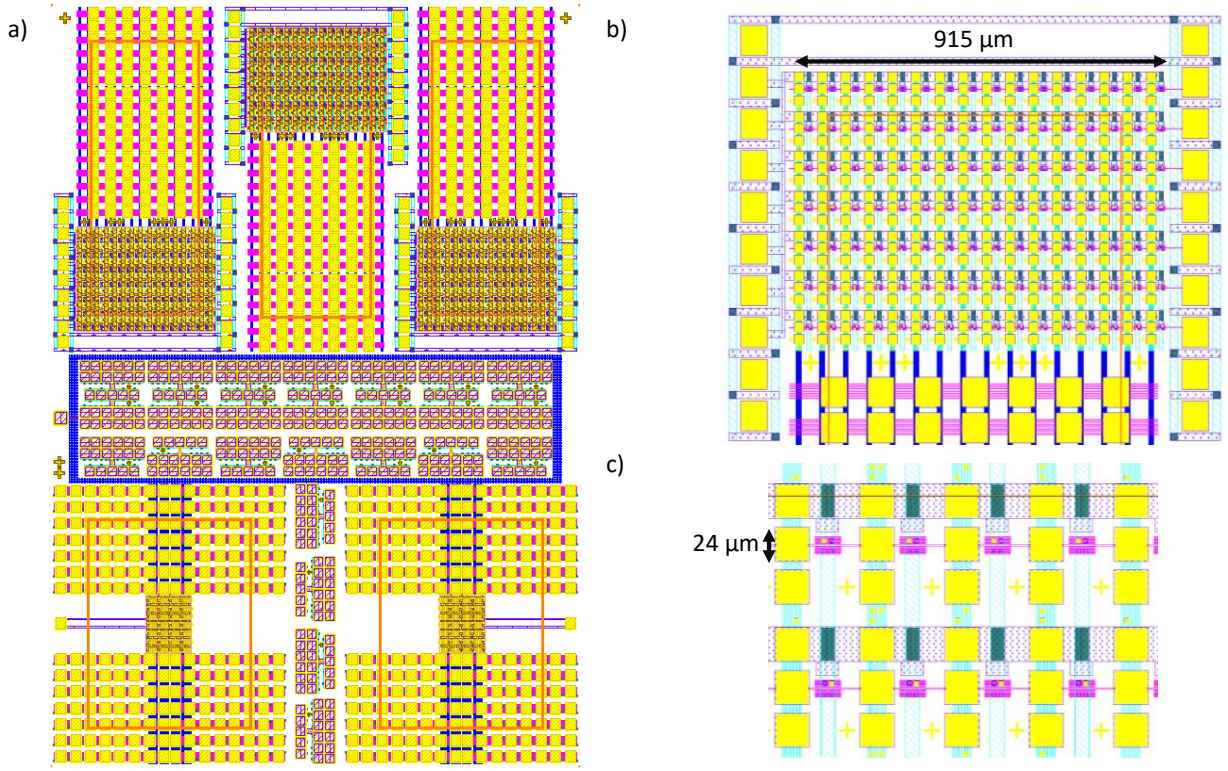

Figure 11 a) high level view of the tile array, b) a closer up view of a local signal distribution network, c) a close up view of the nanofabrication region.

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11 Tile Title: NanoCMOS ActiveTile

Team: LBNL\UCB

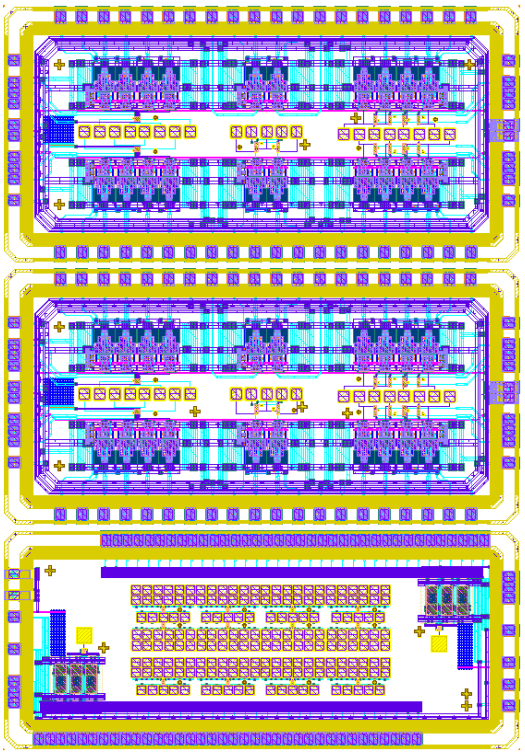
PI(s): Maurice Garcia-Sciveres

Contact: mgarcia-sciveres@lbl.gov

Description: This tile contains several designs of ~100MHz bandwidth pre-amplifiers designed to be integrated with single nanodevices, such as carbon nanotubes. Some preamps are designed for voltage drop measurement on devices with a bias current and a gate voltage, while others are designed for the nanodevices to act as the input transistor of a high gain preamp. The preamp outputs are designed to drive 50 Ohms off-chip. All preamps have dedicated input vias and macroscopic output pads (no

multiplexing). This will enable, for example, a project to develop frequency-resolving single photon sensors using functionalized nanodevice active receivers.

a)



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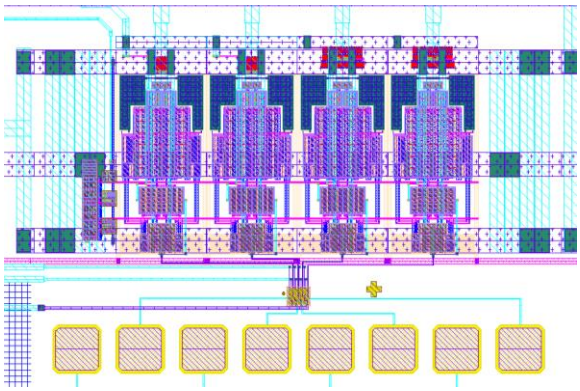

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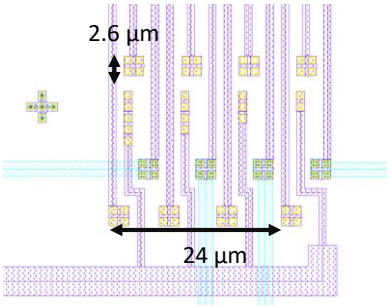

12 Tile Title: Scanit Tile

Team: LBNL\UCB

PI(s): Peter Denes

Contact: pdenes@lbl.gov

Description: This tile is designed to readout from a dense array of 2400 pico-Ampere sensitive preamplifier test points which are the size of a single 500x500 nanometer via. The purpose is to study the distribution and behavior of electrically conductive nanopore membranes where the nanopores are randomly distributed across a membrane painted over the chip. This chip is designed for the study of the surface preparation of nanopore chips as well as the preparation and study of the nanopore membranes themselves.

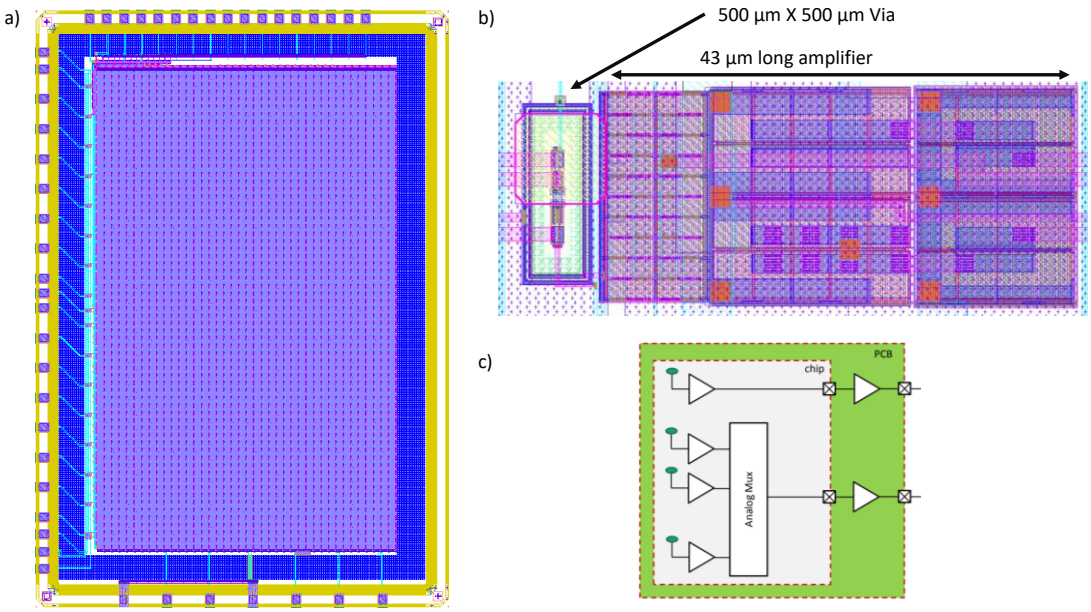

Figure 12 a) overview of the tile featuring thousands of amplifier test points, b) isolated view of a single amplifier and test point, c) conceptual view of the ability to access any test point.

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13 Tile Title: CV Measurement Tile

Team: University of Michigan

PI(s): Mehdi Saligane

Contact: mehdi@umich.edu

Description: This chip contains an array of on-chip integrated charge based capacitive voltage (CV) measurement systems. Conventional CV measurements are limited by the relatively low frequency (10MHz) and high parasitics (due to cabling) of conventional probing. In foundry environments, embedded CV measurement capability with on-chip VCOs is conventionally used to measure the CV characteristics of nanoscale transistors.

To extend this capability to researchers, this tile contains a set of charge based capacitive-voltage measurement systems which can be either externally pumped or driven by an on-chip 1GHz voltage controlled oscillator. This capability extends the performance of CV measurements to nanoscale device structures. The use of both target and reference arms in the structures makes them ideal for differential measurements which could include comparing the capacitance of memory devices in different states. This structure is compatible with contact lithography with a 10 micron feature size.

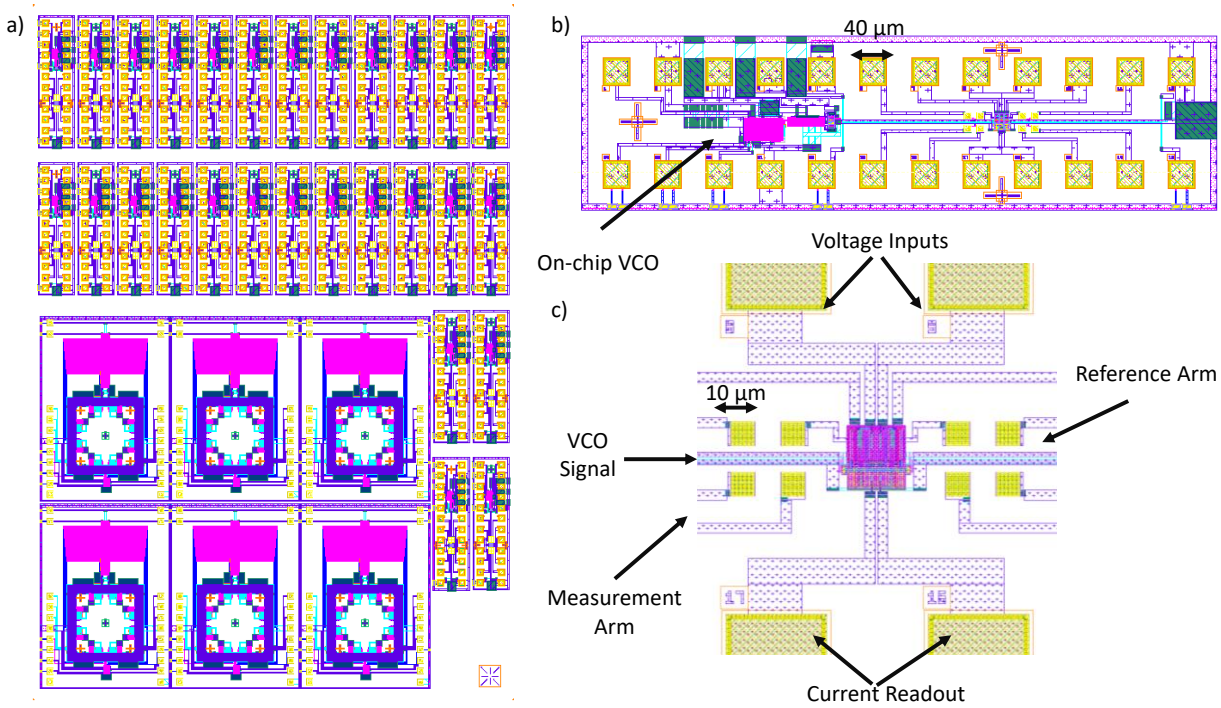

Figure 13 a) overview of the tile featuring multiple test structures, b) view of a single test structure which can be probed via probe card, c) local view of the nanofabrication region where a device and control region for capacitance measurement.

14 Tile Title: PLL Tile

Team: University of Michigan

PI(s): Mehdi Saligane

Contact: mehdi@umich.edu

Description: This tile includes both on-chip op-amps as well as a high frequency LNA co-integrated with a Phase-Locked Loop. This structure is ideal for performing on-chip high frequency measurements of signal response and phase when the DUT is driven by a high frequency electromagnetic source such as an RF signal or a pulsed laser for optical spectroscopy experiments.

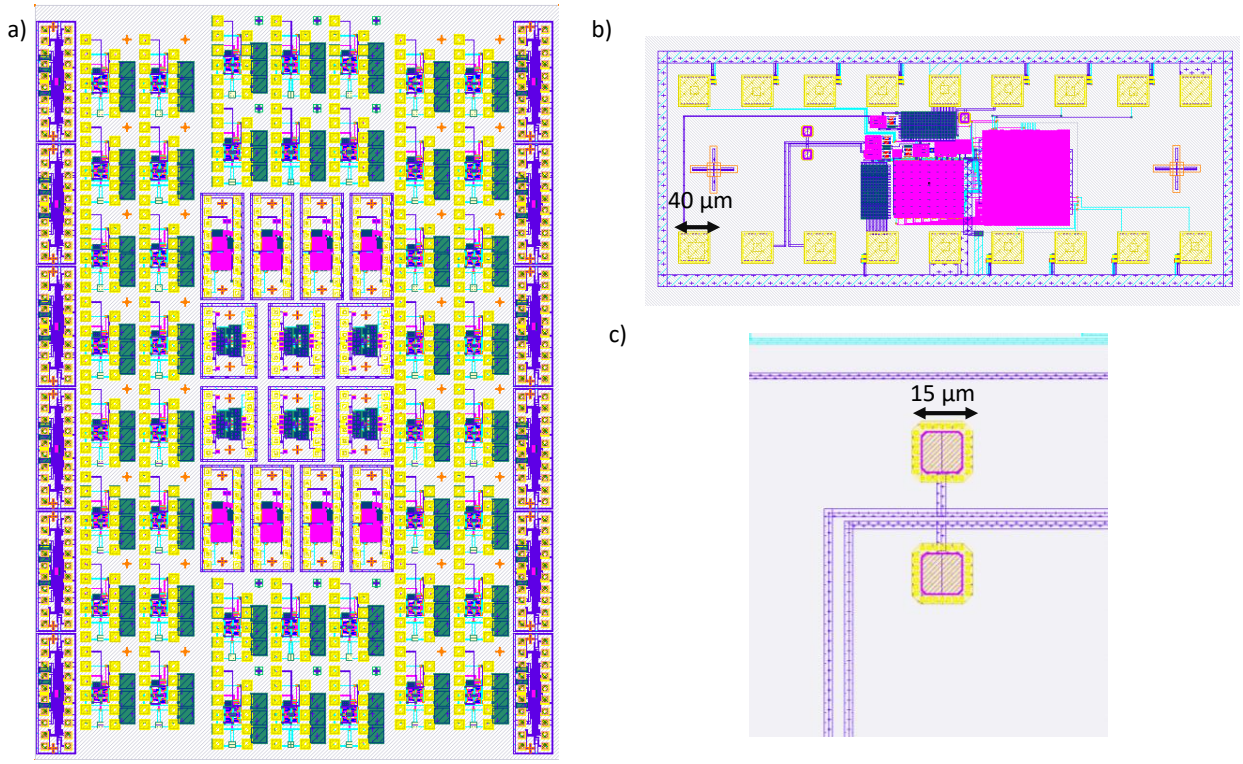

Figure 14 a) overview of the chip features PLs in the center surrounded by amplifiers, b) isolated PLL structure, c) region where electrical contacts can be directly routed to a PLL or nanodevice could be built.

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15 Tile Title: Room Temperature (RT) Amplifier Tile

Team: University of Michigan

PI(s): Mehdi Saligane

Contact: mehdi@umich.edu

Description: This tile contains an array of operational amplifiers designed to be co-integrated with nanodevices. Users can wire the amplifiers in any chosen configuration and fabricated their own on-chip capacitors and feedback resistors.

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16 Tile Title: Cryogenic Amplifier Tile

Team: University of Michigan

PI(s): Mehdi Saligane

Contact: mehdi@umich.edu

Description: This tile is similar to the RT amplifier tile but instead used 4 Kelvin device models of Sky130 to optimize the device performance.

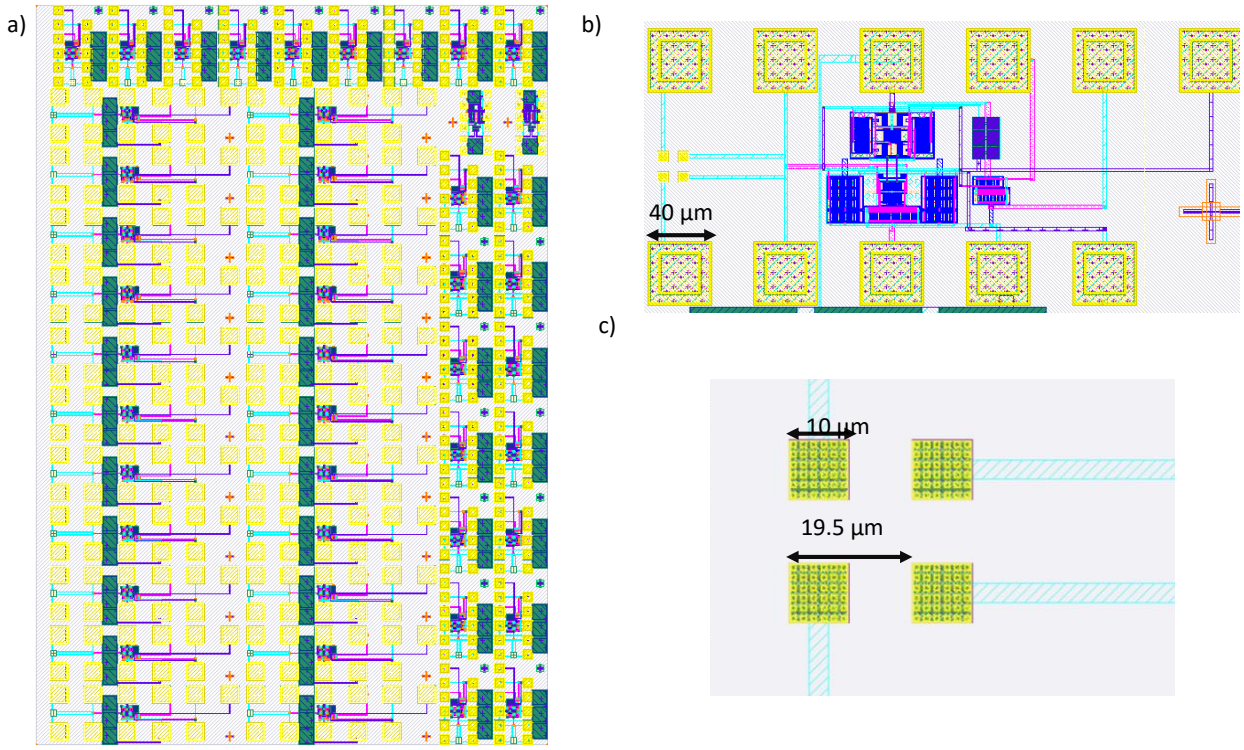

Figure 15 a) overview of the cryo tile (the RT tile looks almost identical), b) probe land level view of a test structure with a local nanofabrication region to add a nanodevice, b) region where a nanodevice could be built and routed to either the amplifier or external pads.

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17 Tile Title: P-Bit Test Vehicle

Team: University of Maryland + NIST

PI(s): Advait Madhavan

Contact: amadha1@umd.edu

Description: The P-Bit test vehicle is an array of high-density test structures for measuring stochastic magnetic tunnel junctions and other random telegraph noise-generating devices. While many test structures are stand-alone metal connections for device-only characterization, the vast majority are

composed of probe points with additional inverters that can be used to threshold the random telegraph noise against a reference. The test structure therefore transforms noise from nanodevices into high-speed bit streams with potential applications in probabilistic and stochastic computing.

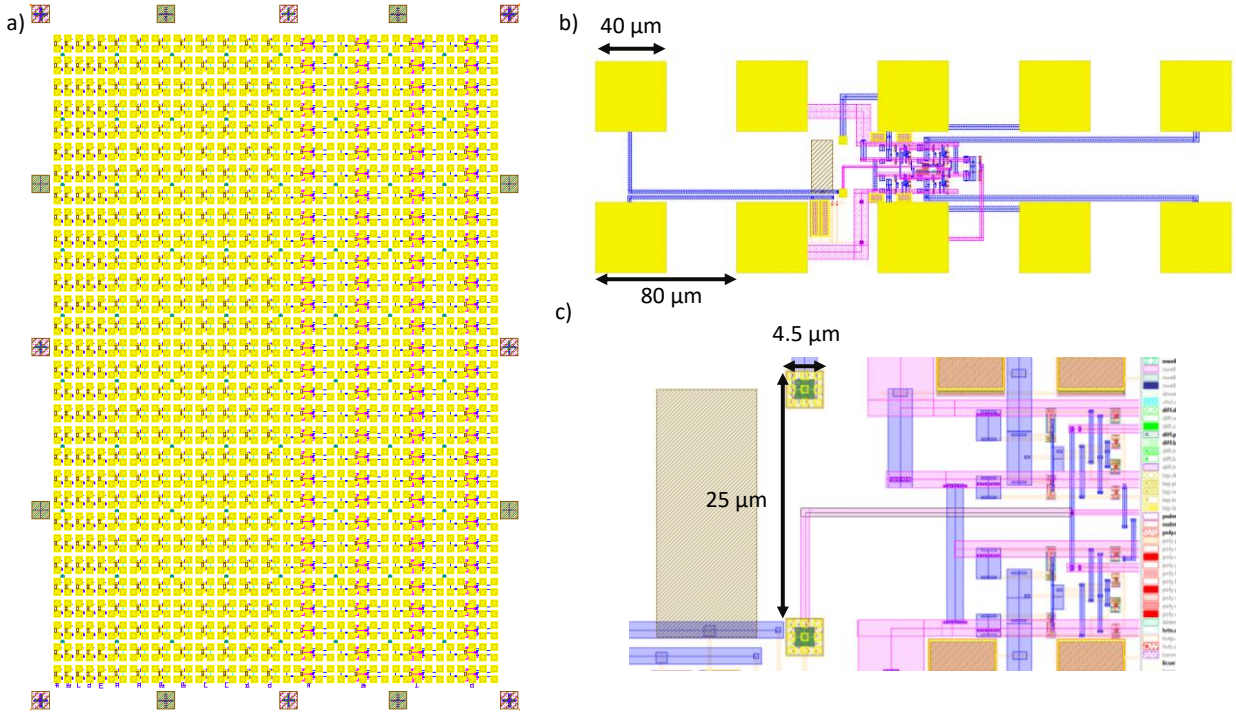

Figure 16 a) High level view of the tile with multiple test structure types, b) probe land level view of an individual thresholding test structure, c) view of the region where a 2-terminal stochastic device could be built.

18 Tile Title: Bio-Capacitive Device Sensor Array (Large Capacitance) and Bio-manufacturing Test Vehicle

University: University of Maryland + NIST

Team: Advait Madhavan

Contact: amadha1@umd.edu

Description: Many novel concepts in bioelectronics involve developing capacitive sensors. For this project, an array of 16 capacitive test points have been laid out. Each test point has an opamp-based capacitive sensor which can measure a capacitance shift in the liquid above each point with sub pF accuracy. This project exploits the wafer scale nature and planarized surfaces received to study the optimal surface properties of CMOS wafers needed to functionalize the surface of these tests points with biosensor materials that have a strong capacitive response. In one proposal, this would involve attaching DNA to an appropriately prepared dielectric on the CMOS chip surface.

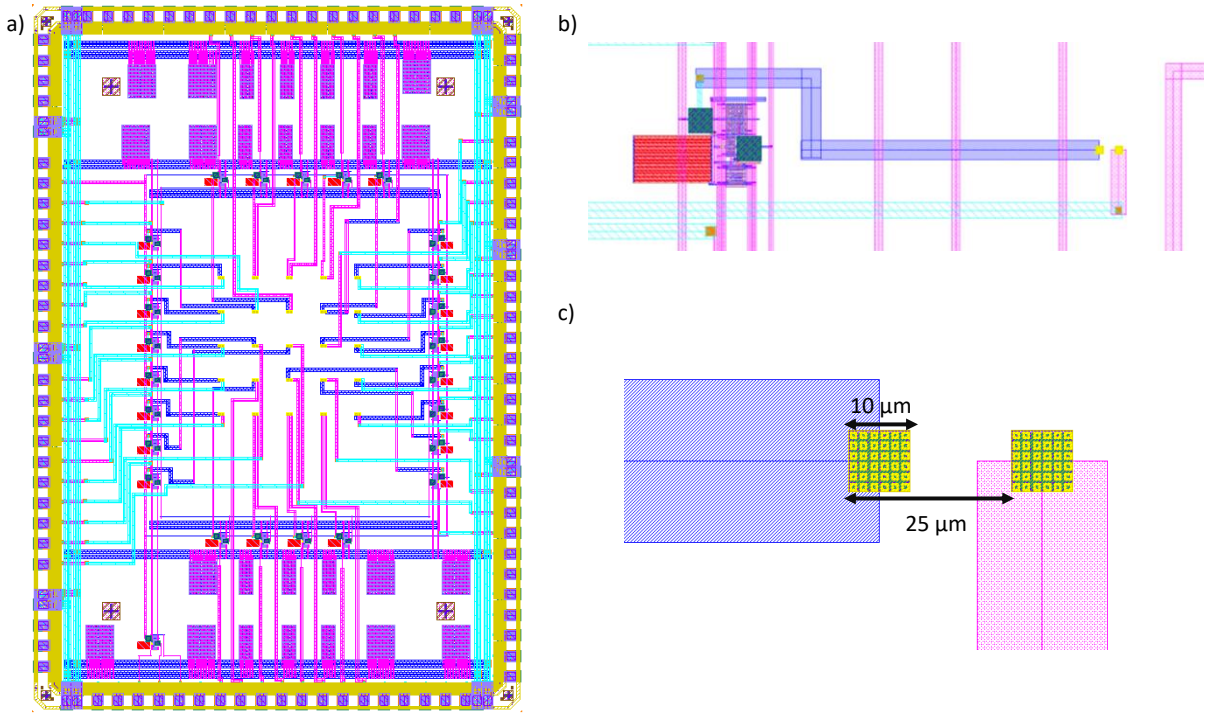

Figure 17 a) High level view of the overall chip featuring 16 test points, b) a selected view of a single amplifier routed out to test points and c) individual test points which could be functionalized with biomolecules.

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19 Tile Title: 18-Kb test vehicle for novel 2-Terminal Memory Devices

Team: University of Maryland + NIST

PI(s): Advait Madhavan

Contact: amadha1@umd.edu

Description: Most university researchers studying memory devices may only measure a handful of devices. In this project, a test vehicle has been developed that is optimal for nanofabrication researchers

to be able to measure thousands of 2-terminal memory devices (ReRAM or MTJs) using off-chip source and measure units. The chip is composed of an array of pass gates designed to allow access to any one of 18kb of devices made by university researchers. Each device is designed to have a 5-micron feature size. This chip comes in a version with strong electrostatic discharge (ESD) protection and in a version without any ESD protection.

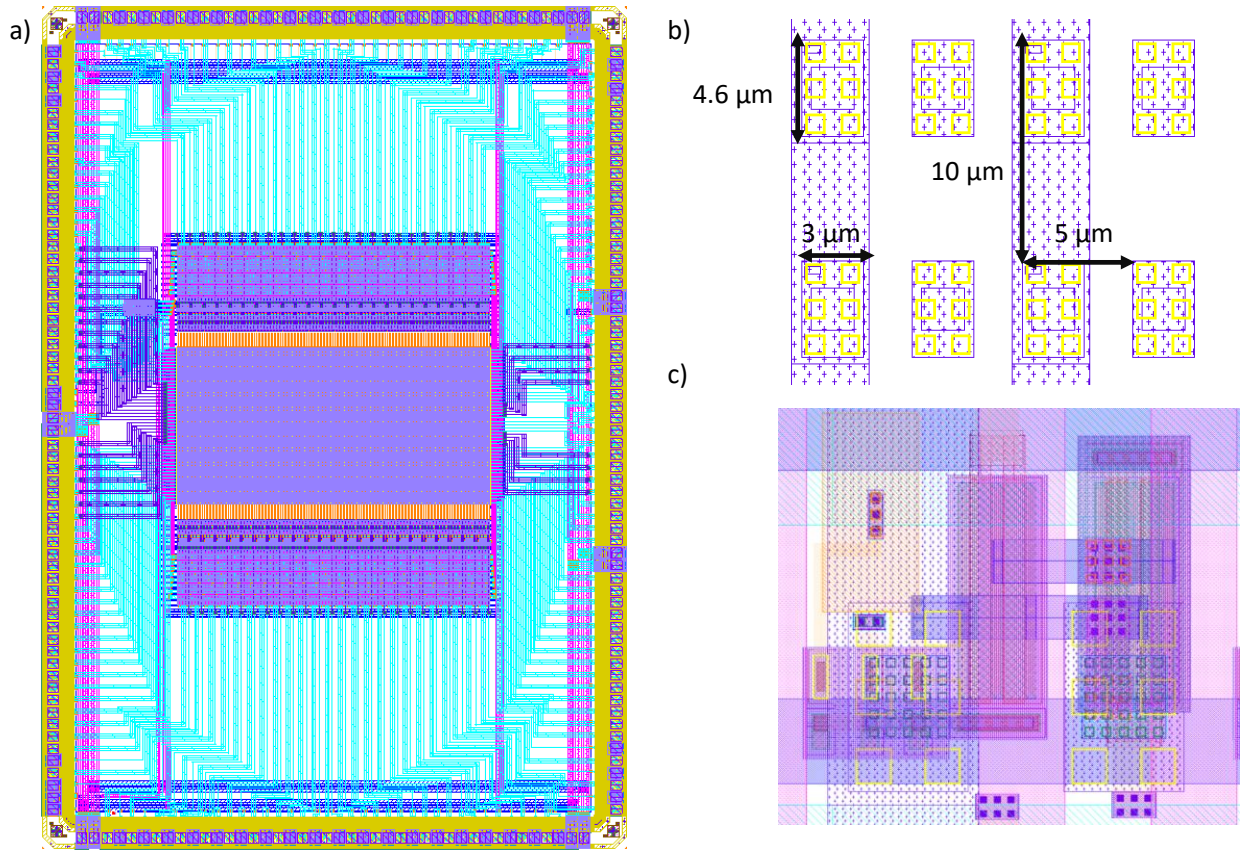

Figure 18 a) overview of an 18kb memory array, b) array level view of the nanofabrication region and exposed vias, c) full chip view with exposed vias with nearby nmos and pmos passgate transistors.

20 Tile Title: Bio-Capacitive Device Sensor Array (Fringe Capacitance) and Bio-manufacturing Test Vehicle

University: University of Maryland

PI(s): Sahil Shah and Pamela Abshire

Contact: sshah389@umd.edu and pabshire@umd.edu

Description: Many novel concepts in bioelectronics involve developing capacitive sensors. For this project, an array of 256 capacitive test points have been laid out. Each test point has a ring-oscillator based capacitive sensor which is designed to measure the impedance of individual living cells and to help study the optimal preparation of CMOS surfaces for cellular culturing.

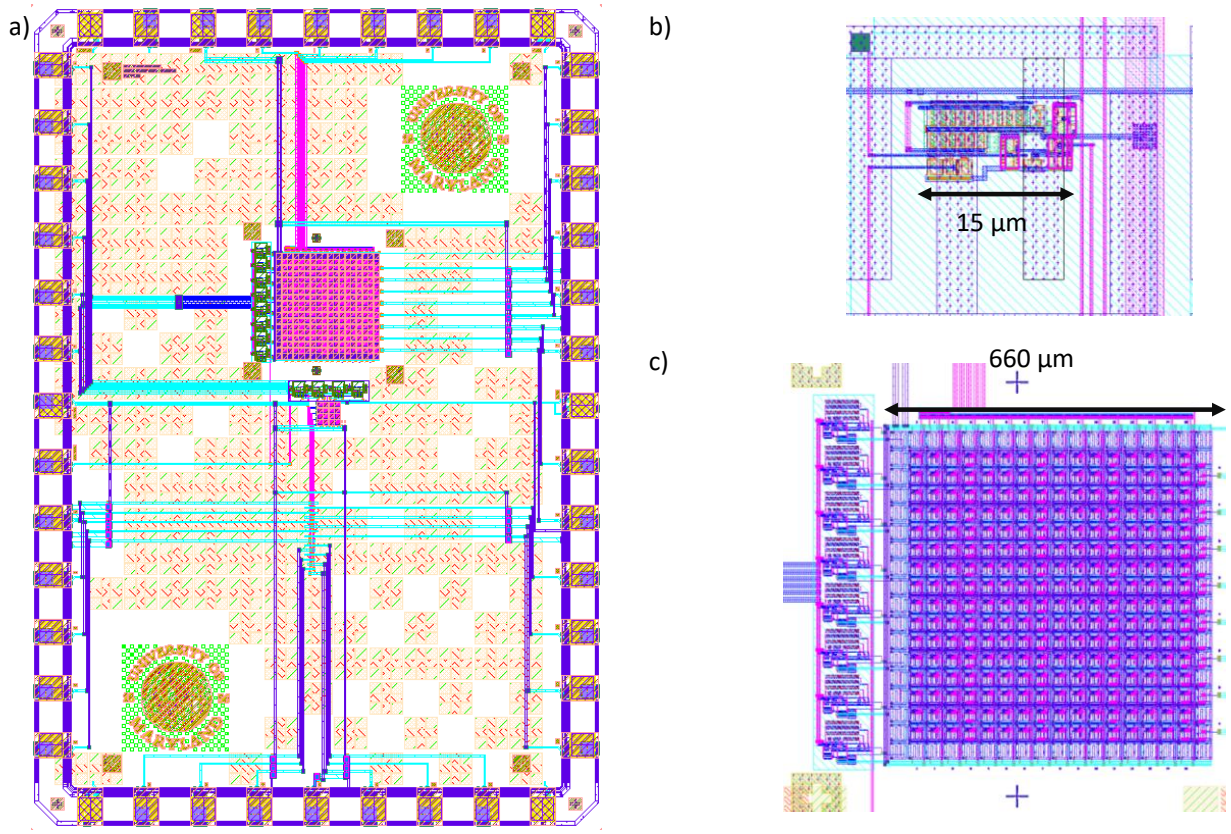

Figure 19 a) high level view of the chip, b) view of a local capacitive sensor, and c) view of one of the primary test arrays on the chip.

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21 Tile Title: Ion-sensitive Field Effect Transistor Array Test Vehicle

University: University of Maryland

PI(s): Sahil Shah and Pamela Abshire

Contact: sshah389@umd.edu and pabshire@umd.edu

Description: This chip is composed of an array of transistors with their gates exposed to the surface so as to enable the measurement of the pH of a liquid above. This chip will primarily be used to study the optimal surface preparation of a CMOS chip for pH measurements. Secondarily, it can also be used to optimize thin encapsulation materials which avoid contamination of the underlying CMOS with mobile ions.

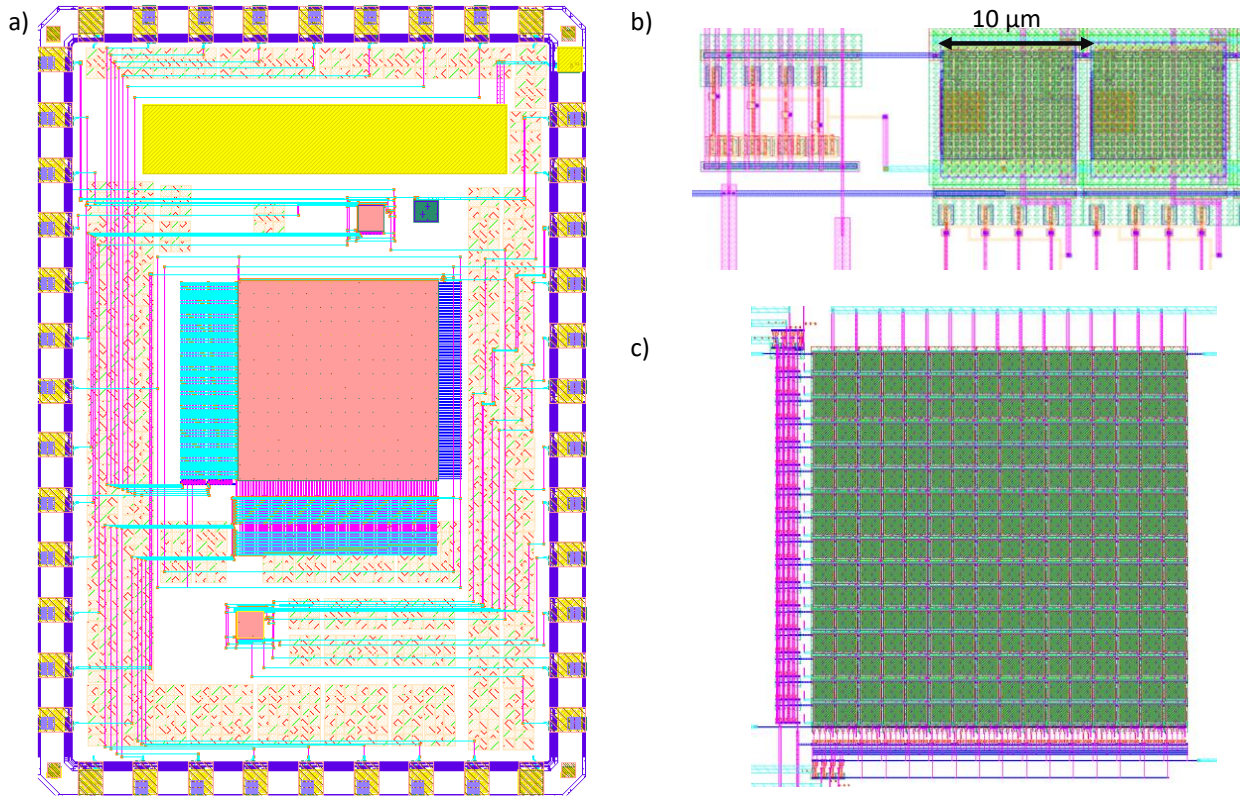

Figure 20 a) high level view of the chip, b) view of one of the individual ion-sensitive FET devices, c) a view of the main array of FETs.

22 Tile Title: GaN-CMOS NIR heterogenous integration test vehicle

University: University of Maryland and University of Virginia

PI(s): Sahil Shah and Kyusang Lee

Contact: sshah389@umd.edu and kl6ut@virginia.edu

Description: This chip is composed of 16x16 arrays of test points of different sizes which can be used to test the contact reliability of bonding a material from a different substrate onto it. Such a substrate could be, for example, GaN.

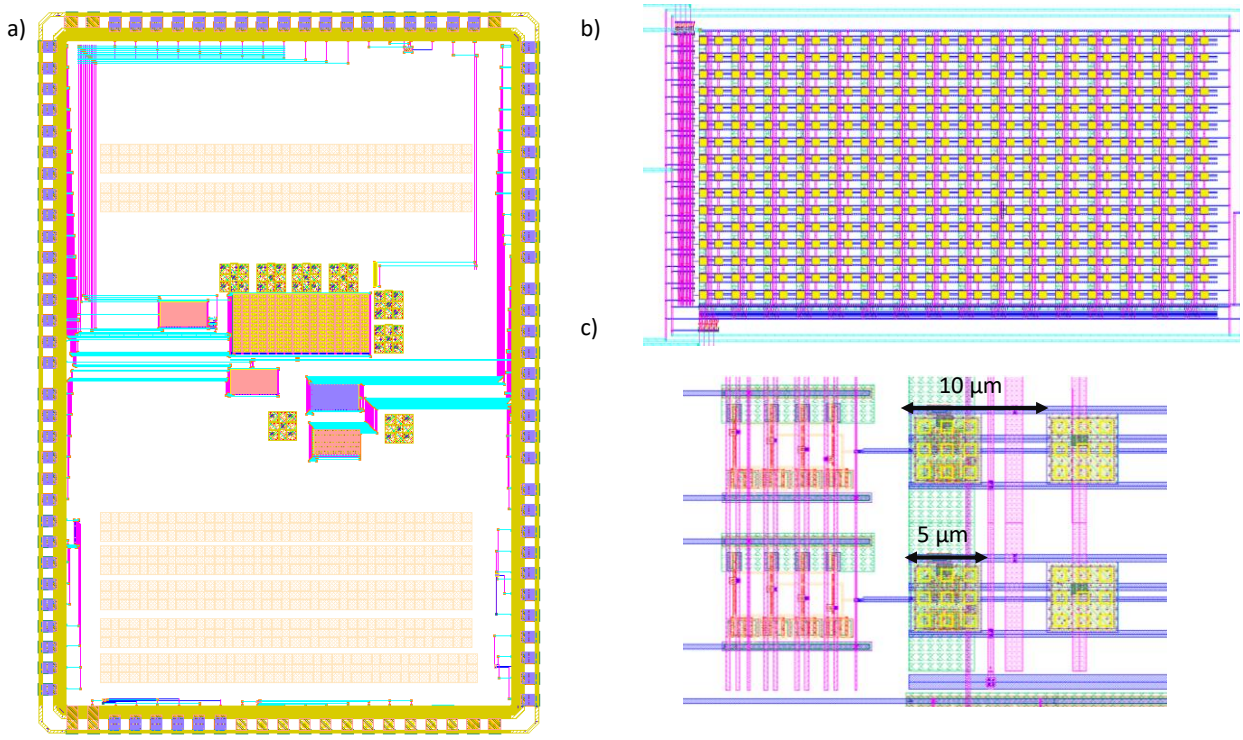

Figure 21 a) a high level view of the chip, b) a view of the array of flip chip assembly test points, c) a local view of the exposed tungsten vias which are designed to be flip chip bonded to another substrate.

23 Tile Title: Multi-modal biosensor test vehicle

University: University of Tennessee

PI(s): Nicole McFarlane

Contact: mcfarlane@utk.edu

Description: Contains multi-modal system with electrodes/circuits to enable/characterize biosensors such as pH, electrochemical, and optical (bioluminescence) detection. The post fabrication use/characterization aims to integrate carbon based electrodes (electrochemical) and thin passivation (pH) to enable spatial resolution and biosensor sensitivity/limits of detection.

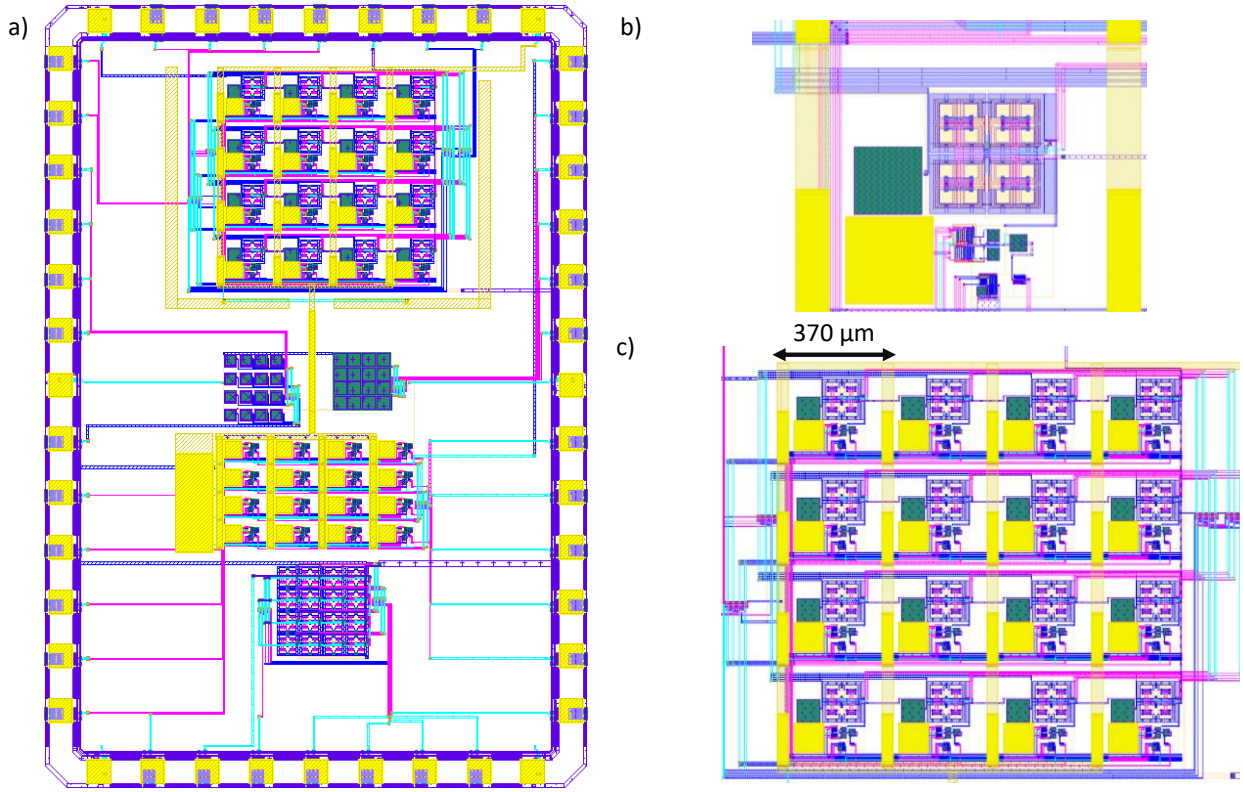

Figure 22 a) high level view of the chip which includes individual arrays for different sensing modalities, b) a view of the multi-modal sensing cell, and c) an array level view of the multi-modal cell with both electrical and optical characterization capability.

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24 Tile Title: 1kb 3-Terminal Device Test Vehicle (5V Version)

University: University of Virginia

PI(s): Mircea Stan

Contact: mrs8n@virginia.edu

Description: Most university researchers studying memory devices may only measure a handful of devices. In this project, a test-vehicle has been developed which is optimal for nanofabrication researchers to be able to measure thousands of 3-Terminal memory devices (such as spin orbit torque

devices) using off-chip source and measure units. The chip is composed of an array of passgates designed to allow access to any one of 1kb of devices made by university researchers. Each device is designed to have a 5-micron feature size. This chip comes in a version with strong electrostatic discharge protection and in a version without any protection. The ESD-free version could support higher frequency measurements (1GHz+) as well as lower leakage measurements for novel FETs (such as carbon nanotube based devices).

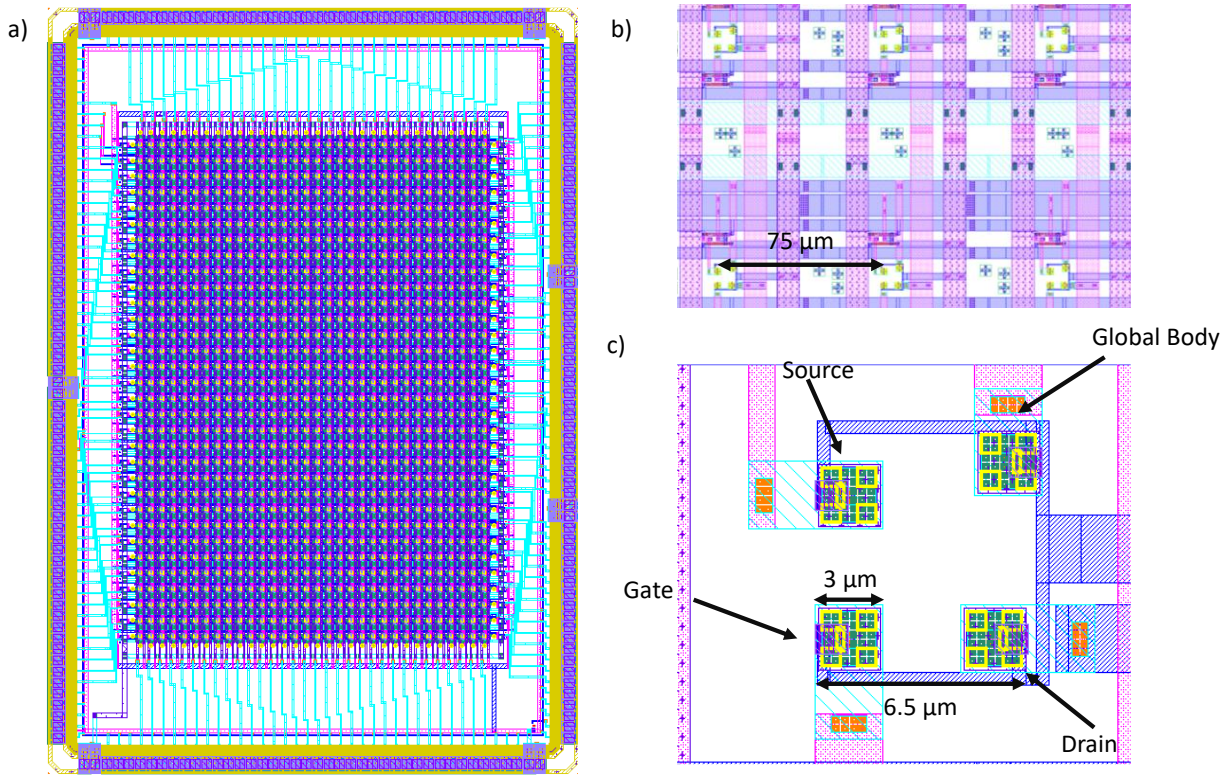

Figure 23 a) a high level overview of the chip, b) an array level view of multiple nanofabrication test points, c) a local view of the nanofabrication region for an individual 3-terminal memory device.

25 Tile Title: 1kb 3-Terminal Device Test Vehicle (20V Version)

University: University of Virginia

PI(s): Mircea Stan

Contact: mrs8n@virginia.edu

Description: Most university researchers studying memory devices may only measure a handful of devices. In this project, a test-vehicle has been developed which is optimal for nanofabrication researchers to be able to measure thousands of 3-Terminal memory devices which require high voltages (up to 20V, such as FeRAM) using off-chip source and measure units. The chip is composed of an array of passgates designed to allow access to any one of 1kb of devices made by university researchers. Each device is designed to have a 5-micron feature size.

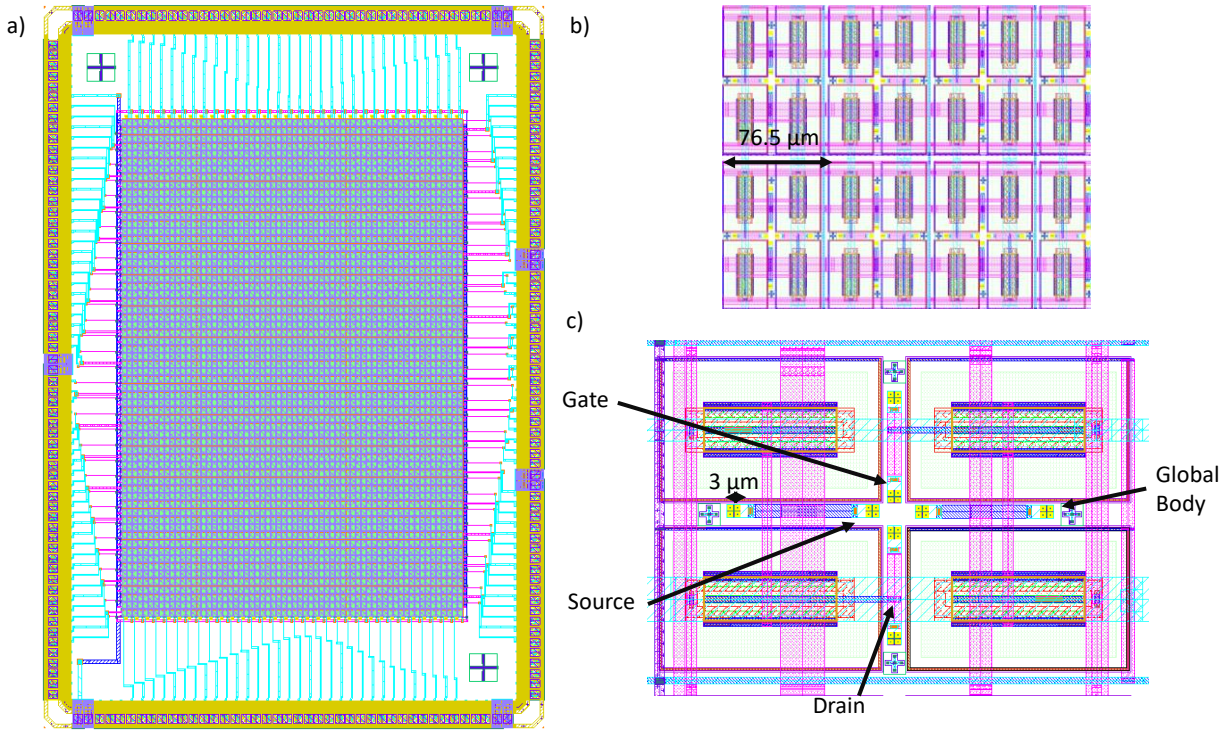

Figure 24 a) a high level view of the chip, b) array level view of multiple unit cells and c) a single unit cell view which includes both inner and outer electrodes for small and large high voltage devices. The inner and outer connections are shorted.

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26 Tile Title: Integrated Current sensor test vehicle for biomembrane current measurements

University: York University

PI(s): Sebastian Magierowski

Contact: magiero@yorku.ca

Description: Contains an array of 16 transimpedance amplifiers with pA sensitivity. Each amplifier has a 110 by 130-micron fabrication area where researchers can develop the optimal surface preparation for

membrane devices. After post-fabrication of the optimal surface in the university fab, researchers can paint biomembranes onto the chip with functional nanopores which produce current when the appropriate molecules traverse them. This current can then be read out through the amplifier. This chip can therefore be used to study novel nanopores and functional proteins in membranes for use as electronic devices.

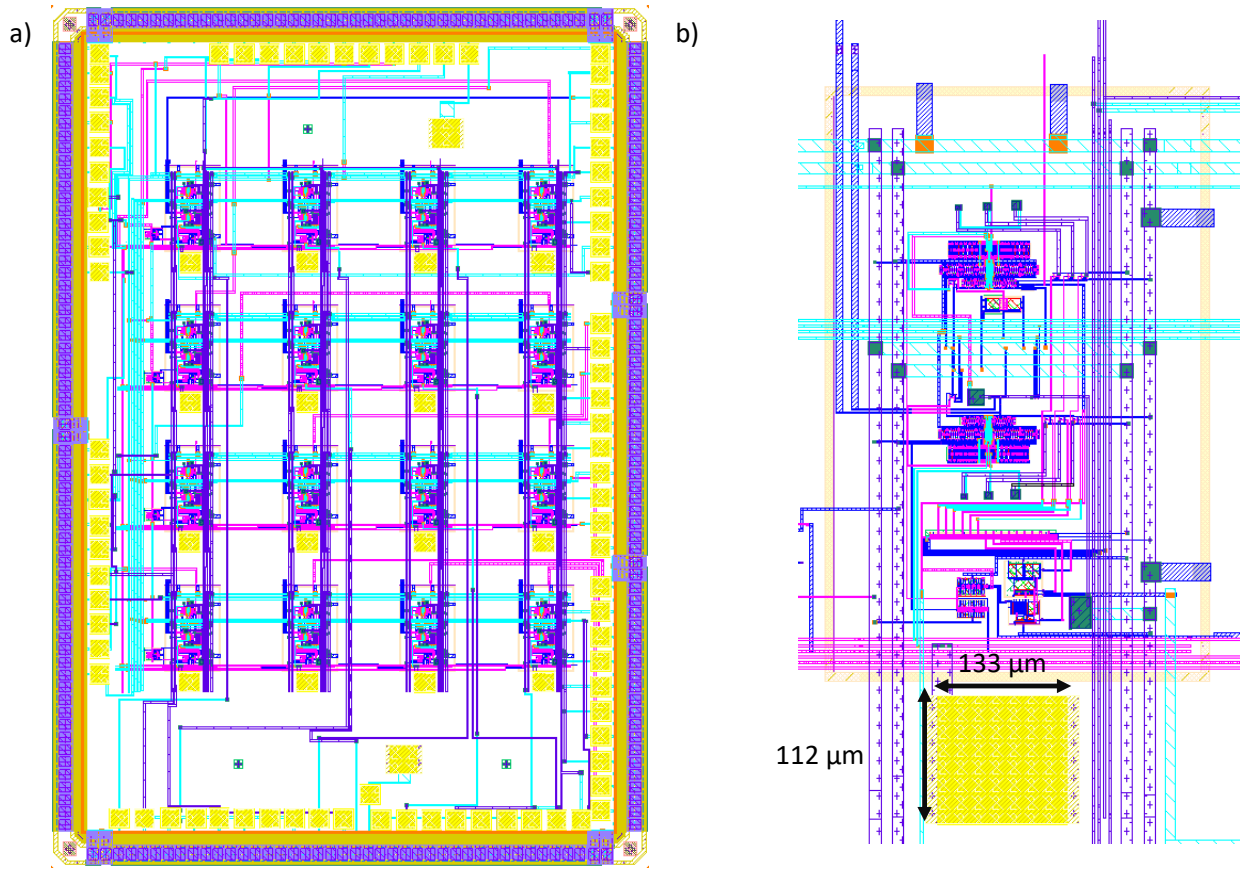

Figure 25 a) a high level overview of the chip with b) a view one of the local picoampere sensitive amplifiers combined with an exposed via collection area which can be optimized in the user's nanofabrication facility.

27 Tile Title: Large Ion-Sensitive FET

University: York University

PI(s): Ebrahim Ghafar-Zadeh

Contact: egz@yorku.ca

Description: A single, large area ISFET capable of achieving high sensitivity.

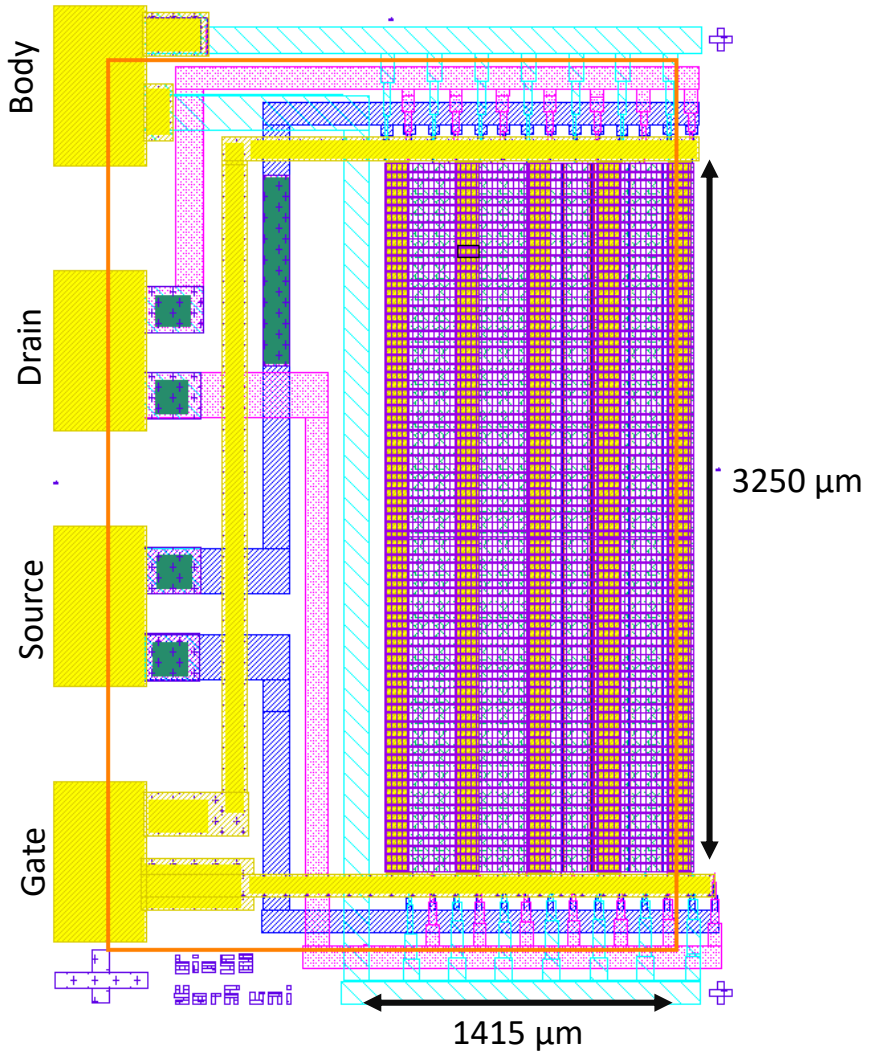

Figure 26 an overview of the large single FET chip