Semiconductor Research Corporation

PIONEERS IN COLLABORATIVE RESEARCH®

nanoelectronics RESEARCH INITIATIVE

NIST & SRC Nanoelectronics Research Initiative: Partnership for Innovation

Dr. Jeff Welser
Director, SRC Nanoelectronics Research Initiative
IBM Almaden Research Center

October, 2008

Semiconductor Research Corporation: Collaboratively Sponsored University Research

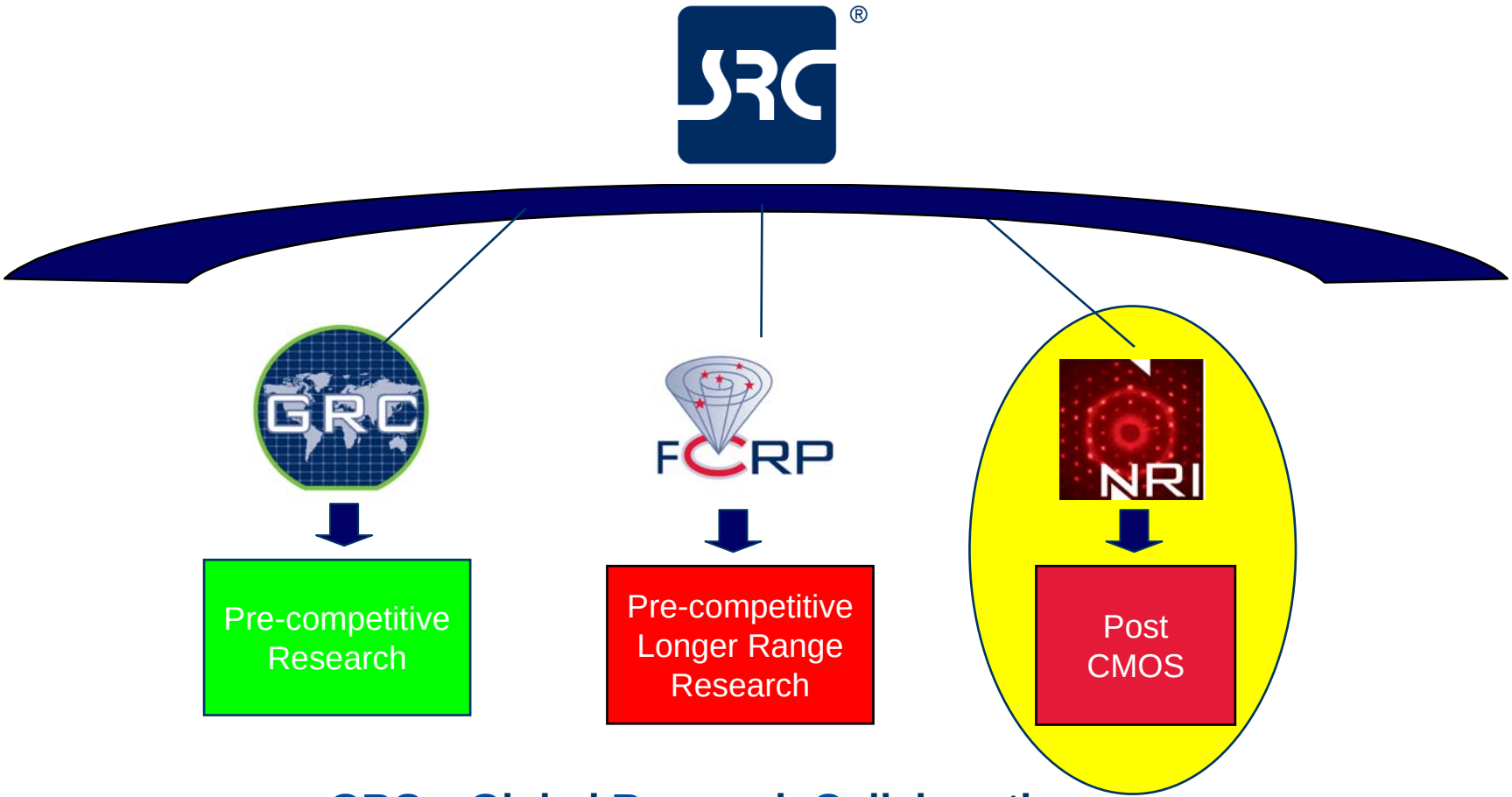
- The Semiconductor Industry Association (SIA) members have recognized that collaboration among industry, government and academia is the most efficient means of advancing university research capabilities

- Strong university research is critical to maintain technology innovation
  - Research in new concepts, breakthrough ideas and solutions to problems for which no currently known solutions exist
  - Development of talent pool of scientists and engineers

- Semiconductor Research Corporation (SRC) has been established to facilitate collaboratively sponsored university research
  - Manages full spectrum of research related to CMOS and beyond technology

- Awarded the 2005 National Medal of Technology
  - "For building the world's largest and most successful university research force to support the ... semiconductor industry …"

SRC Global Research Collaboration



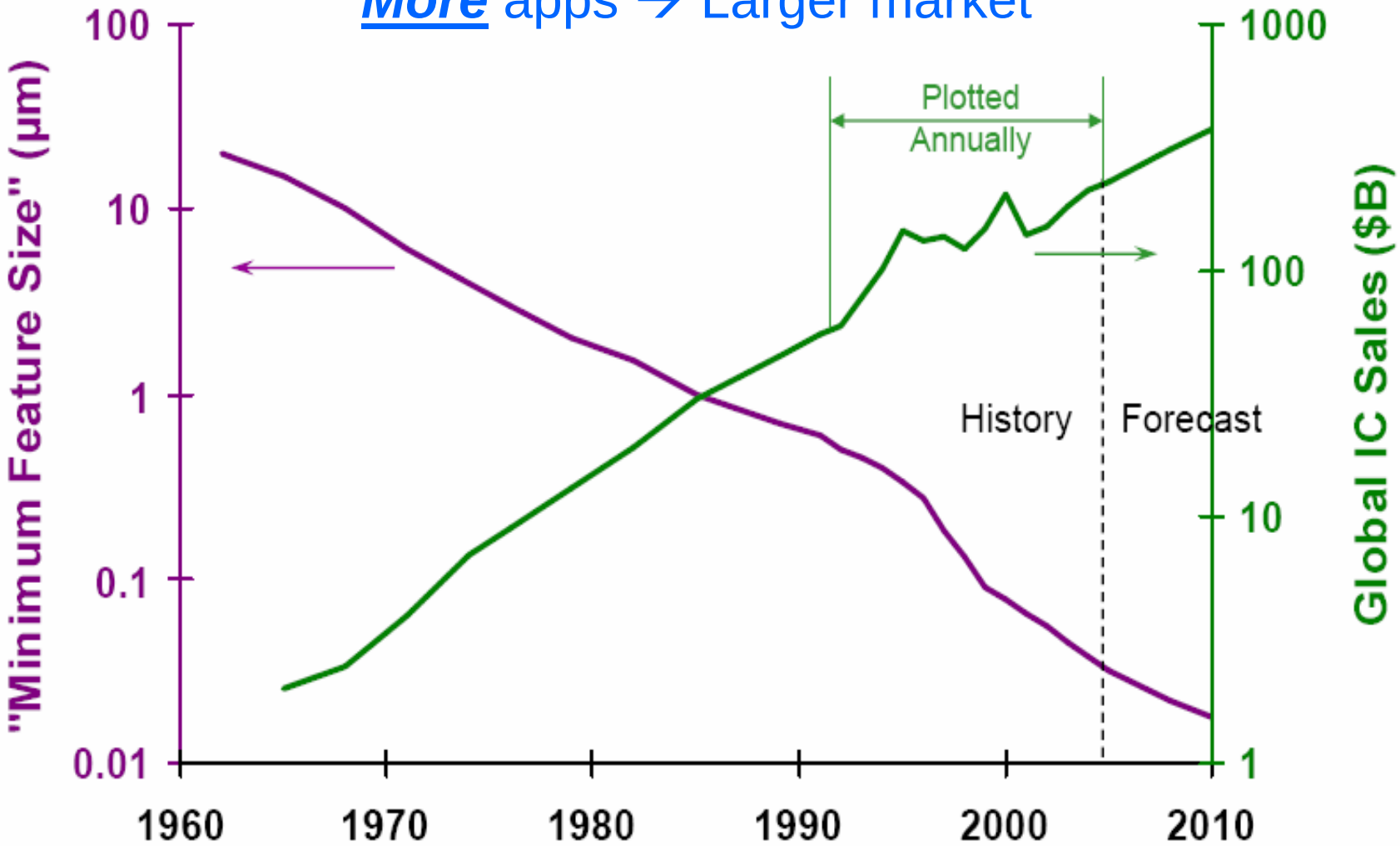
GRC – Global Research Collaboration

FCRP – Focus Center Research Program

NRI – Nanoelectronics Research Initiative

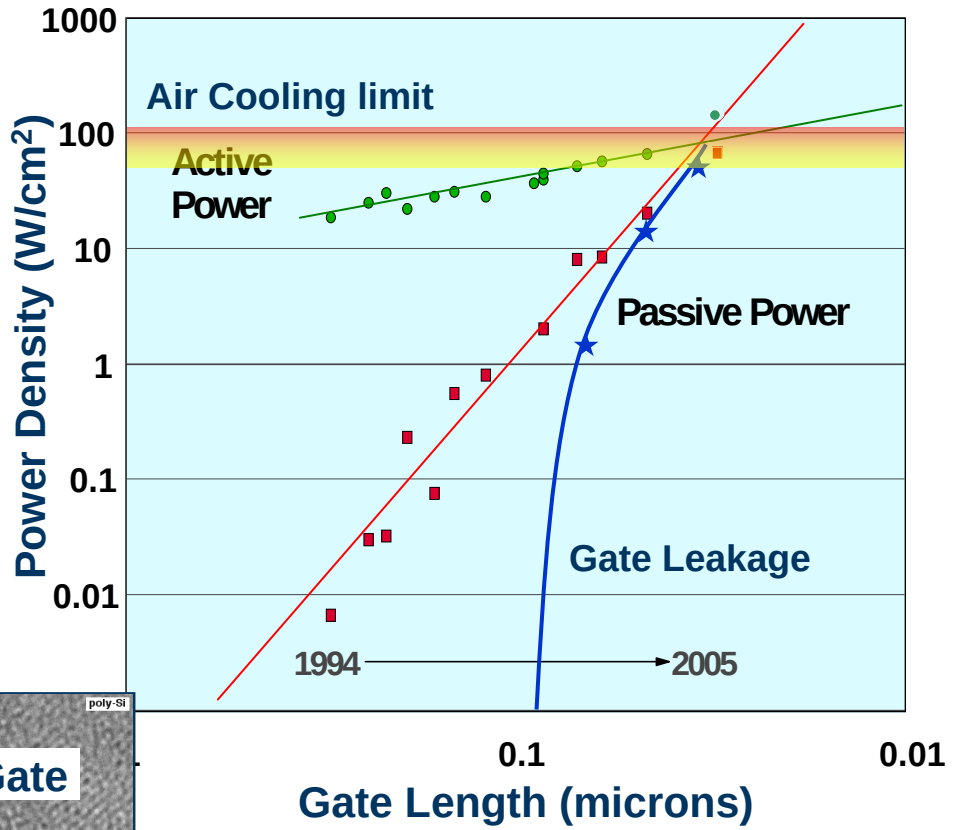
Scaling *Drives* the Industry

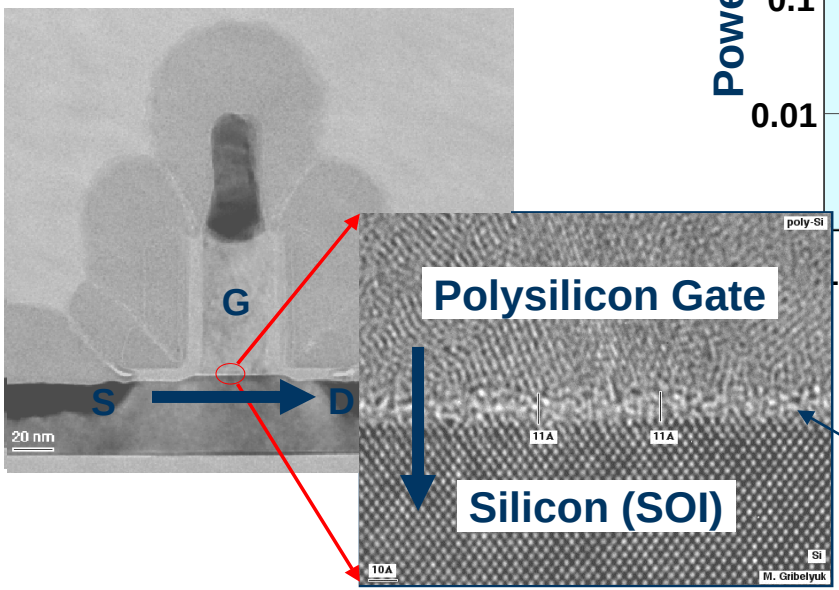
Smaller features → Better performance & cost/function → ***More*** apps → Larger market



CMOS Power Issue: Active vs. Passive Power

- Power components:
  - Active power
  - Passive power
    - Gate leakage
    - Source - Drain leakage





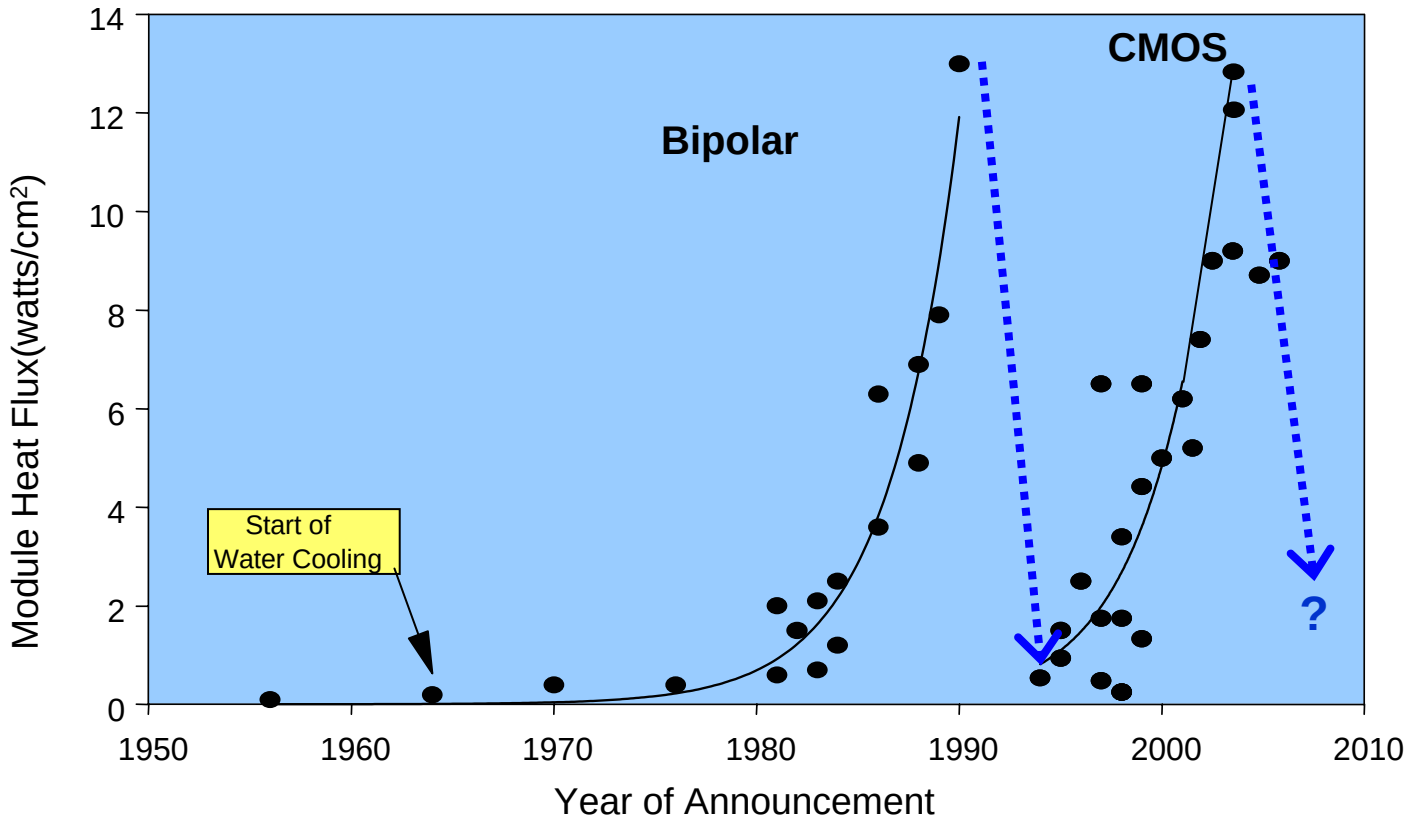
Implications for Nanoelectronics Circuits

- **Circuit heat generation is the main limiting factor for scaling of device speed and switch circuit density**

- Scaling to molecular dimensions may not yield performance increases
  - We will be forced to trade-off between speed and density
- Optimal dimensions for electronic switches should range between 5 and 50 nm
  - Likely achievable with Si – easily within the scope of ITRS projections
- Going to other materials for FETs will likely achieve only "one-time" percentage gains

➢ ***Need a new device mechanism or computation architecture to enable a new scaling path***

Has This Ever Happened Before?



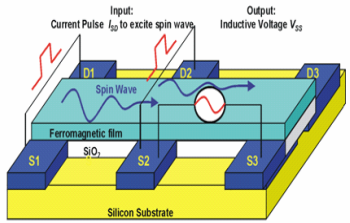
- 2005 ~ 2015: New technology enhancements
  - Continued CMOS shrinking, multi-core chips, 3D packaging, new memory devices, etc.
- > 2015? : New device? → NRI's Goal

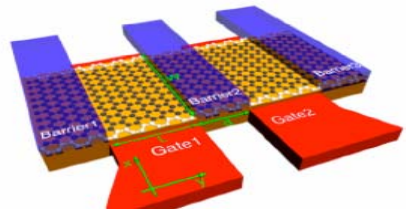
NRI Mission Statement

- **NRI Mission: Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.**
  - These devices should **show significant advantage over ultimate FETs** in power, performance, density, and/or cost to enable the semiconductor industry to **extend the historical cost and performance trends** for information technology.
  - To meet these goals, NRI pursues **five research vectors**, focused on discovering and demonstrating new devices and circuit elements for doing computation.
  - Finally, it is desirable that these technologies be **capable of integrating with CMOS**, to allow exploitation of their potentially complementary functionality in heterogeneous systems and to enable a smooth transition to a new scaling path.

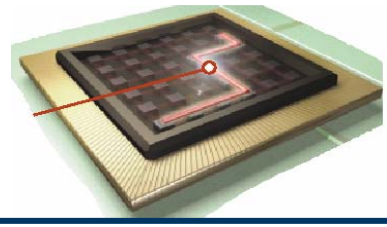
NRI Primary Research Vectors

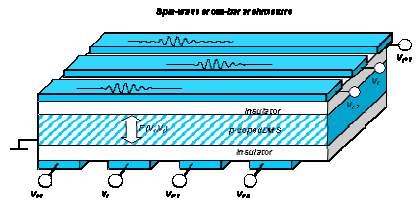
- **NEW DEVICE**
  Device with alternative state vector



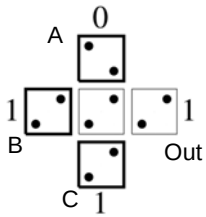


- **NEW WAYS TO CONNECT DEVICES**
  Non-charge data transfer

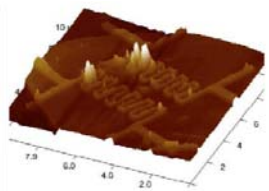




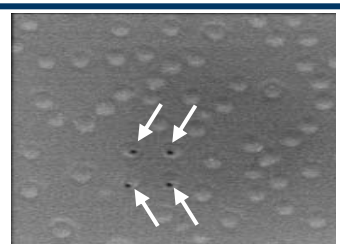
- **NEW METHODS FOR COMPUTATION**
  Non-equilibrium systems



- **NEW METHODS TO MANAGE HEAT**
  Nanoscale phonon engineering



- **NEW METHODS OF FABRICATION**
  Directed self-assembly devices



Nanoelectronics Research Initiative Milestones

- 2001-2004: Defining Research Needs
  - ITRS-Emerging Research Device Technical Working Group
  - NSF-SRC Ind-Academia-Govt "Silicon Nanoelectronics and Beyond" Workshops
  - SIA Technology Strategy Committee workshops
  - ➢ *Defined 13 Research Vectors for finding the "next switch"*
  - ➢ *SIA Board passes resolution for formation of NRI*
- March 2005: Six Companies sign NRI Participation Agreement

AMD freescale semiconductor IBM intel Texas Instruments Micron

- Sep 2005: First NRI and NRI-NSF Solicitations released
- Jan 2006: Research Programs started

NSF

- Sep 2007: NIST joins NRI

NIST

- NRI partnership model highlighted in as sidebar in the National Nanotechnology Initiative (NNI) Strategic Plan (NNCO, 1/08)

NRI-NSF Interaction:

Co-funding Projects at NSF Centers

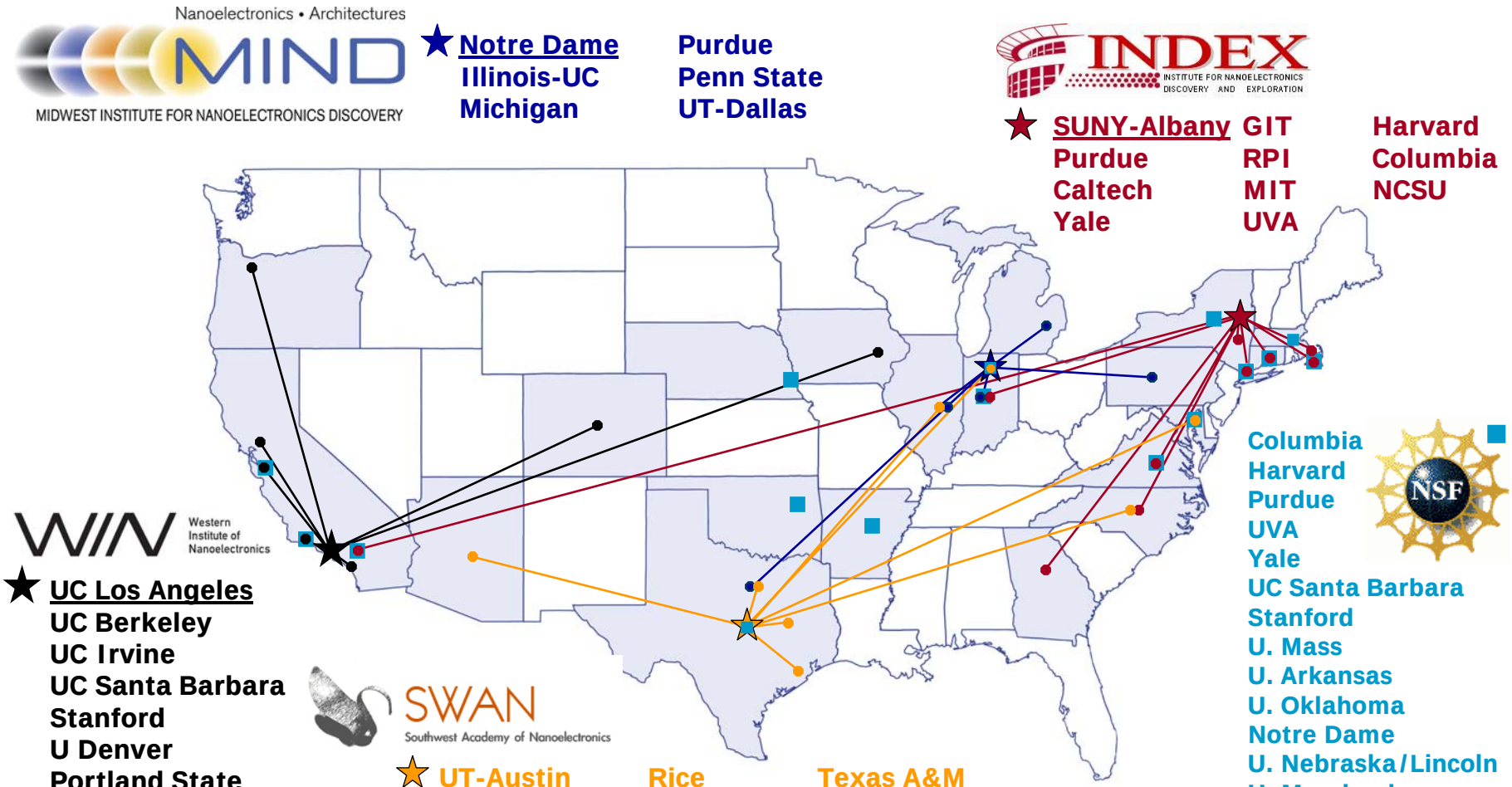
Columbia NSEC	*2006: Non-equilibrium Quantum Coherent Devices in 1-D materials* *2008: Novel Device Arch. based on Quantum Transport Phenomena in Graphene*
UCSB MRSEC (Stanford, U Mass)	*2006: Development of Next Generation Devices using Nanolithography*
Harvard NSEC	*2006: Ultrasmall Nanowire and Oxide Switches* *2008: Tunable Ultra-fast Conductance Switching through External Fields*
U. Arkansas/U. Oklahoma MRSEC	*2006: Nanoferroelectric Random Access Memory*
Purdue NCN	*2006, 2007: Exploratory Theory, Modeling, and Simulation for the NRI* *2008: Experimental Realization of Low-power Transistors with Negative Capacitors*
UVA MRSEC (Notre Dame, UCSB)	*2006: Directed Assembly of Epi Semiconductor Nanostructures for Novel Logic Switches; 2007: Coherent Spin Dynamics in Single Ion-doped Semiconductors: Towards a Coherent or Quantum Spin Switch*
U. Nebraska MRSEC	*2007: Multiferroic Interfaces: New Paradigms for Functional Switching*
Yale MRSEC	*2007: Design and Fab of Magnetic-based Devices with Complex Oxide Materials*
Maryland MRSEC (UT Austin)	*2007: Pseudospintronics* *2008: Controlling the Electronic Properties of Graphene*
Cornell NSEC	*2007: Controlled Orbital Hybridization in the CNT Quantum-Modulated Transistor*
Stanford NSEC (UT Austin)	*2008: Ultra-Low Power Pseudospintronic Switching in Bilayer Graphene at Room T*
Caltech MRSEC	*2008: Graphene Atomic Switches for Ultracompact Logic Devices and NV Memory*

NRI-NIST Interaction:
Full Partners in NRI Centers

- Leveraging industry, university, and both state & fed government funds, and driving university nanoelectronics infrastructure

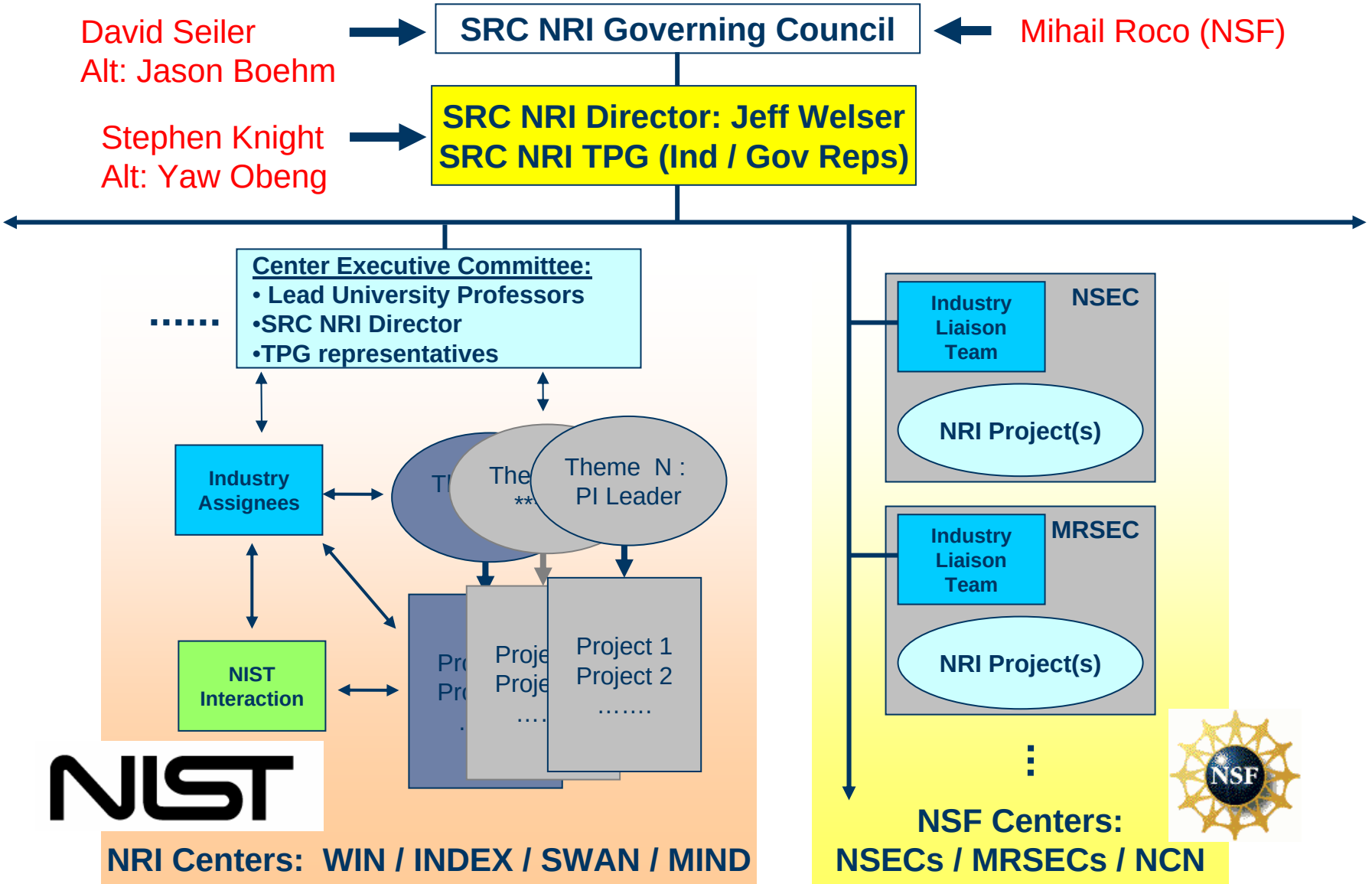
WIN Western Institute of Nanoelectronics	**INDEX** Institute for Nanoelectronics Discovery & Exploration	**SWAN** SouthWest Academy for Nanoelectronics	**MIND** Midwest Institute for Nanoelectronics Discovery
UCLA, UCSB, UC-Irvine, Berkeley, Stanford, U Denver, Iowa, Portland State	**SUNY-Albany**, GIT, RPI, Harvard, MIT, Purdue, Yale, Columbia, Caltech, NCSU, UVA	**UT-Austin**, UT-Dallas, TX A&M, Rice, ASU, Notre Dame, Maryland, NCSU, Illinois-UC	**Notre Dame**, Purdue, Illinois-UC, Penn State, Michigan, UT-Dallas
Theme 1: Spin devices Theme 2: Spin circuits Theme 3: Benchmarks & metrics Theme 4: Spin Metrology	Task I: Novel state-variable devices Task II: Fabrication & Self-assembly Task III: Modeling & Arch Task IV: Theory & Sim Task V: Roadmap Task VI: Metrology	Task 1: Logic devices with new state-variables Task 2: Materials & structs Task 3: Nanoscale thermal management Task 4: Interconnect & Arch Task 5: Nanoscale characterization	Theme 1: Energy Efficient Devices Theme 2: Energy Efficient Architectures

NRI Funded Universities



Over 30 Universities in 20 States

SRC NRI Management Structure



NRI Funding Model

$2.75M per year NIST

$5M per year Industry Partners

~$15M per year/ States

University-Based Research

- **INDEX: Institute for Nanolectronics Discovery and Exploration**
- **MIND: Midwest Institute for Nanoelectronics Discovery**
- **SWAN: South West Academy of Nanoelectronics**
- **WIN: Western Institute of Nanoelectronics**

Research Results

>$200M / over 5 years States & Private

Business Start-up, Development, and commercialization

Regional Government Contributions:
- Grants
- Tax Incentives

Industry Contributions
- VC Funds
- Direct Investment

NRI Center Example

INDEX

To discover and demonstrate nanodevice innovations that surmount CMOS scaling limits that will impede the historical rate of progress of US Semiconductor Industry

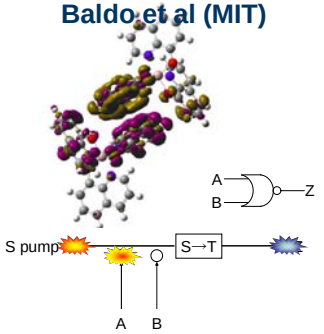
Five fully-integrated and synergistic research tasks for magnetic and molecular device paradigms

First Phase Focus: Task I (Novel Computing Devices) and Task II (Self-Assembly and Fabrication)

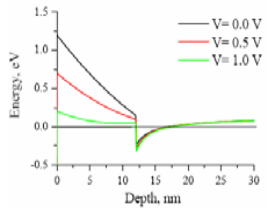
NRI Center Example

National synergistic network of centralized core fabrication and metrology facilities at UAlbany supporting tasks of all INDEX partners, coupled to a comprehensive array of design and fabrication nodes at all INDEX partners

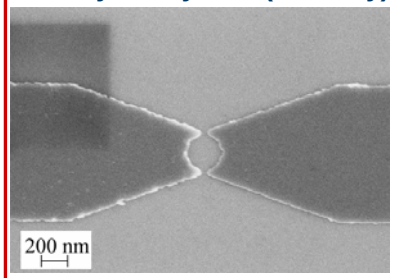
Molecular Excitons Spintronics
Baldo et al (MIT)



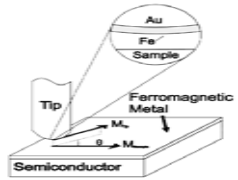
Quantum Dot Modeling
Shur et al (RPI)



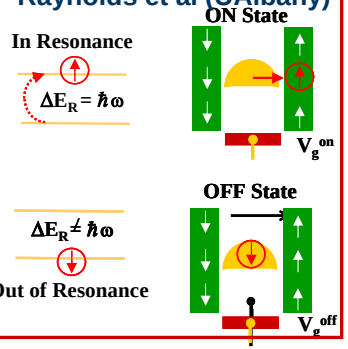
Quantum Dot Devices
Oktyabrsky et al (UAlbany)



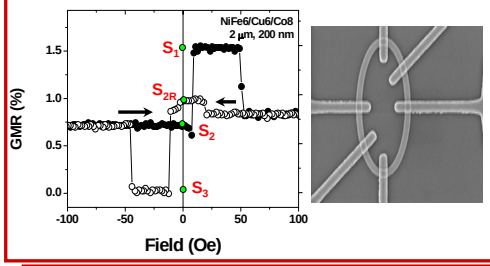
Ballistic Spin Devices
Labella et al (UAlbany)



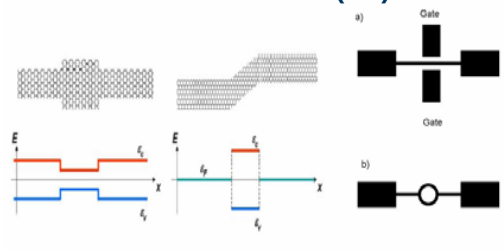
Single Electron Spin Devices
Raynolds et al (UAlbany)



Magnetoelectronic Devices
Multi bits logic Ross et al (MIT)

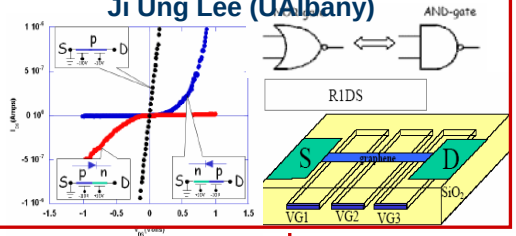


Graphene Nanowire Switches
Murali and DeHeer (GT)

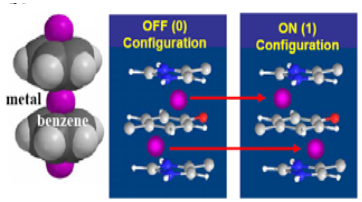


Post CMOS Switches

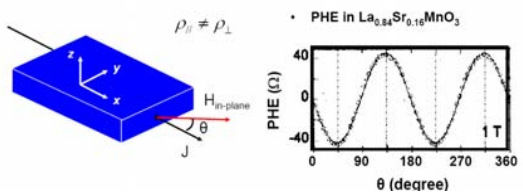
Reconfigurable One-Dimensional (1D) Switch (R1DS)
Ji Ung Lee (UAlbany)



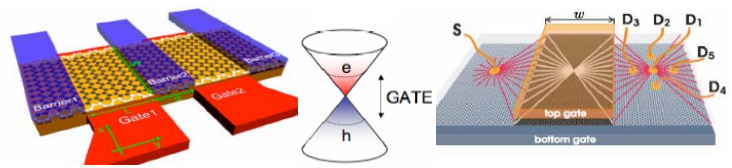
Molecular Nanowire Switches
Kaloyeros et al (UAlbany)



Logical Switches based on Complex Oxides
Ahn et al (Yale)



Graphene based Quantum Devices
Charles Marcus (Harvard)



NIST – INDEX Projects

PI	Project	NIST Collaborator
Karl Berggren	He Ion Microscope	Mike Postek
Alain Diebold	Optical measurement of Phonons in Graphene and their connection to electron mean free path	Ward Johnson Vinod Tewary
Robert Geer	Nanoscale electrical measurements and SPM of Graphene	Joe Kopanski
Julia Greer	Graphene mechanical properties	Ward Johnson
Phillip First	Atomic-scale electrical metrologies specifically for graphene	Joseph A. Stroscio; Mark D. Stiles
Philip Kim	Studying quantum Hall effect in graphene as a resistance standard	David Newell

Research Progress

- Key vision for NRI: Creating a *goal-oriented*, *basic science* research program
- No new device yet, but research results indicate strong progress already in three key areas to achieve this:
  - Studying new science phenomena with device potential
    - Pseudospintronics for giant "electro-resistance"
    - Digital Ballistic Anisotropic Magneto-Resistance (BAMR)
  - Linking scientists to engineers, to focus research on the key device issues (E.g. logic gates, room temp operation, power dissipation, connecting devices, etc.)
    - Spin wave logic devices and circuits "roadmap"
    - NOR-gate based on molecular excitons
  - ➢Linking work across groups / universities / centers to maximize progress
    - Study of graphene electronic and spintronic properties
    - Spin Hall effect experiments and modeling
- Points to initial success in focusing the science towards switch technology
  - Get the right information early to direct research on most promising path
  - From industry member at INDEX review (9/08): "NRI experiment is working; we learned more about graphene for device applications in the last 2 years than we would normally learn in 5 or 10 years in the business-as-usual research model."

Industry Support of NIST's Involvement

- "NIST joining NRI enabled the recent expansion of the program, and also was instrumental to convincing the NRI industry members to extend their commitments for funding the program beyond 2008, so this partnership has already resulted in increased support for the program."
  -- Jeffrey Welser, Director of the Nanoelectronics Research Initiative

- "There is tremendous interest in every part of the world to win the nanoelectronics race and reap the economic rewards that will go with it. For America to win, it will take radical collaboration between government, higher education and industry. The best example of this type of collaboration is the important work going on in the Nanoelectronics Research Initiative at more than 30 universities with funding and participation from NIST, IBM and other major semiconductor and research institutions."
  --John E. Kelly III, IBM Senior Vice President and Director of Research

- "The research results from this new initiative will enable the semiconductor industry to extend Moore's Law -- the 40-year-old prediction that the industry can double the amount of transistors it places on a computer chip every couple of years -- far beyond the year 2020 when the potential limits of the current industry technology may be approached."
  -- Larry Sumney, President and CEO of the Semiconductor Research Corporation

- "The Nanoelectronics Research Initiative (NRI) and the regional research centers exemplify what can be done when industry, government and academia work together. This investment is likely to pay substantial dividends in the future. Leading-edge university research centers have proved to be powerful magnets for investment by technology companies and will help build the high-tech ecosystem for high-value jobs in the future."
  -- George Scalise, President of the Semiconductor Industry Association

NRI Technical Directions

- Grow NRI as a strategic *goal-oriented*, *basic-science* research program
  - Expanded focus on specific key areas in the first three research vectors:
    - Devices with alternate state variables – emphasis on new, *non-spin* options
    - Device-to-device communication of alternate state variables
    - Non-equilibrium computation systems
  - Expanded focus on combining these 3 vectors for logic gate implementations
    - Still want more ideas on novel computational architectures
  - Expanded modeling to extrapolate both device and computation "gate" potential characteristics
    - Increased focus on nano-metrology to link theory to experimental work

- Create set of benchmarks / report card to assess device potential for new technologies compared to "ultimate CMOS"
  - Tailor assessment appropriately for stage of research, leading up to "logic gate" evaluation
    - New phenomena: operation temperature, on/off ratio, energy dissipation, etc.
    - More advanced device ideas: speed, area, gain, communication, etc.
  - Benchmarking working group led by MIND center started 6/08

Continuous Research to Product Evolution

Research Focus

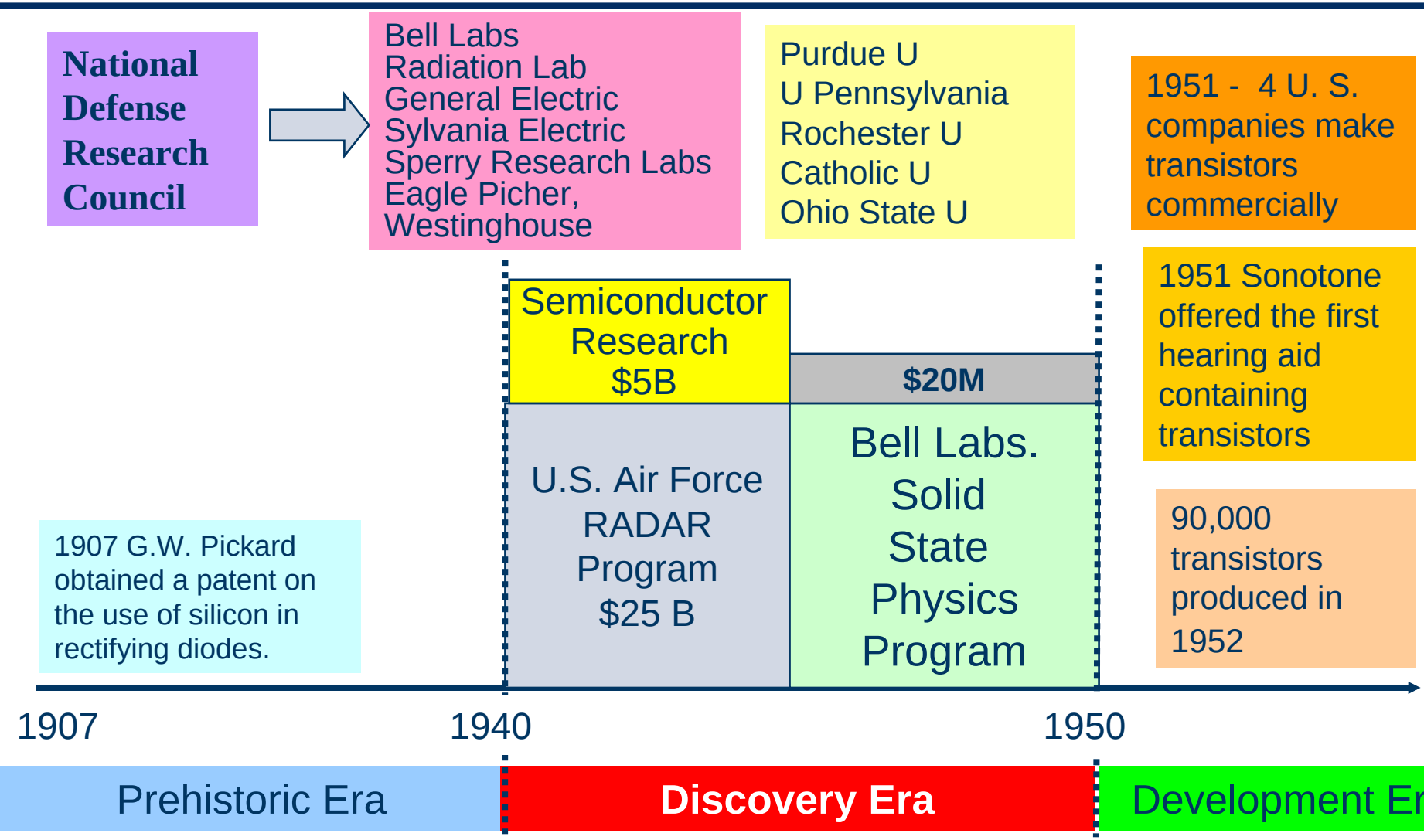
- "Thousand Flowers Bloom" (2005-2010)
  - Projects: Many, moderate size, new science/technology ideas
  - Results: Science, new materials/structures knowledge, initial device demos, opportunities for early introduction of spin-off technologies and product innovations
- "Cultivating Flowers" (2010 and beyond)
  - Projects: Expanded work on 2-3 promising devices/architectures, larger-scale prototypes
  - Results: Prove-out technologies before transfer to advanced R&D (FCRP/GRC/Industry), more rapid uptake of technologies into products

Program Management

- Continue to organize work into multi-university centers
  - Maintain balance between sufficient autonomy for new idea generation and guidance towards a practical device – strong interaction with industry assignee / liaison teams
- Continue to partner with states to expand existing centers and create new centers
  - Target states with nanotechnology infrastructure initiatives and technical match
- Expand program with Federal and state partners in three areas:
  - Expand direct Fed-Ind partnership on post-CMOS nanoelectronics
  - Expand Fed and state investements in nanoelectronics infrastructure at universities
  - Expand interaction with national labs and encourage funding for one-of-a-kind tools

From Vacuum Tubes to Diodes

The cost of Inventing the Transistor



(2004 Dollars)

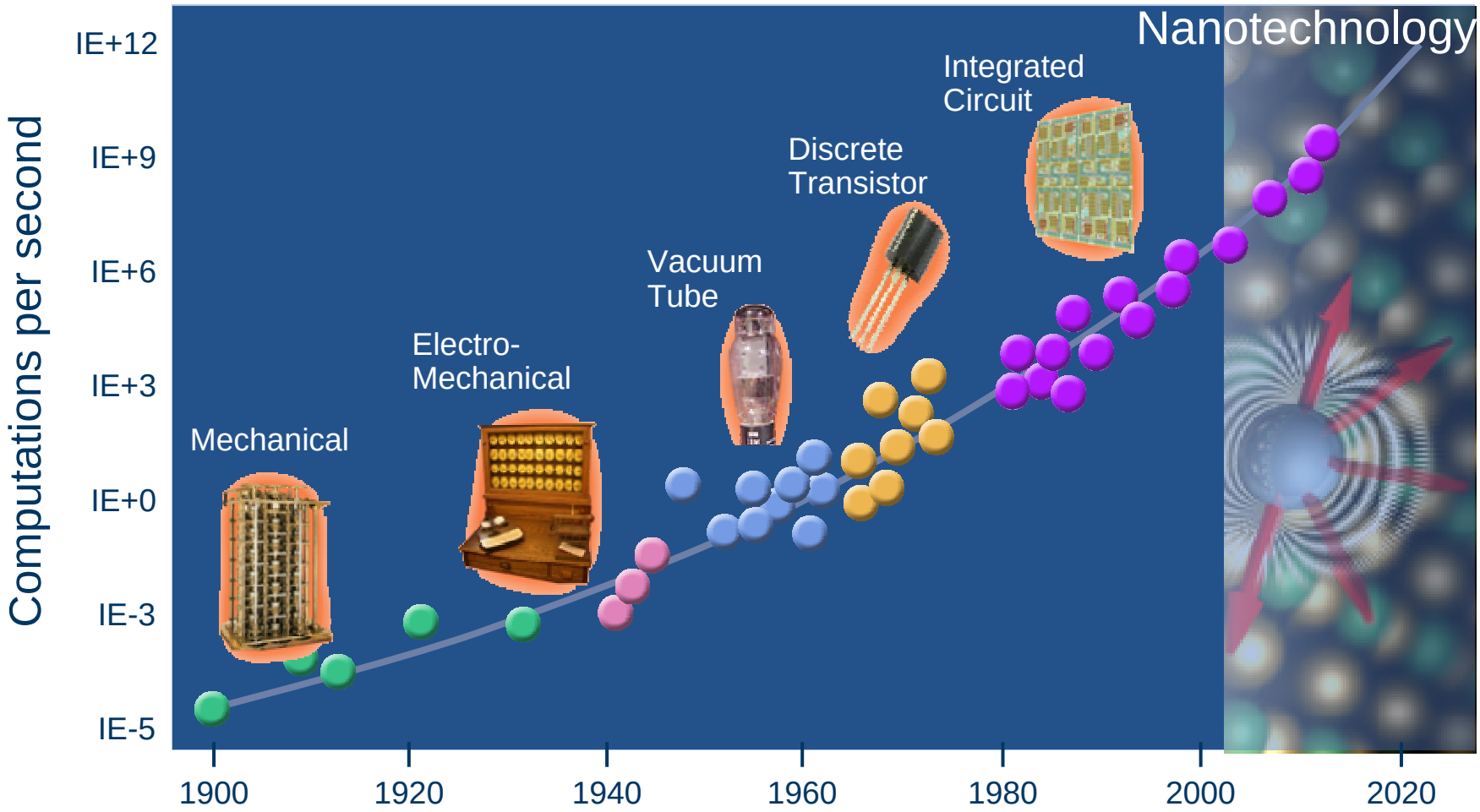
Ralph Cavin and Victor Zhirnov, Semiconductor Research Corporation, 2006

Summary

- Power will continue as the principal scaling issue all IC applications
  - CMOS will continue to scale over at least the next decade, with emphasis on utilizing increasing transistor density over increasing frequency
- Continuing the trend of increased function / dollar is critical to maintaining the exponential growth of our IT-based economy
  - The country/state/companies that find the “next switch” first will likely dominate the Nanoelectronics Era the way the U.S. has dominated the Microelectronics Era for the past half century
- Similar to the vacuum tube to transistor transition in the 1940-50’s, Industry – government – academia partnership is crucial to success
  - Funding and focusing basic research at universities and national labs to find a new device to scale beyond CMOS by 2020
  - Building up nanoelectronics infrastructure leadership at U.S. universities
  - Training the next generation of science & engineering students
  - Rapidly commercializing new technology as it is discovered

NRI Goal: Continue the Curve . . .

$1000 Buys:



Source: Kurzweil 1999 – Moravec 1998

Questions? More Information?

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