Ions and Chemistry to Fulfill Observation and Probing Specifications of sub-28nm devices

G. Goupil[1], P. Gounet[2], C. Hollerith[3], F. Altmann[4], S. Brand[4] and A. Delobbe[1]

[1] Orsay Physics/Tescan Orsay Holding, Fuveau, France [2] ST Microelectronics, Grenoble, France [3] Infineon Technologies AG, Neubiberg, Germany [4] Fraunhofer Institute IMWS, Halle, Germany

INTRODUCTION

Physical failure analysis (PFA) of ICs is an integral part of the device analysis to pinpoint physical defects and identify failure mechanisms arising from fab-related process issues. The process flow for PFA on aggressive Back-End-of-Line (BEOL) scaling technologies involves a repetitive procedure of chip deprocessing, visual inspection under optical / electron microscopes, followed by defect isolation by electrical methods such as probing or by other innovative technics such as Scanning Acoustic Microscopy (SAM).

AIM OF THIS WORK

As process nodes scale down further, deprocessing via manual polishing has become very challenging due to shrinking of the critical dimensions for metal interconnects and transistors leading to global reduction of spacing between metal layers. Alternatively, traditional milling using purely focused or broad beam ion beams is insufficient in achieving planar delayering surface due to the varying etch rates of materials.

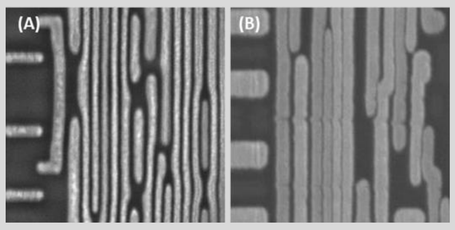
Plasma Focused Ion Beam (PFIB) delayering is a promising technique used to sputter metal and dielectric materials present in the IC chips. By adjusting beam parameters, a large panel of sample preparation can be achieved. As a result, the technique enables a site-specific, artifact-free uniform large area delayering for advanced node semiconductor devices.

Gas-assisted etching (GAE) is a very useful extension of the PFIB technique. With the introduction of reactive chemical precursors, a FIB is able to control the etching effect on selected regions.

In SC field, the target area includes a mixture of copper/tungsten and dielectric layers. Direct delayering of such devices would produce an inhomogeneous surface topography. The idea of injecting a specific precursor during delayering is to uniformly smooth the floor in the milled target area by milling the copper at substantially the same rate as the dielectric.

To date, 3 new precursors developed by TESCAN ORSAY HOLDING have shown good results for planar deprocessing using PFIB:

NanoFlat, **A-Maze** and **Chase**

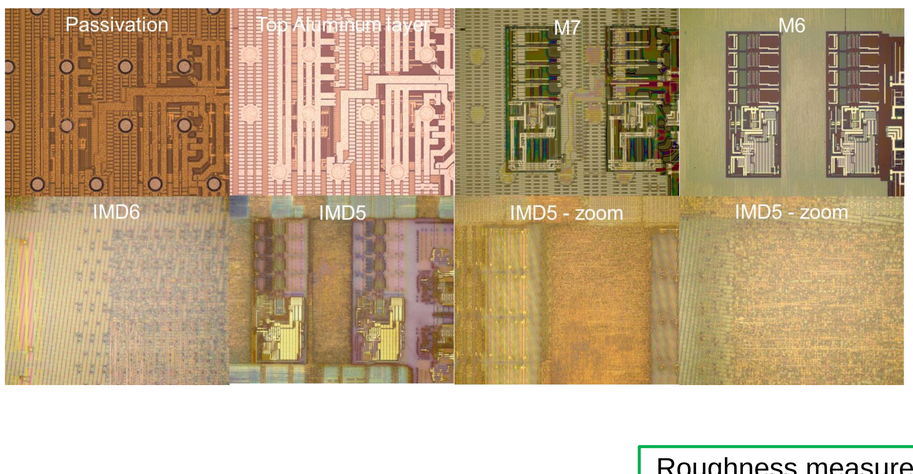


Topographical comparison of (A) plasma FIB's artifact-free delayered surface vs (B) smeared surface from mechanical polishing.

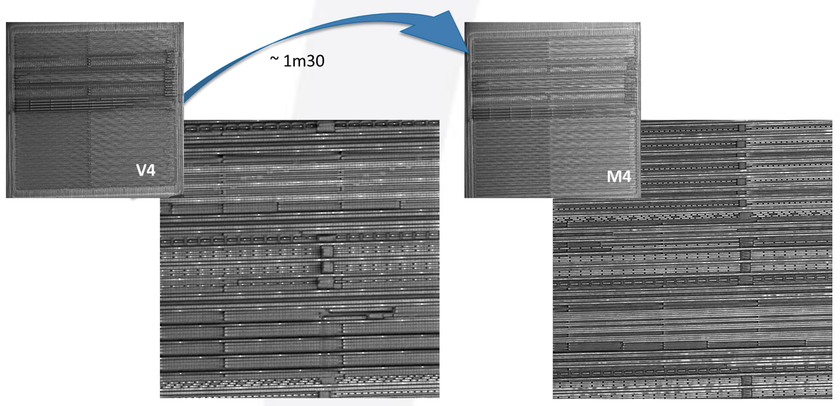
DELAYERING AND PROBING

SAMPLE PREPARATION:

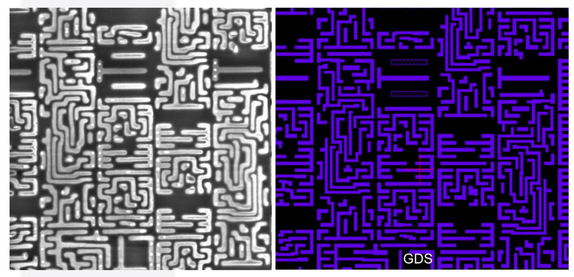
Die was first delayered up to IMD5 by dry & wet chemistries to speed up the process



FIB Process parameters: Xe+ ion beam at 15 kV, 3.2 nA for all layers



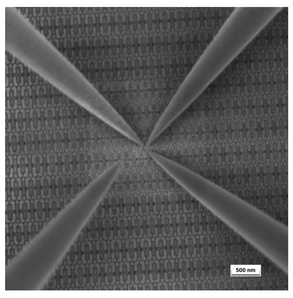
Metal 1 Observation



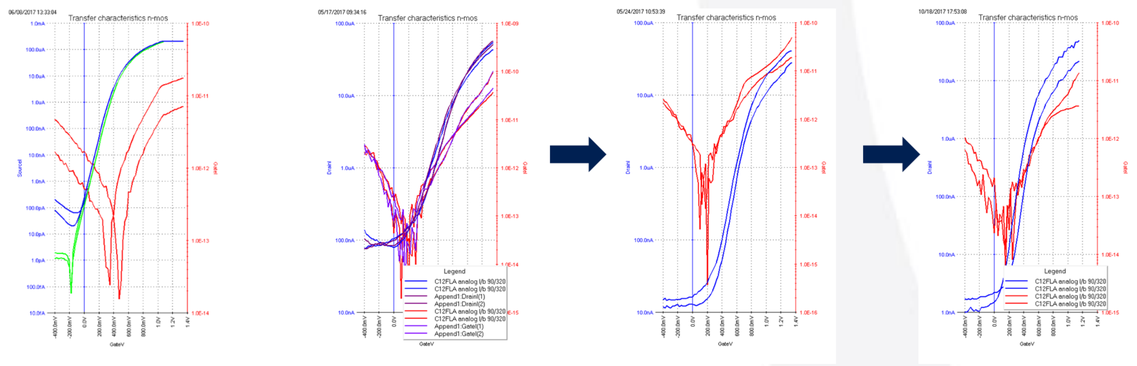
Roughness measurements were conducted on the sample by the mean of AFP technic & system
Max value is at **10nm** – after 3 microns deprocessing

ELECTRICAL MEASURMENTS

Off current measurements realized to estimate the impact of the deprocessing process were performed using Nanoprobing.

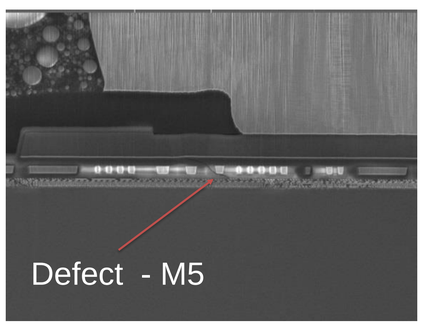


500 eV SEM image of transistor layer with nanoprobes



After optimization of the process, nearly no modification of the electrical behavior of the transistor layer appears due to the sample preparation

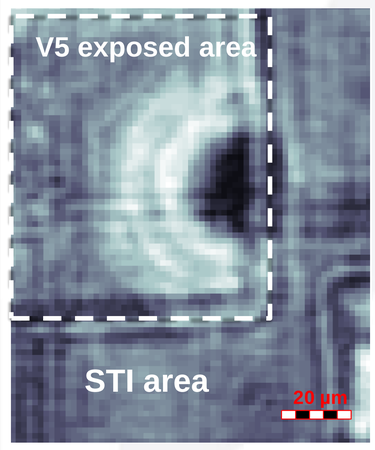
SAM OBSERVATION



A series of samples presenting a known defect in M5 below a solder bumps were tested. Due to the morphology of the bump, it is often difficult to remove it without creating topology artifacts on the milled surface or mechanical stress.

For this test, the sample was backside chemically polished until the STI layer and then delayered by FIB-GAE stopping in V5 (before the failure). Scanning Acoustic Microscopy done with a 1GHz lens studied at the IWMS-CAM institute have been taken on the prepared area.

The bump and defect are clearly visible with 1 Ghz lens inside the delayered box. Outside it cannot be recognized with this frequency
The preparation shows a much improved image: Bump visible but there is still much influence of the metallization between the defect and the final layer reached during the process.



CONCLUSION

- FIB sample preparation is one of the most precise and reliable technic to reach, with the best accuracy, deeply buried region of interest at the nanometric-scale.
- Alone, the FIB cannot reach the final roughness homogeneity necessary to make accurate observation or probing measurements. GAE with the good chemistry regulates the milling rates of the different materials of the circuits to reach a 1:1 selectivity and a final roughness close to a perfect planarity.
- Milling process recipe optimization does not create surface alteration and electrical modification of the semiconductor.
- Thus it was shown that also with PFIB delayering image quality can be significantly improved for surface sensitive observation such as with 1GHz SAM