Semiconductor Performance under Reverse Transient Overvoltages

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Significance
Part 5 –Monitoring instruments, laboratory measurements and test methods
Part 7 – Mitigation techniques

This declassified report is one of several prepared in the early sixties when industry was awakening to the sensitivity of semiconductors to transient overvoltages. Under the reprint number shown above, it is a re-issue of an earlier report, with restricted circulation within GE, dating back to 1963 and covering research on the subject performed in 1961 and 1962.

One of the findings was that the so-called PIV rating of a diode or thyristor did not reflect its transient withstand capability, hence the attention focused on that issue in this report. At that time, circuit designers afflicted with field failures attempted to mitigate the problem by selecting semiconductors with higher PIV rating – which proved to be an expensive illusion.

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SUMMARY: Reverse transient voltage pulses were applied to five types of selected semicondutors until failure occurred.

A number of test conditions were used, including fast and slow rise pulses, room temperature and high temperature, steady-state current flowing or not flowing at the time of surge application.

Within each type of device, various groups were tested with different PIV ratings, or avalanche voltage class and aging or no aging.

The results, covering two noncontrolled avalanche diodes and one controlled avalanche diode, plus two types of SCRs show the following:

1. There is no correlation between the voltage rating (PIV) and the withstand capability under transient conditions.
2. Aging does not affect conclusion 1, nor does it substantially decrease the withstand capability.

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KEY WORDS: PIV, overvoltages, transients, semiconductors, breakdown

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Electronic Physics Laboratory

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Introduction

The behaviour of semiconductors under reverse transient overvoltages, and especially their failure levels, has been investigated during the two previous years under the Transient Overvoltage Pooled Program.

One of the most interesting conclusions reached after testing several types of devices was that the PIV rating of the device was not a significant indication of the withstand capability of this device beyond its rating. In other words, an increased PIV was not a guarantee of a higher transient withstand capability. With hindsight, this may now appear obvious; however, questions were still raised on the general validity of this conclusion.

Therefore, the test program reported here was undertaken for the purpose of verifying this lack of correlation on a greater number of types, and also to investigate if it would remain valid after ageing, such as that produced by high temperature storage.

Test Results and Discussions

Tests and discussions leading to specific conclusions are grouped in five separate sections of this report, corresponding to the three types of rectifiers and two types of SCRs included in this program. General conclusions are summarized below.

Conclusions

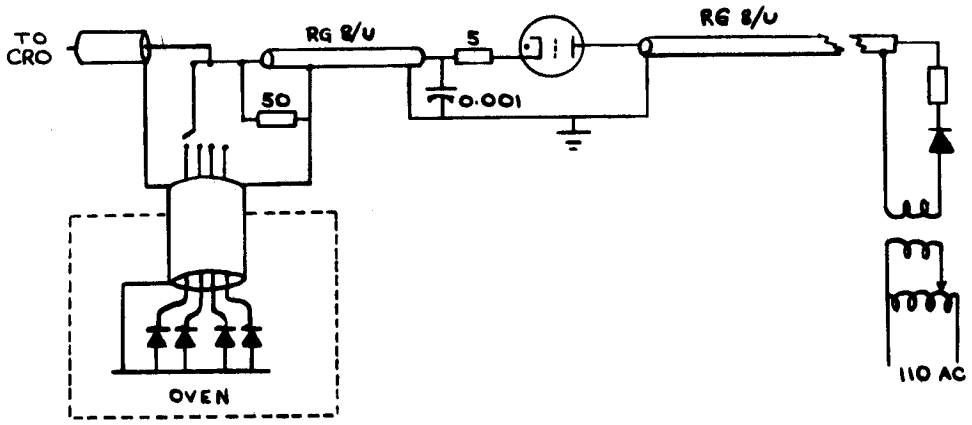
1. The PIV rating or the voltage class of an avalanche device does not offer a valid indication on the transient withstand capability beyond the rating.

2. This conclusion is likely to be valid for all semiconductors under the present system of ratings, and is not affected by factors such as ageing and temperature.

Tests on 4JA10 Rectifiers

Summary of Tests

Test Samples:	200 volts and 400 volts PIV units, aged and unaged
Tests:	Reverse transient with no bias, to failure
Results:	Neither PIV nor ageing significantly affect the failure level



Notes: 5 ohm - 0.001 RC to reduce overshoot

Connection of probe 18" from test piece required for hot oven, but checked against connection at test piece with open-door oven.

Tests on 4JA10 Rectifiers

1. Purpose of the Tests

Limited tests (63GL133) on new samples of these diodes had shown that the "TIV" did not seem related to the "PIV" of the diode. Therefore, a larger group of samples were obtained in order to conduct a planned experiment to show the effect of the PIV rating on new as well as on aged samples.

2. Test Specimens

Four groups of A10 rectifiers were obtained from the Rectifier Components Department. First, two groups were obtained by precise voltage grading, 200 and 400 volts PIV. Then, half of each group was aged by storage at 200°C for 1000 hours (with little effect on the characteristics), followed by 500 hours at 225°C which produced a significant shift of the characteristic as tested on the production line. In this manner, a direct comparison is possible between aged and unaged devices of the same voltage class, as well as comparisons between voltage classes, aged or unaged.

3. Test Procedure

The reverse voltage pulse was supplied by a square pulse generator consisting of a coaxial cable discharged into a resistance equal to its surge impedance (see sketch). Since the high voltage probe for measuring the voltage across the diode could not withstand the oven temperature, it was connected immediately outside of the oven, at the selector switch. However, comparison of the voltages there and directly across the diode (with a cold oven) showed no significant difference. The RC network at the thyratron was added to minimize the overshoot on the front of the square pulse due to the necessary cable length between the thyratron and the oven.

This diode does not exhibit any reverse avalanche phenomenon under reverse voltage. The voltage of the applied wave was raised after each pulse application

by steps of 100 volts, and the voltage at which failure occurred recorded.

Tests were made with 25°C and 150°C ambient on the four groups, and the results are tabulated below. Failure was on the surface of the junction.

	200 Volts	200 Volts, aged	400 Volts	400 Volts, aged
25°C Ambient Test Points	1000	900	1100	1000
	1100	1100	1100	1000
	1200	1000	1000	1200
	1100	1000	1300	900
	1000	1000	1000	1000
	1000	900	1000	1100
	1100	1200	1100	900
	1100	1000	1200	1000
Avg.	1075	1010	1100	1050
150°C Ambient Test Points	1700	1600	1900	1700
	1700	1700	2000	2000
	1700	2000	1700	1700
	1800	1600	1800	1700
	1900	1700	2000	1800
	1700	1800	1900	2000
	1800	1900	1900	2000
	2000	1700	1800	1900
Avg.	1800	1750	1875	1800

Testing the eight averages of these test groups against each other, or grouping for instance all 400 volts units on one hand and all 200 volts units on the other hand or all aged versus all unaged show that the differences are significant at the 5% level and generally at the 2% level.

Nevertheless, the differences in the averages are small.

I have no explanation to suggest for the increase in withstand voltage when the test temperature is increased from 25°C to 150°C. In order to show a possible effect, 2 of each group of diodes were baked for 30 minutes at 150°C (approximately the time required to insure stabilization of the oven and junction temperatures), then brought back to 25°C and tested. The failure levels for each group was not significantly different from the level found at 25°C without prior heating.

Comments from the Rectifier Components Department suggest that this may be due to higher bulk leakage and avalanche, although contrary to steady-state surface quality-temperature relationships which they have observed.

Another way to present the results of these tests is to express the averages in percent of each other. This yields the following comparisons:

1. Effect of PIV Rating

New Units	200 Volts PIV Withstand Level (index)	400 Volts PIV Withstand Level
At 25°C	100%	102%
At 150°C	100%	104%
Aged Units		
At 25°C	100%	104%
At 150°C	100%	104%

2. Effect of Aging

200 Volts Units	Unaged Units Withstand Level (index)	400 Volts PIV Withstand Level
At 25°C	100%	94%
At 150°C	100%	97%
400 Volts Units		
At 25°C	100%	95%
At 150°C	100%	95%

3. Effect of Temperature

New Units	Withstand Level at 25°C (index)	Withstand Level at 150°C
200 volts	100%	167%
400 volts	100%	170%
Aged Units		
200 volts	100%	173%
400 volts	100%	172%

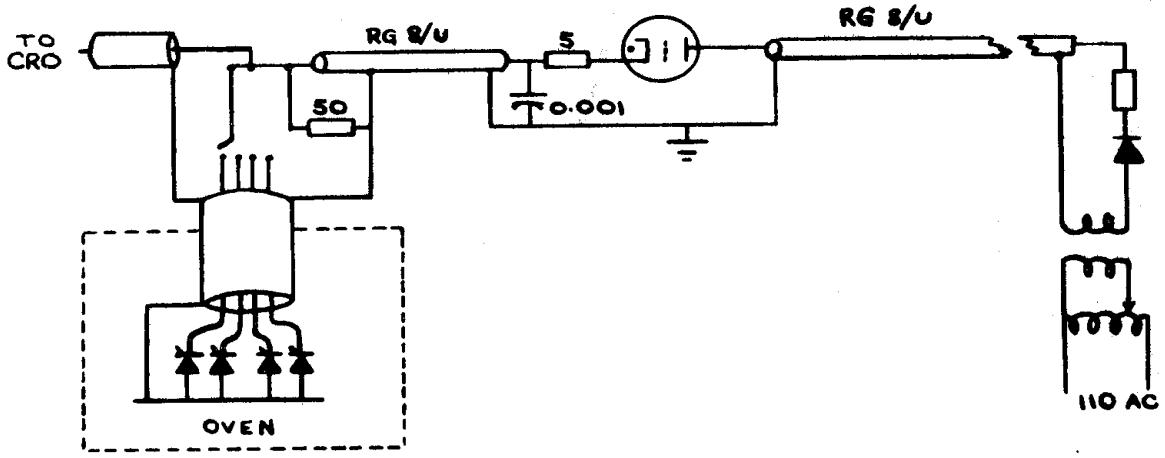
Summary

1. Increasing the PIV from 200 V to 400 V increases the withstand level by no more than 4%, aged or unaged, at 25 or 150°C ambient.
2. Ageing by storage at 225°C for 500 hours decreases the withstand level by no more than 6% 25 or 150°C, 200 volts or 400 volts.
3. The withstand level at 150°C ambient is 170% of the level at 25°C ambient, 200 volts or 400 volts, aged or unaged.

Tests on C20 SCR's

Summary of Tests

Test Samples:	100 and 400 volts PIV, aged and unaged.
Tests:	Reverse transient with and without bias.
Results:	The device exhibits avalanche characteristics but fails at the surface. Neither PIV, ageing or bias affect the failure level.



Notes: 5 ohm - 0.001 RC to reduce overshoot (see unloaded generator oscillogram #1 next page)

Connection of probe 18" from test piece required for hot oven, but checked against connection at test piece with open-door oven.

Tests on C20 SCRs

1. Purpose of the Tests

Following earlier tests (TIS 63GL144) on this device, it appeared worthwhile to also investigate for this device the possible effect of ageing. In addition, no tests had been performed on the SCR during conduction; in view of the substantial reduction of the withstand capabilities when conducting observed on some diodes,[1] this also seemed to warrant investigation.

2. Test Specimen

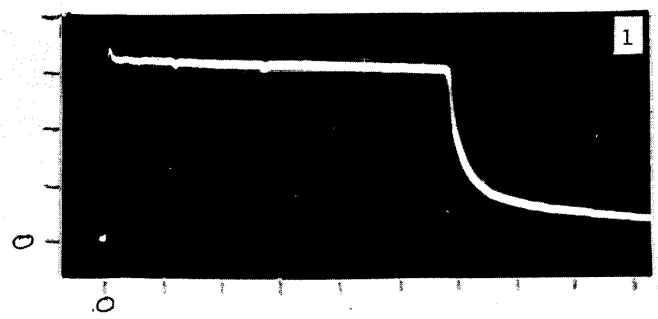
Four groups of C20 SCRs were supplied by the Rectifier Components Department. First, two groups were obtained by precise voltage grading, C20A and C20D. Then, half of each group of A's and D's were "aged" by storage at 200°C for one week, in order to produce a significant shift in the device characteristics as tested at the production line. In this manner, a direct comparison is possible between aged and unaged devices of the same voltage class, as well as comparison between voltage classes, aged or unaged.

3. No-Load Tests

A first test series was performed by applying reverse voltage pulses to the SCR without any steady-state voltage or current.

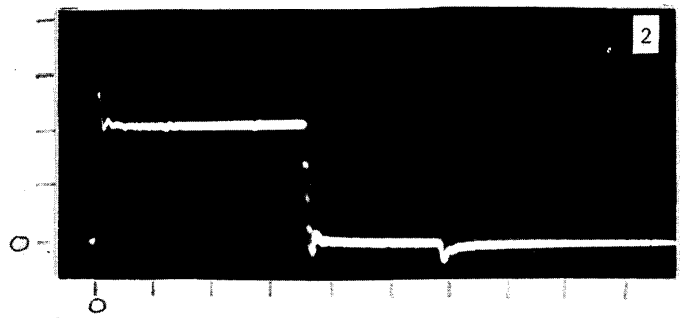
The pulse was delivered from a square pulse generator consisting of a coaxial cable discharged into a resistance equal to its surge impedance (see sketch). In contrast to the capacitor discharge test wave used previously,[4] this delivers a pulse with a flat top following a finite rise time instead of the exponential decay in the tail of the capacitor discharge. At voltages close to the anticipated knee of the reverse characteristic (which earlier tests indicated)[4] this should cause a more constant current flow, holding the voltage at one point of the curve.

First, single pulses were applied, with increasing voltage amplitude, until failure of the device was observed, as shown by a "chop" of the voltage wave.

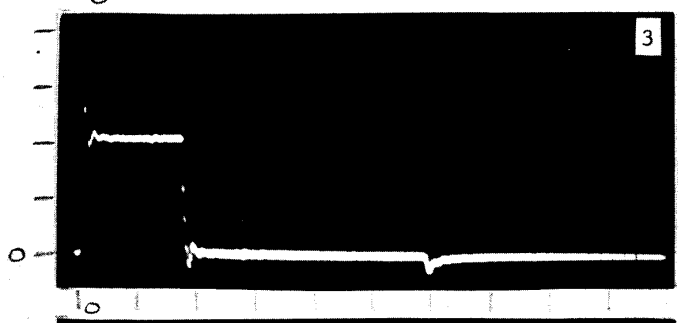


Output of unloaded generator
1600V x 6 μs pulse

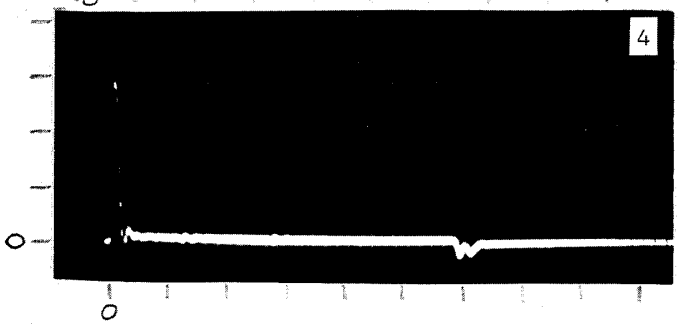
Vertical: 500V/div.
Horizontal: 1 μs/div.
(same settings for all osicllograms on this page)



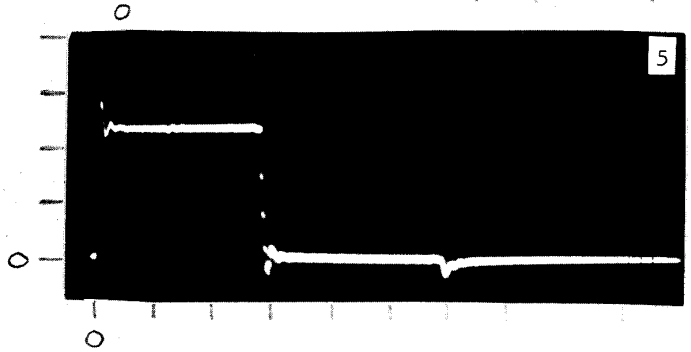
Failure of a C20A SCR in 3.8 μs, while voltage was clamped at 1050 volts.



Failure of a C20D SCR in 2 μs, while voltage was clamped at 1000 volts.



Failure of a C20D SCR in 0.1 μs, before avalanche could produce any voltage clamping.



Failure of a C20A SCR (aged by high temperature storage) in 3 μs, while voltage was clamped at 1200 volts.

With this test procedure, the onset of avalanche is quite apparent as the voltage recorded across the device stops increasing from shot to shot while the generator voltage is still increased. This approach normally produces the failure level corresponding to the minimum voltage and maximum time to failure.

A second test procedure consisted in pre-setting the output of the pulse generator at values above the minimum determined in the first series. Presumably, this could produce failures at higher levels corresponding to shorter times to failure.

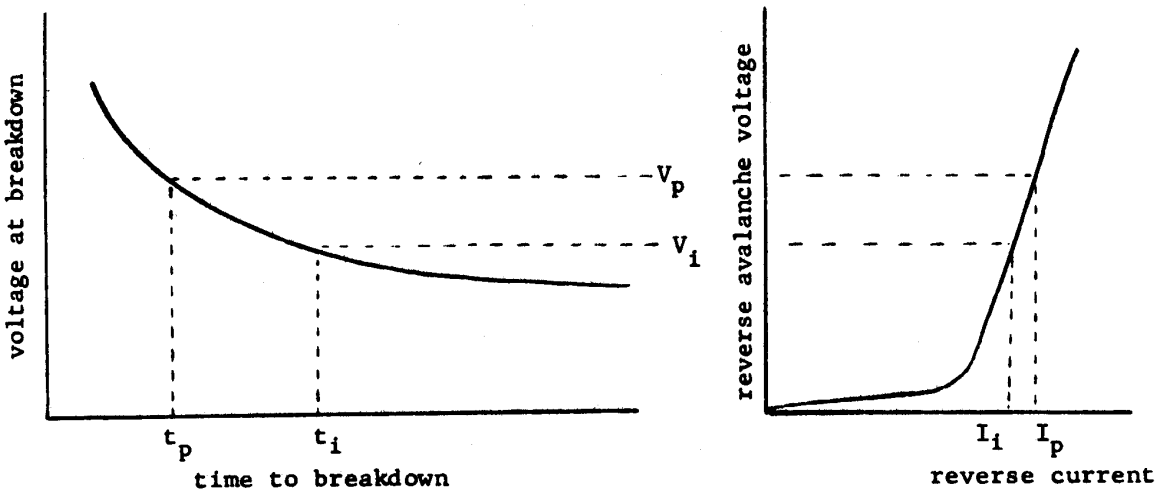
Both of these test methods were applied on all four groups of test pieces. Furthermore, two series of tests were made with a 25°C ambient and a 100°C ambient.

The failure level and time to failure are tabulated below. Typical test waves are also shown in the test oscillograms, corresponding to a preset voltage of 1600 volts, a duration of 6 μs, and a rise time of 0.1 μs on all oscillograms shown.

4. No-Load Test Results

	Test Sample	C20A	C20D	C20A Aged	C20D Aged
		volts and time to failure in μs			
	Test Condition				
25°C	Increasing pulse	1100 6	1000 5	1000 6	900 6
		1100 5	1000 6	900 5	1100 6
		1000 4	1100 4	1000 5	1000 5
		1110 5	1100 5	1100 4	1100 5
	Preset 1600 V	--- .1*	1000 5.5*	1100 4*	1000 .5
	6 μs	1000 2	--- .1*	1000 .2	1000 3.5
		1000 4*	1000 3	--- .1*	--- .1
100°C	Preset 1400 V (3 μs long only)	no failure	no failure	no failure	--- .1
	Preset 1600 V (1)	1050 3.8 (2)	1200 2.5	1000 3.8	1100 5
	6 μs	1100 2.5	1000 2 (3)	1000 4.5	1200 3 (5)
		1000 3	--- .1 (4)	1200 3	1100 2.5
	Preset 3200 V	--- .1	1100 .8	--- .1	--- .1
	6 μs	1000 .9	1100 .9	1100 .2	--- .1

--- Indicates failure before onset of avalanche.
* These samples were dissected after failure--see discussion below.
(1)-(5) indicate oscillograms of failures on opposite page.


voltage at breakdown
V_p
V_i
t_p
t_i
time to breakdown
reverse avalanche voltage
I_i
I_p
reverse current

5. Discussion of the Results

The avalanche effect in the SCR, although neither deliberate nor advertized as such is effective in clamping the voltage appearing across the device and will reduce the risk of flashover, or breakdown of the surface. However, it is apparent that the time to failure, at the voltage corresponding to the avalanche, can be quite short. Thus, the effectiveness of this avalanche is rather limited. On the other hand, it makes it rather difficult to select a quantitative criterion of the ability of the SCR to withstand reverse transients in the failure range.

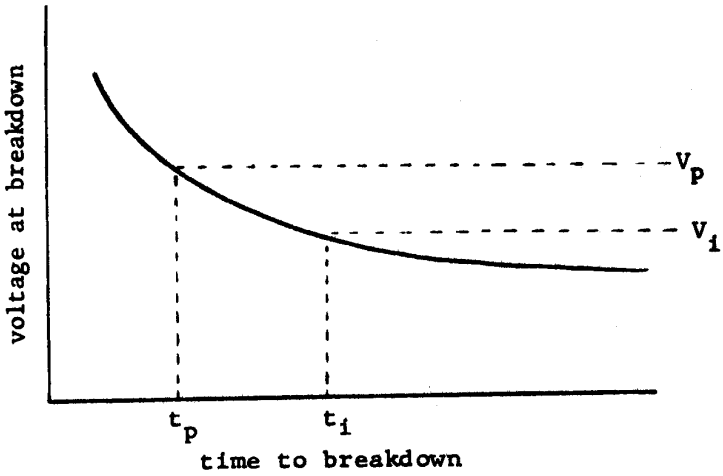
In order to investigate the possibility that the very short time to failure observed or some samples could be the result of a different breakdown mechanism, six cells were carefully examined by RCD. These units are marked (*) in the test result table, and were selected in each of three groups to include a 0.1 μs time to failure and a time to failure over 4 μs/ However, no correlation was found between the time to breakdown and the type, degree or location of the failure. All were due to surface arcing.

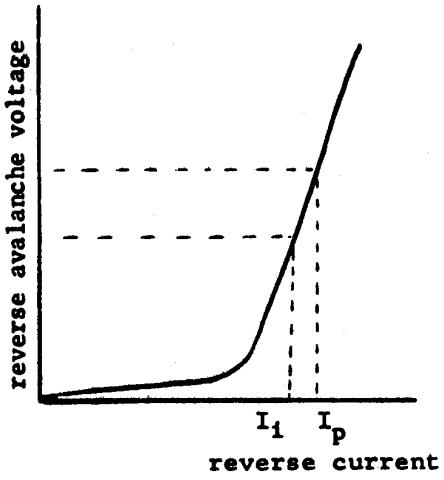
Inspection of the test results reveals some significant points.

1. • The increasing pulse approach produces the longest time to failure, with voltages somewhat lower than the preset pulse approach.

   • This is not surprising as this method, although bringing the device into the avalanche state, does it with the minimum current. This means that the voltage is somewhat lower on the Zener characteristic than it would be for the higher preset condition. Thus, breakdown of the surface dielectric corresponds to the right part of its volt-time characteristic.

   This is shown in the sketch on the opposite page. A hypothetical curve for the breakdown of the surface insulation and a zener curve for the reverse avalanche are drawn. Consider two currents I_p and I_i,


voltage at breakdown
V_p
V_i
t_p
t_i
time to breakdown


reverse avalanche voltage
I_i
I_p
reverse current

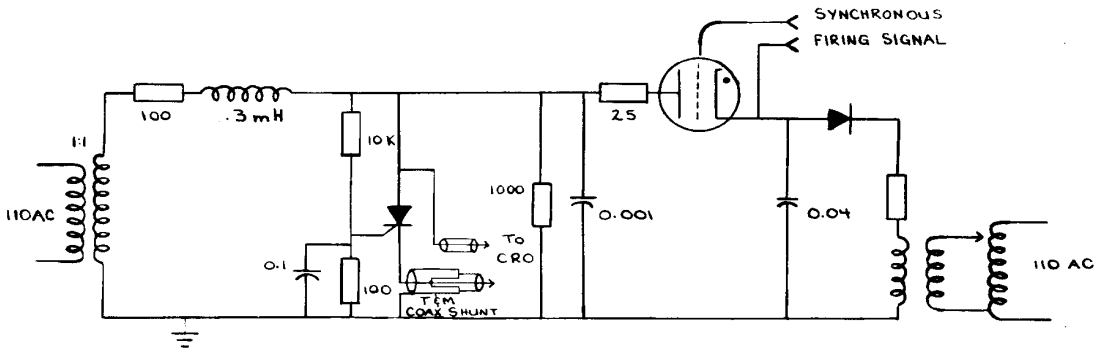
respectively for preset and increasing pulse methods, producing the corresponding avalanche voltages V_p and V_i. These voltages will in turn cause breakdown at the times t_p and t_i, with t_i longer for the lower I_i than t_p for the higher I_p.

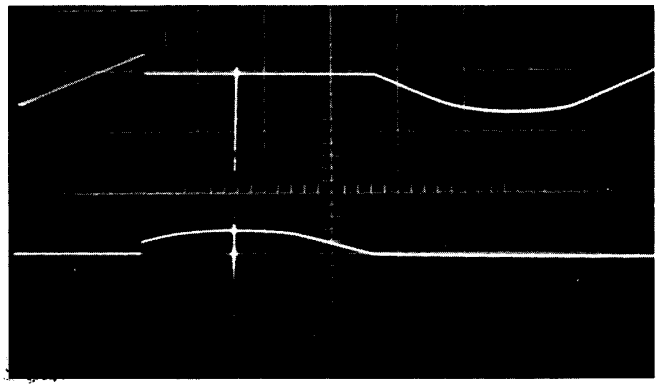
- As a result of this, low voltage preset pulses of short duration may not cause failure of the device.

2. There is no significant difference in the time to breakdown observed here for the A's or D's or for the aged or unaged SCRs. Even if there were, as reported in 63GL144, the practical value of this difference would be cancelled by the fact that short time failure (0.1 μs) can and does happen in any group, so that the average time to breakdown is meaningless.
3. The avalanche voltages observed at 100°C tend to be higher than those at 25°C (not on the same devices). This is due to the fact that the thermal vibration of the semiconductor lattice increases with temperature and acts as a brake on the carriers, so that a higher accelerating field, i.e., the avalanche voltage, is required to maintain the avalanche state.
4. Increasing the preset voltage value tends to shorten the time to failure, which means that as the corresponding point climbs on the zener characteristic to slowly increase the avalanche voltage, the failure point of the surface dielectric moves towards the left on its ascending volt-time characteristic.

6. Conclusions From No Load Tests

For reverse transients such that the avalanche voltage of the device can be reached or even exceeded, there is very little if any difference in the performance of the four groups of SCRs. Specifically, this means that the PRV rating of these devices does not reflect a difference in the ability to withstand surges beyond their ratings, and that this conclusion is not affected by ageing of the device.



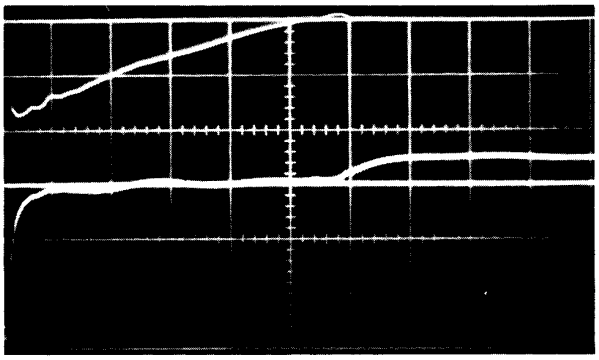


Timing of Reverse Transient

Top Trace: voltage across SCR with transient applied during conduction

Bottom Trace: Current in SCR with current reversal but no turn off

Sweep: 2 ms/div.



Same as above except 1 μs/div. with sweep triggered by reverse voltage transient and zero lines added

7. Tests With Steady-State 60 cps Voltage Applied

Earlier tests (62GL191) have shown the substantial reduction of the withstand capabilities of diodes when the reverse transient is applied during conduction. Similar results are also reported by Chowdhuri. [5]

7.1 Tests with Capacitor Discharge

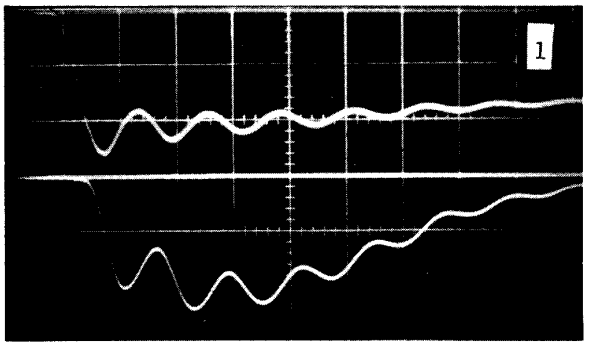
In order to apply this type of transient to the SCR, the test circuit sketched on the opposite page was first used. It is similar to the circuit suggested in AIEE standard #59 for the measurement of reverse recovery time. [8] A steady-state 60 cps voltage is applied across the SCR, which is turned on soon after the start of the forward voltage when the gate is fired from the 100-10 K divider. A capacitor charged by a DC supply is discharged into the combination of the output capacitor, resistor and test piece, when the thyratron is turned on by a synchronous firing circuit. Forward current is limited by the 100 ohm resistor, and the pulse is blocked from the 60 cps supply by the 0.3 mH choke.

The first oscillogram shows timing of the reverse transient to coincide with the peak of the forward current (the trace brightener of a Tektronix 535 was used to record the otherwise invisible spike at this slow sweep rate, even with repetitive shots).

The second oscillogram shows at a high sweep rate the applied reverse voltage transient and the resulting reverse current in the SCR, with forward current resuming as soon as the reverse transient has vanished.

In these two oscillograms the voltage amplitude was held below the avalanche region, so that negligible current flows after the initial reverse recovery period.

The effect of timing on the device behaviour is illustrated by the oscillograms on the next page. There were all recorded with a voltage output of the surge generator sufficient to drive the SCR into avalanche.



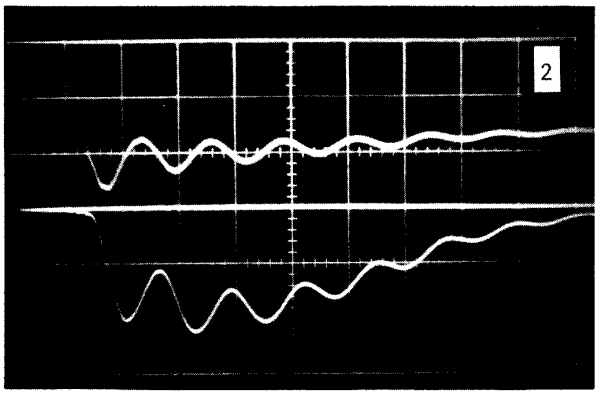
All Oscillograms:

Top Trace: Voltage across SCR
500 V/div.

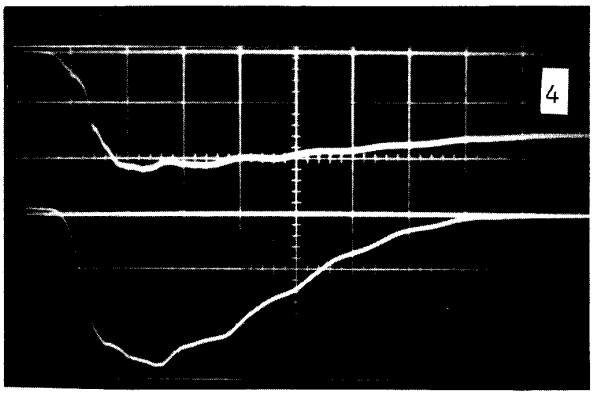
Bottom Trace: Current through SCR
20 A/div.

Sweep: 0.1 μs/div (repetitive)

No steady state 60 cps voltage

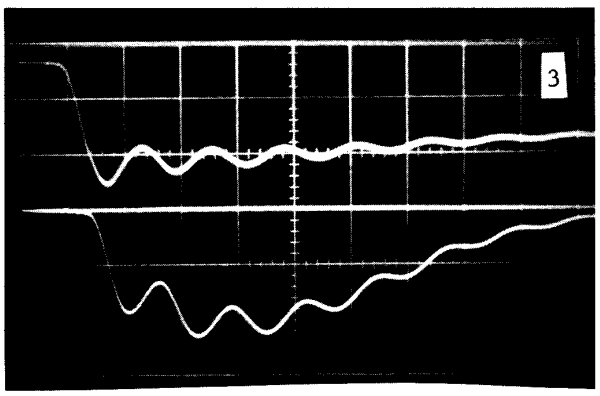


No forward current (gate open)

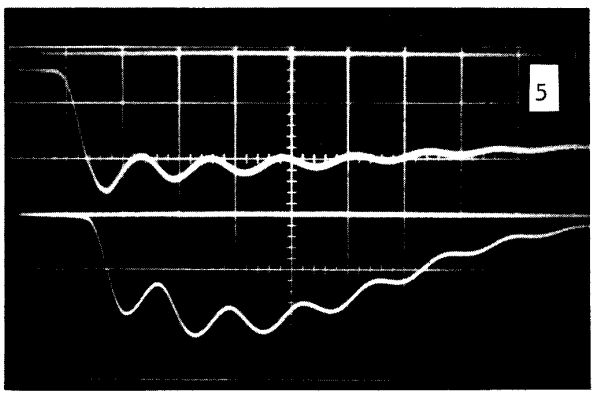


Forward current flowing at start of surge

Surge applied at peak of forward 60 cps voltage



No forward current (gate open)



Forward current flowing during alternate ½ cycle

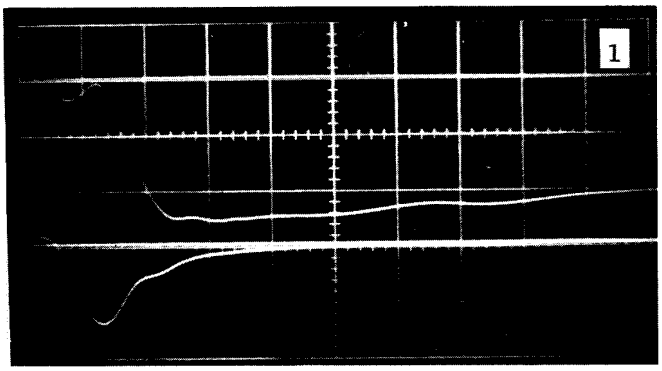
Surge applied at peak of reverse 60 cps voltage

Oscillograms 1, 2, 3, 5 corresponding to surge application at various times but not during forward conduction all exhibit the same general appearance. The voltage trace starts above, at, or below zero depending upon the value of the 60 cps voltage applied at the time of the impulse, but the current is not significantly affected. The apparent oscillations of the current and voltage traces are most likely due to the combination of natural frequencies in the circuit with the swinging of the current and voltage on the Zener characteristic.

Oscillogram 4 corresponds to impulse application at the peak of forward current (condition shown on previous page, note the current trace starting above zero). It differs significantly in that the initial current rise is steeper, the current is larger and the large oscillations absent. The Zener effect is quite apparent between .1 and .4 μs where the current changes 2:1 with only a 10% change in voltage.

These oscillograms show that while there is a difference in the response of the device, the ultimate performance under transient conditions, within the limitation of rise times longer than 0.1 μs, will still exhibit the voltage clamping effect of the avalanche characteristics of the device.

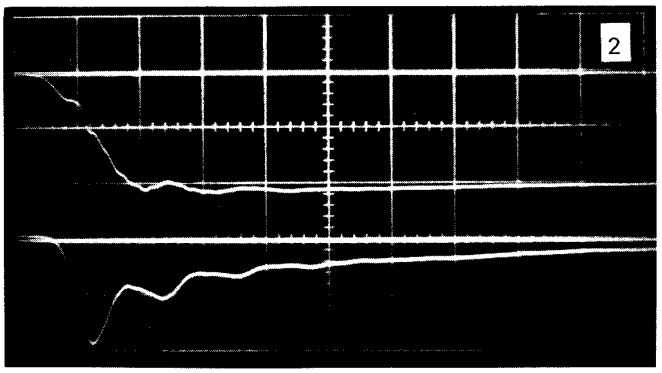
In order to illustrate further the initial response of the device, the three oscillograms on the next page were recorded during conduction, below, at the start, and well after the start of the avalanche.



Top Trace: Voltage across SCR
200 V/div.

Bottom Trace: Current in SCR
10 A/div.

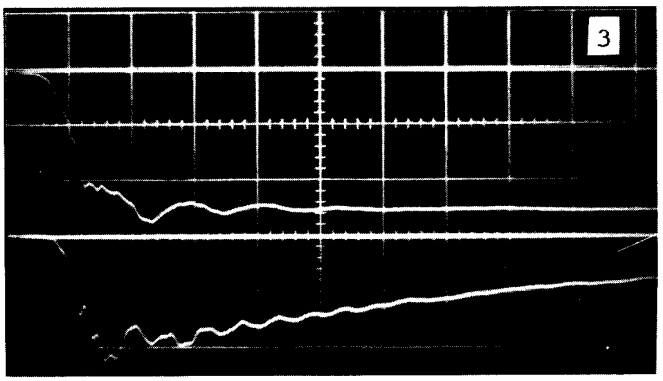
Sweep: 0.1 μs/div.



Top Trace: Voltage across SCR
500 V/div.

Bottom Trace: Current in SCR
20 A/div.

Sweep: 0.1 μs/div.



Top Trace: Voltage across SCR
500 V/div.

Bottom Trace: Current in SCR
40 A/div.

Sweep: 0.1 μs/div.

Oscillogram 1, with only 500 volts, shows a current flowing during the voltage rise, with a peak at 15 amperes, corresponding to the "charging" current of the junction capacitance, which is due mostly to minority carrier storage.

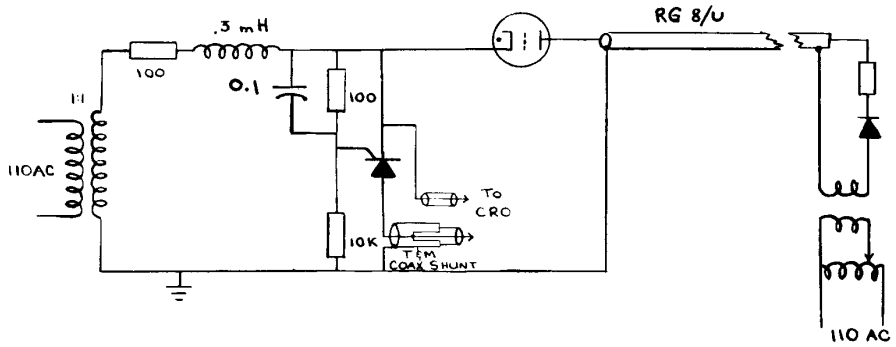
Oscillogram 2, at the onset of the avalanche above 1000 volts shows the same initial current with a peak at 38 amperes followed by the avalanche current.

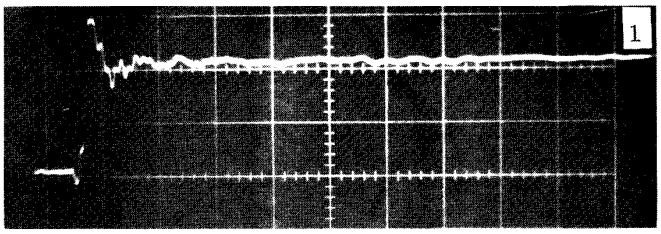
Oscillogram 3, well above the start of the avalanche, shows the initial "charging" current soon swamped out by the avalanche current which reaches 80 amperes for 1300 volts. Note that this voltage is significantly higher than those reported as causing failure in the no-load tests. There are probably two reasons for this: one is the higher steady-state junction temperature due to the flow of forward current (the test was made with 25°C ambient but after steady-state current flowed for several minutes). For this particular specimen, the volt time characteristic of the junction insulation surface was then such that no breakdown would occur for this short pulse duration. Raising the generator voltage effectively increases the time for which the SCR is held in the avalanche state as the portion of the exponential decay above 1000 volts will then increase. This increased duration above 1000 volts then makes possible for a number of devices to fail by breakdown of the surface, as shown by the failure voltages and times tabulated below.

Test Sample	C20A	C20D	C20A Aged	C20D Aged
Test Condition	Numbers show volts at failure and time to failure			
Junction at ≅ 80°C (due to fw'd current)	1100 .5	1100 .2	1100 1.5	1000 .4
	1200 .4	1200 .4	1000 .5	1100 .9
	1100 .9	1100 .5	1000 .7	1000 .4

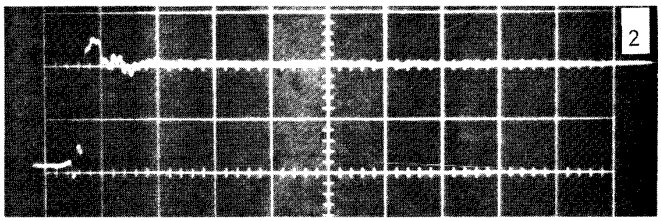
Pulse applied by increasing steps with .1 x 5 μs waveshape, applied at peak of forward current

Applied reverse voltage (no-load generator output) was in the 1100-2000 volts range for these tests.

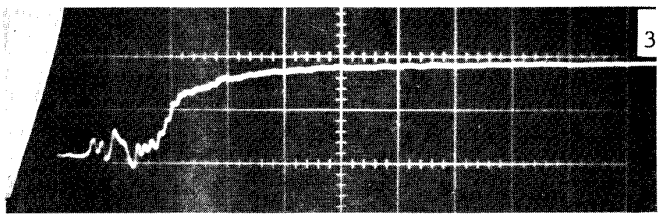




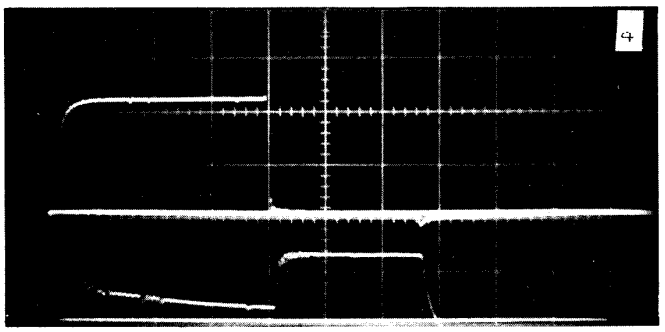
Output of unloaded generator
(500 volts/div, .1 μs/div.)



Voltage across SCR with no
steady state 60 cps
(500 volts/div, .1 μs/div.)



Voltage across SCR with 60 cps
forward current
(500 volts/div, 1 μs/div.)



Failure of C20A SCR with forward
current in 3.5 μs
Top: 500 volts/div.
Bottom: 40 amp/div.
Sweep: 1 μs/cm
Available pulse length 6 μs

7.2 Tests with Square Pulse Generator

In order to eliminate the effect of the decaying waveshape obtained from the capacitor discharge circuit, a few more samples were subjected to the same type of test, i.e., impulse during forward conduction, but the impulse was delivered from the cable discharge generator.

The test circuit is shown on the opposite page. The only difference from the capacitor discharge test is that a cable is used in a manner similar to no-load tests described in section 3.

The oscillograms on the opposite page, as well as others in this report, exhibit some minor oscillations at the start of the traces, between time zero and 0.1 μs. These are more likely to be caused by measurement problems than by device phenomena, so that the reader should be cautioned against attempting to draw conclusions from these initial oscillations. Several examples of these spurious signals are discussed in the appendix.

Oscillogram 1 shows the output of the test circuit with no test piece connected, while oscillograms 2 and 3 correspond to the same setting, with the test piece connected. Oscillogram 2 was recorded with no forward current in the SCR while oscillogram 3 was recorded with forward current. Compared to the unloaded output, the rise time of the voltage appearing across the SCR with forward current is substantially longer, as the result of the larger junction capacitance. The initial overshoot of the generator output is also removed by the loading effect of the test sample, which results from this minority carrier storage due to the forward current.

Oscillogram 4 shows, with a slower sweep rate, a typical failure oscillogram.

Test results with this procedure on the four groups of C20 SCRs are tabulated below:

Test Sample	C20A	C20D	C20A Aged	C20D Aged
Test Condition	Numbers show volts at failure and time to failure			
Junction at = 80°C 5 μs square pulse applied by increasing steps at peak of forward current	1000 .4 1100 4	1300 3 1000 6	1200 .4 1000 .9	1200 .6 1100 1
Same except pre-set pulse for higher voltage with high avalanche current	1100 35 1300 1 1200 2			

7.3 Discussion of the tests with forward current and comparison with no-load tests

The immediate effect of the forward current is to increase the effective junction capacitance due to minority carrier storage, compared to the lower diffusion or barrier capacitance existing when there is no forward current.

The consequence of this capacitance is that the rise time of the voltage is increased so that the avalanche effect can take place without the overshoot in voltage which was observed in the no-load tests, and which sometimes caused (see page) flashover of the device before the voltage clamping effect could take place.

Therefore, the flow of a forward current at the time of the reverse transient application seems to reduce the risk of early flashover. The device behaviour is then controlled exclusively by the avalanche voltage and the dielectric capability of the anode junction surface.

The avalanche voltage of this device, as previously stated, is not deliberately controlled, so that sample variations may be expected. Furthermore, this voltage will depend on the junction temperature so that the test values of the avalanche voltage with forward current reported

here, i.e., with junction at about 80°C can be expected to be somewhat higher than the values with no load.

Failure of the device is caused by surface flashover. This flashover voltage should exhibit for one sample the typical volt-time characteristic of insulation breakdown, for which of course only one point per sample be obtained here since each flashover is destructive. However, considering all the samples, there is a trend towards shorter time to flashover with increasing avalanche voltage. Thus, if a higher transient current is available and can drive the voltage higher on the avalanche characteristic, failure is likely to occur for a shorter pulse duration; however, the data shows this increase in bulk avalanche voltage to be rather small.

8. Conclusions on the C20 Tests

1. Failure occurs by surface arcing while the voltage is held in the 1000 volts range by the avalanche effect of the anode junction.
2. There is no significant difference between the performance of a 200 or 400 volt SCR, and ageing does not change this lack of correlation.
3. Ageing of the SCR by high temperature storage does not significantly affect the transient behaviour of the device.
4. Timing of the transient during forward current does not reduce the withstand capability of the device; actually, this capability may be enhanced as the increased junction capacitance will reduce the initial rate of voltage rise, before avalanche can occur.
5. While the transient behaviour is dominated by the avalanche phenomenon, this should not be construed as a suggestion that this can be used to advantage, as the present withstand capability of the junction surface is such that the SCR will fail in the range of this avalanche voltage.

Tests on A92 Rectifiers

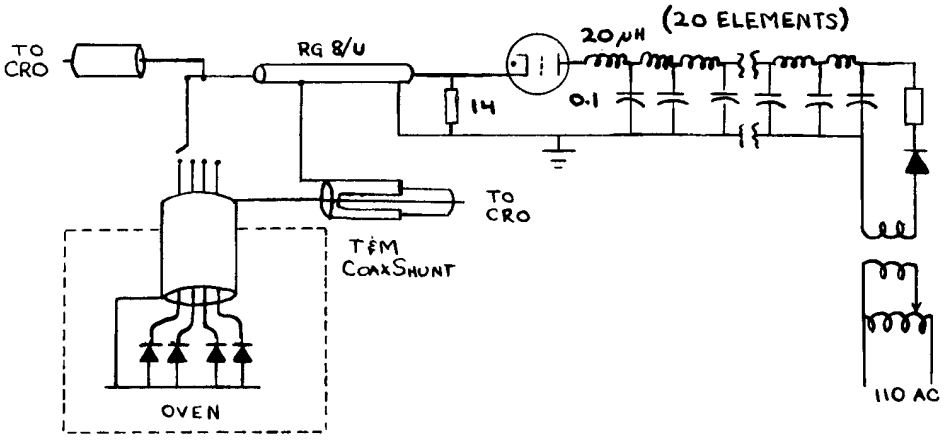
Summary of Tests

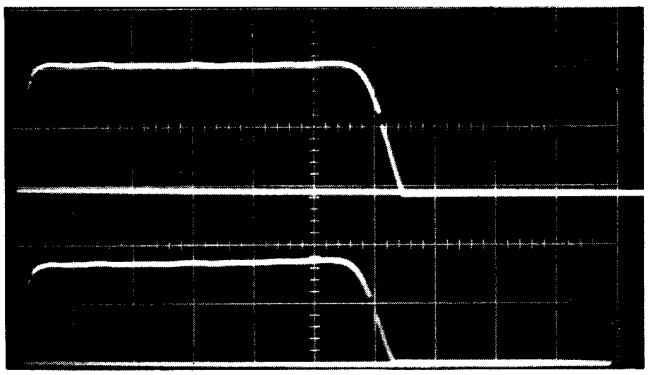
Test Samples: 500, 900, 1100 volts units

Tests: Avalanche characteristics
Reverse transients at slow and fast rate of rise, no bias

Results: Bulk failure will occur for low (relatively) current of long duration
Surface failure will occur for very high currents, even of short duration

The avalanche voltage class is not a valid indication of the transient voltage withstand capability. Energy levels are essentially the same for all.





Recording with 7 ohm carbon resistor instead of test diode.

Top trace: 500 V/div.
Bottom trace: 100 A/div.
Sweep: 10 μs/div.

Tests on A92 Controlled Avalanche Rectifiers

1. Purpose of the Tests

All tests reported so far in this program were conducted on non-controlled-avalanche diodes. It is then appropriate to investigate the behaviour of controlled-avalanche rectifiers under reverse transients in excess of their ratings.

2. Test Specimens

Three groups of A92 rectifiers were supplied by the Rectifier Components Department, graded 1100, 900 and 500 volt avalanche. The three groups were obtained from two diffusion processes.

3. Test Procedure

Reverse voltage was applied to the diode without other steady-state voltage. The avalanche of the rectifier would lower the impedance of the device to the point where the available surge generators had too high internal impedance to deliver sufficient energy to the test piece. An LC line was then built for storing the energy, instead of the cable used for smaller devices. The test circuit is shown on the opposite page, with a typical oscillogram of the voltage and current delivered to a fixed resistor instead of the non-linear test piece.

The rise time is relatively long, but since the tests produced failures in long times, as will be seen below, it would seem that this low rate of rise is not objectionable.

Tests were performed with 25°C and 150°C initial ambient temperatures on several diodes. In addition, the avalanche characteristics of one diode below the failure level were obtained with a range of initial ambient temperatures in order to correlate with the rise in avalanche voltage observed during the length of the test pulse.

Avalanche Characteristics

Starting with 500 volts for the reverse pulse, the setting of the generator was progressively increased, while the voltage across the diode and the resulting current flowing through it were simultaneously recorded.

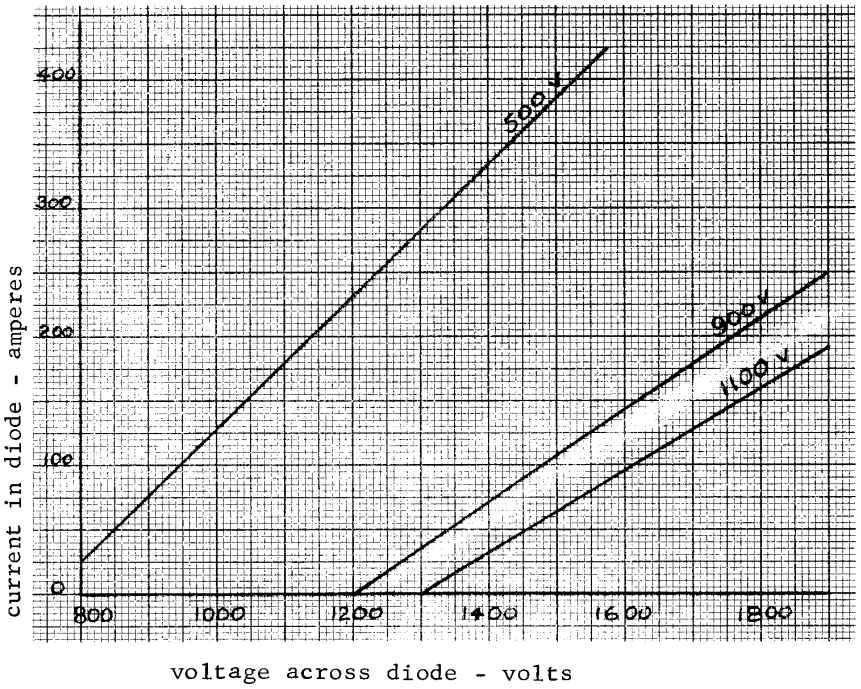


Figure 1

Avalanche characteristics of 500, 900, & 1100 volts A92 test samples

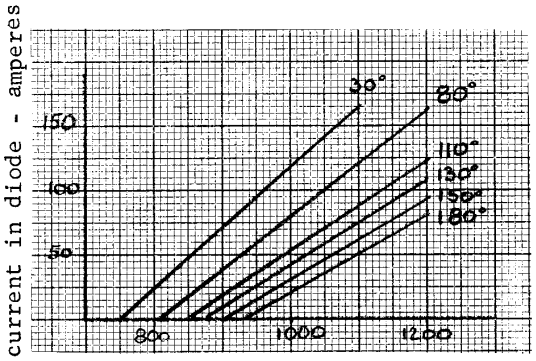


Figure 2

Avalanche characteristics of a 500 volt diode, measured at start of pulse, with junction at the initial temperature shown

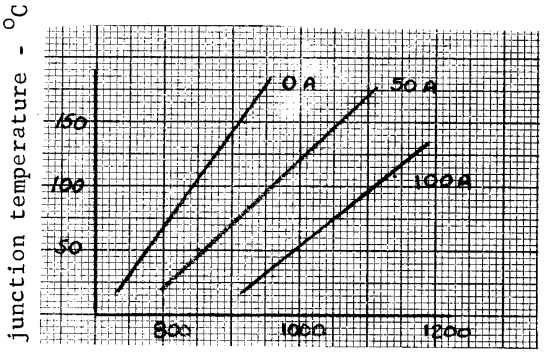
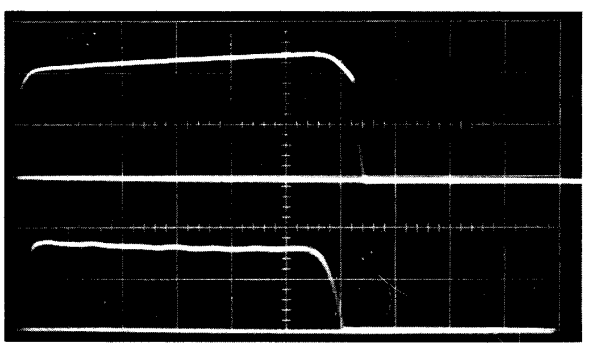


Figure 3

Junction temperature as a function of the voltage measured across the diode for the constant current shown



Oscillogram recorded with 500 volt diode at 30°C ambient temperature

Top trace: Voltage across diode 500V/div.
Bottom trace: Current in diode 100 amp/div.
Sweep: 10 μs/div.

Note constant current and voltage rise of 200 volts from start to end of pulse

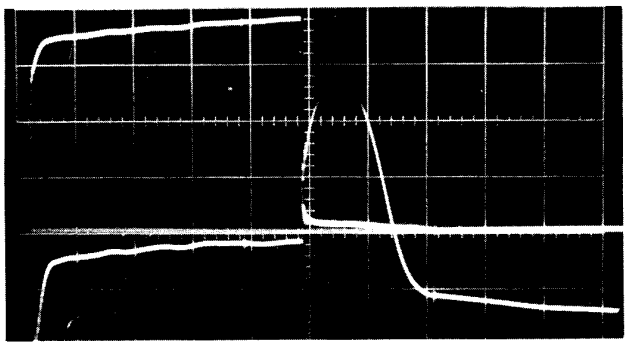
The test points for one device fell on an approximately straight line with linear volt and ampere scale (see Figure 1). Furthermore, the lines for a group of devices graded in the same voltage class lie within a 100 volt band and run parallel; only one has been drawn in Figure 1 in the case of the 500 volt characteristic which corresponds to three test samples. The slope of the 500 volt rectifiers on one hand and 900 and 1100 on the other hand are different, corresponding to constant dynamic resistance of 1.6 and 2.6 ohms respectively.

With increasing current levels, an increase in the voltage across the diode between the start and the end of the pulse became apparent, as seen on the oscillogram on the opposite page. In order to correlate this voltage rise with the change of avalanche voltage (or, more accurately, voltage across the device) due to temperature, a series of recordings were also made on one 500 volt diode with several values of ambient temperature, assumed to be the initial junction temperature. Thus, from the family of curves shown in Figure 2, the instantaneous temperature increase at various times of the pulse duration at constant current can be calculated. This is shown in Figure 3, in a plot of avalanche voltage vs. average junction temperatures.

For two specific current levels, the instantaneous volt amperes dissipated in the device were calculated; these two values of energy input into the semiconductor were compared to the temperature increase derived from Figure 3 and the apparent voltage change. Excellent correlation was found, i.e., for energy inputs with a 2:1 ratio, the calculated temperature increase was also 2:1.

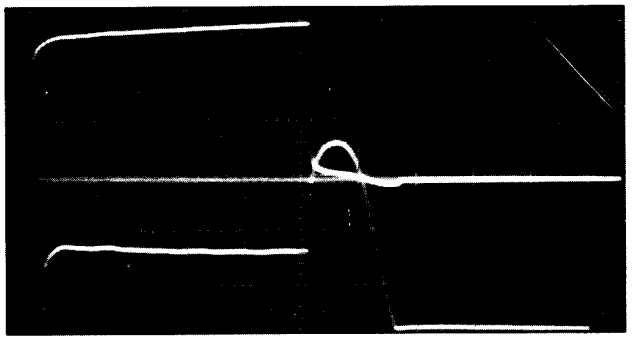
Therefore, with the high reverse currents involved in this investigation (well above the rated values) the pulse duration has the effect of increasing the voltage across the device for long pulses.

The question then is to know which will increase fastest. The temperature of the semiconductor will increase until the melting temperature is reached at a hot spot (temperatures shown in Figure 3 are average temperatures.) On the other hand, the voltage also increases with this temperature, so that flashover voltage may be



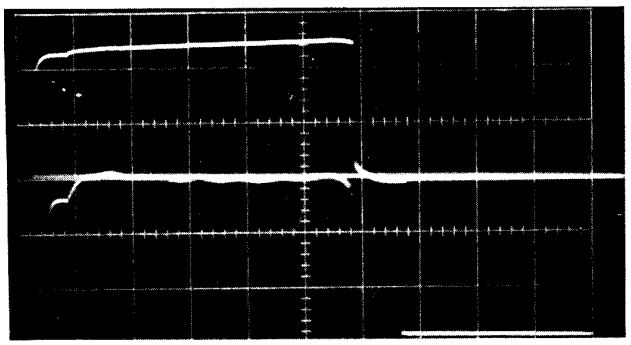
Failure of 1100 volts unit at
1900 volts, arc across varnish
Test at 30°C ambient

Top trace: Voltage across diode
500V/div.
Bottom trace: Current in diode
100A/div.
Sweep: 10 μs/div.



Failure of 500 volts unit at
1400 volts, arc at upper PP^+
junction due to field pinch
Test at 150°C ambient

Top trace: Voltage across diode
500V/div.
Bottom trace: Current in diode
100A/div.
Sweep: 10 μs/div.



Failure of 500 volts unit at
1250 volts, bulk failure
Test at 150°C ambient

Top trace: Voltage across diode
500V/div.
Bottom trace: Current in diode
40A/div.
Sweep: 10 μs/div.

Bulk failure vs. Arc failure

Note how breakdown occurred as voltage had begun to decrease shortly before end of applied pulse, in contrast with arc failure which occurred during voltage rise.

reached towards the end of a pulse which could not produce at the start a high enough voltage to cause immediate flashover.

It may also be possible to derive from these tests some information on the hot spot effect in the junction. When a "bulk" failure is observed, (i.e., not a surface breakdown), it may be assumed that the melting temperature of the material was reached, or exceeded at one hot spot. As discussed above, the increase in voltage observed between the initial voltage at the start of the pulse crest and the voltage reached just before failure yields an estimate of the average temperature rise during this interval. A comparison of the difference between the initial temperature plus this estimated average increase, and the temperature at which local thermal failure occurs should yield an index of the importance of hot spot effects. The small number of tests as well as the general scope of the present investigation, however, would not justify a thorough evaluation of this idea.

Tests to Failure

Typical oscillograms recorded during the tests are reproduced on the opposite page. Failure is apparent as the voltage across the diode is abruptly chopped while the current on the diode jumps from the Zener current to the maximum current available from the pulse forming network.

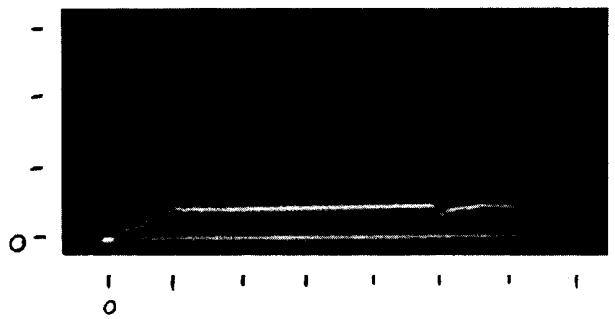
Results on individual diodes are tabulated below, listing ambient temperature, current, and voltage at failure and nature of the failure:

Voltage Grade	Diffusion I			Diffusion II		
500	30°C	450 amp	1700 volts, surface	30°C	300 amp	1100 volts, surface
	30°C		1500 volts, surface	30°C		1150 volts, surface
	150°C	160 amp	1450 volts, bulk	150°C	160 amp	1400, surface arc
	150°C	120 amp	1250 volts, bulk			
900	30°C	200 amp	1750 volts, surface	30°C	280 amp	2000 volts, surface
	30°C	300 amp	1950 volts, surface	30°C	420 amp	2200 volts, surface
1100	30°C	190 amp	1900 volts, surface		--------	

Unloaded generator output

Vertical: 2300 volts/div.
Sweep: 10 ns/div.

(50 ns pulse duration)



Voltage across diode

Vertical: 2300 volts/div.
Sweep: 10 ns/div.

Avalanche at 900 volts occurs in less than 10 ns.

(Power pulse ends at 50 ns, but cable reflections hold the voltage up for a longer duration)

Discussion of the Test Results

The relatively slow rise of the voltage, made necessary by the design of the line, might appear a limitation of the tests. Work sponsored by ATL at the Laboratory Operation of the Power Transmission Division includes an evaluation of semiconductor performance under fast transient conditions[1]. Instrumentation as well as short pulse generator techniques were developed in this work, with the capability of producing and accurately recording pulses of several kilovolts with rise times of less than 10 nanoseconds. A sample of the A92 diodes involved in the present test series was also subjected in Philadelphia to this extremely steep voltage pulse. The oscillograms on the opposite page show the output of the unloaded pulse generator and the voltage measured across the diodes.

These show that the avalanche voltage can be reached in less than 10 nanoseconds, and that the device will then hold the voltage at that level without any disturbance. The tests made with the slow rise time have shown that breakdown will occur only after a sufficiently high voltage is reached on the dynamic characteristic of the diode to cause flashover. Since the avalanche voltage is reached without other overshoot or excursion in 10 nanoseconds, the failures produced with the slow rise circuit, during avalanche, represent valid tests which are not restricted by the slow rise time.

The failure levels for the Diffusion I group, due to surface breakdown, are all in the 1500 -1950 volts range, without any correlation with the voltage class of the diode. Failures in the bulk occurred at lower avalanche voltages, but these are not related to voltage but rather to initial temperature and total energy input in the device.

The failure levels of the Diffusion II group are all lower. This fact was previously established by the Rectifier Components Department and led to abandonment of this experimental process.

(1) This work will be reported by the Philadelphia Laboratory Operation in the near future; the distribution of the report will include all sponsors of the present Pooled Program.

Conclusion of the Tests on the A92 Rectifiers

These rectifiers exhibit a substantial capacity for dissipating reverse surge energy. Unless the initial junction temperature is already high and the pulse duration long enough to raise the temperature of the junction hotest spot to its melting point, the actual failure may still be caused by arcing over the junction surface. The avalanche characteristic is such, however, that it requires extremely high reverse current to drive the voltage up, in fact well above the rated current.

On the other hand, a lower current is required to bring a high avalanche voltage diode to the danger point (see Figure 1) so that a high voltage diode is more sensitive to a current source type of surge. This is pointed out in the specification sheets and application notes.

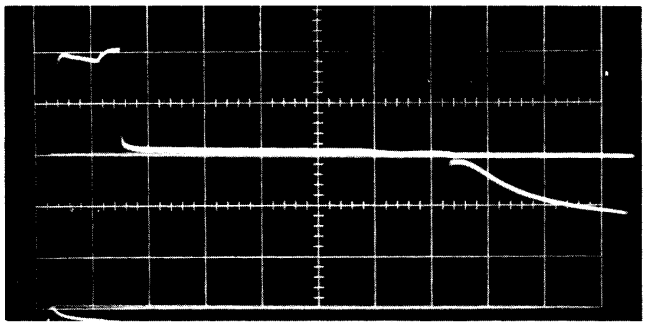
Failure by surface breakdown can occur with high currents, while bulk failure is more likely with lower but longer current values.

In the case of surface breakdown, when it occurs, the rating of the diode, again, has no bearing on the actual failure level; however, surface breakdown is less likely to occur on lower voltage diodes for a given energy pulse, and in that sense the rating of the diode is significant.

Tests on A90 Rectifiers

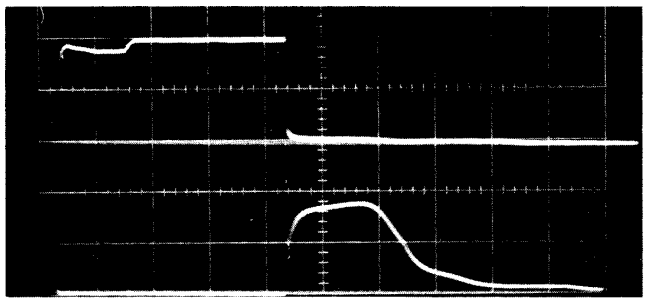
Summary of Tests

Test Samples:	Small number of 200 and 1200 PIV units
Tests:	Reverse transient with no bias
Results:	Neither PIV of the unit nor energy of the transient affect the failure level



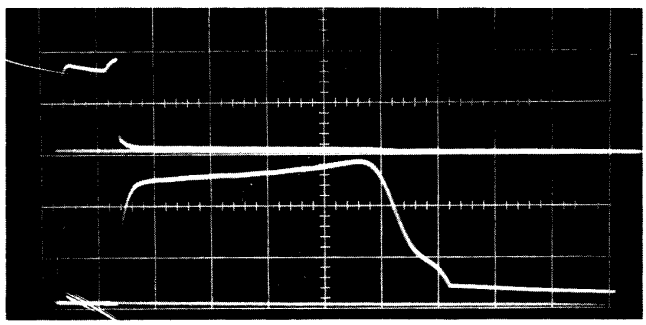
1200 volts PIV unit test at 30°C ambient

Failure at 2000 volts in 12 μs
Arc across varnish



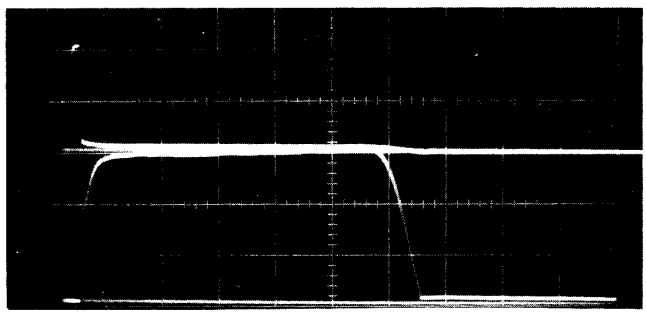
200 volts PIV unit test at 30°C ambient

Failure at 2000 volts in 40 μs
Arc across varnish



1200 volts PIV unit test at 150° ambient

Failure at 1800 volts in 12 μs
Arc at upper PP^+ junction



200 volts PIV unit test at 150°C ambient

Failure at 2000 volts in 4 μs
Arc across varnish

Oscillograms showing failure of A90 rectifiers at 30°C and 150°C

All oscillograms: top trace: voltage across rectifier - 1000 volts/div.
bottom trace: current in rectifier - 100 A/div.
(except first oscillogram, 10 A/div.)
sweep: 10 μs/div.
applied pulse width: 60 μs

1. Tests on A90 Diodes

A limited number of A90 diodes were subjected to tests similar to those applied to the A92 diode in order to illustrate the difference in the performance between a controlled-avalanche rectifier (A92) and a non-avalanche rectifier (A90).

Six units were obtained from the Rectifier Components Department, three were 200 volts and three were 1200 volts units.

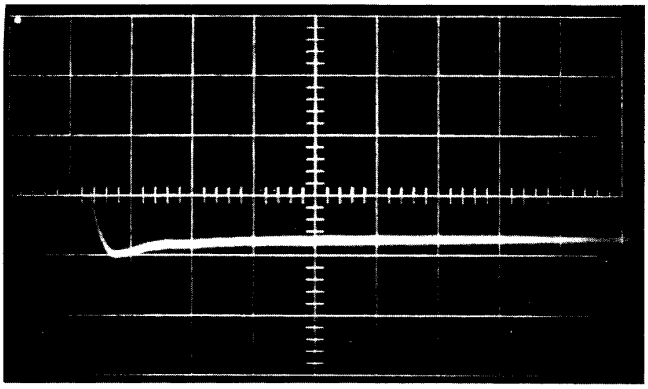
Four units were subjected to the long, slow rise pulse generated by the LC line described for the A92 tests. One of each voltage class was tested at 30°C ambient and at 150°C ambient. This provides direct comparison with the A92 tests.

All of these three test series were made with no steady-state bias on the diodes.

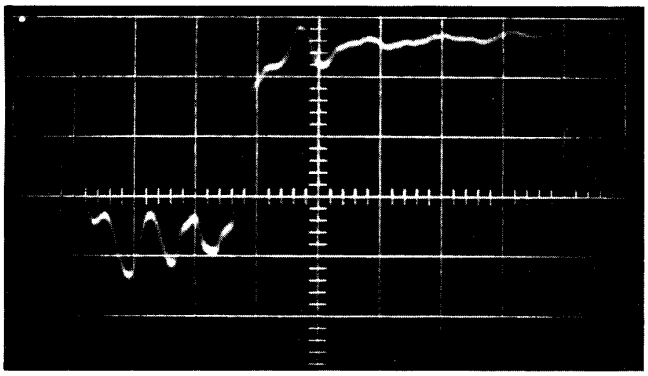
In the case of the slow rise pulse, the voltage of the generator was progressively increased, with a constant pulse duration of 60 μs, applied by single shots, until the failure occurred, as recorded in oscillograms 1 to 4 on the opposite page. The step appearing in the pulse top is due to a partial arc-over in the thyratron of the pulse generator, reducing the thyratron drop and thereby increasing the voltage applied to the diode. Failure, of course, occurs when the voltage trace is abruptly chopped while the current trace jumps from zero to the value of current available from the pulse generator.

Although the time to breakdown of the 200 volt diode at 150°C was shorter compared to the time at 30°C the difference is well within what might be expected from a gap breakdown at the minimum voltage which can cause breakdown.

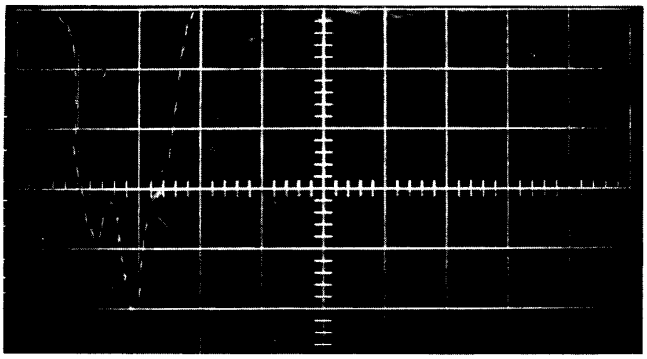
Dissection of the four units revealed surface breakdown. In one case, removal of the tracked-over varnish allowed the diode to recover satisfactory characteristics. However, had 60 cps power-follow current been available, the flashover triggered by the pulse would most likely have caused permanent damage.



No-load output of generator
(2000 volt setting)



Failure of 200 volts PIV unit
same generator setting as above,
with oscillations caused by
interaction of the diode capacitance.
Failure at 1800 average volts in
250 ns
Arc across varnish



Failure of 1200 volts PIV unit
No-load generator setting 2200 volts
Failure at 1900 average volts in
200 ns
Arc across varnish
(trace indicated by scratches for
reproduction)

Tests on A90 rectifiers at 30°C
with capacitor-discharge generator

All oscillograms: 500 volts/div. - voltage across rectifier
0.1 μs/div. - sweep

The remaining two units were subjected to a fast rise pulse from the capacitor discharge generator, in order to evaluate the response to a fast rise surge, which did not produce early failure in the case of the A92 diode.

Here again, the voltage was progressively raised for each single shot, until failure occurred as recorded in the two oscillograms shown on the opposite page. Interaction between the diode capacitance and the generator caused the oscillations shown on the two oscillograms. By coincidence, the chop due to the flashover across the varnish occurred at a minimum of the oscillation; for evaluation purposes we chose to take the average value of the oscillation as the failure level.

By comparison with the tests made with slow rise waveshape, failure occurred very early, i.e., in less than 0.3 μs. The long tail of the wave (see no-load oscillogram) could have produced failures with longer time to breakdown at slightly lower voltage, but this did not occur.

2. Discussion of the Tests on A90 Rectifiers

The failure levels with slow rising wave and with the fast rising wave are not significantly different, nor is there any difference in the levels or time to failure of the 200 volts units compared to the 1200 volts units. All failed between 1800 and 2000 volts.

The long time to failure observed in one case is probably the result of a slightly increasing voltage in the top of the "flat top" pulse. In all the other slow rise cases, failure occurred within less than a microsecond as the voltage was still rising. In the case of fast rise wave, failure occurred in less than 0.3 μs.

Furthermore, as the rectifier does not draw an appreciable reverse current, it cannot contribute to dissipating the surge energy, so that a low energy pulse (capacitor discharge) will produce failure at voltage levels comparable to a high energy pulse (line discharge).

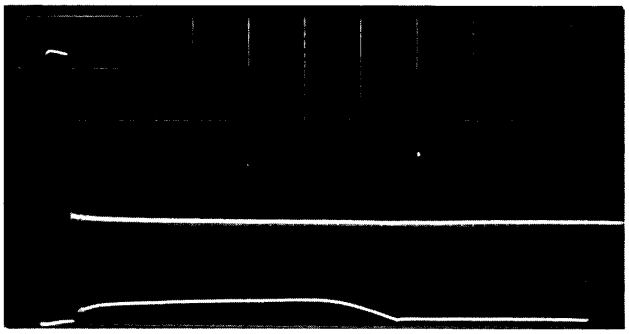
3. Conclusions

The failure level of the A90 rectifier is primarily determined by the dielectric strength of the junction surface. Neither temperature, energy of the pulse or PIV rating of the diode affect the failure level. Energy levels at failure are substantially less than for controlled avalanche (A92) rectifiers of same current rating.

Tests on ZJ 260 SCR's

Summary of Tests

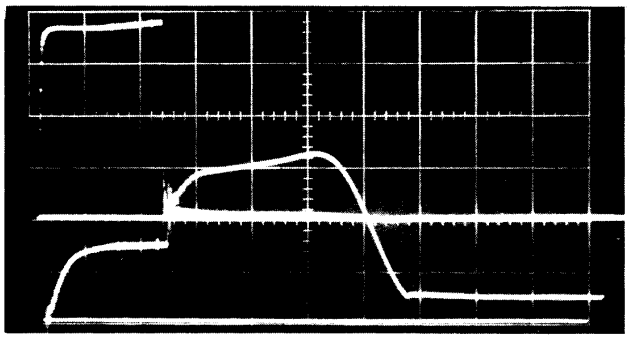
Test Samples:	Units with 200 to 1000 volts class
Tests:	Reverse transient with no bias
Results:	No clear indications - in any event voltage class does not correlate with failure level



1000 volts unit

Failure at 1600 volts with
low current - 10A

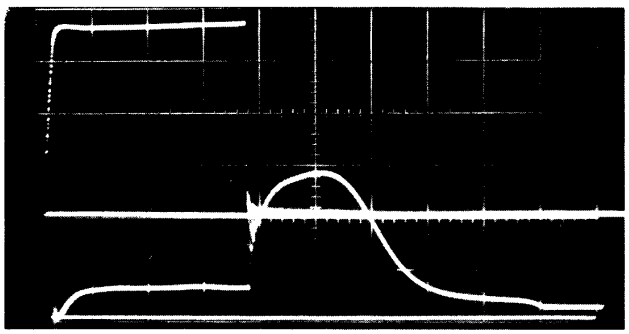
(100 A/div.)



1000 volts unit

Failure at 1900 volts with
high current - 300A

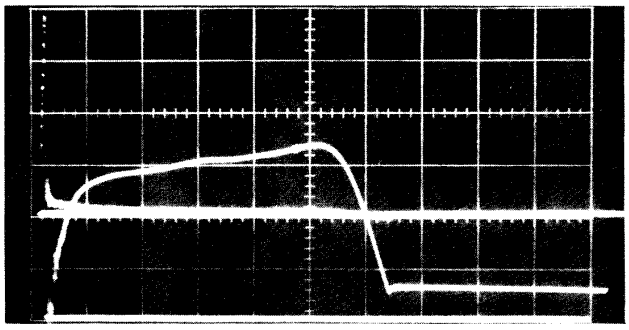
(200 A/div.)



800 volts unit

Failure at 1850 volts with
medium current - 60A

(100 A/div.)



500 volts unit - preset test

Failure at 1900 volts in short time

(200 A/div.)

Failures of ZJ260 SCRs

All oscillograms: Top Trace: Voltage across SCR - 500 V/div.
Bottom Trace: current in SCR - 100 or 200 A/div. as shown
Sweep: 5 μs/div.

1. Tests on ZJ260 SCRs

A number of ZJ260 SCRs with voltage grades ranging from 200 to 1000 volts were obtained from the Rectifier Components Department. Reverse voltage pulses delivered from the LC circuit described in the A92 tests were applied to these rectifiers in two manners.

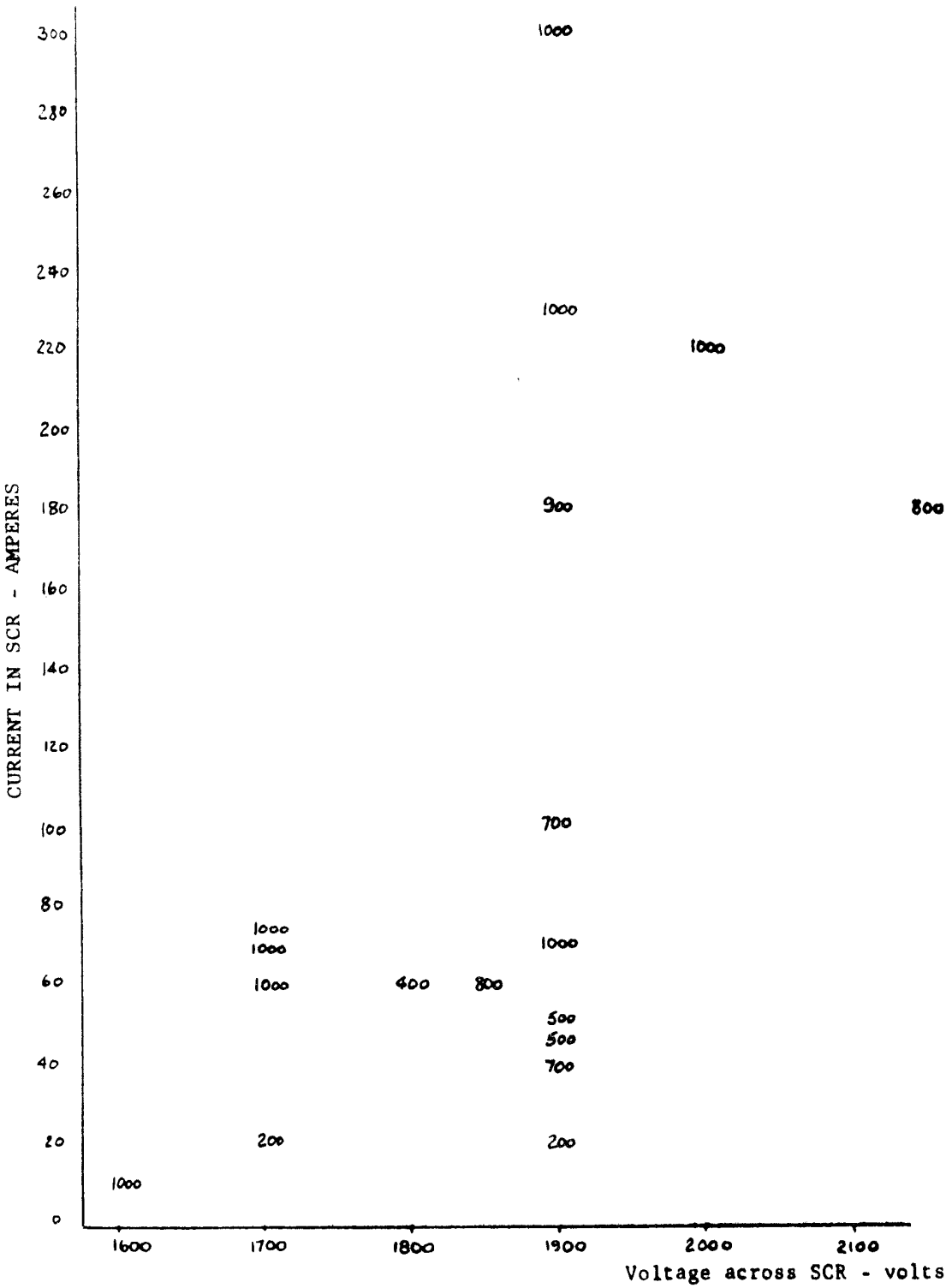
One series of tests was made by applying single shot pulses, with increasing voltage, until a failure was observed. This generally occurred after more than 5 or 10 microseconds, as the voltage across the device was raised by heating of the junction, in a manner similar to that discussed for the A92 rectifiers.

A second series of tests was made by setting the generator to the maximum available voltage, in order to cause breakdown at the first pulse, presumably very early in the pulse duration rather than after "prolonged" heating.

Both test series were made without bias on the SCR, in the first approach. Attempts were made to also perform these tests with forward or reverse bias, but instrumentation problems prevented doing this within the available time. Typical oscillograms recorded during the test series are reproduced on the opposite page. The voltage across the SCR is abruptly chopped as failure occurs, while the current jumps from its avalanche level to that of the maximum available from the pulse-forming network.

The first three oscillograms correspond to the increasing voltage steps test procedure, while the fourth was recorded with a preset voltage pulse.

Three of these samples were dissected by the Rectifier Components Department with the following results: all three units failed in the bulk. They were not surface limited. The failure occurred by overheating at some weak spot in the bulk, such as a diffusion spike.



DISTRIBUTION OF FAILURE POINTS - VOLTAGE VS CURRENT FOR VOLTAGE CLASS SHOWN

The voltage and current at the time of failure, and the time to failure are tabulated below for the specimens which were subjected to the two test methods.

Sample Number	Voltage Class	Type of Test	Voltage At Failure	Current At Failure	Time To Failure
	Volts		Volts	Amp	μs
1	200	increasing steps	1900	50	2
2	200	preset	1700	50	0.5
3	400	increasing steps	1800	60	25
4	500	preset	1900	100	0.5
5	500	preset	1900	100	0.5
6	700	increasing steps	1900	40	25
7	700	preset	1900	100	1
8	800	preset	2100	180	2.5
9	800	increasing steps	1850	60	15
10	900	increasing steps	1900	180	15
11	1000	increasing steps	1900	230	10
12	↓	↓	2000	220	8
13			1700	60	3
14			1700	70	2
15			1700	70	25
16			1900	70	25
17			1600	10	2
18			1900	300	12

2. Discussion of the Test Results

Inspection of the tabulated results shows several interesting points: The voltage at failure varies between 1600 and 2100 volts, for a range of voltage class ratings from 200 to 1000 volts; there is no correlation between the voltage class on one hand and the voltage and current at failure on the other hand.

The plot shown on the opposite page was made in an attempt to correlate voltage across the SCR with the avalanche current, for a specific voltage class. The number plotted represents the voltage class while the coordinates are the voltage and current at the time of failure. There is no readily apparent correlation or trend in the location of the failure points in this plot.

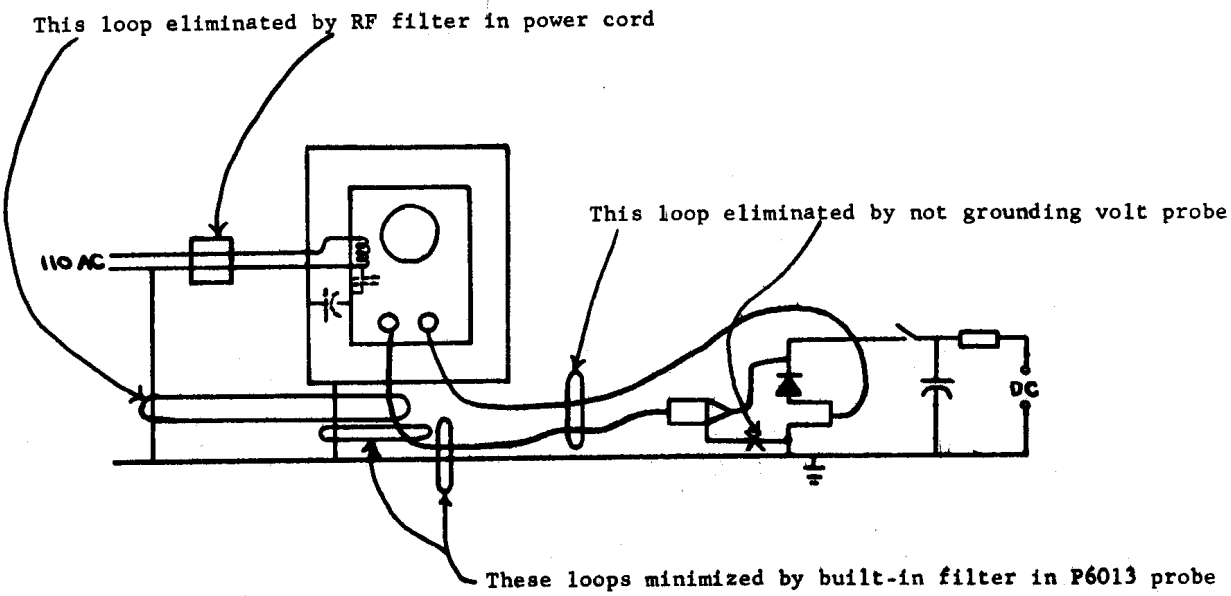
3. Conclusions of the Tests on the ZJ260 SCRs

The test results do not show any clear correlation between the voltage class of the SCR and the voltage at which it will fail under reverse transient.

Furthermore, there is no correlation between the voltage and current at the time of failure.

Therefore, the voltage class of the device cannot be used as a measure of the withstand capability under reverse transients beyond the values specified by the manufacturer.

APPENDIX


This loop eliminated by RF filter in power cord
This loop eliminated by not grounding volt probe
110 AC
DC
These loops minimized by built-in filter in P6013 probe

APPENDIX

Notes on Two-Channel Transient Recordings

The normal difficulties encountered in making single sweep transient recordings are increased when two rather than one signal are to be recorded. The perennial problem is that of ground loops, deliberate or unsuspected, which must be weeded out.

Some of the failure oscillograms recorded for this report included a current trace as well as a voltage trace. The voltage measurements were obtained through a Tektronix P6013 high voltage probe while the current measurements were derived from a T&M Research Associates coaxial shunt.

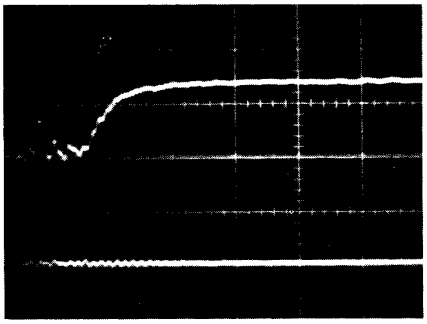
The oscilloscope used for the two-trace measurements was a Tektronix 555 oscilloscope.

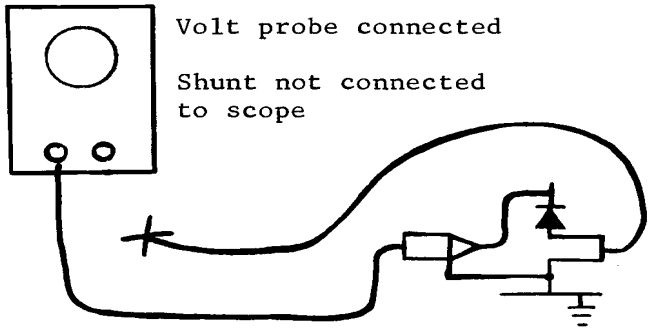
The sketches on the opposite page show some of the most obvious "unsuspected" couplings in the power and measuring circuit, as well as the steps taken to eliminate them.

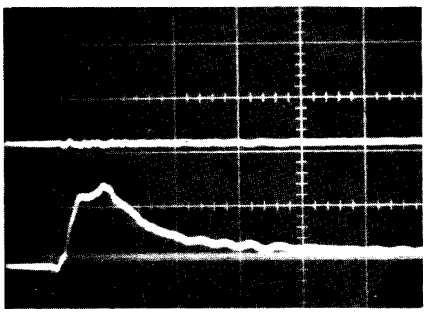
The following circuit elements are connected directly to a common grounding point, which is connected to the building ground via bench ground: the low side of the DC high voltage source, the low side of the energy storage element (line or capacitor) and the shell of the coaxial shunt. One might also connect to this point the ground side of the high voltage probe.

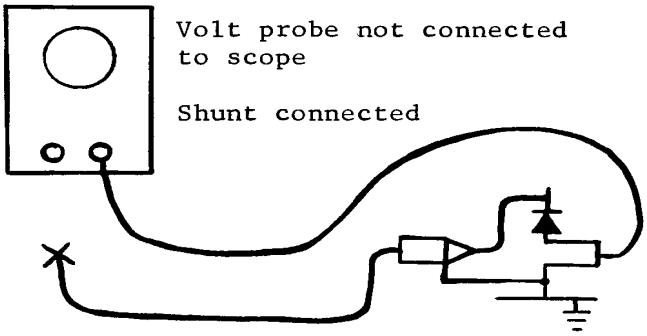
In addition, the oscilloscope power supply, through the line cord and the power transformer, is capacitively coupled to the ground, by a rather substantial stray capacitance. At high frequencies, it was also found that the perforated oscilloscope cabinet can allow direct radiation into the oscilloscope circuitry.

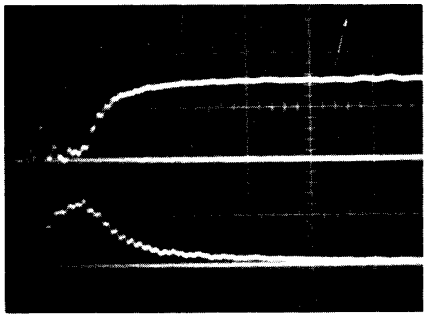
Therefore, a number of precautions were taken, some of which are rather obvious, some others had to be tried out and still did not entirely clean up the measurements, as we will see later.

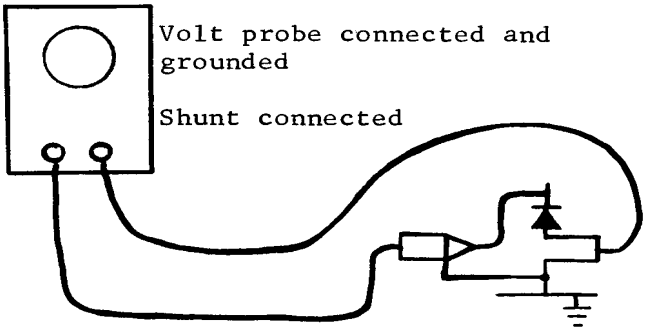


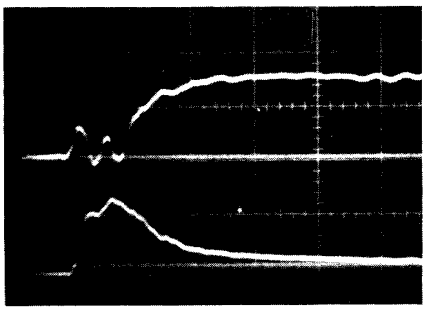

Volt probe connected
Shunt not connected
to scope

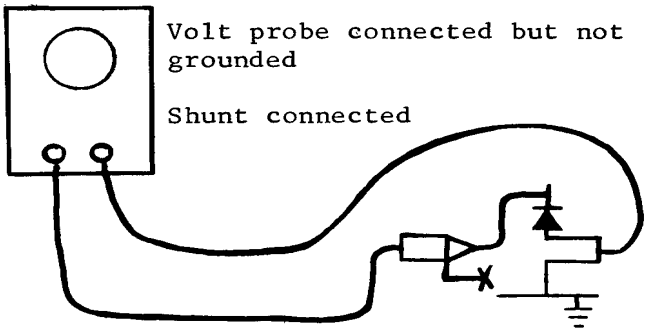



Volt probe not connected
to scope
Shunt connected




Volt probe connected and
grounded
Shunt connected




Volt probe connected but not
grounded
Shunt connected

First, an RF filter was inserted in the line cord of the oscilloscope, and the oscilloscope was placed in a copper enclosure tied to the bench ground. This reduced to less than 2% of the normal signal level the noise still displayed by the oscilloscope, even with its input shorted.

The Tektronix P6013 probe has a built-in filter consisting of several turns of the probe lead wound on a powder core offering a high impedance to high frequency circulating current in the sheath of the probe lead. However, this is not quite sufficient if another ground lead, such as the current lead from the shunt, would also be connected to the oscilloscope.

This is illustrated in the four circuit arrangements shown on the opposite page.

With the volt probe only connected, circulating current in a ground loop is limited as the only possible loops involve stray capacitances from the scope to its grounded box and the built-in filter of the P6013 probe. Therefore, the first oscillogram, recorded with a 0.1 μs rise time pulse applied to a test diode, can be expected to fairly represent the voltage across the test piece. The current channel, which is not connected to the circuit, does however, display a small high frequency signal.

The second oscillogram, recorded with the same applied pulse but with the volts probe disconnected, can in a similar manner be expected to fairly represent the current in the test piece. A small signal is displayed on the disconnected voltage channel.

Connecting both channels produces the display recorded on the third oscillogram. While the main rise of the voltage signal is not seriously affected, it does display a low amplitude, high frequency oscillation which was not present in the first oscillogram, and the signal before the main rise is definitely changed. The current trace is not changed as far as major waveshape is concerned,

but a rather large, high frequency oscillation persists for the duration of the current pulse display.

A fourth oscillogram corresponds to an arrangement with the current probe connected (both sides of the coax shunt are shown in schematic form by a single line) and the ground (sheath) side of the voltage probe floating. This configuration, which produces the two-channel display used in a number of recordings in this report, exhibits the smallest distortion compared to single voltage or current traces.

However, small high frequency signals are displayed during the initial part of the pulse, which are more likely to represent spurious signal rather than significant, actual device phenomena. Therefore, caution is required in attempting to draw conclusion from some of the minor ripples which can be observed in a number of oscillograms within the main part of this report.

References

1. TIS 62GL191 Tests on 1N679 Diode - effects of - waveshape
   - temperature
   - steady-state current
   - timing of surge
   - PIV

2. TIS 63GL133 Limited tests on GE 4JA4, 4JA10, 1N1696 and other manufacturers.

3. TIS 63GL132 Tests on 1N679, 4JA4 - effects of rate of voltage rise.

4. TIS 63GL144 Tests on C20 SCR's - effects of - PIV
   - surge energy

5. DF 63LC1342 Tests on 1N690 manufactured by G.E. and others. Limited tests on other devices.

6. DF 64LC1605 Tests on 1N539, 1N547, 1N560, 1N1117, 1N1120 diodes also 2N525, 2N333, 2N2714 transistors.

7. TIS 65ESP3 Tests at high speed on various devices - to be issued in first half of 1965 by the Laboratory Operation of the Power Transmission Division.

8. AIEE Standard #59 Semiconductor Rectifier Components.

Acknowledgements

The test samples were selected, and representative failed units were dissected through the cooperation of Messrs. Bisson, Knaus, Jalbert, Lyon, and Werner of the Rectifier Components Department.

Messrs. F.W. Gutzwiller and J. Read of the Rectifier Components Department made helpful suggestions to improve the manuscript of this report.

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