2D Materials Beyond Graphene For Future Electronics

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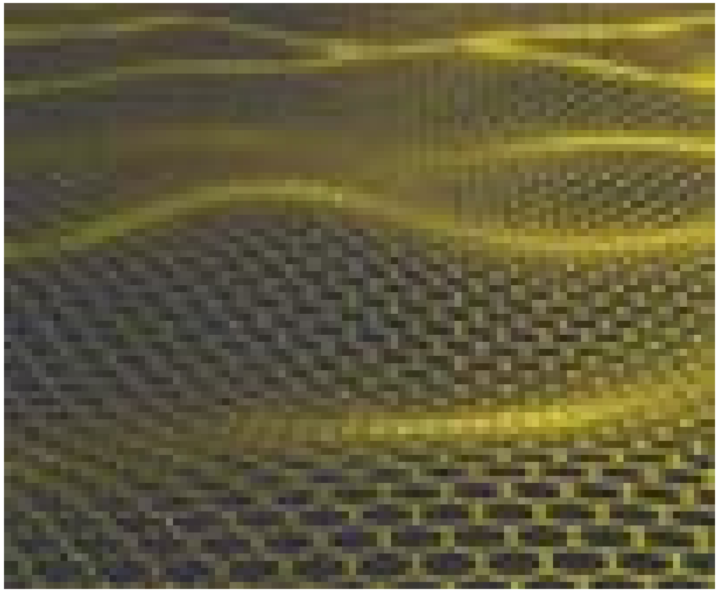
- Introduction
- An (Incomplete) Overview of 2D Materials
- 2D Transistors – State of the Art
  - 2D Transistors for More Moore
  - 2D Transistors for More Than Moore
- Metrology Needs for 2D Transistors and 2D Electronics
- Conclusion

Frontiers of Characterization and Metrology for Nanoelectronics FCMN
Hilton Dresden Downtown, Dresden, Germany, 14-16 April 2015

2D Materials – An (Incomplete) Overview

The most well-known 2D material: Graphene



Artistic representation of graphene.
Source: Jannik Meyer

- First 2D material studied in detail.
- Long history, finally became famous by the works of Novoselov & Geim and Berger & de Heer from 2004.
- High mobilities (>100 000 cm^2/Vs @ 300K) raised expectations regarding electronic applications (possible successor of Si).
- European Graphene Flagship.

Meanwhile

- The prospects of graphene electronics are considered less optimistic.
- However, significant attention for 2D materials beyond graphene.
- So far, more than 500 layered materials discovered.
- Many of them semiconducting and possibly useful for electronics.

2D Materials – An (Incomplete) Overview

X-enes

- Graphene, silicene, germanene
- Graphene nanoribbons (GNR)
- Bilayer graphene (BLG)
- Phosphorene, stanene

2D TMDs

- MQ_2: M = transition metal, Q = chalcogene (S, Se, Te)
- Mo-based TMDs, e.g., MoS_2
- W-based TMDs, e.g., WS_2

2D Materials

X-anes

- Graphane
- Silicane
- Germanane
- Stanane

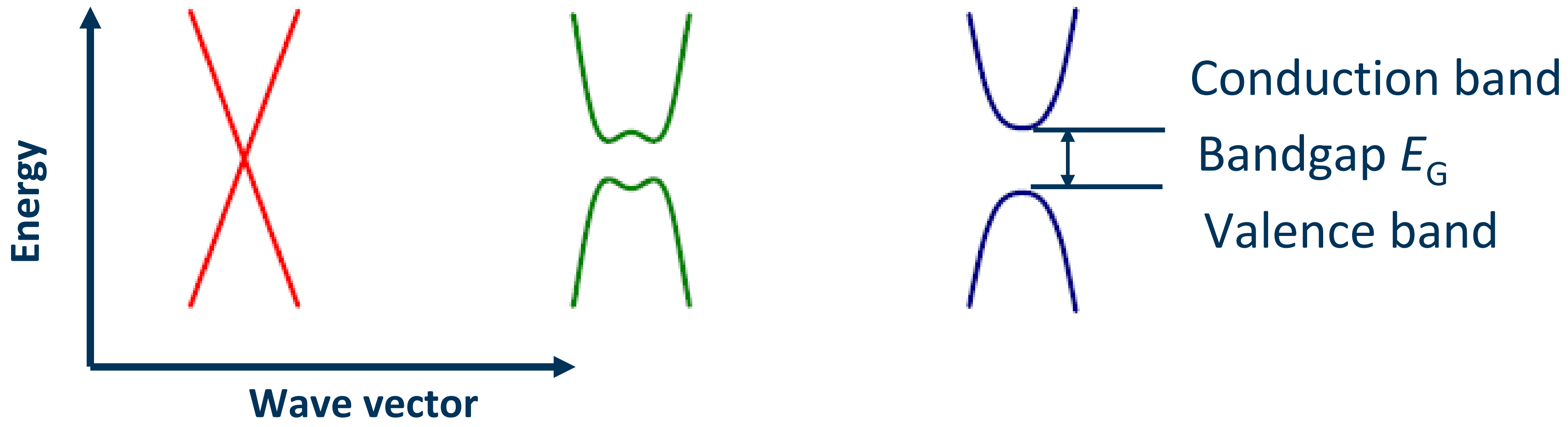
MX-enes

- M_2X: M = early transition metal, X = C or N
- M_2X plus F_2, $(OH)_2$, O_2 e.g. Ti_2CO_2, Sc_2CF_2, …

Many Further 2Ds

Flouro-X-enes, Chloro-X-enes, SMCs, 2D III-Vs, 2D IV-IVs, 2D elementals, etc.

2D Materials – An (Incomplete) Overview



X-enes
- Graphene
- Silicene
- Germanene

No gap, $E_G = 0$! This is really a pitty, since the missing gap causes serious problems for transistors.

BLG

$E_G \leq 130$ meV Too narrow for logic transistors.

X-enes
- Phosphorene
- Stanene
- GNRs

X-anes
- Graphane
- Silicane
- Germanane

MX-enes
- Sc_2CF_2
- $TiCO_2$

2D TMDs
- MoS_2, $MoSe_2$, $MoTe_2$
- WS_2, WSe_2, WTe_2

etc., etc.

Many of these materials have a gap $E_G = 0.5 \ldots 2.5$ eV, perfect for transistors.

How Promising are 2D Materials Beyond Graphene?

5 December 2011 Last updated at 17:19 GMT

Silicon rival MoS2 promises small, low-energy chips

The first computer chip made out of a substance described as a "promising" alternative to silicon has been tested by researchers.

The Switzerland-based team used molybdenite (MoS2) - a dark-coloured, naturally occurring mineral.

The group said the substance could be used in thinner layers than silicon, which is currently the most commonly used component in electronics.

The researchers say molybdenite microchips would need less power than existing silicon-based circuits

http://www.bbc.co.uk/news/technology-16034693

How Promising are 2D Materials Beyond Graphene?

IEEE SPECTRUM

Graphene or Molybdenite? Which Replaces Silicon in the Transistor of the Future?

By Dexter Johnson

Posted 2 Feb 2011 | 19:25 GMT

http://spectrum.ieee.org/nanoclast/semiconductors/nanotechnology/graphene-or-molybdenite-which-replaces-silicon-in-the-transistor-of-the-future

KURZWEIL ACCELERATING INTELLIGENCE | News

April 12, 2013

‘Germanane’ may replace silicon for lighter, faster electronics

Germanane single- or multiple-atom-layer sheets can be exfoliated onto silicon dioxide or silicon surfaces (AFM image) (credit: Elisabeth Bianco et al./ACS Nano)

The chemists found that it conducts electrons more than ten times faster than silicon and five times faster than conventional germanium — the same material that formed the first primitive transistors more than 60 years ago

http://www.itpro.co.uk/635173/qa-what-will-wonder-material-graphene-give-us

Things seem to look good – TOO GOOD TO BE TRUE ?

We should consider such statements very careful !

More Moore & More Than Moore

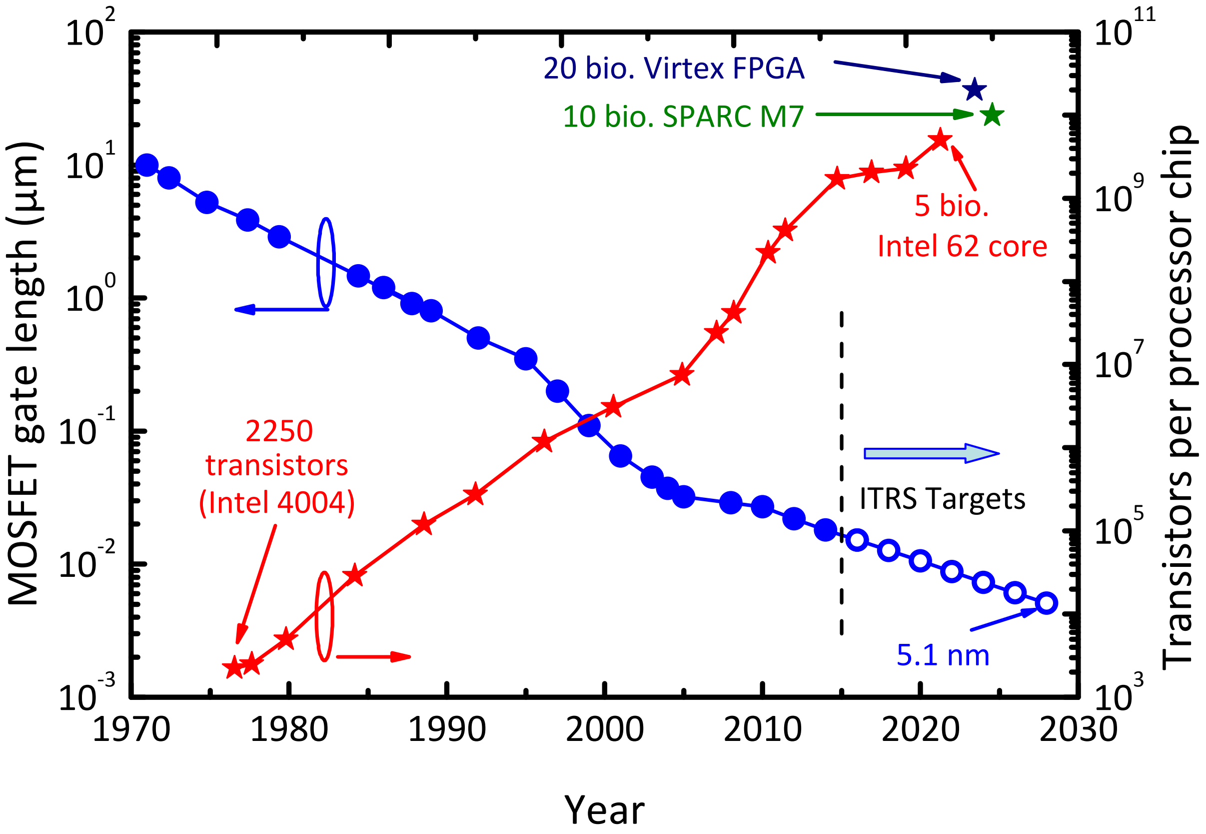
Digital CMOS
Logic *Memories*

Analog *RF* *High-volt.* *Power* *Sensors* *Actuators* *Flexible* *Printable* *Opto* *MEMS*

More Moore	***More than Moore***
Compute ***Store*** ***Key enabler: CMOS scaling***	***Interact with people + environment*** ***Exchange information*** ***Enhanced functionality***
2015: 16-nm gate MOSFETs, Si	*2015: Si, SiGe, GaAs, InP, GaN, SiC, …*
2028: 5-nm gate MOSFETs *Si, Ge, III-Vs*	*2028: Si, SiGe, GaAs, InP, GaN, SiC, …* *plus most likely 2D materials*
Beyond 2028: < 5-nm gate MOSFETs *Si, Ge, III-Vs, plus possibly 2D materials*	

≈ 70 % of the overall chip market.

Trends In More Moore

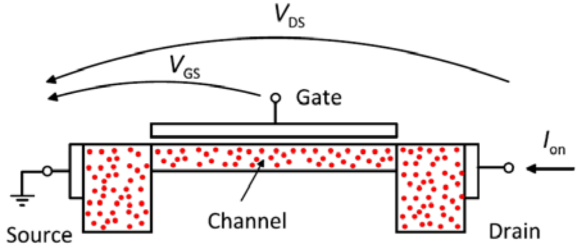


- Moore‘s Law: Doubling transistor count / chip every 18…24 months.
- Smaller transistors (scaling).

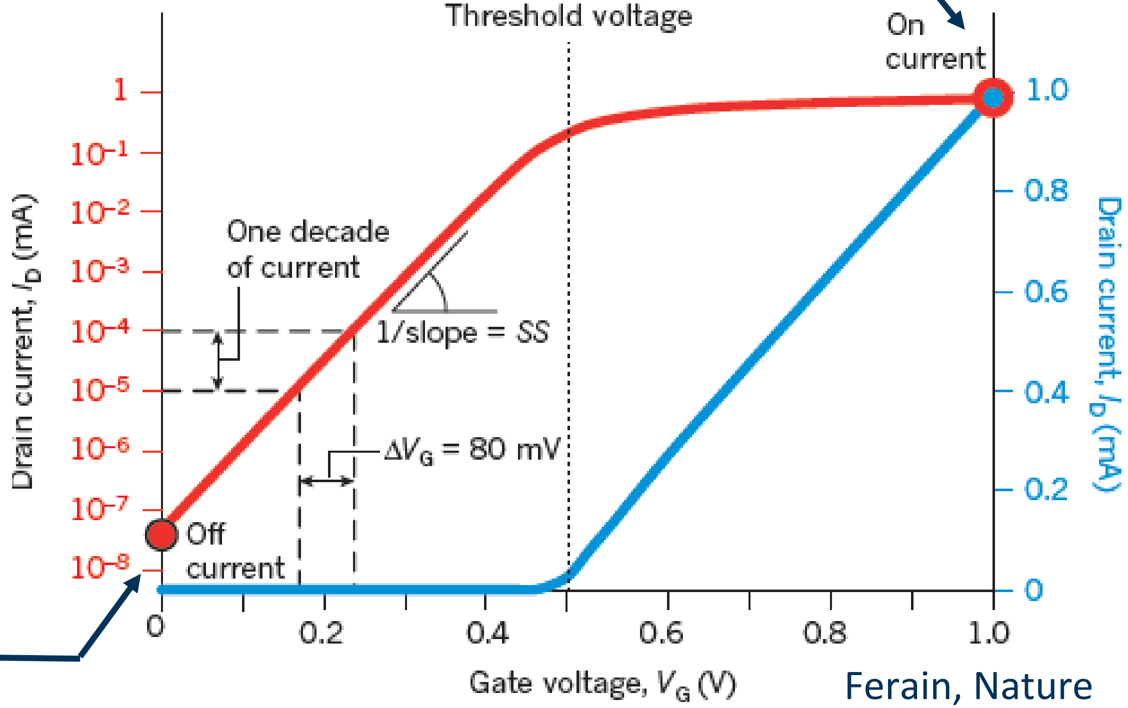
FS, Nature Nanotechnol. 5, 487 (2010), updated.

- So far: Only one single device type – MOSFET.
- So far: Only one single semiconductor – Si.
- So far: Only one single technology – Si CMOS (complementary MOS, n-channel and p-channel Si MOSFETs).
- The problem: An end of the Si MOSFET scaling is in sight!

FET Basics – Digital CMOS



On-state

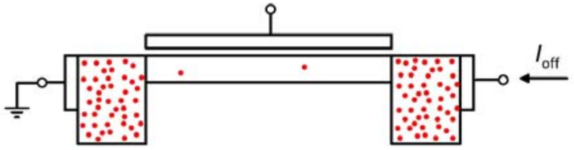


Ferain, Nature 479, 310 (2011).

Requirements for logic

- High on-off ratio I_{on}/I_{off} $10^4 \ldots 10^7$.
- High I_{on} (high speed).
- Low I_{off} (low static power).
- Steep slope in sub-threshold, i.e., small *SS*.

Off-state



Long channels: $I_{off} \propto \exp \dfrac{-E_G}{m\, k_B\, T}$

A sizeable gap is mandatory!

Trends in More Moore

High on-current I_{on}

- High carrier mobility μ needed, introduction of high-μ light-m_{eff} channels.

Low off-current I_{off} and small $\boldsymbol{SS}$

- Good electrostatic integrity required to suppress short-channel effects, a short scale length λ is beneficial.

$$\lambda = \sqrt{\frac{\varepsilon_{ch}}{\varepsilon_{bar}} t_{ch} \, t_{bar}}$$

λ expression for single-gate SOI MOSFETs
Yan et al., TED 39, 1704 (1982).

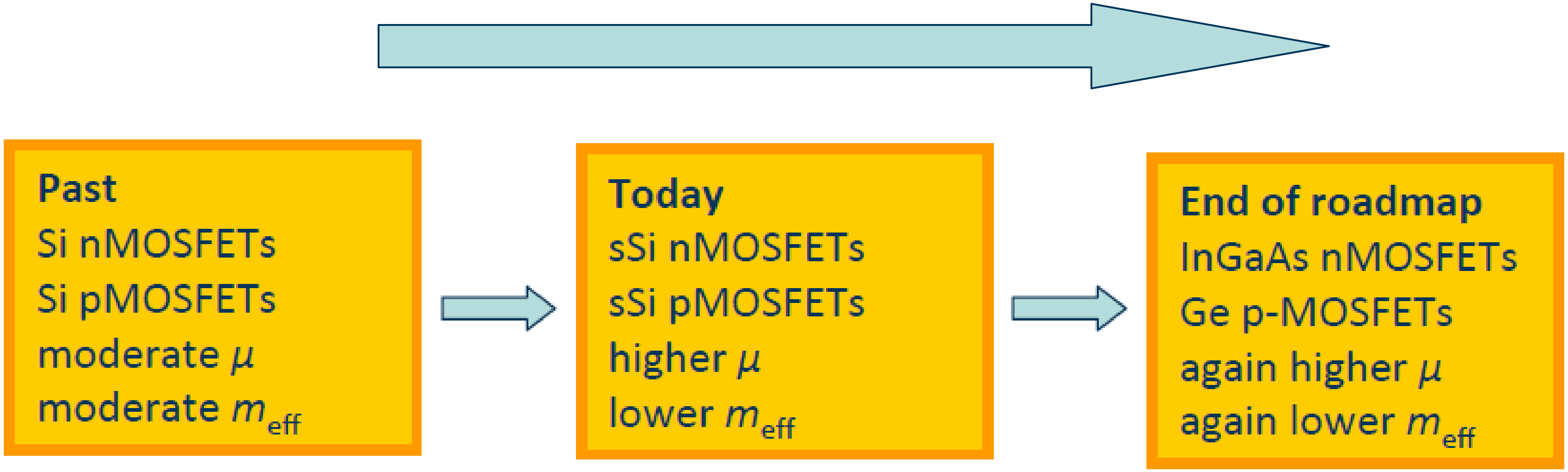
Expressions for other MOSFET architectures (multi-gate, nanowire, 2Ds) have been elaborated.

In any case: Thin and narrow channel regions favorable. Introduction of ultra-thin body SOI, multi-gate, and possibly 2D MOSFETs.

- Suppression of direct source-drain tunneling.
  - Currently ($L \geq 10$ nm) not a problem.
  - Will become an issue at ultra-short gate length levels.

Trends In More Moore

A trend today: High-μ channel materials for Si-based CMOS.
Higher mobility to enhance on-current and transistor speed.



Past
Si nMOSFETs
Si pMOSFETs
moderate μ
moderate m_{eff}

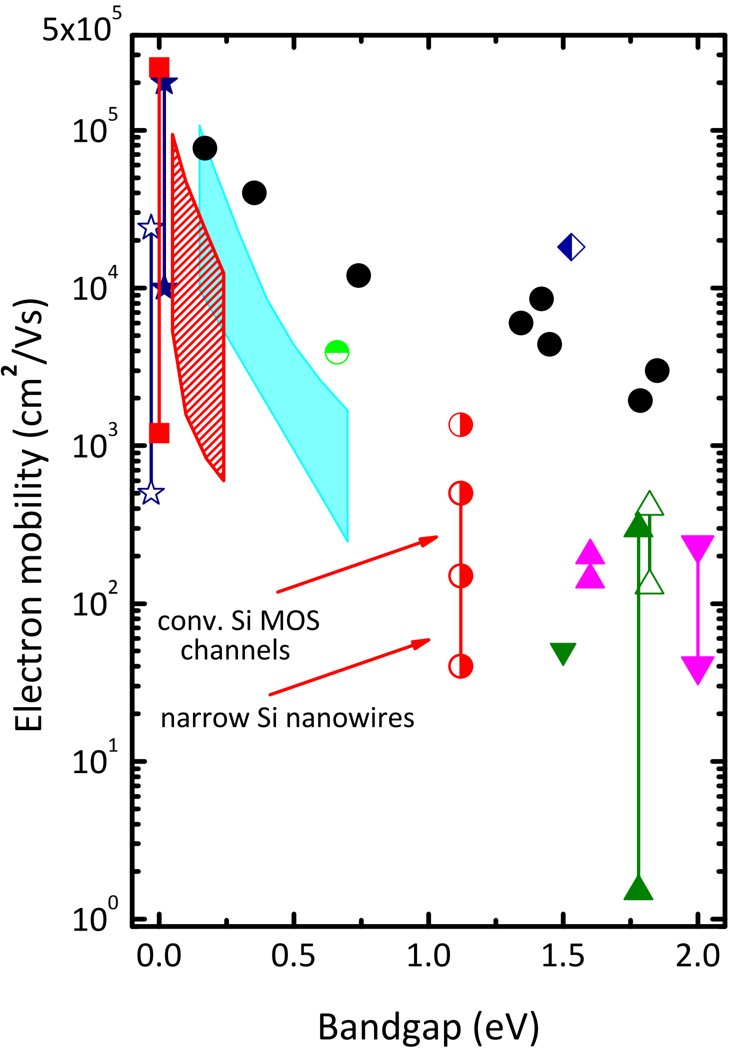
Today
sSi nMOSFETs
sSi pMOSFETs
higher μ
lower m_{eff}

End of roadmap
InGaAs nMOSFETs
Ge p-MOSFETs
again higher μ
again lower m_{eff}

- Strained Si (sSi) with enhanced μ & lower m_{eff}.
- 2003: Intel introduced sSi into mass production.
- Today: All major chip-makers use sSi.

- Expectation (ITRS 2013): High-µ channel materials in production around 2018.
- InGaAs for nMOS.
- Ge for pMOS.

Mobility vs Bandgap



- The hole mobility (not shown) exhibits a similar trend.
- Regarding mobility, the 2Ds do not show a distinct advantage over the conventional 3D bulk materials. HOWEVER, …

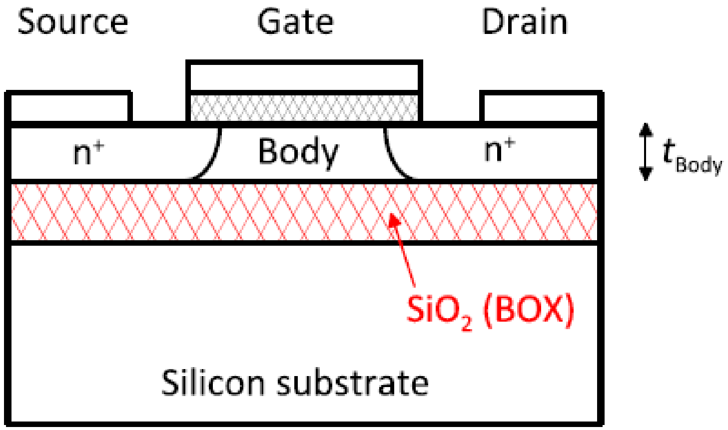
Electron mobility of different semiconductors vs bandgap.
FS, Proc. IEEE 101, 1567 (2013), updated; FS, Nature Nanotechnol. 5, 487 (2010), updated.

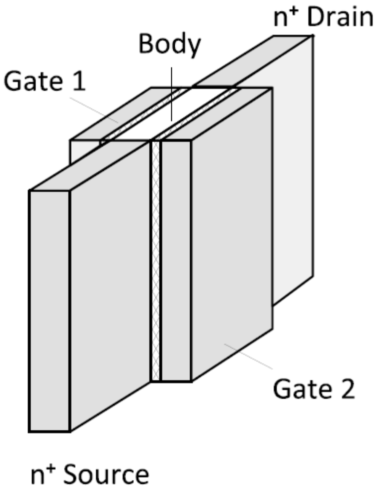
Mobility

… However, to maintain good electrostatic integrity,

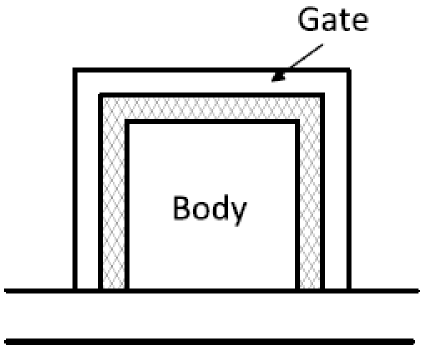
(i) UTB SOI MOSFETs
(ultra-thin body)

(ii) Multiple-gate MOSFETs
with narrow bodies, such as
FinFETs, nanowire FETs, etc.





FinFET



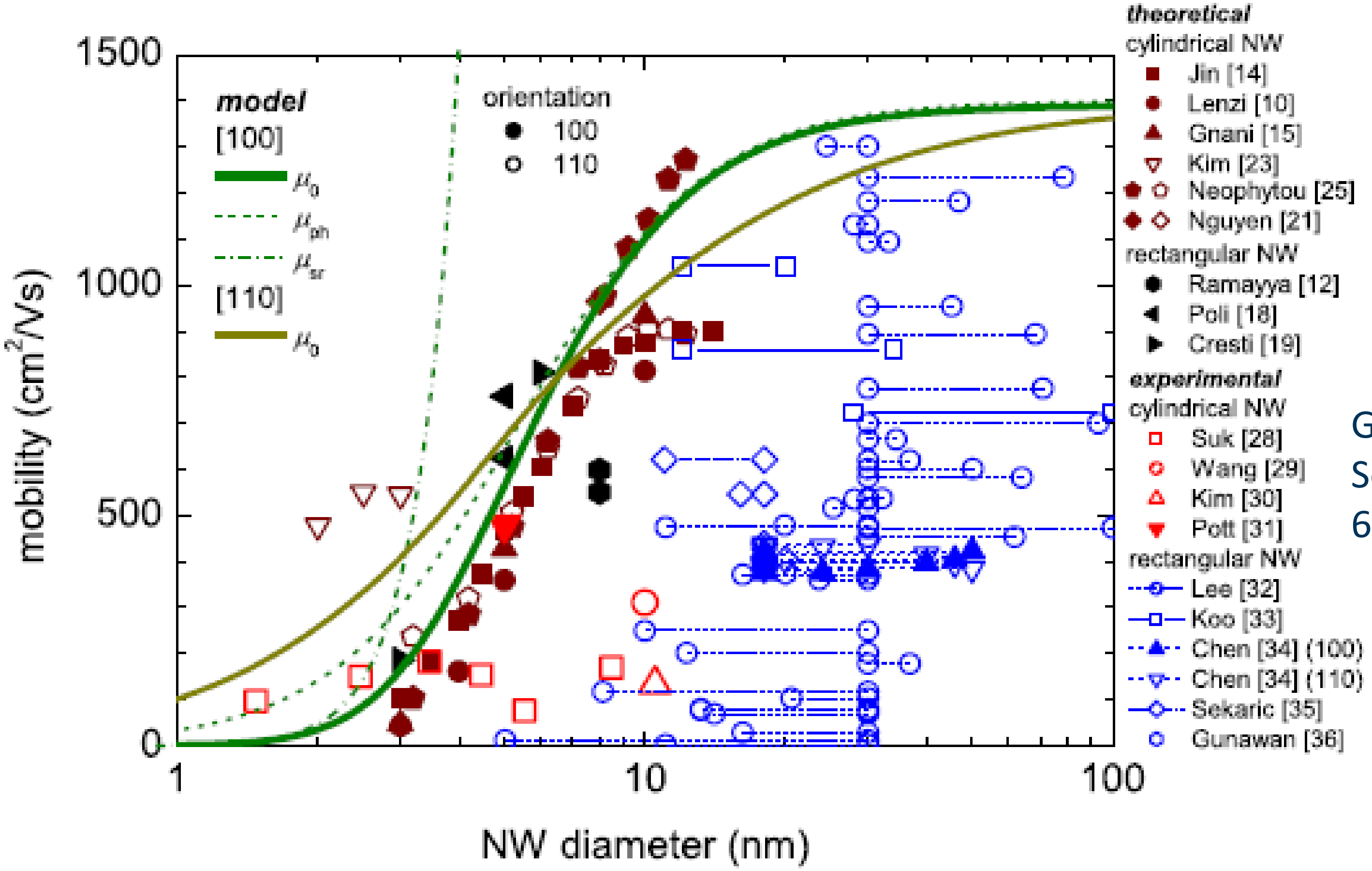
Tri-Gate FET

FS, H. Wong, and & Liou, Pan Stanford (2010).

replace the conventional single-gate bulk MOSFET.

Thin & narrow bodies ↷ reduced mobility.

Mobility



Granzner, Polyakov, Schippel & FS, IEEE TED 61, 3601 (2014).

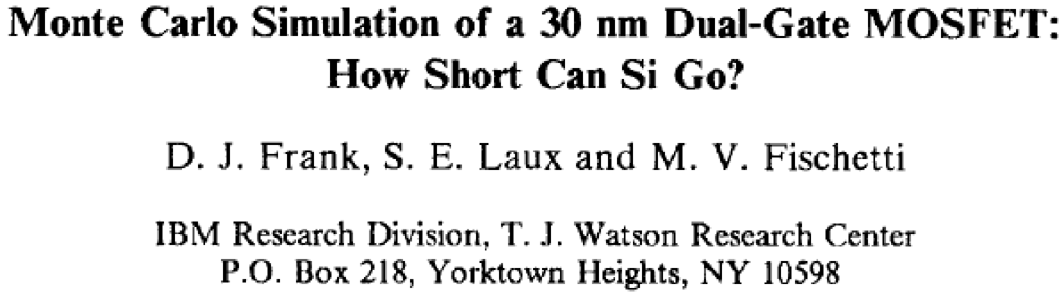
Severely degraded electron mobility in small-diameter Si nanowires.

⇩

The picture gets less cloudy for the 2Ds. The 2Ds are by nature ultimately thin

A View Beyond the ITRS Horizon

- How far can the MOSFET be scaled? Unclear at present.
  Many problems: - Degraded electrostatics, degraded switch-off.
  - Variability and processing issues
  - Economic issues, cost.
- We remember: The 2013 edition of the ITRS requires 5-nm gate MOSFETs for the year 2028.
- One could say “5-nm MOSFETs – this is wishful thinking“, BUT the same has been said about 30-nm MOSFETs 20 years ago.



Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go?

D. J. Frank, S. E. Laux and M. V. Fischetti

IBM Research Division, T. J. Watson Research Center
P.O. Box 218, Yorktown Heights, NY 10598

IBM paper at IEDM 1992.

Note: In 1992, 500-nm single-gate MOSFETs have been in production.

- Production-stage 5-nm CMOS should not be ruled out. Let us be optimistic and assume the MOSFET can be scaled to sub-5-nm.

A View Beyond the ITRS Horizon

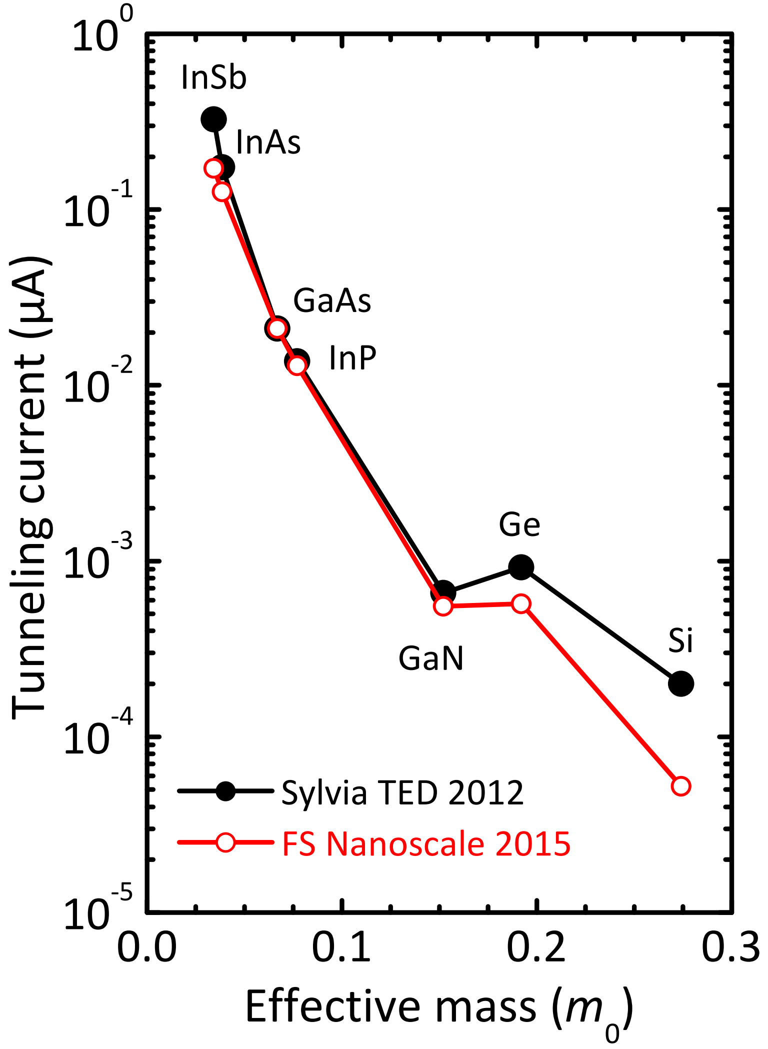
Meanwhile several theoretical studies on 5-nm gate MOSFETs:

- Luisier et al., IEDM, 251 (2011).
- Alam & Lake, IEEE TED 59, 3250 (2012).
- Sylvia et al., IEEE TED 59 2064 (2012).
- Mehrotra et al., IEEE TED 60, 2171 (2013).
- Luisier & Szabo, ULIS, 53 (2013).

- etc.

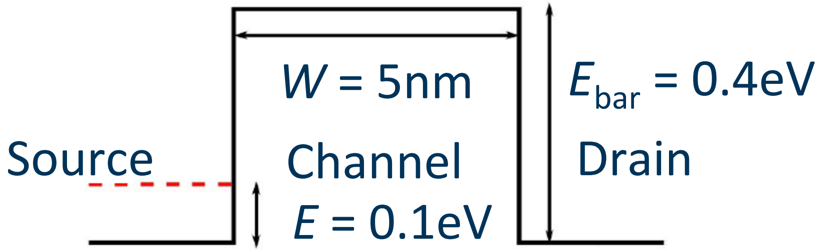
- Consistent conclusion: At 5-nm and below gate lengths levels, ***source-drain tunneling will become an issue***.
- Tunneling ⟶ degraded *SS* and switch-off, high I_{off}.
- High-μ, i.e., light-m_{eff} narrow-gap channel materials are expected to fail.
- Heavy-m_{eff} materials (with lower μ and wider gap) are expected to become favorable.

5-nm NW MOSFETs – Source-Drain Tunneling



Tunneling current in 5-nm gate length, 6-nm diameter nanowire MOSFETs.

Our approach: Simple textbook expressions, critical input data from a more elaborated study (Sylvia et al.)



$$TC = \left[1 + \frac{E_{bar}^2 \sinh\left(|k| W\right)}{4E\left(E_{bar} - E\right)}\right]^{-1}$$

$$k = \sqrt{2 m_{eff} \left(E_{bar} - E\right)} / \hbar$$

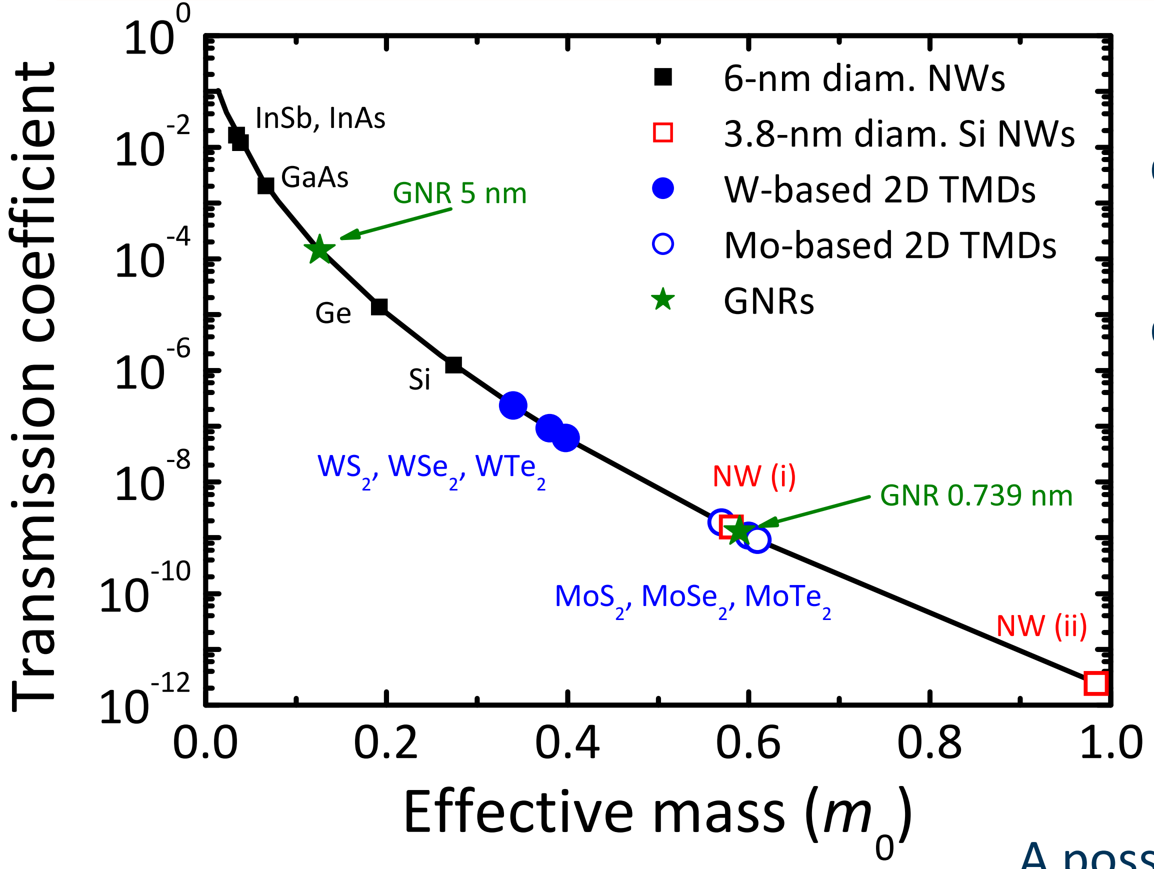
$$I_{tun} \approx c \times M \times TC$$

M : Conduction band degeneracy factor
4 for Si and Ge NWs, 1 for III-V NWs.

c: a constant, here 10.4 µA.

Our simplified approach reproduces the trend reported by Sylvia et al. nicely.

5-nm MOSFETs – Source-Drain Tunneling



NW(i): <110> Si, 3 GPa compressive strain.

NW(ii): <100> Si, 2 GPa compressive strain.

Si remains a strong contender!

m_{eff} for 3.8-nm Si NWs: Mehrotra et al., TED 60, 2171 (2013).

A possible scenario for the selection of MOSFET channel materials.

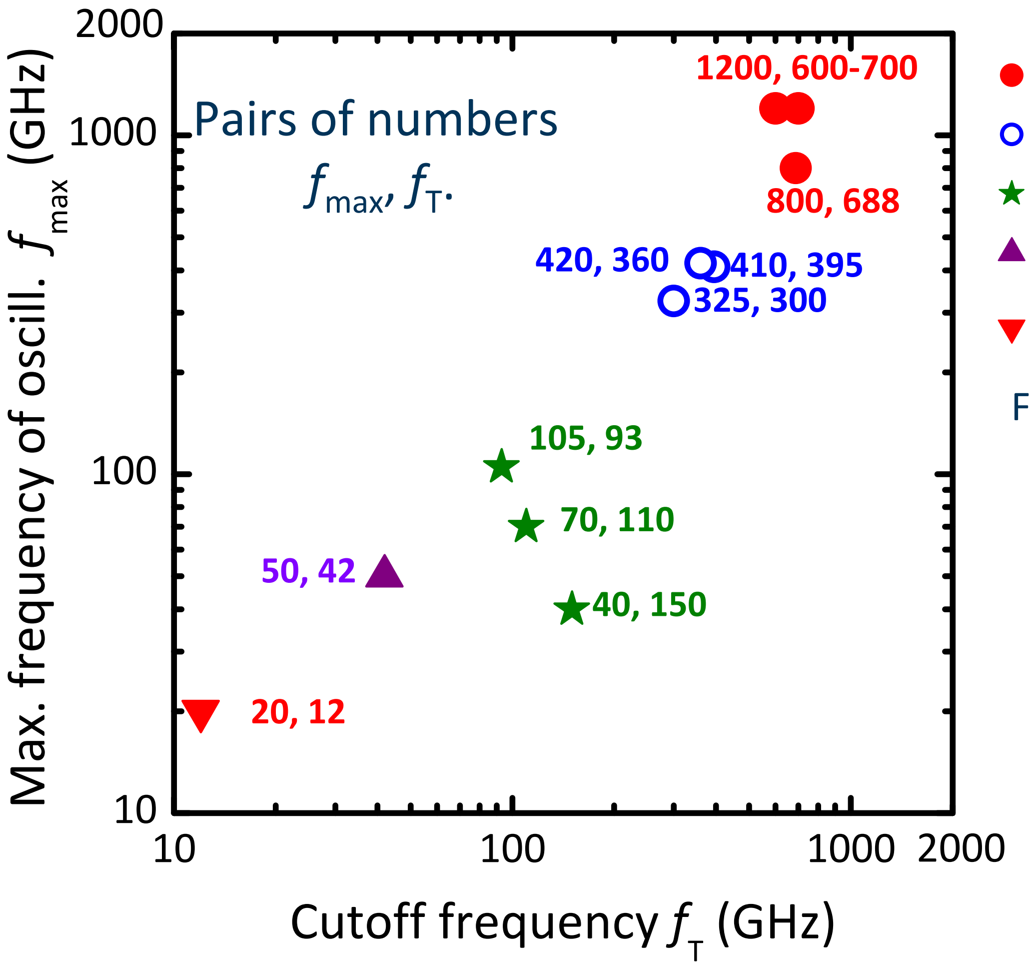
Past
Si nMOS
Si pMOS
Moderate μ
Moderate m_{eff}

Today
sSi nMOS
sSi pMOS
Higher μ
Lower m_{eff}

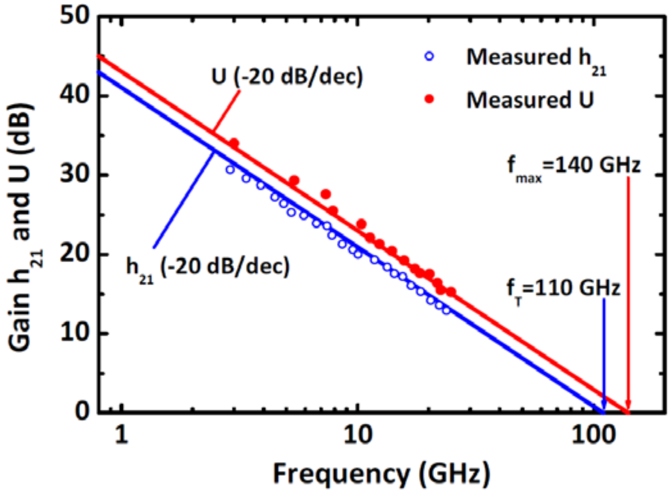
End of roadmap
III-V nMOS
Ge pMOS
Even higher μ
Even lower m_{eff}

Beyond roadmap
$L \leq 5$ nm
2Ds or Si NWs or GNRs
Low μ
High m_{eff}

2D Transistors for More Than Moore – RF



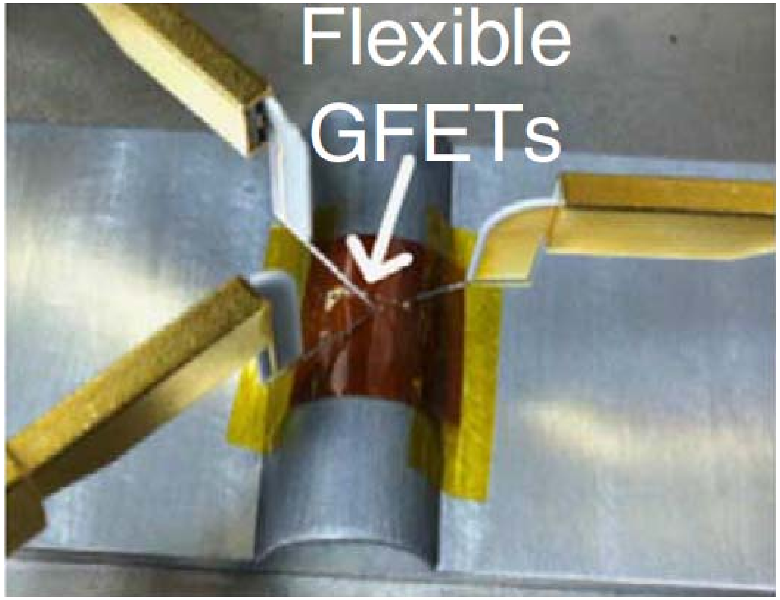
FS, Nature 472, 42 (2011), updated.



2D transistors

- Are definitely capable of RF operation.
- Cannot compete with high-performance III-V and Si RF transistors.

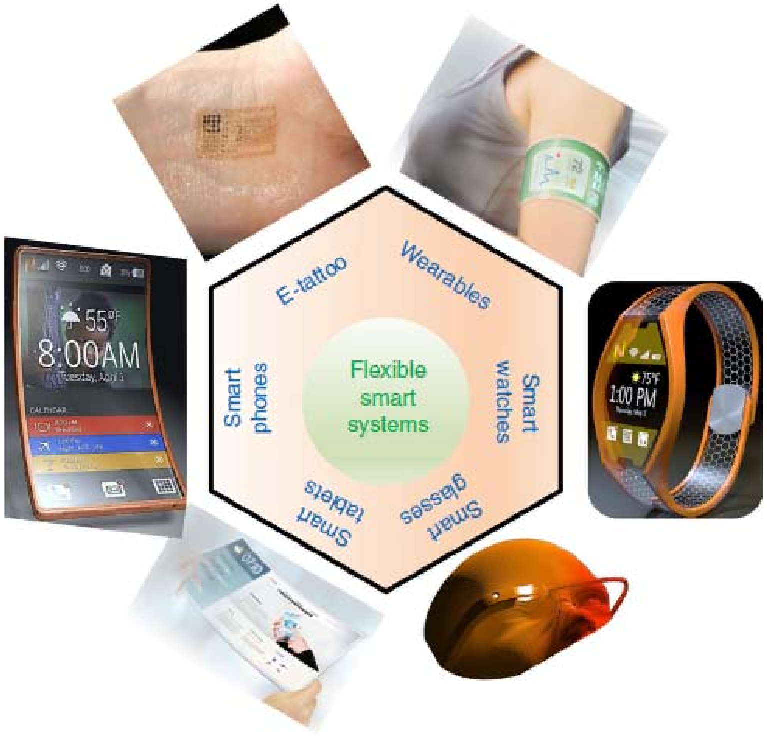
2D Transistors for More Than Moore – Flexible



Flexible Graphene FETs
Akinwande et al., Nat. Comm. 5, 5678 (2014).

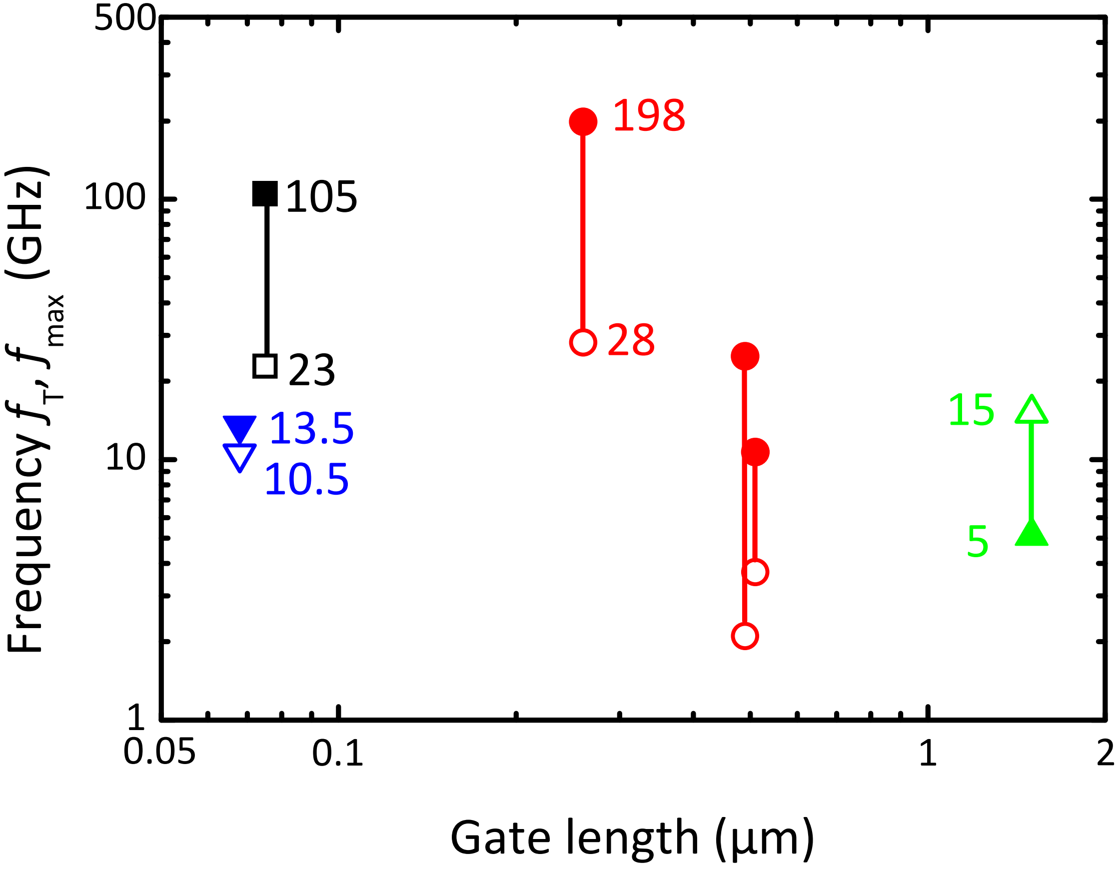
Promising:

- Flexible Graphene FETs for RF
- Flexible TMD FETs for digital logic and RF



Applications for flexible electronics
Akinwande et al., Nat. Comm. 5, 5678 (2014).

2D Transistors for More Than Moore – Flexible



Another competitor:
Organic semiconductors
- Ultra-low mobility.
- Slow (record f_T 27 MHz (L = 2 µm).

Data compiled from the literature.

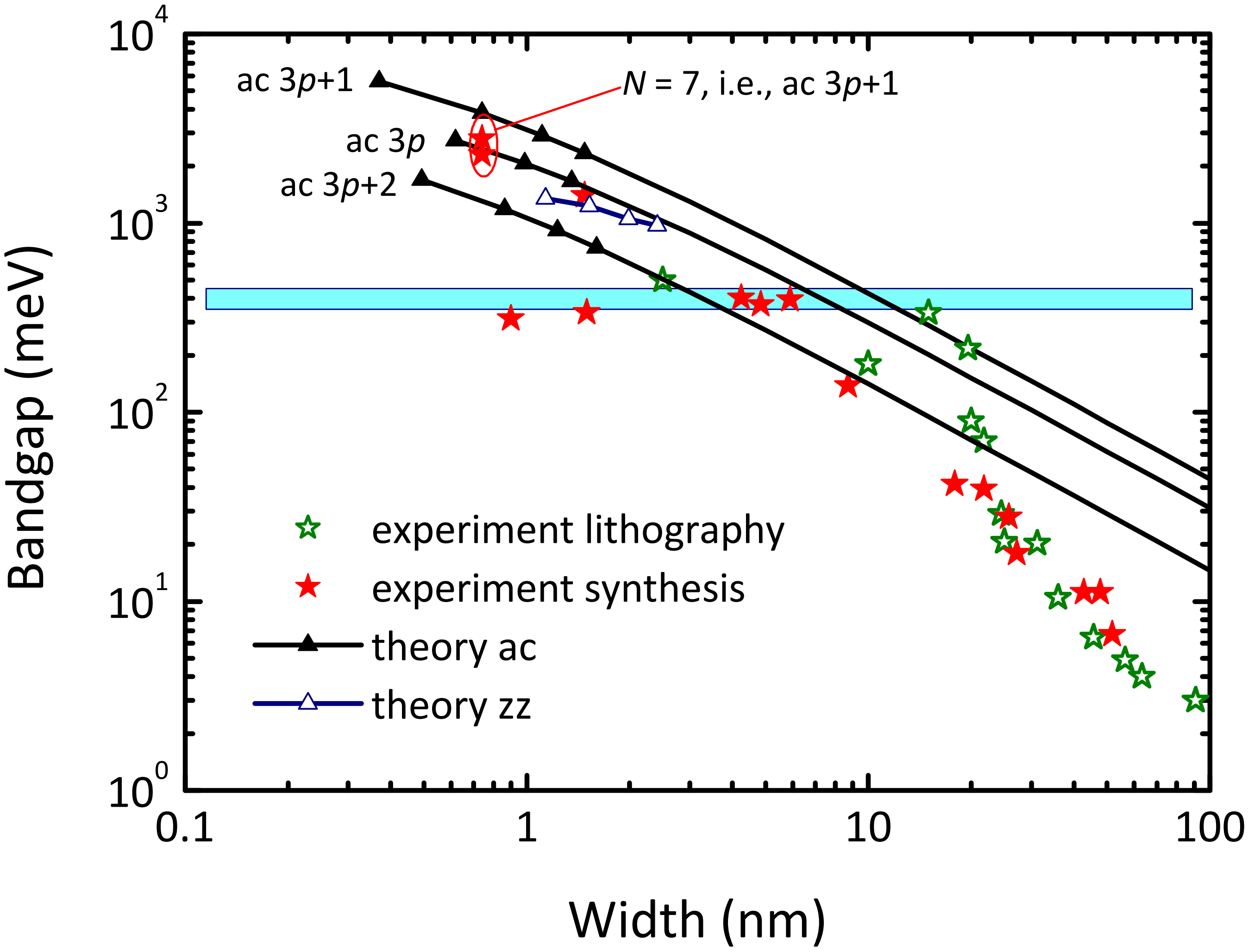
- Flexible 2D transistors perform VERY competitive!
- The 2Ds are flexible – and it is more elegant and more reasonable to use a flexible-by-nature material for flexible electronics.

Metrology Needs for 2D Electronics

Processing 2D transistors and circuits (with the exception of starting material preparation) is based on the well-established Si technology. Thus, many metrology needs for 2D electronics are the same as those for Si technolgy. There are, however, several additional needs, such as

- Analysis of crystallographic structure of 2D layers (at atomic level).
- Identification of the layer number of 2D sheets.
- Accurate measurement of width, edge configuration, and bandgap of narrow GNRs.
- Correct extraction of the mobility of top-gated 2D MOS channels.
- Analysis of the properties of contacts metal – 2D materials (contact type, i.e., Schottky or Ohmic, contact resistance).
- Measurement of heat transport properties of 2D materials: thermal conductivity and thermal boundary resistance (between 2D materials and the substrate/insulator underneath).

Metrology Needs – GNR Gap vs Width

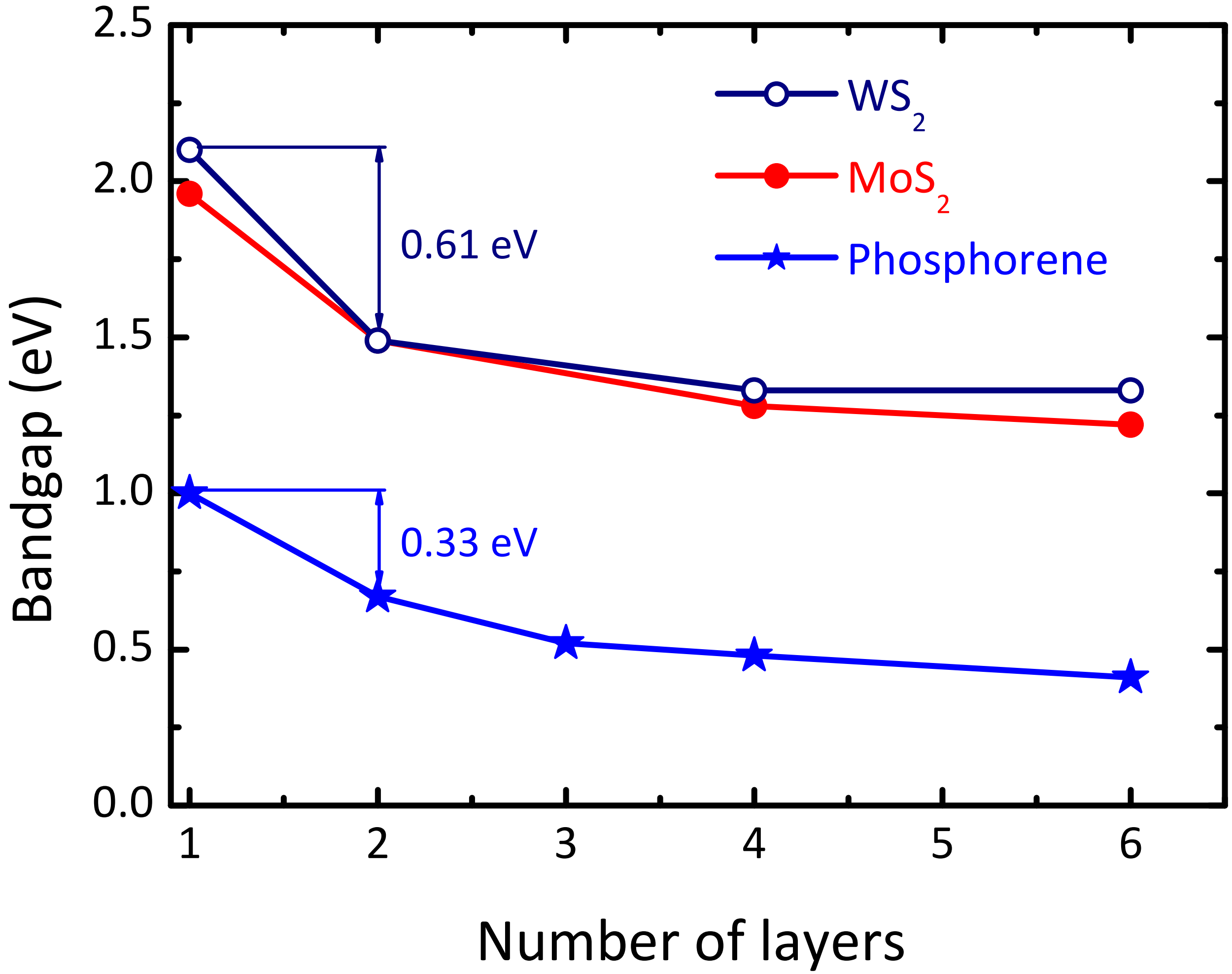


GNR bandgap vs width.

FS, Pezoldt, Granzner, Nanoscale 2015.

The bandgap of GNRs depends strongly on the ribbon width and the edge configuration!

Metrology Needs – Gap vs Layer Number



Data compiled from the literature.

- Kuc et al., Phys. Rev. B 83, 245213 (2011)
- Liu et al., ACS Nano 8, 4033 (2014).

For many 2D materials, the gap varies significantly when the number of layers changes.

Conclusion

- **The 2D materials are DEFINITELY promising for many applications.**
- **2D MOSFETs for More Moore**
    - No significant impact expected in the near to medium term, i.e., within the current ITRS horizon ($L > 5$ nm).
    - Potential beyond the ITRS horizon ($L \leq 5$ nm)
        - 2Ds offer short scale length and excellent electrostatics.
        - TMD and GNR MOSFETs: Efficient suppression of direct source-drain tunneling).
- **2D MOSFETs for More Than Moore**
    - Promising (already in the near to medium term) for flexible electronics, both digital and analog/RF.
    - 2Ds promising for printable and transparent electronics.

Conclusion

Metrology Needs

- Many of the metrology needs for 2D electronics are the same as for Si technolgy.
- There are, however, several additional needs regarding
  - Crystallographic structure of 2D layers at the atomic level.
  - Layer number of 2D sheets.
  - Width, edge configuration, and bandgap of narrow GNRs.
  - Mobility of top-gated 2D MOS channels.
  - Properties of contacts metal – 2D materials (contact type,
  - Heat transport properties.

Acknowledgement

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