

Atomic Layer Deposition of High-k Dielectric and Metal Gate Stacks for MOS Devices

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Accelerating the next technology revolution.

Outline

1. Introduction

2. ALD of High-k Dielectric

- High-k dielectric ALD processes
- Electrical properties of MOS devices
- Scaling the Hf-based dielectric

3. ALD of Metal Gate

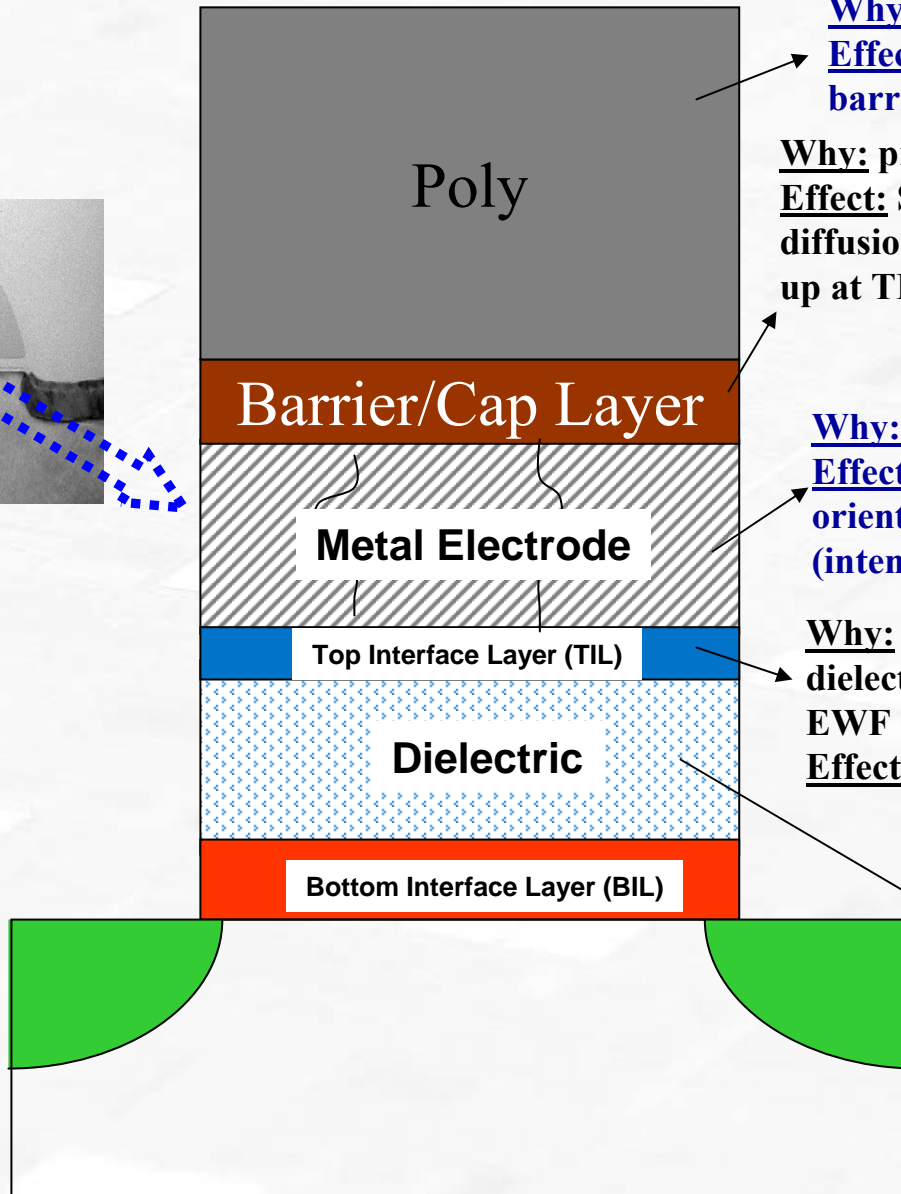
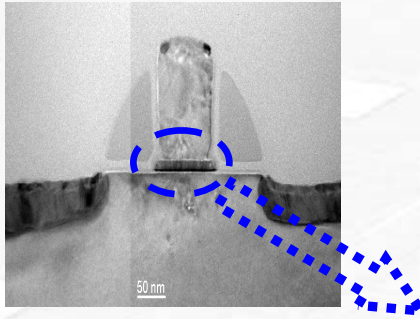
- ALD Metal Nitrides - TiN, HfN, HfSiN, TaN
- Work function evaluation

MOSFET Device Goals for 45 nm node and beyond

Application	EOT (nm)	CET (nm)	Jg (A/cm ²)
High Performance (HP)	≤ 0.8	≤ 1.2	≤ 100
Low Standby Power (LSTP)	≤ 1.6	≤ 2.4	$\leq 2.2 \times 10^{-3}$

- Density of interface traps (D_{it}) $\leq 5 \times 10^{10}$ # / cm²·eV
- High frequency (100kHz) CV hysteresis ≤ 10 mV
- $V_t \pm 0.2V$ of control SiO₂ with same EOT
- V_t stability $\pm 10mV$ of unstressed film
- Mobility $\geq 90\%$ of SiO₂ at EOT 0.8nm
- Defect Density ≤ 0.14 defects / cm²
- Thermal stability (physical and electrical) at 1000°C, 5 sec
- Thickness uniformity (3 sigma) $\leq 4\%$
- Reliability comparable to SiO₂

Factors That Influence Metal Electrode Properties



Why: Ease of integration

Effect: Stress ?, Reaction with electrode if no barrier layer ?

Why: prevent interaction between Electrode and Poly;
Effect: Stress ?, Reaction with metal electrode? Metal diffusion through electrode grain boundary and pile up at TIL ? Overlay effect if electrode very thin ?

Why: Control WF, EOT scaling (no poly depln)

Effect: main contributor to WF , Crystallinity, grain orientation, thickness effect? Overlay effect if TIL (intentional) very thin ?

Why: Unintentional (due to reaction of metal with dielectric); Intentional (dual metal integration and EWF control via overlay effect)

Effect: controls EWF if TIL forms

Why: High-k for scaling

Effect: reaction with metal to form TIL + Fermi level pinning, fixed charges shift V_{fb} shift.

Introduction: Why Metal ALD ?

- Why metal electrodes?
 - ✓ **poly electrode depletion** limits device scaling
 - ✓ poly electrode can interact with high-k materials
- Why ALD metal electrodes?
 - ✓ **Excellent thin film thickness uniformity control**
 - ✓ **Excellent composition control**
 - ✓ **Little damage to gate oxide (compared to PVD)**
 - ✓ **Low temperature deposition with low impurity**
 - ✓ **Conformality at nanoscale structures and potentially 3-D devices**
- Multiple potential applications for ALD metal films
 - ✓ **Metal gate electrode:** TaN, TiN, W, Ru..
 - ✓ **Cu diffusion barrier/adhesion promoter:** TaN, Ta, TaSiN, TiN, WN..
 - ✓ **Cu seed layer:** Cu
 - ✓ **Plug for via hole:** W, WN_x
 - ✓ **Barrier:** TiN, Ti

Gate “ELECTRODE” Specifications

Application	EFW (n metal)	EFW (p metal)
CMOS on bulk Si	4.1 +/-0.05	5.2 +/-0.05
CMOS on FDSOI, FINFET	4.4 +/-0.05	4.9 +/-0.05

- Gate stack subjected to S/D dopant activation anneal (1000 C, 5 sec)
- $V_t \pm 0.1$ V of control SiO_2 with same EOT
- V_t stability ± 10 mV of unstressed film
- Mobility $\geq 95\%$ of SiO_2
- Density of interface traps (D_{it}) $\leq 5 \times 10^{10}$ # / $\text{cm}^2 \cdot \text{eV}$
- High frequency (100kHz) CV hysteresis ≤ 10 mV
- Reliability comparable to Poly/ SiO_2
- Defect Density ≤ 0.14 defects / cm^2
- Thickness uniformity (3 sigma) $\leq 4\%$

ALD Processes: Metal-Organic Liquid Precursors for HfO₂

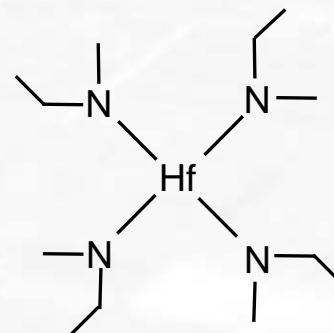
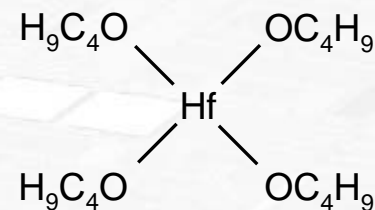
Hf-t-Butoxide $\text{Hf}(\text{C}_4\text{H}_9\text{O})_4$
Dep. Rate: 0.24Å/cycle

TEMAHf (Tetrakisethylmethyl
amino hafnium) $\text{Hf}(\text{NMeEt})_4$

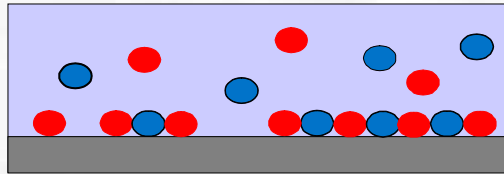
Dep. Rate: 0.89Å/cycle
Less impurities in the HfO₂ films
Lower leakage current of HfO₂

--> Precursor of choice

ECS Proceedings, 2003

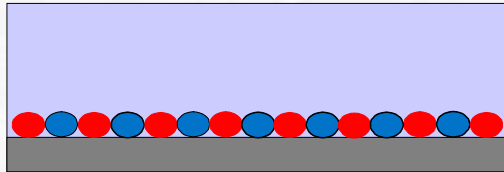


Precursor Co-injection ALD Concept for HfSiOx



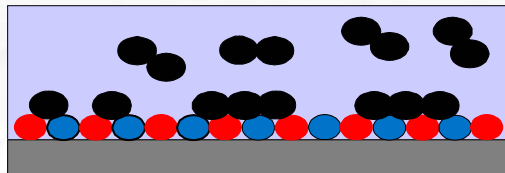
- $A+B(g)$
- Introduction of $A+B(g)$ onto the substrate surface

Introduction of $A(g) + B(g)$ onto the substrate surface



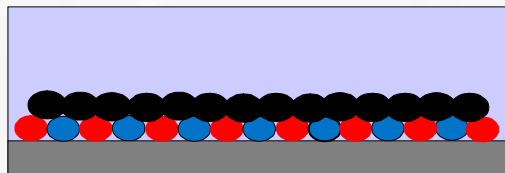
- $A+B(S)$
- Formation of an $A+B(s)$ monolayer surface

Formation of an $A+B(s)$ monolayer surface



- $C(g)$
- Introduction of $C(g)$ onto $A+B(s)$ surface

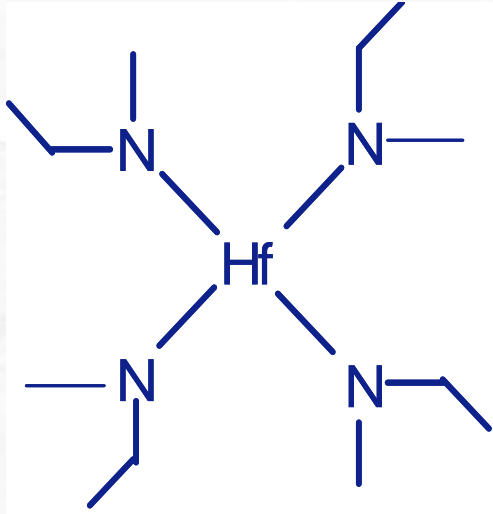
Introduction of $C(g)$ onto $A+B(s)$ surface



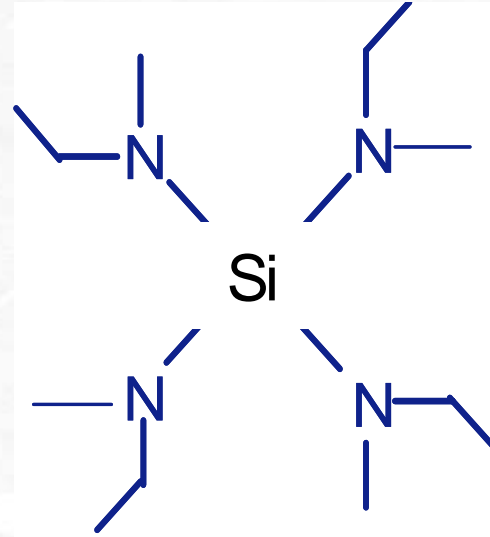
- $C(S)$
- Formation of $C(s)$ monolayer surface

Formation of $C(s)$ monolayer surface

HfSiO_x ALD Precursors



TEMAHf



TEMASi

Chemical compatibility

-> suppresses gas phase reaction

J. Vac. Sci. Technol. (A), vol. 22, p.1175 (2004).

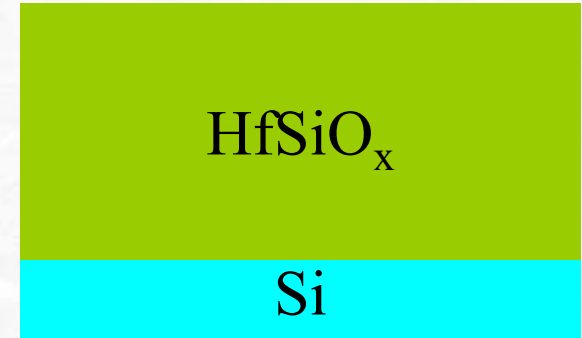
HfSiO_x ALD

Coinjection vs Nano-laminate

Precursor coinjection

Hf/Si pulse/purge

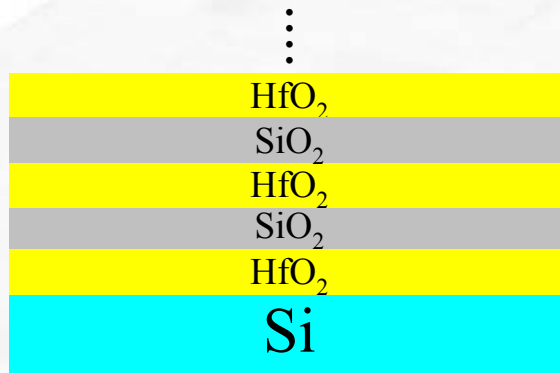
+ Oxidizer pulse/purge



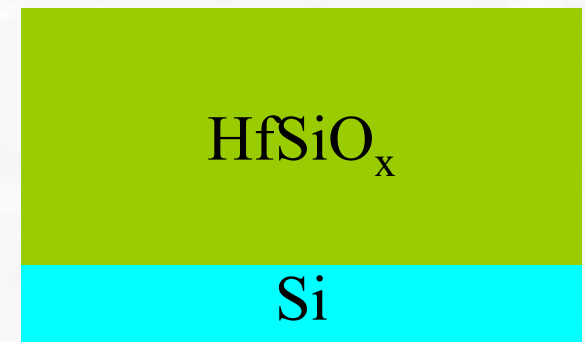
Nano-laminate

Hf pulse/purge + Ox pulse/purge

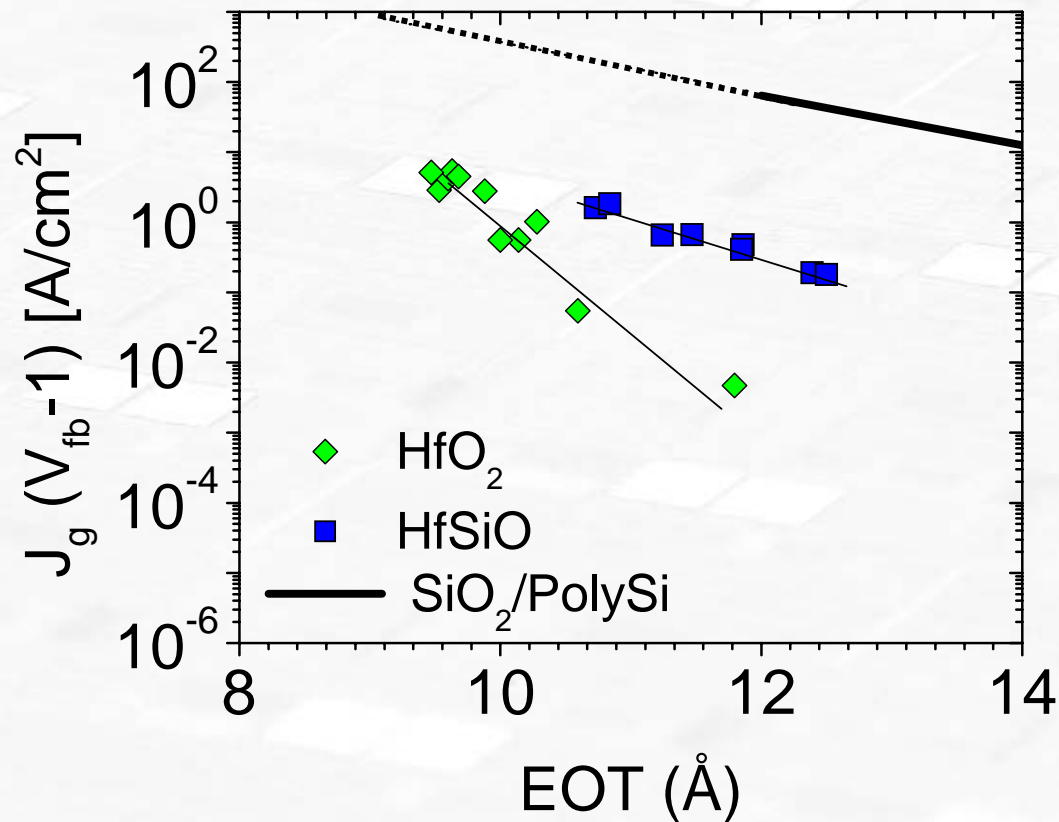
+ Si pulse/purge + Ox pulse/purge → → →



high temperature
anneal →

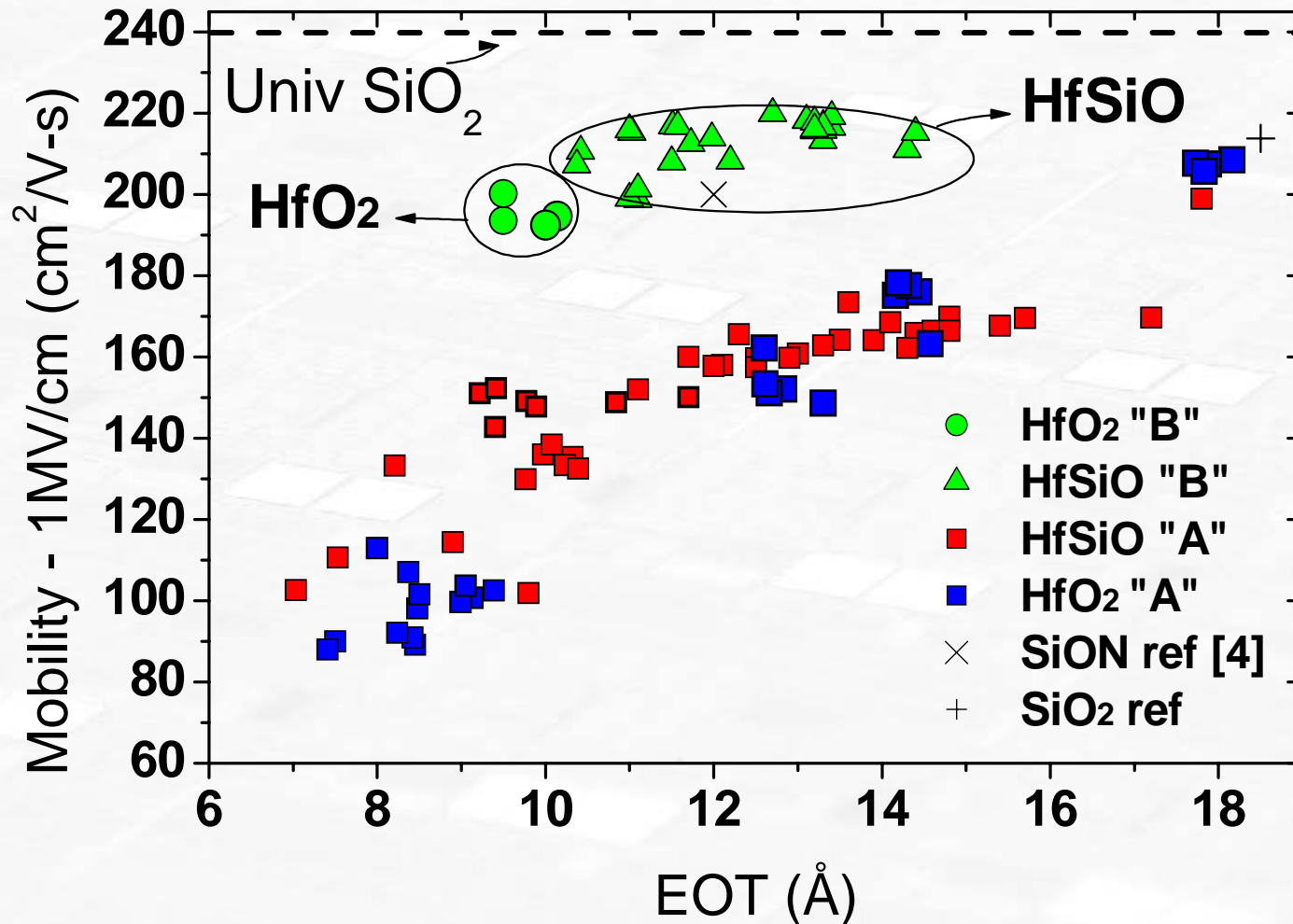


Leakage Current (J_g) Reduction of Hf(Si)O



J_g reduction: $10^2 - 10^3$ x vs. $SiO_2/PloySi$

Mobility Progress with HfO₂ and HfSiO

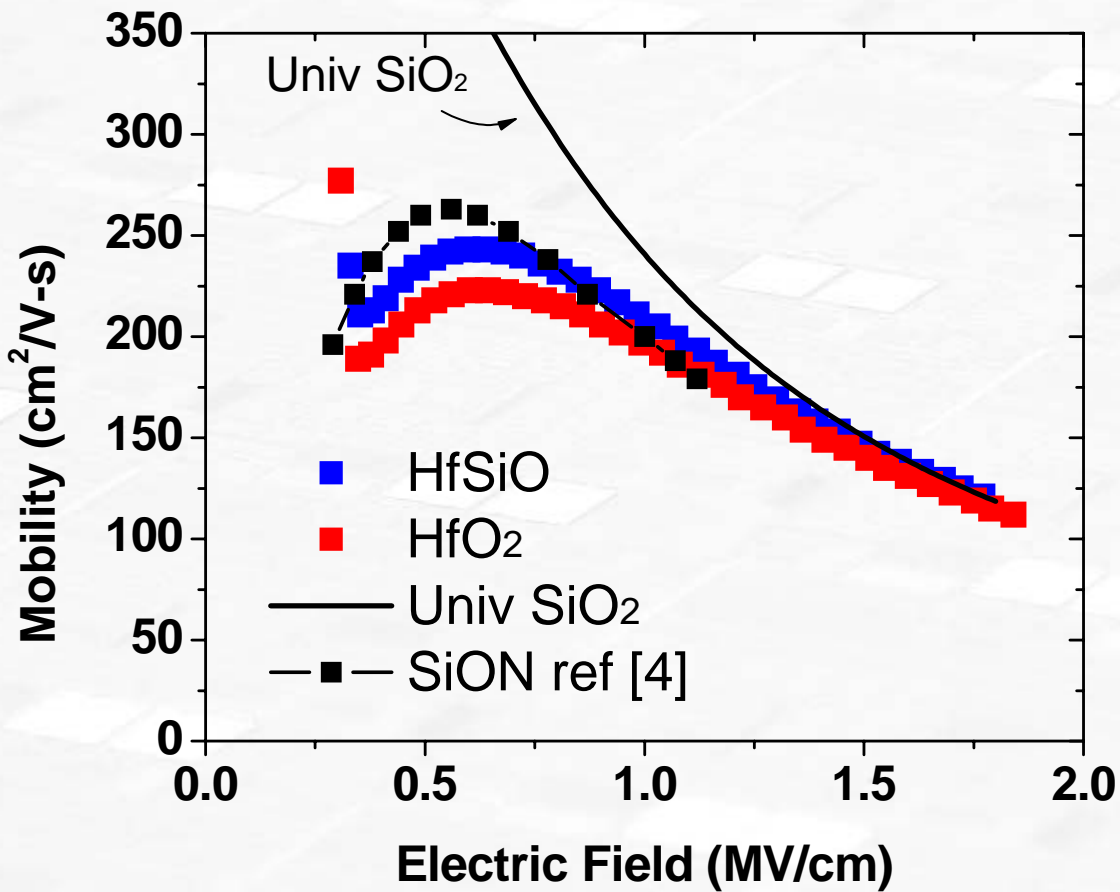


- HfO₂ and HfSiO show mobility results similar to nitrided oxide
- Significant improvement relative to historical dataset



[4] P.A. Kraus *et al.*, Semiconductor Fabtech v. 23, p. 73 (2004).

Mobility Progress at Peak and High Field



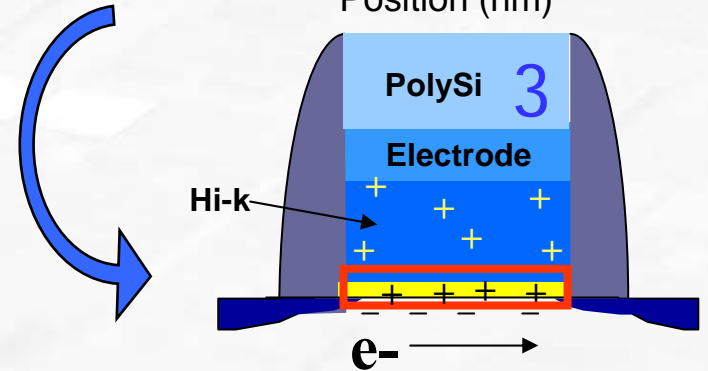
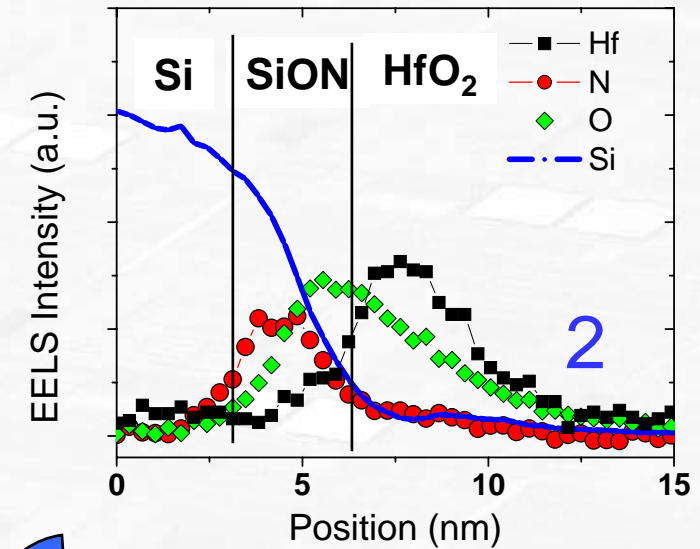
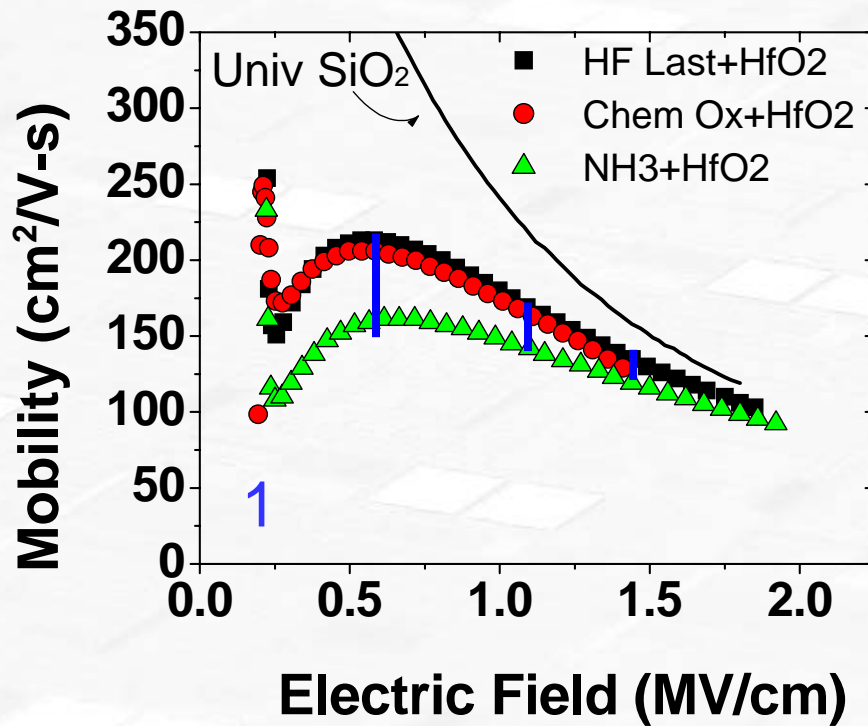
	SiON *	HfSiO
EOT (nm)	1.2	1.07
μ_{pk} (cm ² /V-s)	260	245
μ (1MV/cm) (cm ² /V-s)	200	210
J_g (A/cm ²) (V _t +1V) or (V _{fb} -1V)	150	1

- HfSiO performs similarly to SiON but with scaling benefit



* P.A. Kraus *et al.*, Semiconductor Fabtech v. 23, p. 73 (2004).

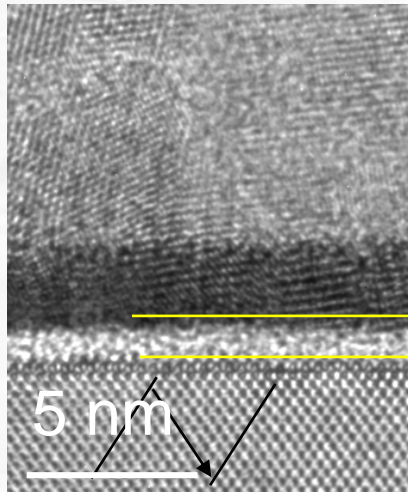
N Content in Interfacial SiON Layer



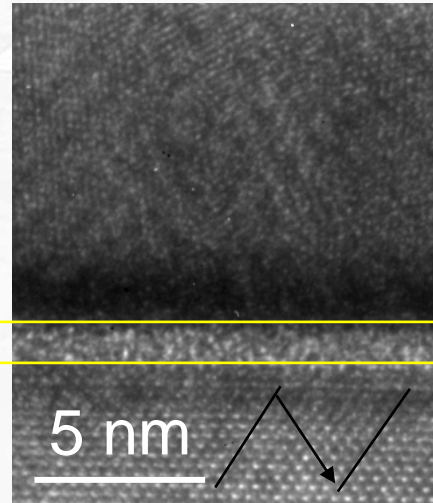
1. Mobility: NH₃ N in interfacial layer degrades mobility.
2. EELS: High N content near Si substrate (inversion layer).
3. -25% (peak μ) -15% (1MV/cm μ).

Similar Physical Thickness in SiO_x and SiON

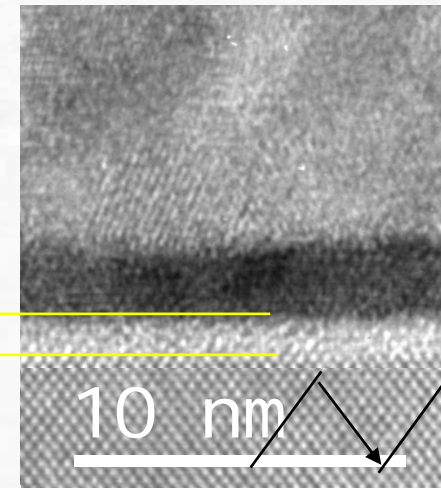
HF Last \HfO₂\TiN



O₃ \HfO₂\TiN



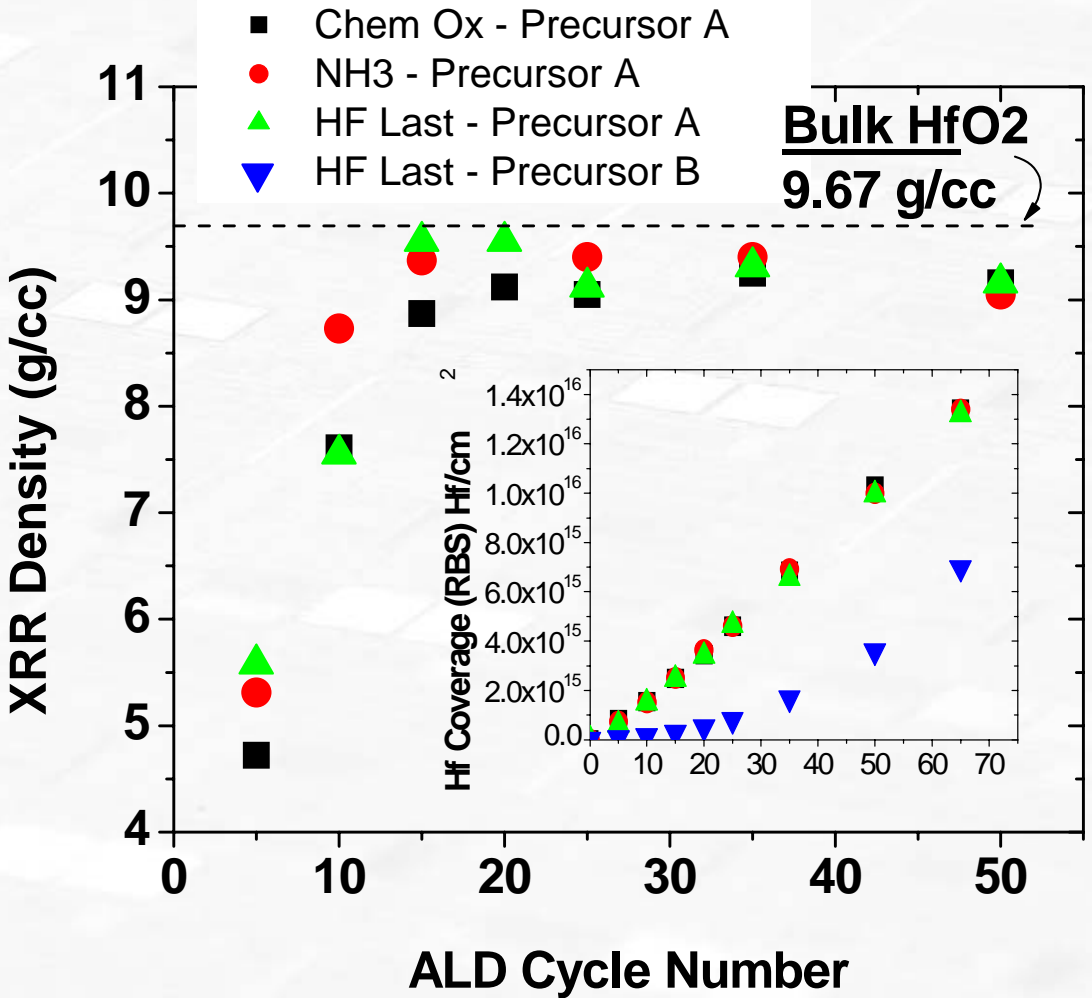
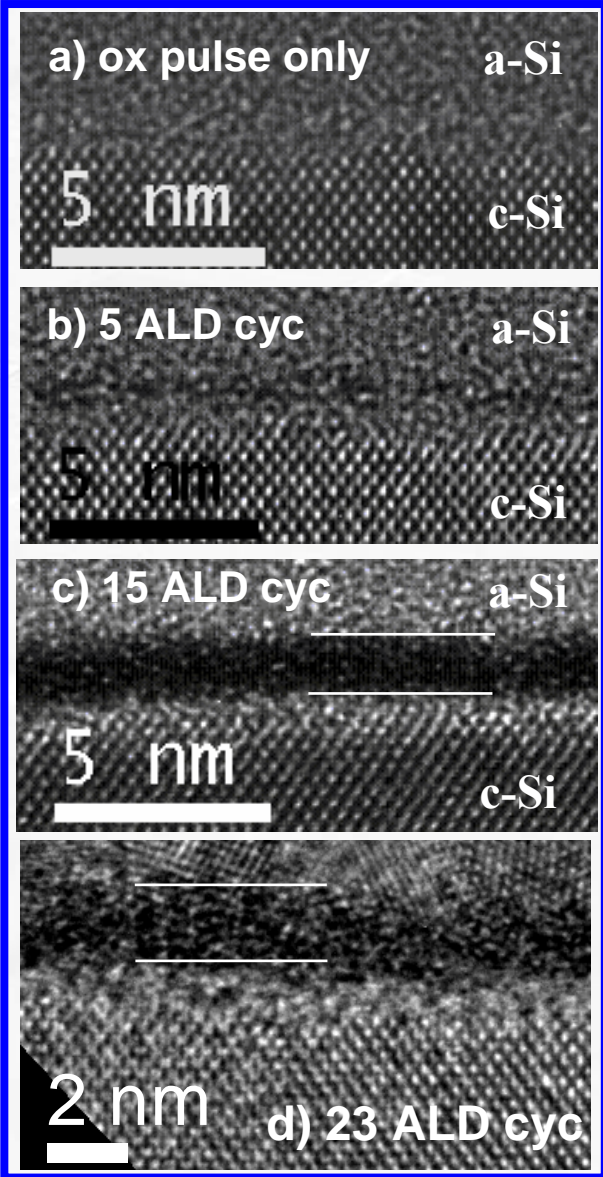
NH₃ \HfO₂\TiN



- After processing (1000C-5s), SiO(N) T_{phy} is similar (TEM is $\pm 2\text{\AA}$)
- Suggests fixed charge from N [rather than physical thickness screening effect] degrades mobility
- Consistent with peak / high field mobility results

Scaling the Hf-based dielectric

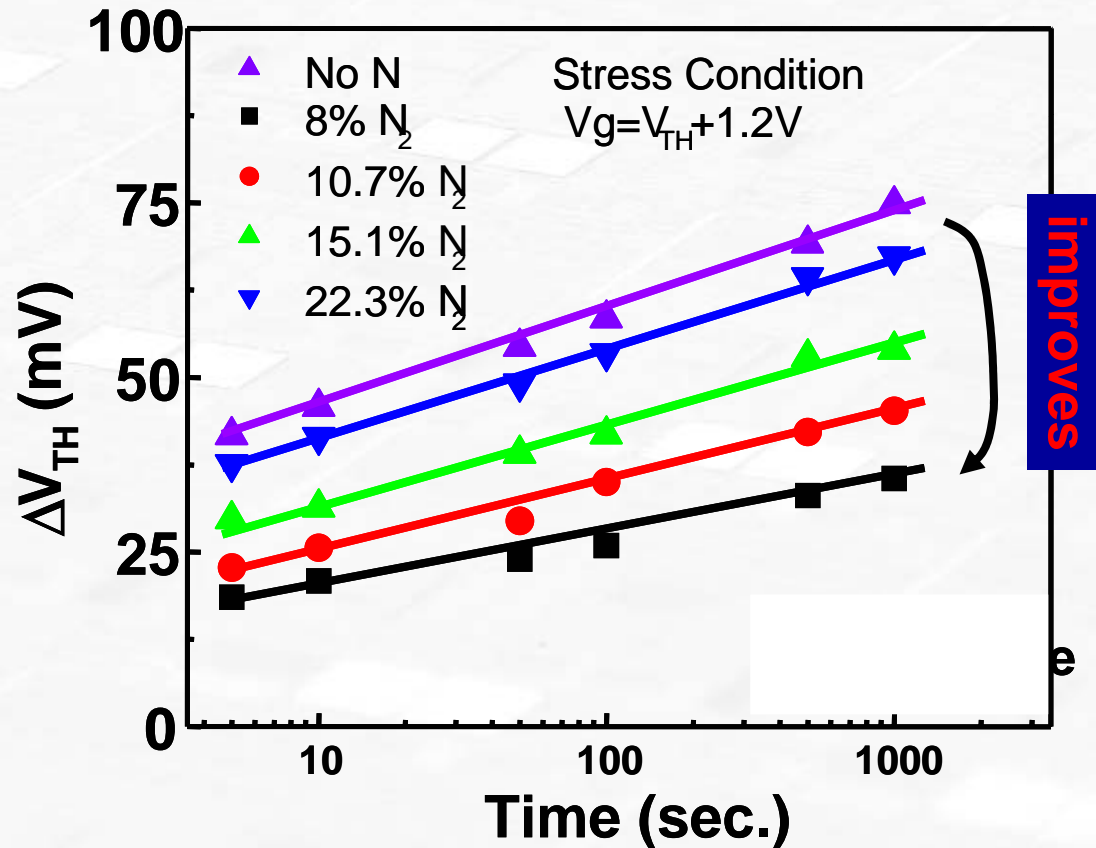
Blanket



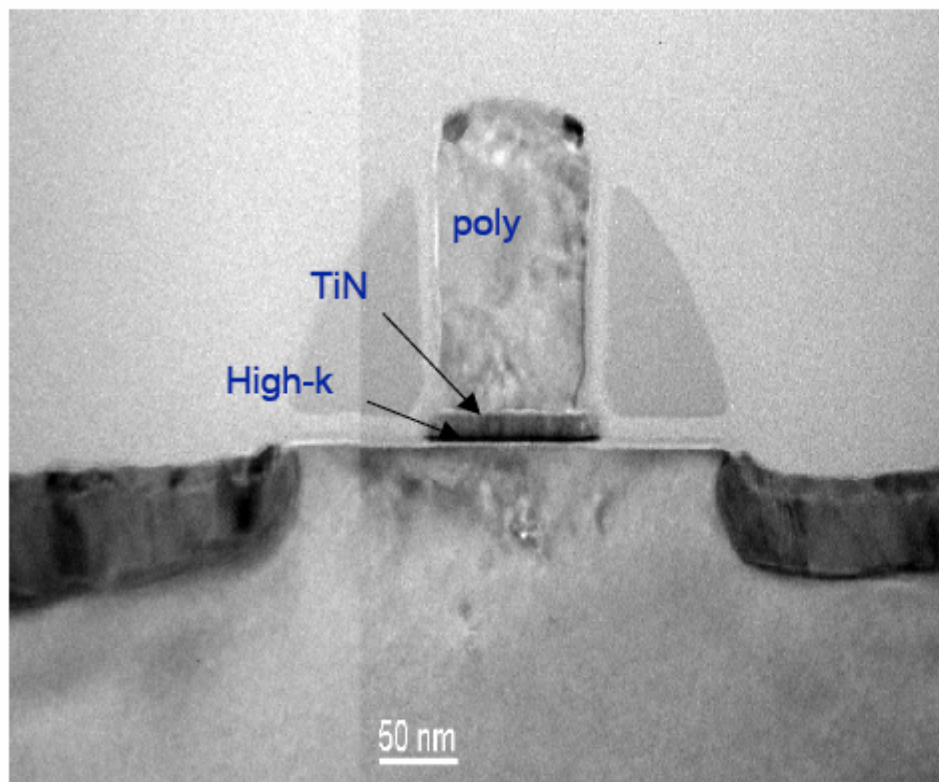
Scaling to below 2.0 nm feasible



HfSiO Nitridation Improves V_t Stability



Metal Electrode: Test Structures

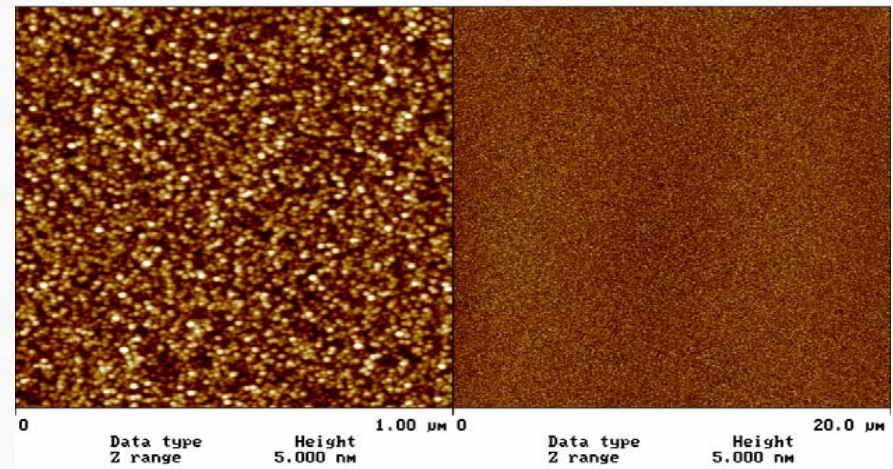
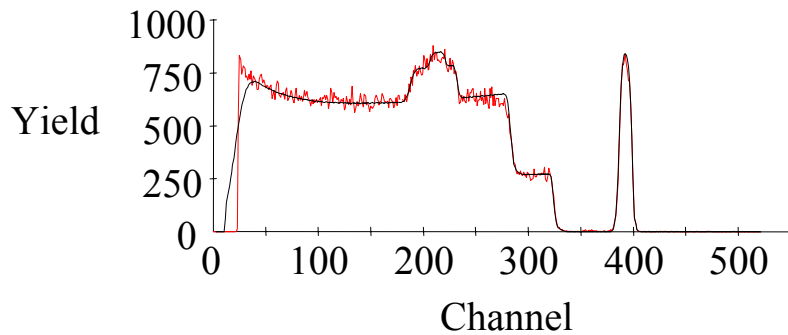
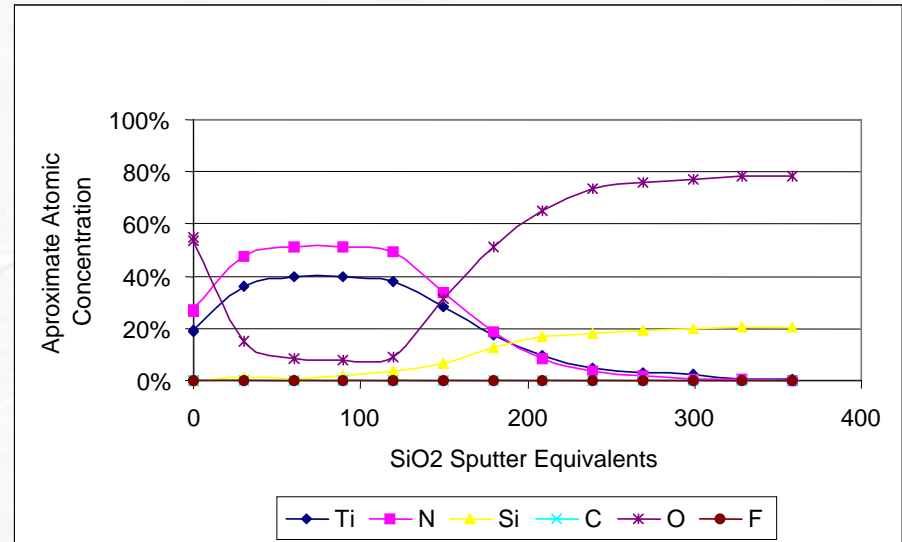


Process route/flow in place for PFET and NFET with various metal gates

- **Capacitors:**
Primary vehicle for initial work-function evaluation
- **Transistors:**
thin (~10 nm) metal layer under poly electrode
- **Concentrating on dual work function (band edge) metal gate stacks in conjunction with Hf-based high-k films**
- **Also assessing near mid-gap metals for FD-SOI applications**

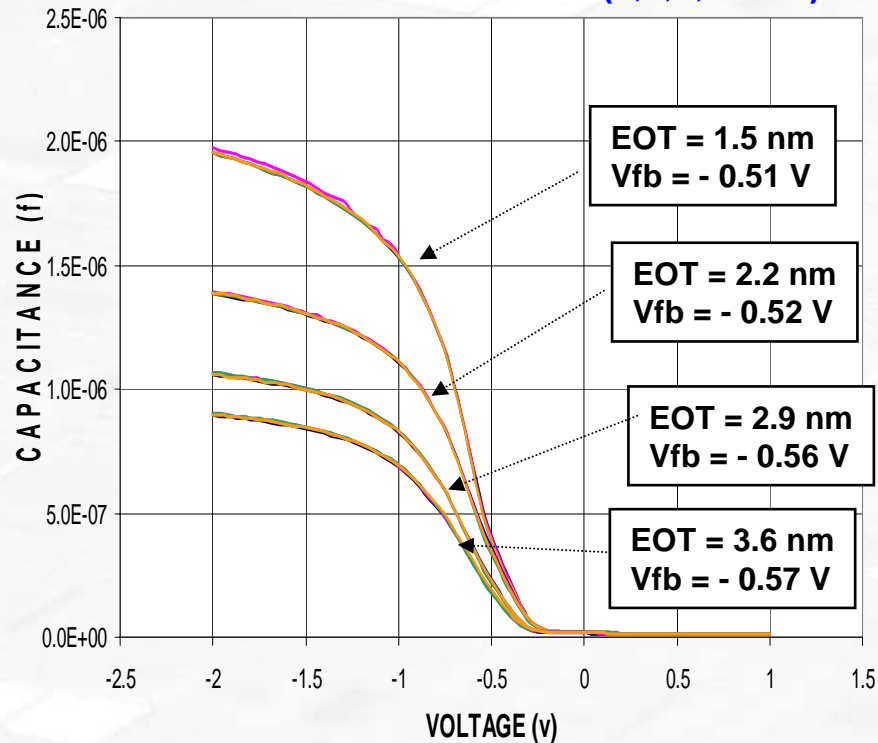
TiN Film Characterization

- Surface oxide that drops to 5-8% in the bulk
- RMS roughness ~0.8 nm
- Ti/N ~1.0-1.2 depending on technique



ALD-TiN MOSCAP Data

ALD TiN on ALD HfOx (4,6,8,10 nm)



$$V_{fb} = \Phi_{ms} - Q_f / \epsilon_{ox} \cdot EOT$$

V_{fb} : flat band voltage

Φ_{ms} : gate work function

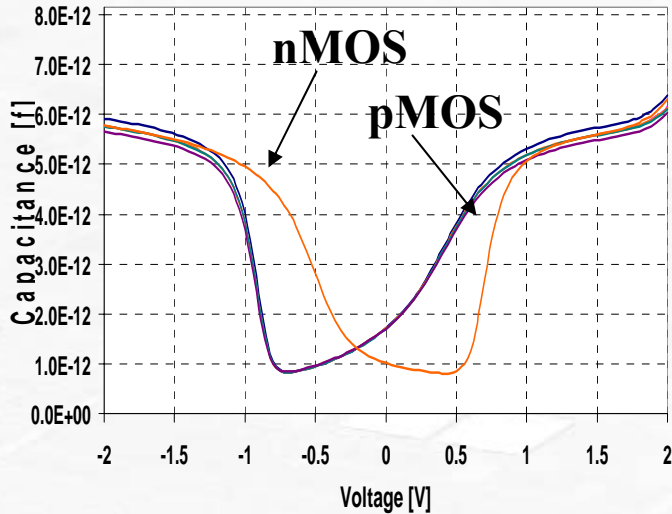
Q_f : interface charge density

Electrode	Gate Dielectric	Φ_{ms} [V]	N_f [chg/cm ²]	Work Function Φ_m [eV]
100 A ALD-TiN	ISSG	-0.52	1.1x10 ¹¹	4.5
100 A ALD-TiN	ALD-HfOx	-0.46	7x10 ¹¹	4.5
100 A ALD-TiN	MOCVD-HfOx	-0.37	1x10 ¹²	4.6

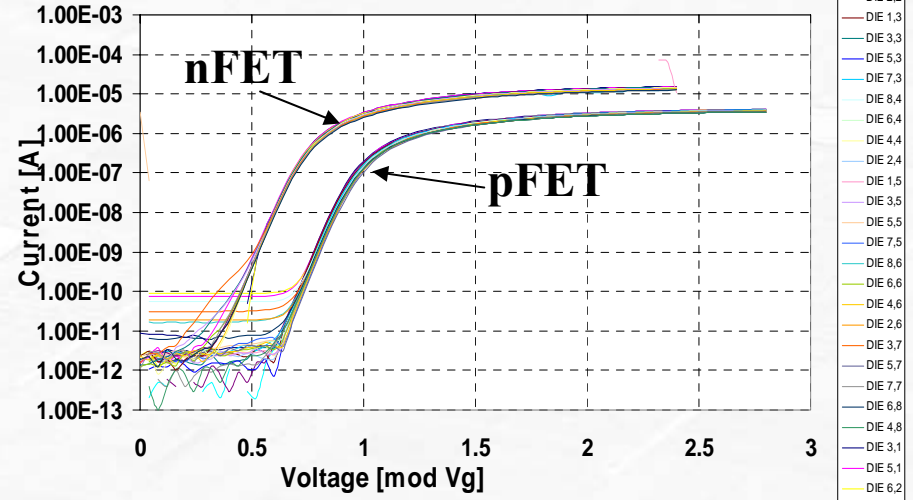
Marginal dependence of Work function and N_f on the gate dielectric material

Transistor Characteristics of ALD TiN on ALD HfSiOx (40 Å)

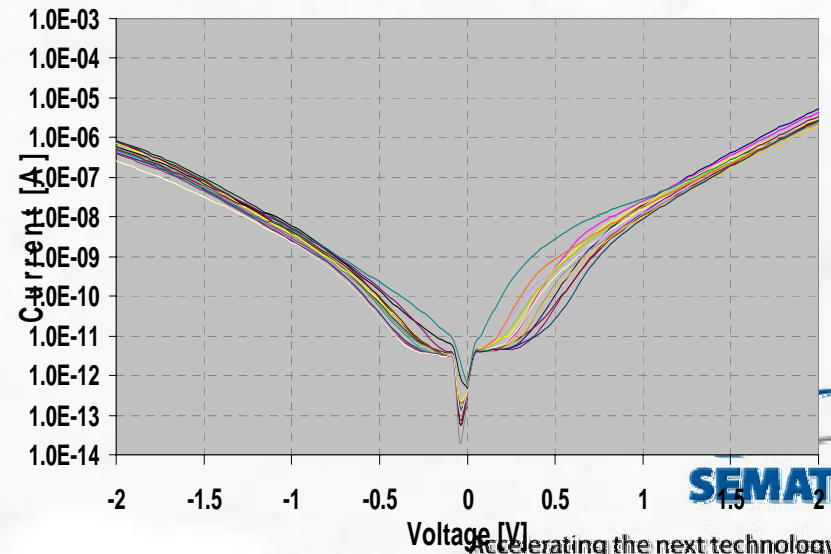
C-V (n/pMOS) of ALD TiN on HfSiOx (40 Å)



I_d - V_g (n/pMOS) of ALD TiN on HfSiOx (40 Å)



I_g - V_g (n/pMOS) of ALD TiN on HfSiOx (40 Å)



$$EOT = 2.0 \text{ nm}$$

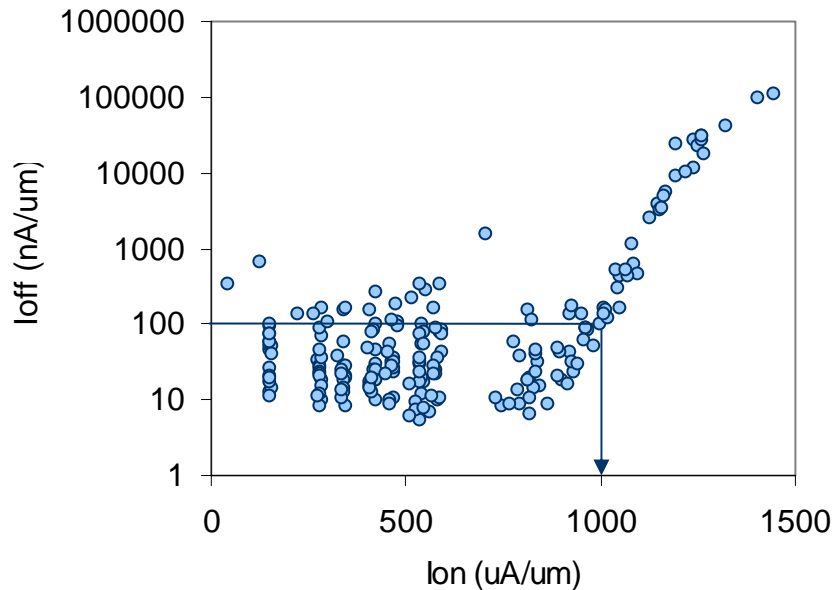
$$V_{fb}(n) = -0.55 \text{ V}$$

$$V_{fb}(p) = 0.45 \text{ V}$$

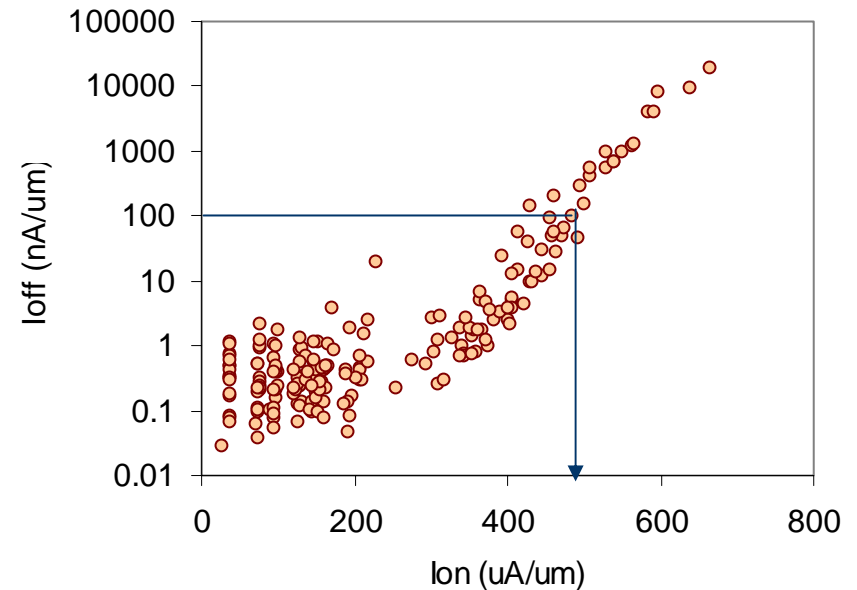
$$J_{g(n)} ([V_{fb}-1]) = 5 \text{ e-3 [A/cm}^2]$$

Demonstration of High Performance with High-k and TiN (Mid-Gap) Gate

NMOS with 30A HfSiO+ALD TiN



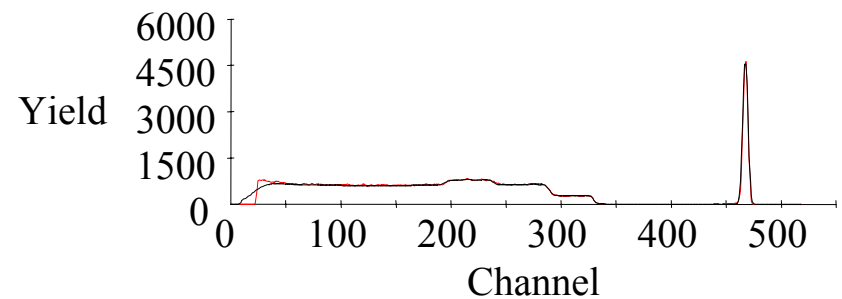
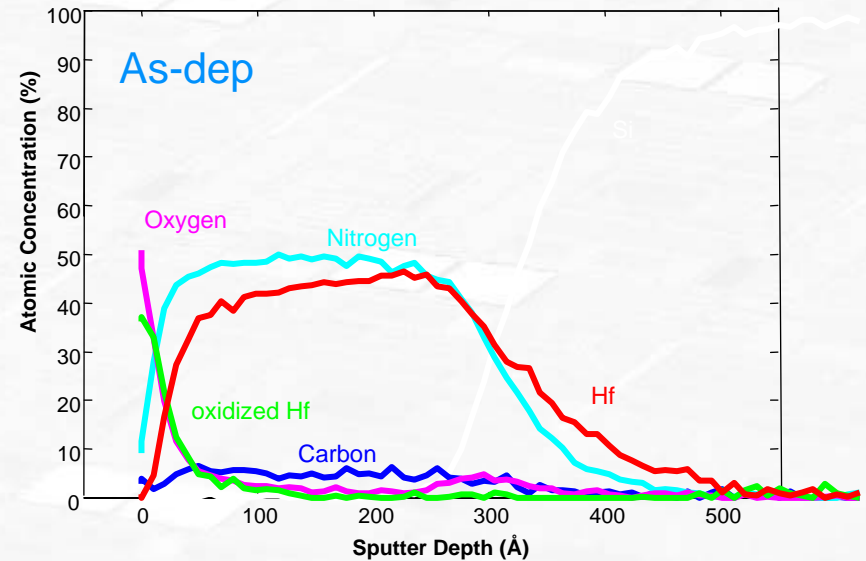
PMOS with 30A HfSiO+ALD TiN



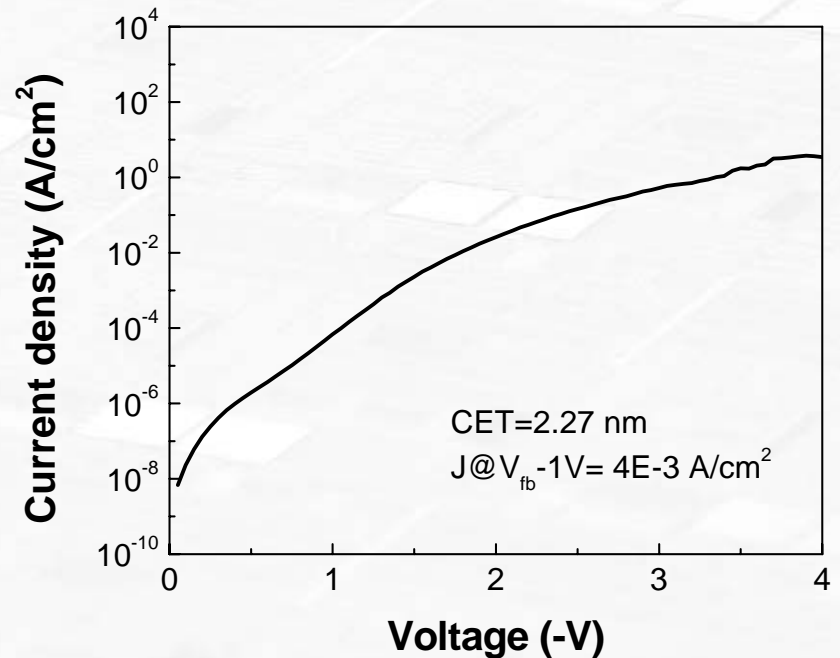
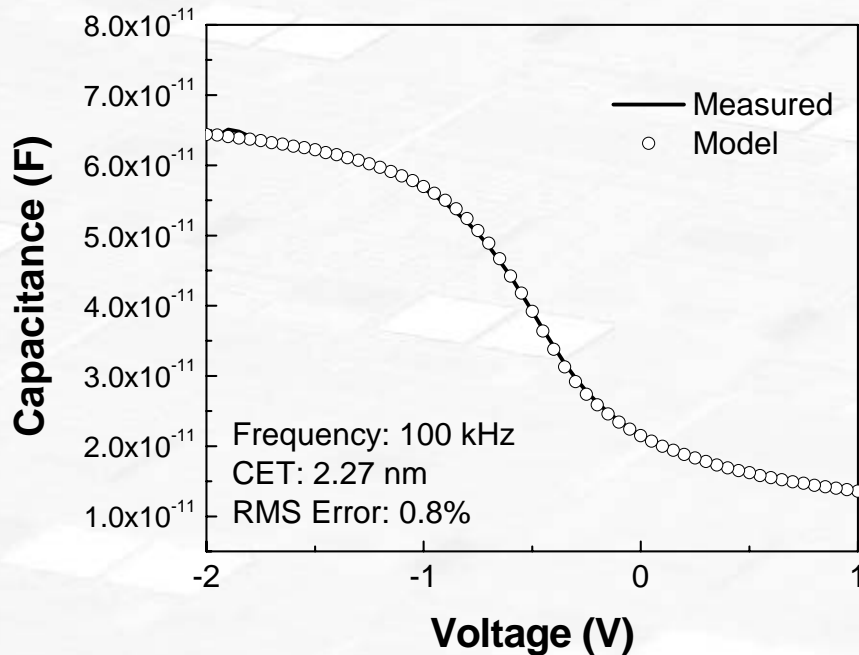
- 85 nm baseline exhibits high performance
- Mobility (e/h) NOT a showstopper
- NEED band-edge metals

HfN Film Analysis

- < 5% Carbon in the film
- High concentration of surface oxide that quickly drops to ~2%

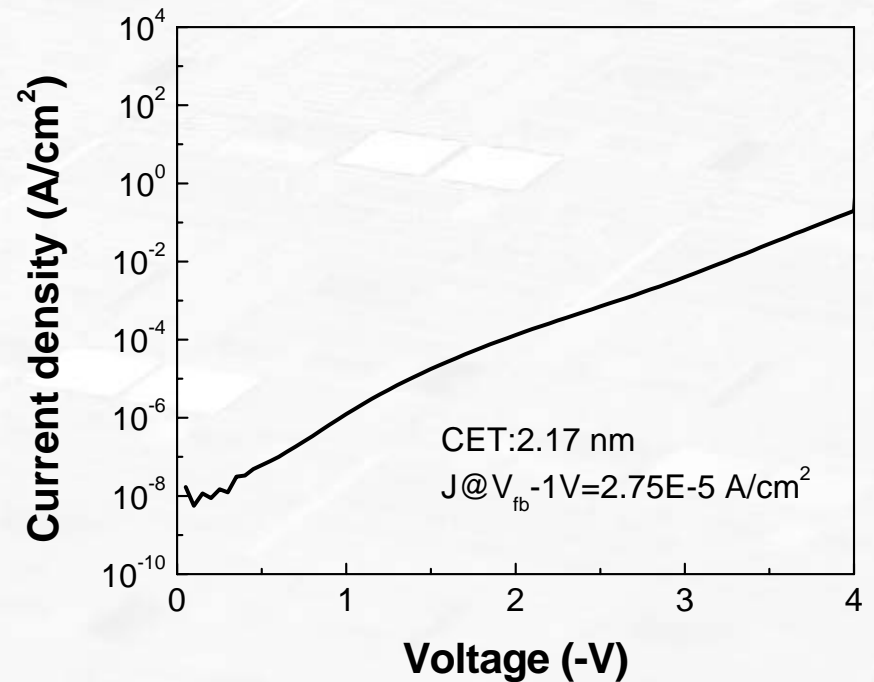
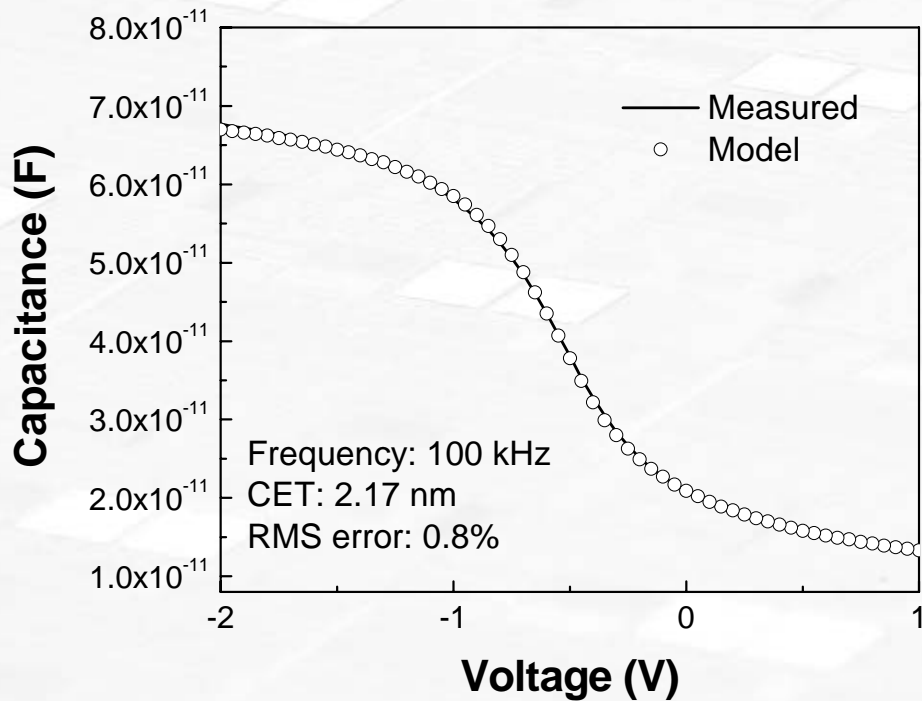


C-V and I-V curves of **HfN**/HfSiO/SiO₂ stack



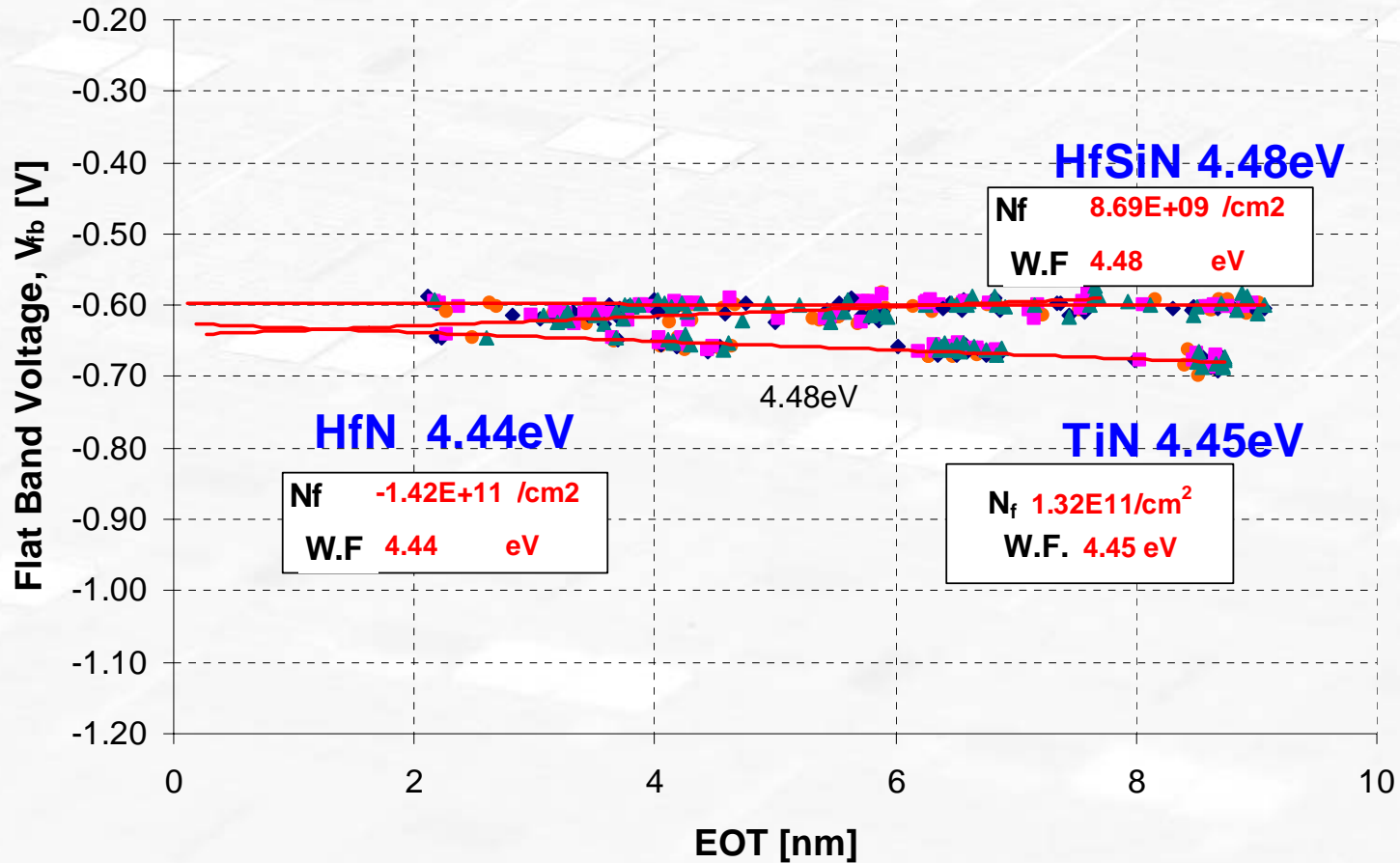
HfN 15nm /HfSiOx 3nm/SiO₂ 2nm
dot size: 5e⁻⁵ cm²

C-V and I-V curves of **HfSiN**/HfSiO/SiO₂

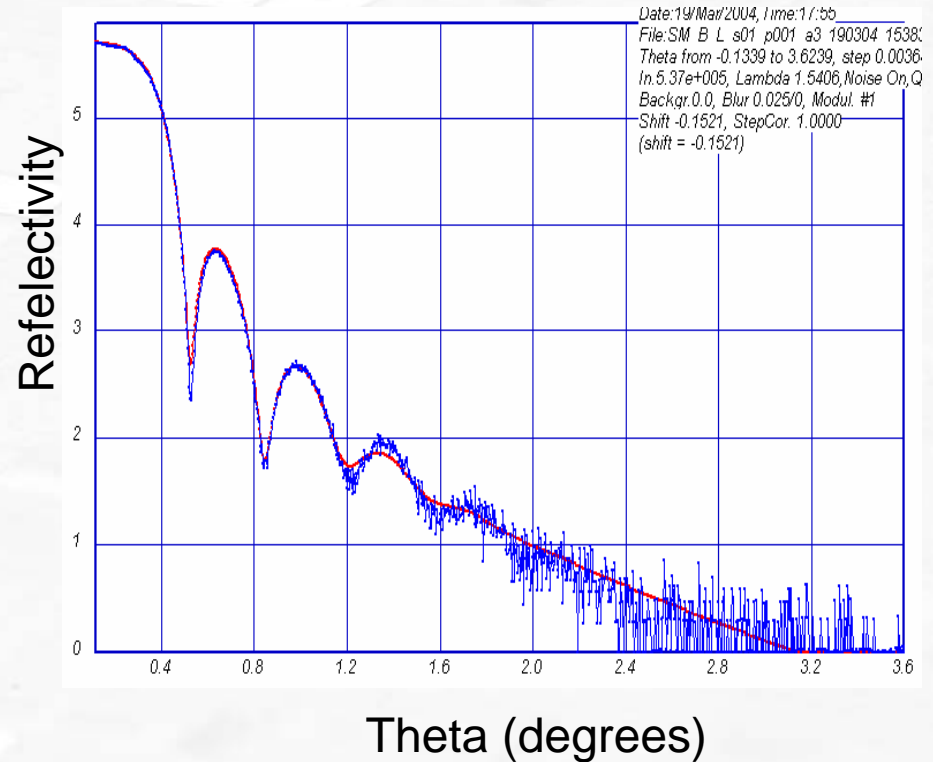
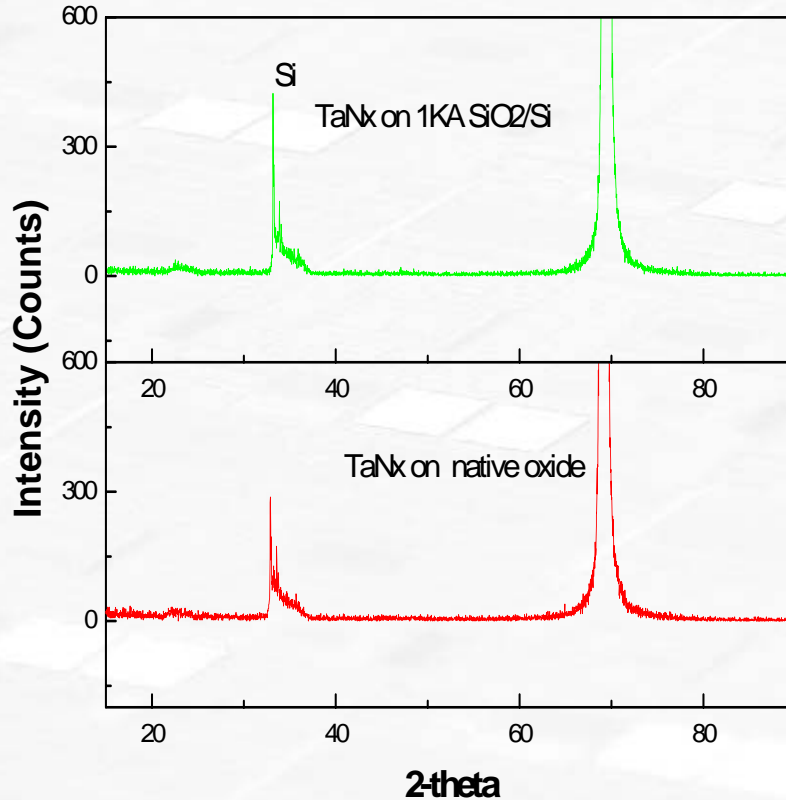


HfSiN 15nm /HfSiOx 3nm/SiO₂ 2nm
dot size: 5e⁻⁵ cm²

Work Function of ALD Metal Nitrides

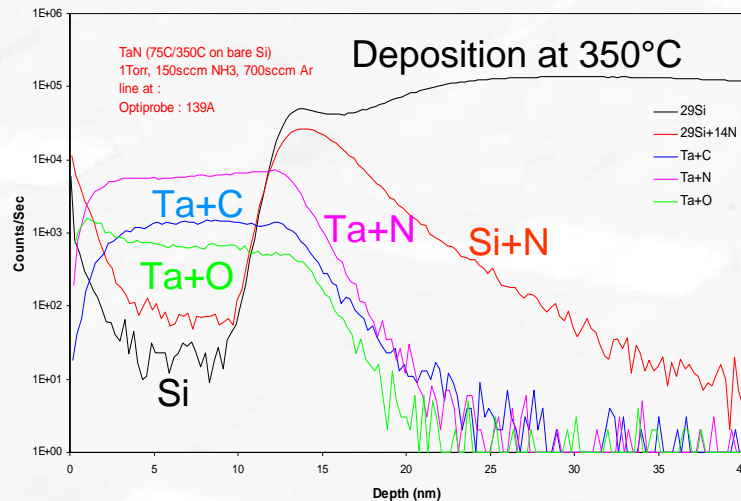
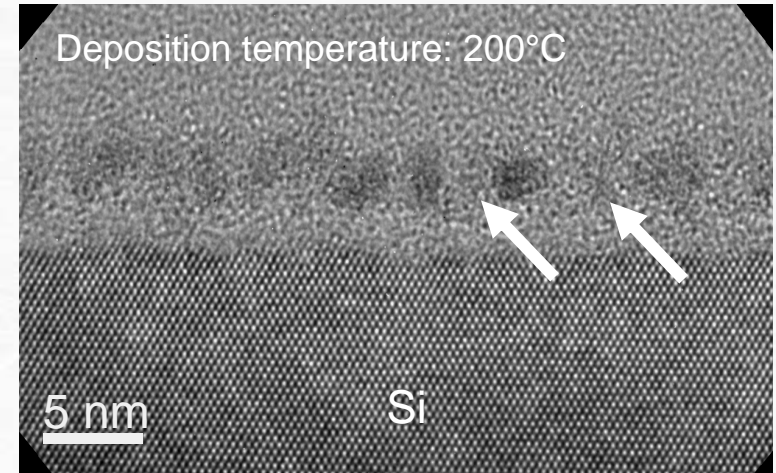
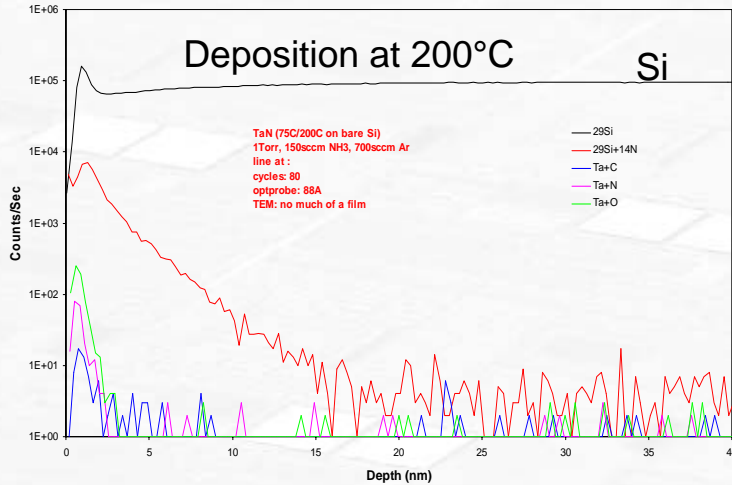


XRD and XRR of ALD TaN_x



- XRD confirmed amorphous nature of films (even after annealing up to 900°C)
- XRR density ~ 8g/cc; half of bulk value

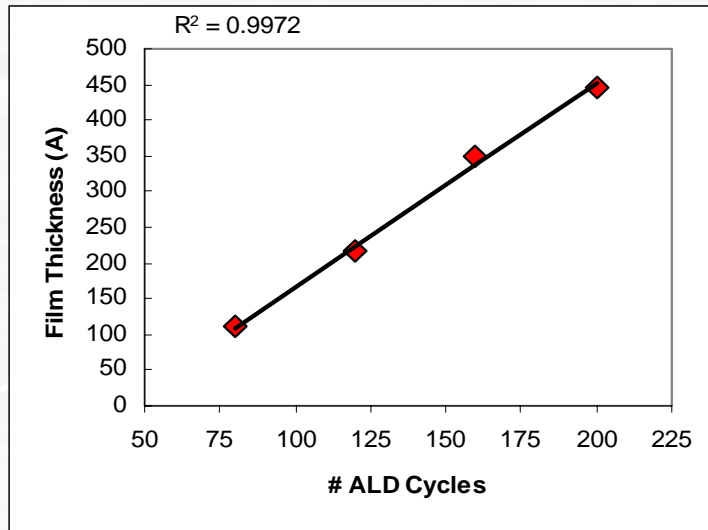
ALD TaN Deposition Temperature Effect



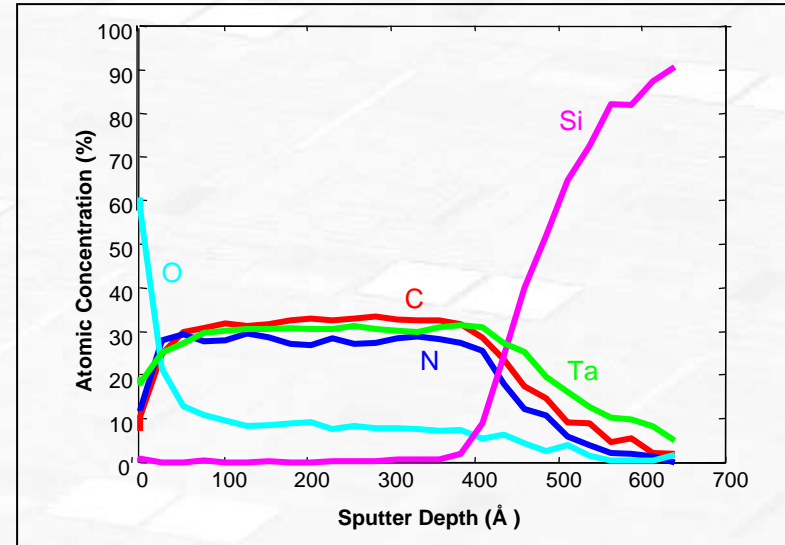
- Dep rate is strongly dependent on temp. (~1.5 Å/cycle at 350°C and ~ 0.25 Å/cycle at 200°C)
- TaN film deposited at 200°C resulted in discontinuous film
- SIMS data with high silicon count at the surface confirms TEM data

350°C ALD TaN Properties of ALD-TaN

Linear growth of TaN Film on bare Si at 350°C



AES data: carbon content in TaN film is high

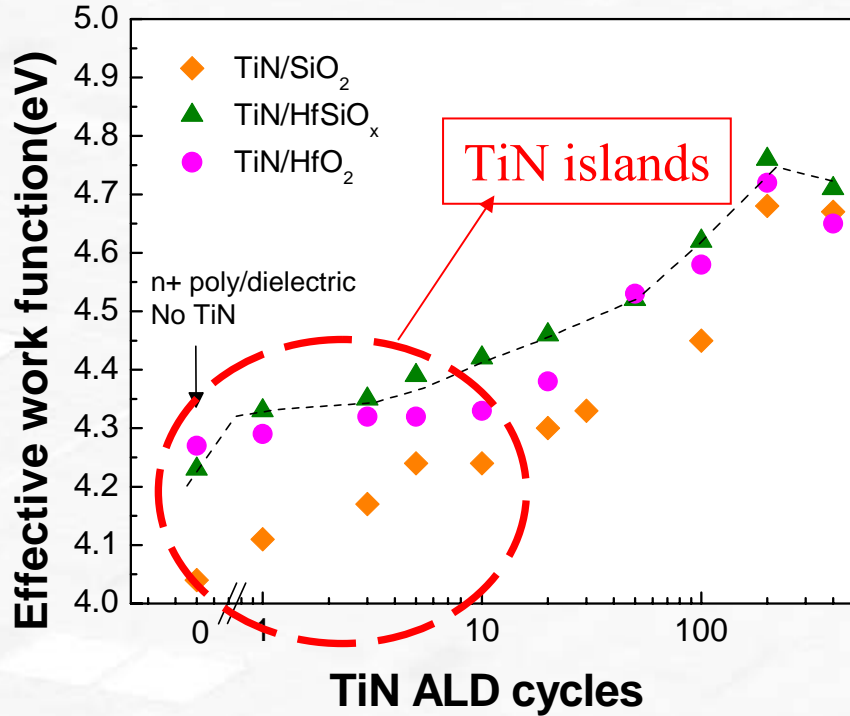


- Linear increase of thickness with # of ALD cycles.
Dep rate > 0.1nm/cycle

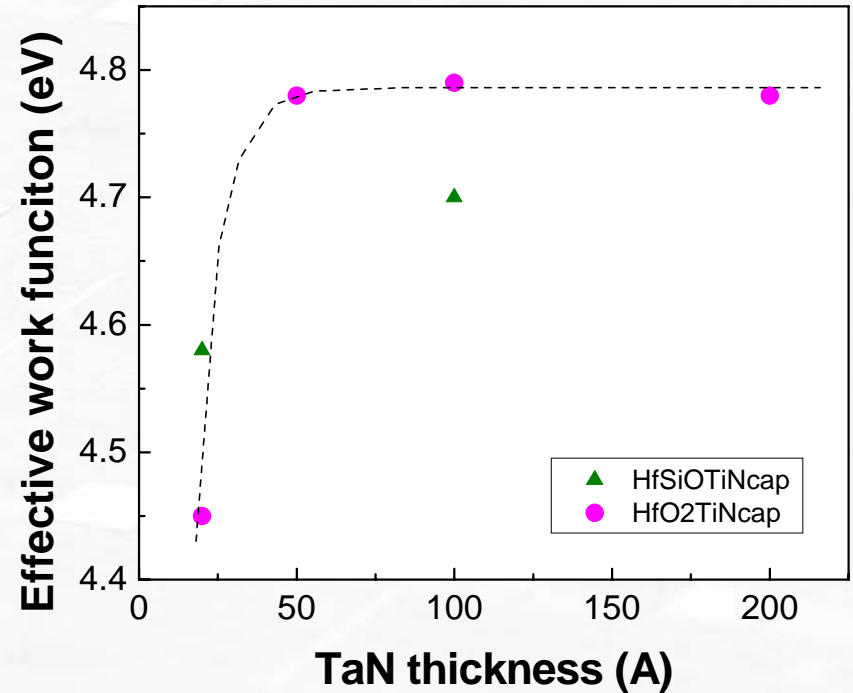
- The TaN film has a surface oxide and ~10% O in the bulk
- The N : Ta in the bulk is nearly 1 : 1
- C present at a similar % ~ 1:1:1 C:N:Ta

METAL ELECTRODE: Thickness Effect

ALD TiN

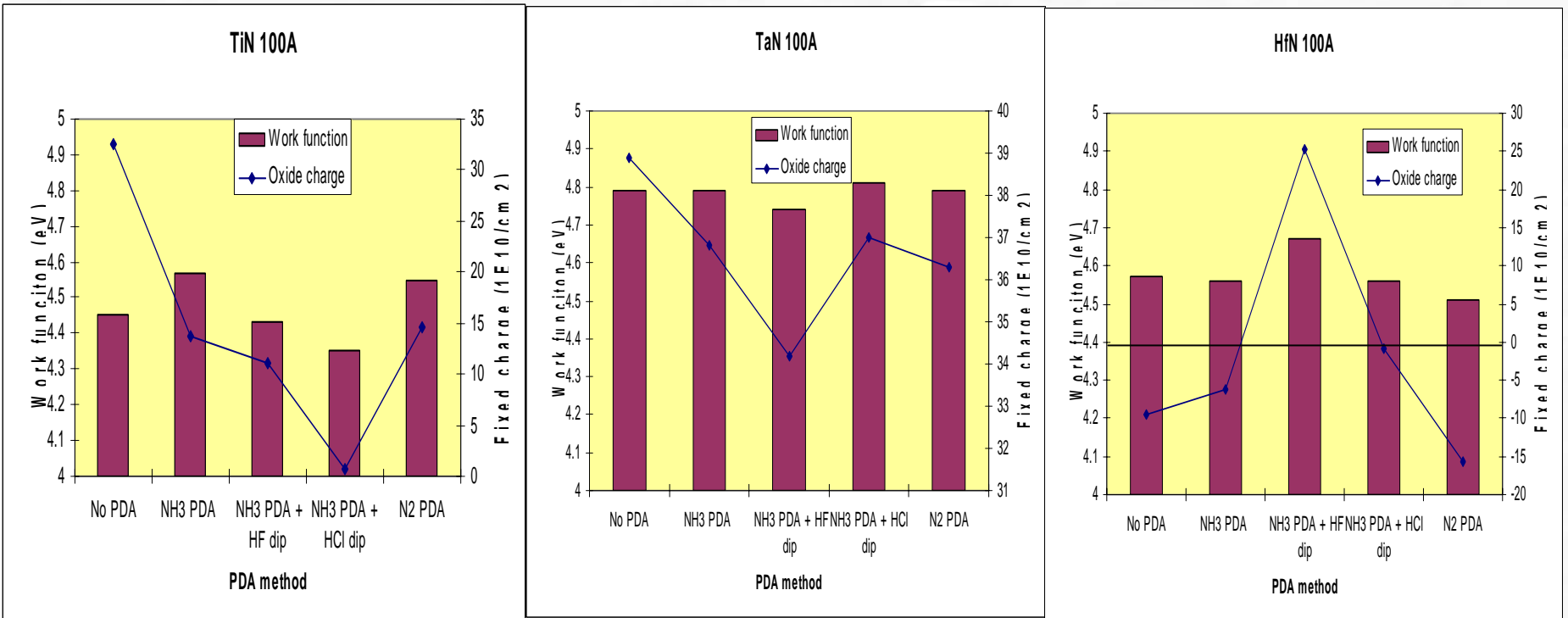


ALD TaN



Work Function of ALD TiN saturates around 200 cycles at ~4.7 eV
Work Function of ALD TaN saturates < 50 Å at ~4.8 eV

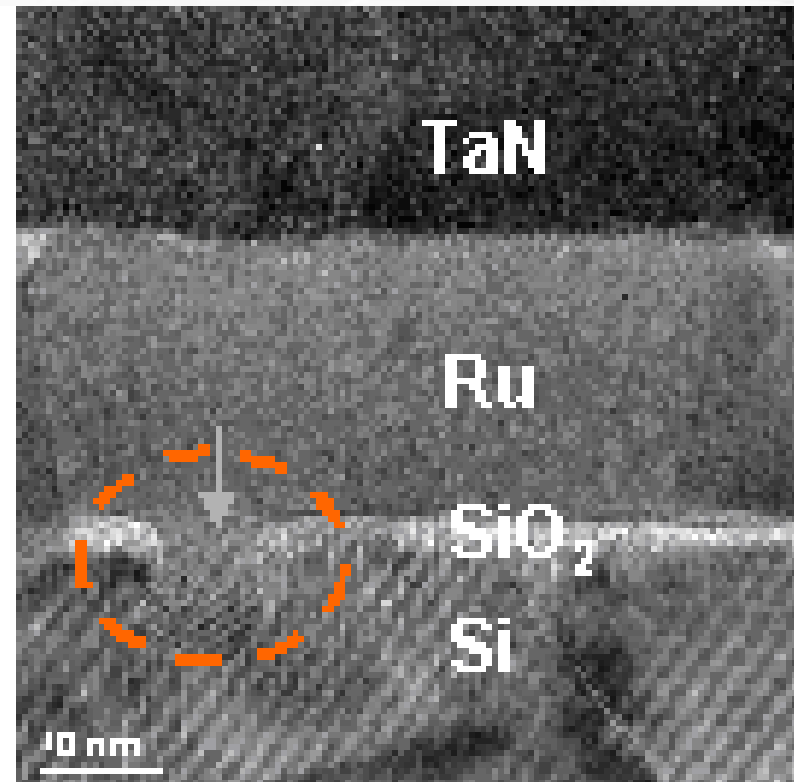
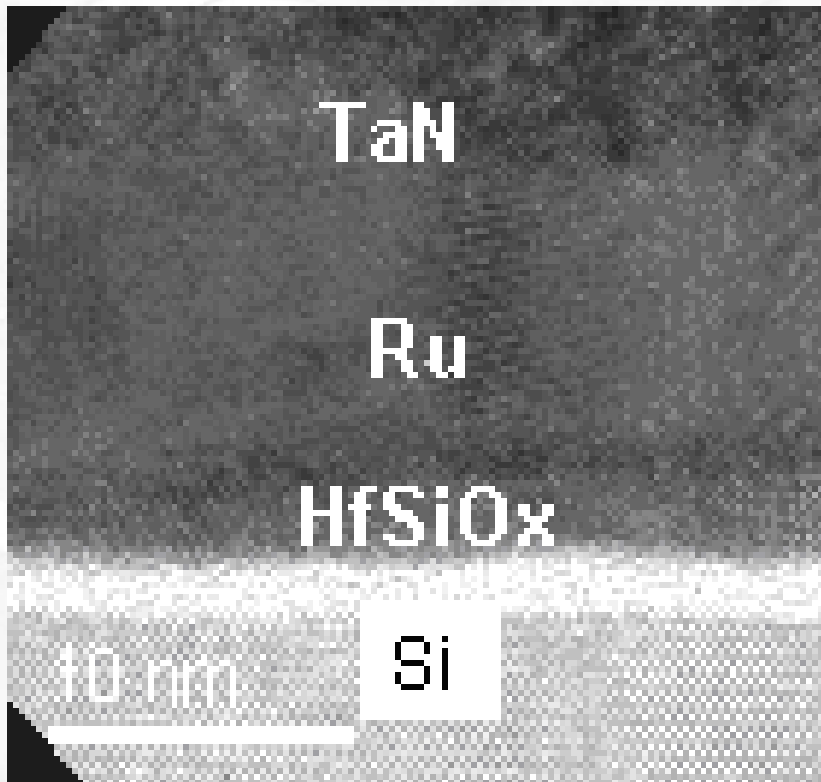
High-k (HfSiOx) Surface Treatment Effects on Work Function of Metal Electrodes



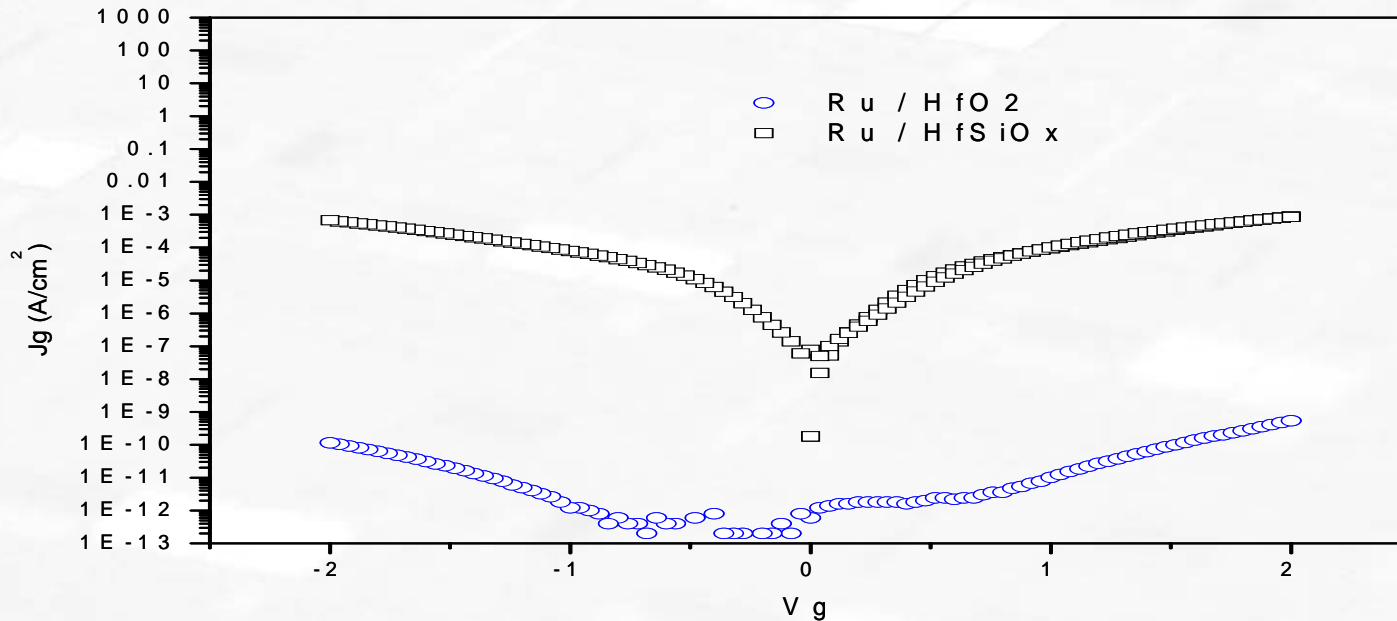
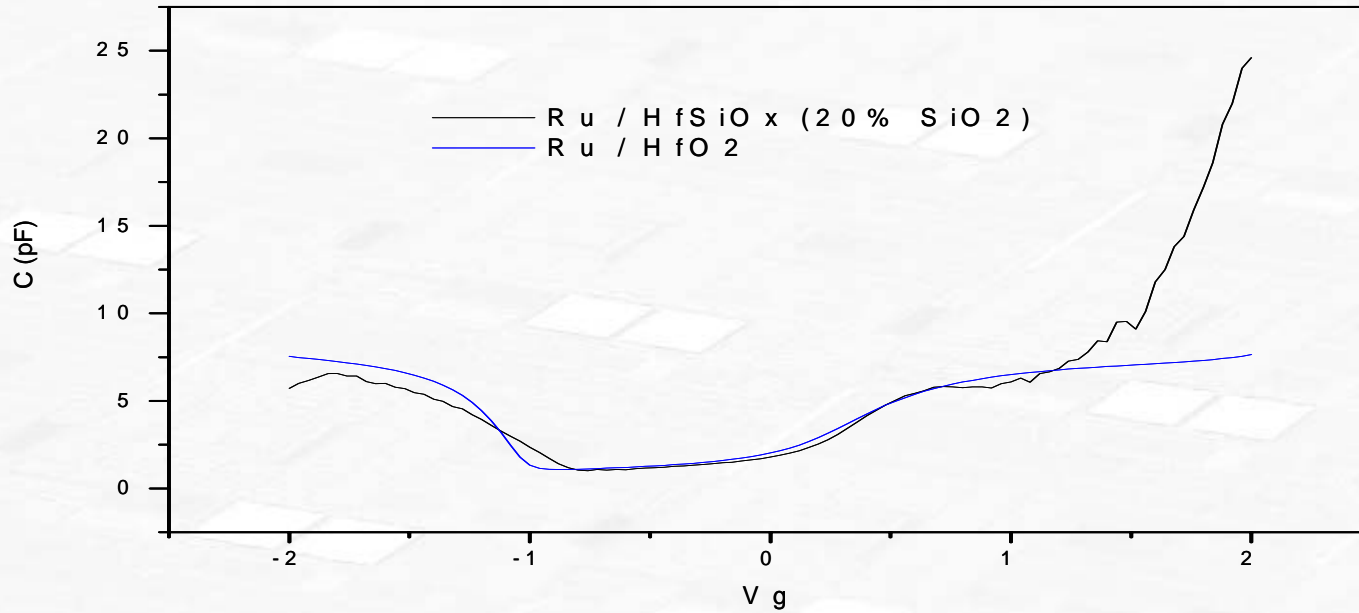
- HCl treatment helps reduce TiN Work Function by more than 0.2eV
- TaN is relatively independent on dielectric modification

Thermal Stability of Ru on HfSiOx and SiO₂

HRTEM cross section analysis



C-V and I-V curves for Ru/HfO₂ vs Ru/HfSiO_x



Conclusions

- 1) HfO_2 and $\text{Hf}_x\text{Si}_{1-x}\text{O}_2$ ALD processes scale physical thickness below $\sim 2\text{nm}$ utilizing metal-amide precursors and ozone.
- 2) ALD chemistry proceeds similarly on multiple surface preparations including HF last without growth incubation.
- 3) Promising high field mobility more than 85% of universal SiO_2 mobility has been achieved at EOT $\sim 1\text{nm}$ with 100-1000x Jg reduction.

Conclusions (cont'd)

- 5) ALD metal gate electrodes such as TiN, HfN, HfSiN deposited on HfO₂ and HfSiO_x showed mid gap characteristics.
- 6) Thickness dependency of Work Function of metal electrode was observed for ALD TiN.
- 7) PVD Ru is thermally more stable on HfO₂ as compared with SiO₂ and HfSiO_x.