Charge-Based Capacitance Measurement Circuits for Interface with Atomic Force Microscope Probes

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Problem

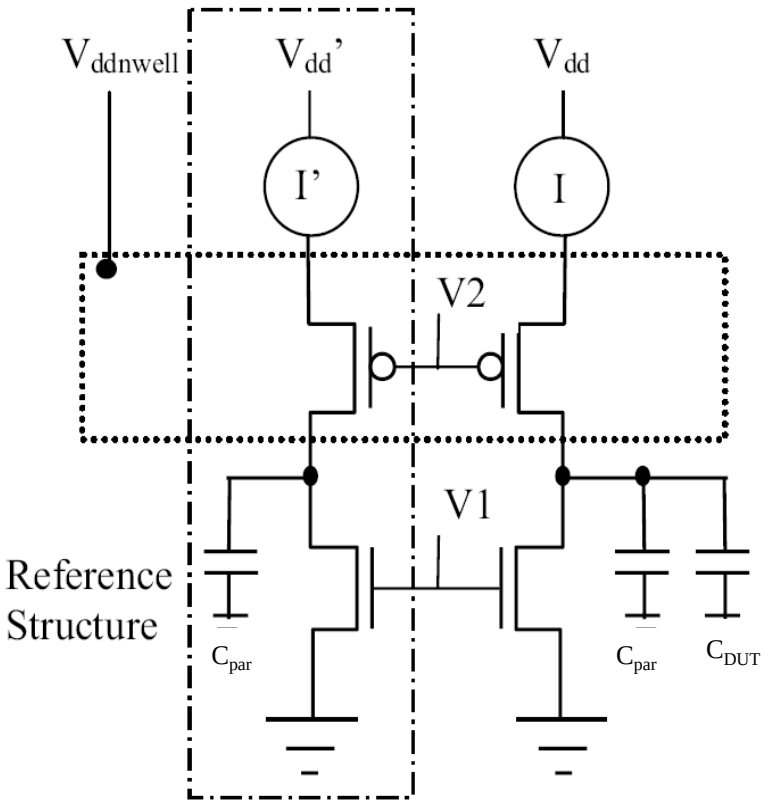
Truly quantitative capacitance measurements of very small capacitors using an atomic force microscope probe to make contact have proven difficult.

APPROACH

Create CBCM circuits capable of measuring capacitances in the presence of large series and parallel stray capacitances by precisely measuring the charge transferred onto the device versus a reference.

Interface the CBCM chip with an AFM tip with associated electronics needed to make quantitative capacitance measurements.

Basics of CBCM



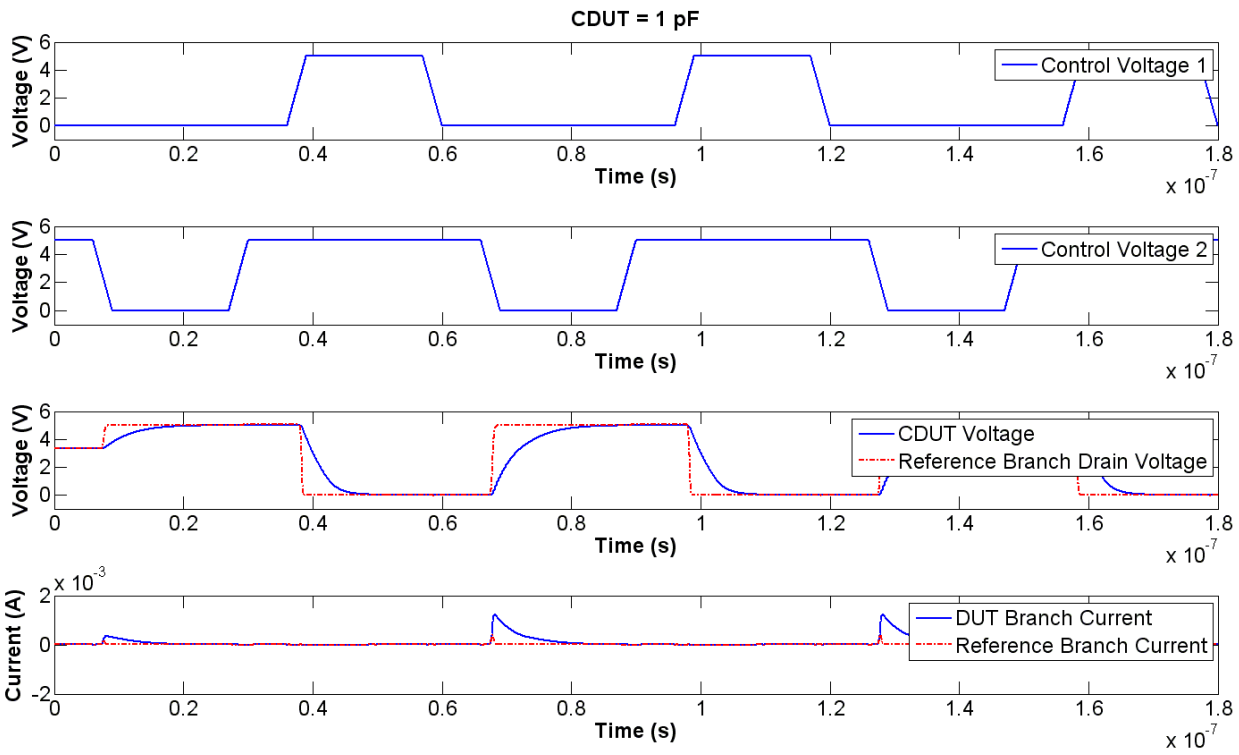
- A complementary pair of transistors (or transmission gates)
- Built-in reference branch to allow separate, simultaneous measurement of stray capacitance

C_{DUT} = "Device Under Test" Capacitor
C_{par}=Parasitic Capacitance

Randy Bach et al. Improvements to CBCM (Charge-Based Capacitance Measurement) for Deep Submicron CMOS Technology. Proceedings of the 7th International Symposium on Quality Electronic Design. 2006. 324-329.

Basics of CBCM

- Two non-overlapping control signals.
- V2 on/ V1 off when charging C_{DUT}
- V2 off/ V1 on when discharging C_{DUT}
- Allows charge to be measured as a dc current.



Basics of CBCM

$$Q = CV \longrightarrow dQ = CdV \qquad I = \frac{\Delta Q}{\Delta t} = \frac{dQ}{dt}$$

Combine These Equations:

$$I = \frac{CdV}{dt} \longrightarrow Idt = CdV$$

Take Average Value:

$$\frac{1}{T}\int_0^T Idt = \frac{1}{T}\int_0^T C\frac{dV}{dt}dt$$

$$I_{avg} = \frac{1}{T}\int_0^{V_{dd}} CdV = \frac{CV_{dd}}{T} = fCV_{dd}$$

$$C = \frac{I_{avg}T}{V_{dd}} = \frac{I_{avg}}{fV_{dd}}$$

Q=Charge
C=Capacitance
V=Voltage
I=Current
t=Time
T=Period
ƒ=Frequency

MOSIS CBCM Test Chip

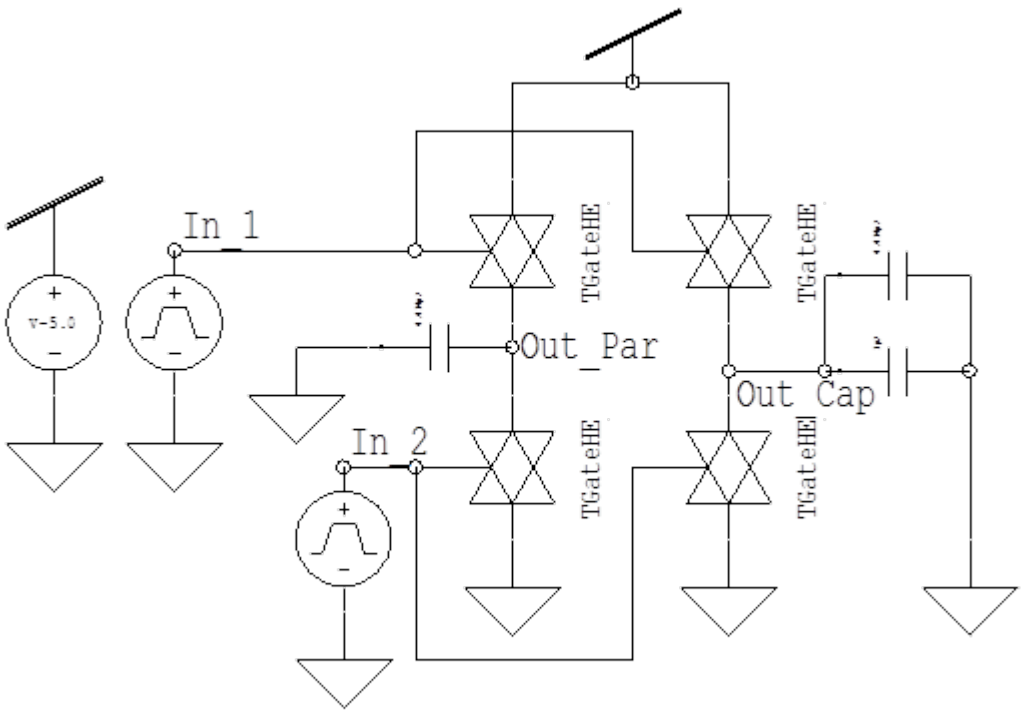
1. Basic CBCM, MOS 4x4 to 40x40 µm
2. CBCM with bias control, MOS 4x4 to 40x40
3. SCM on a chip
4. CBCM with bias, balanced branches with MOS caps
5. CBCM with bias, slightly unbalanced branches, smaller MOS caps
6. CBCM with bias, slightly unbalanced branches, larger MOS caps
7. Metal-to-metal: 8 devices 4x4 to 4x11 λ

Series 7 (metal-to-metal)

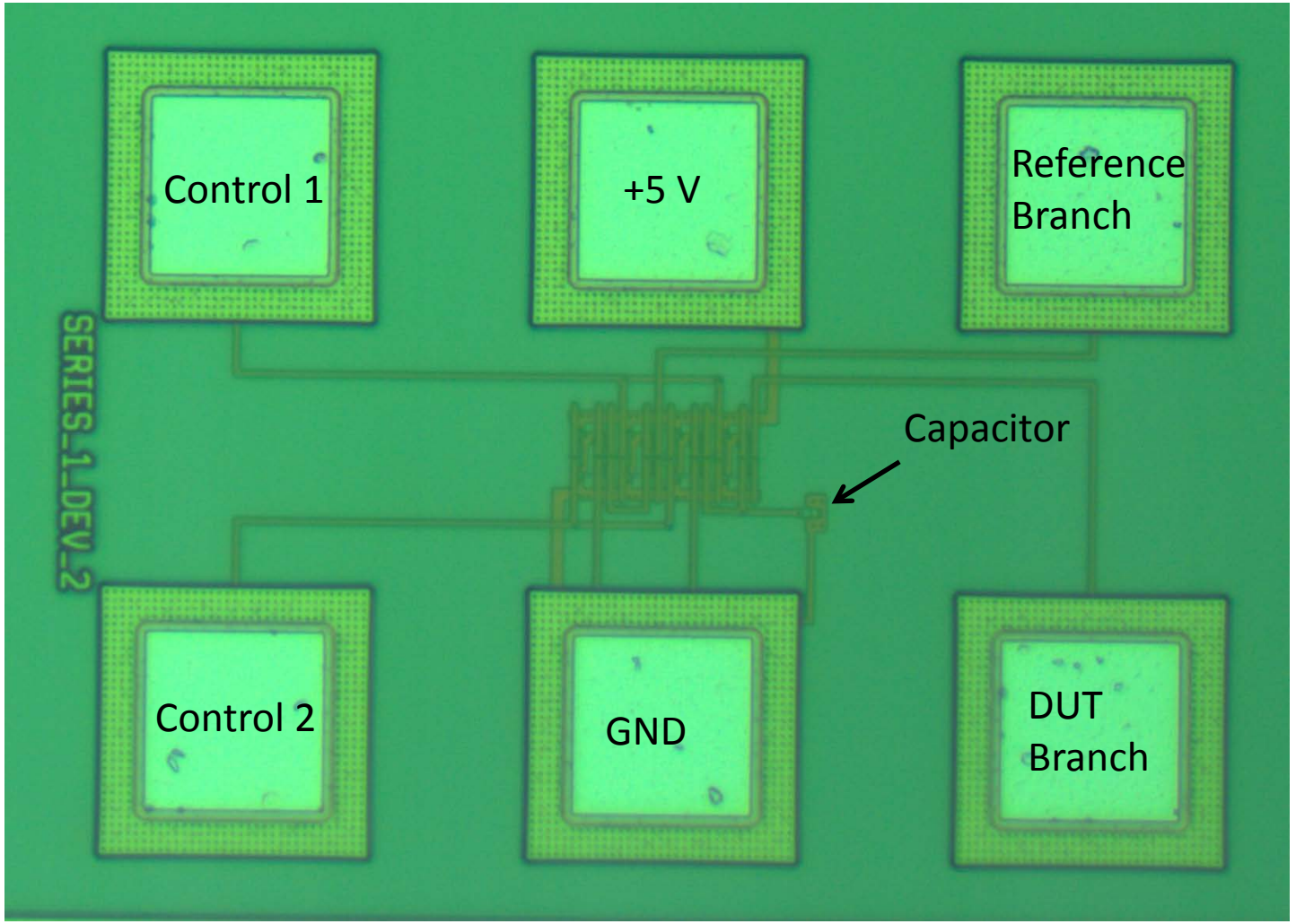
Device	Dimensions (λ)	Area (cm^{-2})	Capacitance (aF)
1	4 x 5	1.80×10^{-8}	191
2	5 x 4	1.80×10^{-8}	191
3	4 x 6	2.16×10^{-8}	229
4	4 x 7	2.52×10^{-8}	267
5	4 x 8	2.88×10^{-8}	305
6	4 x 9	3.24×10^{-8}	344
7	4 x 10	3.60×10^{-8}	382
8	4 x 11	3.96×10^{-8}	421

Theoretical capacitance for ε_{lowK} = 2.4 and inter-metal oxide thickness of 200 nm

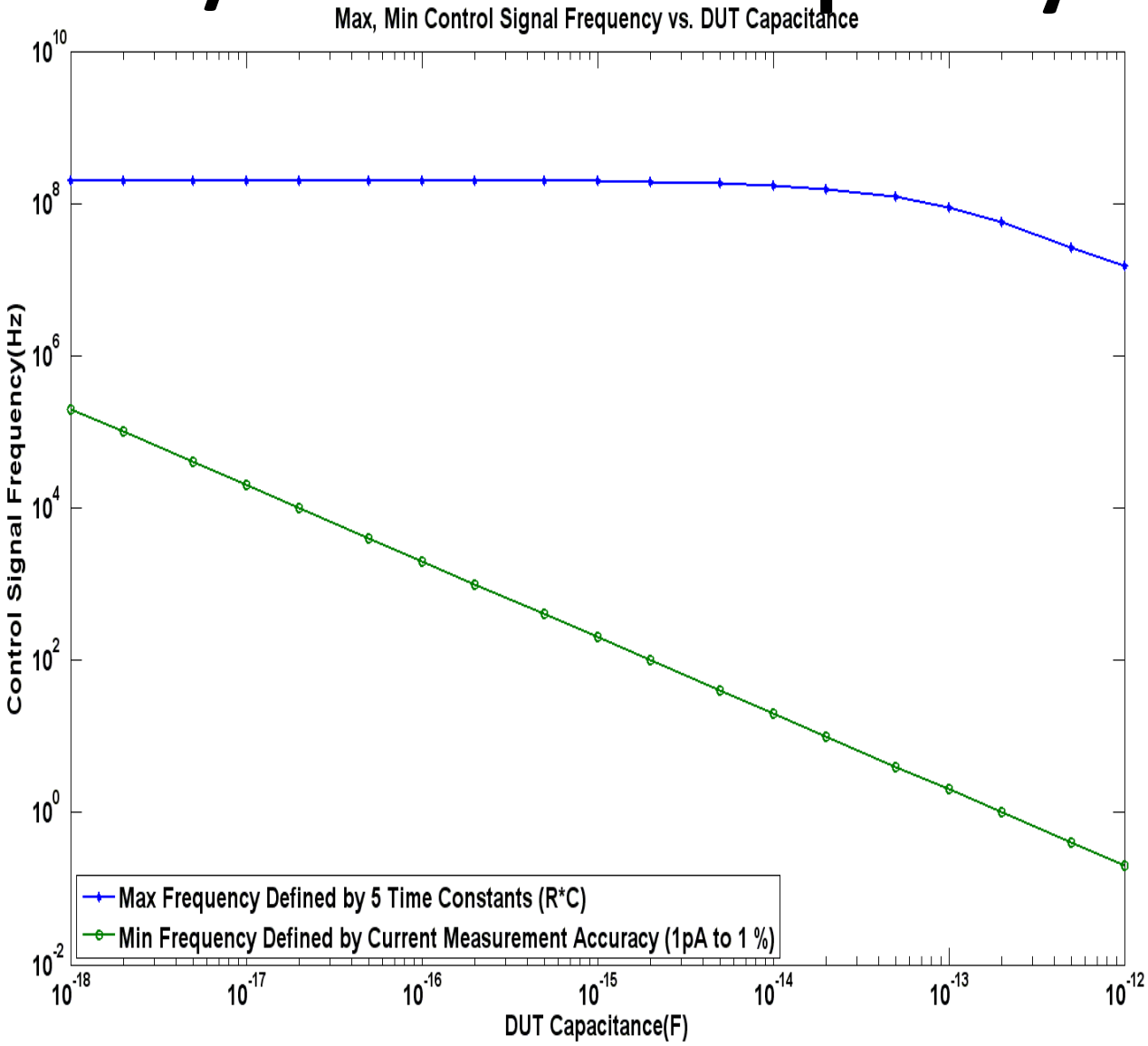
CBCM with transmission gates



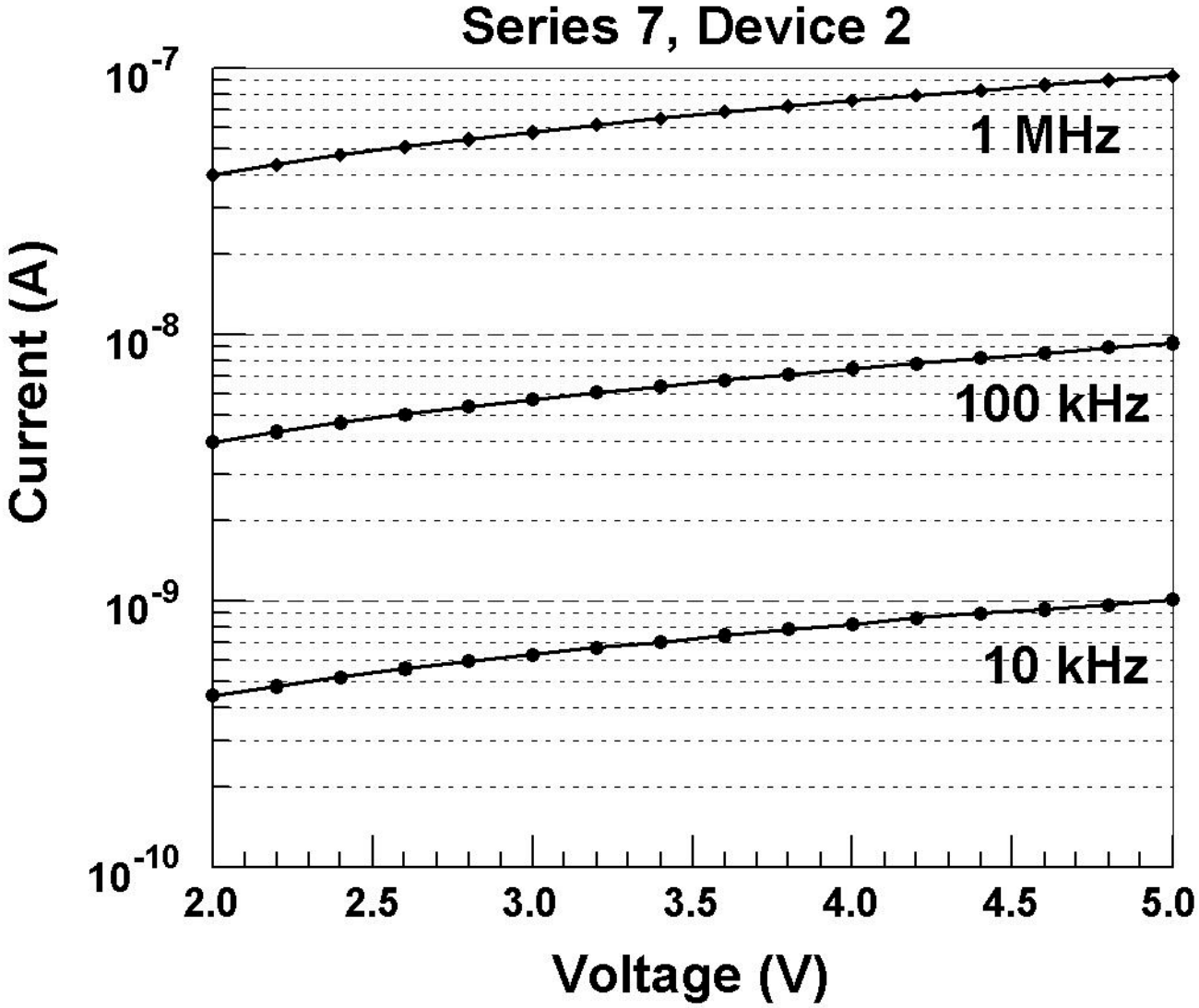
Basic CBCM test Structure with metal-to-metal Capacitors



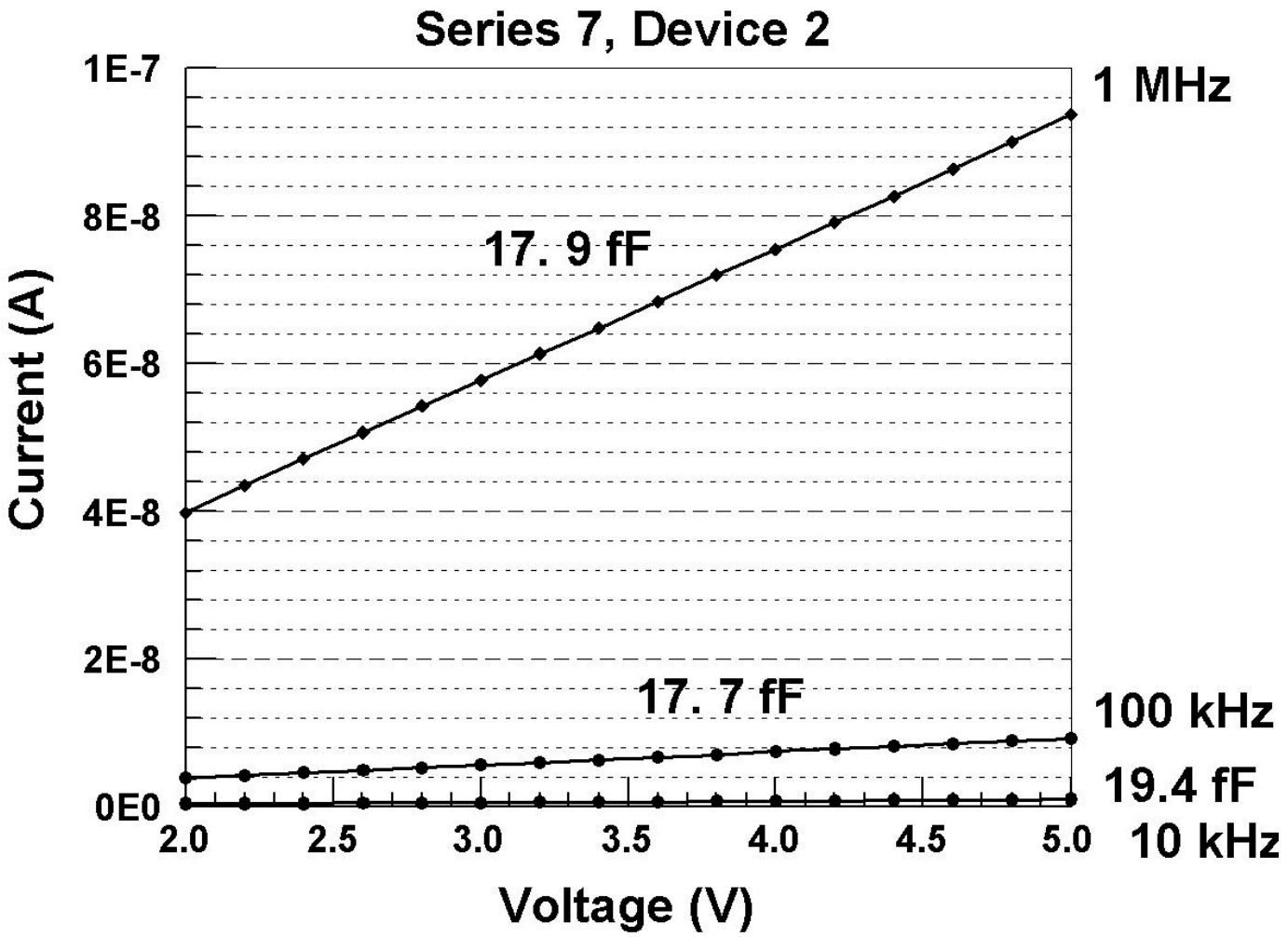
PSPICE Results:
Maximum/Minimum Frequency vs. C_{DUT}



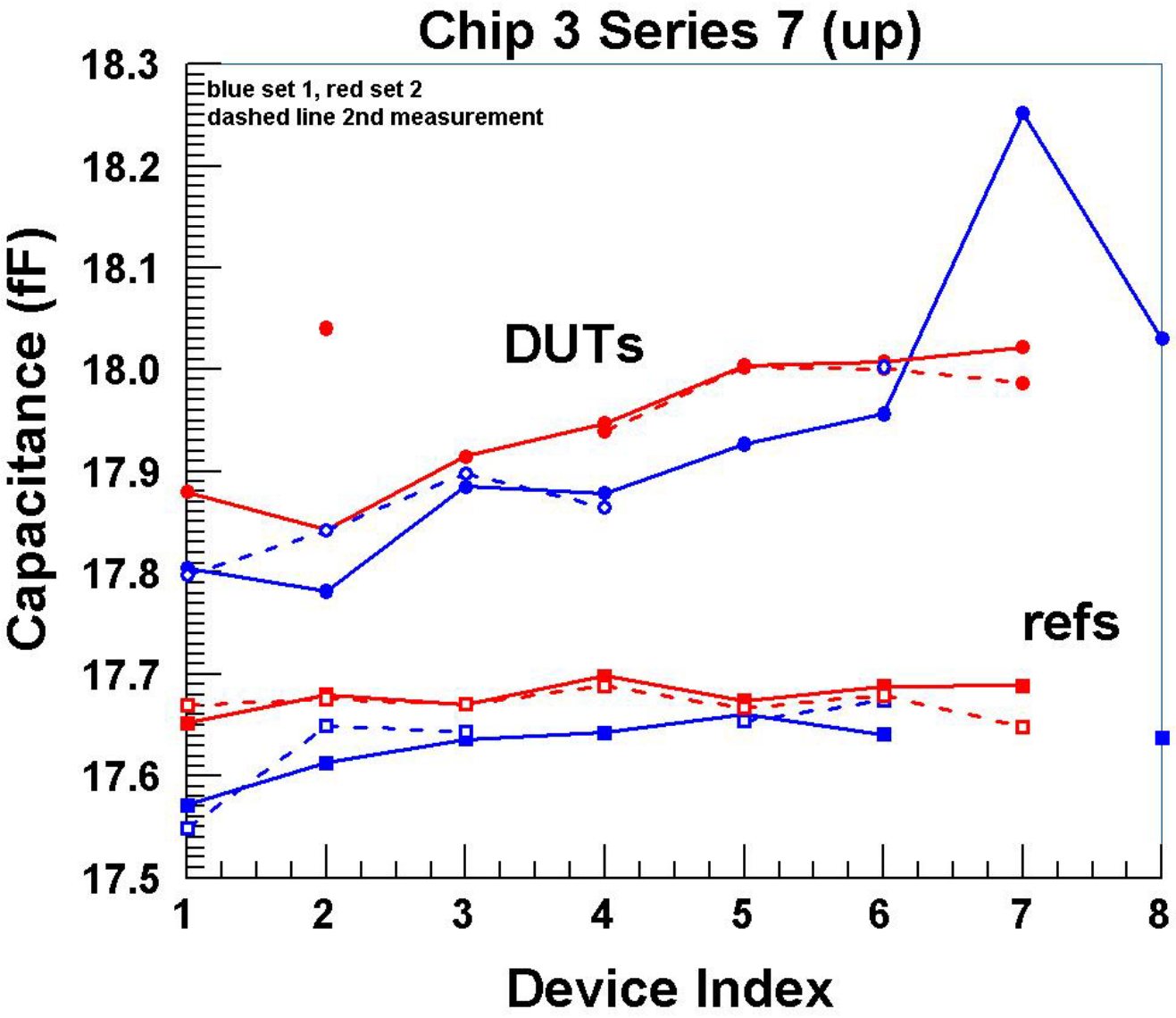
Current scales with Frequency



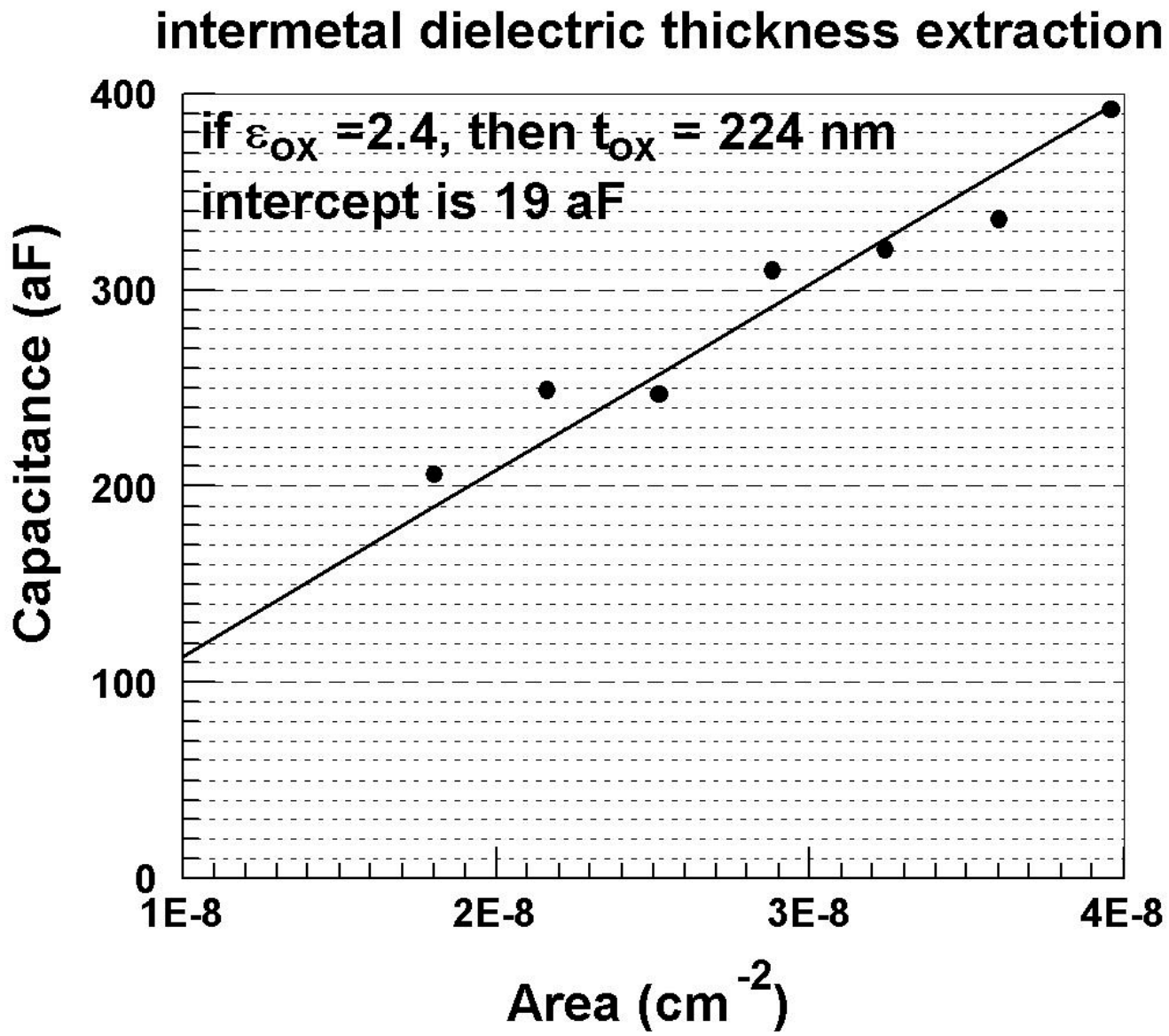
Nicely linear, but slope slightly varies with Freq.



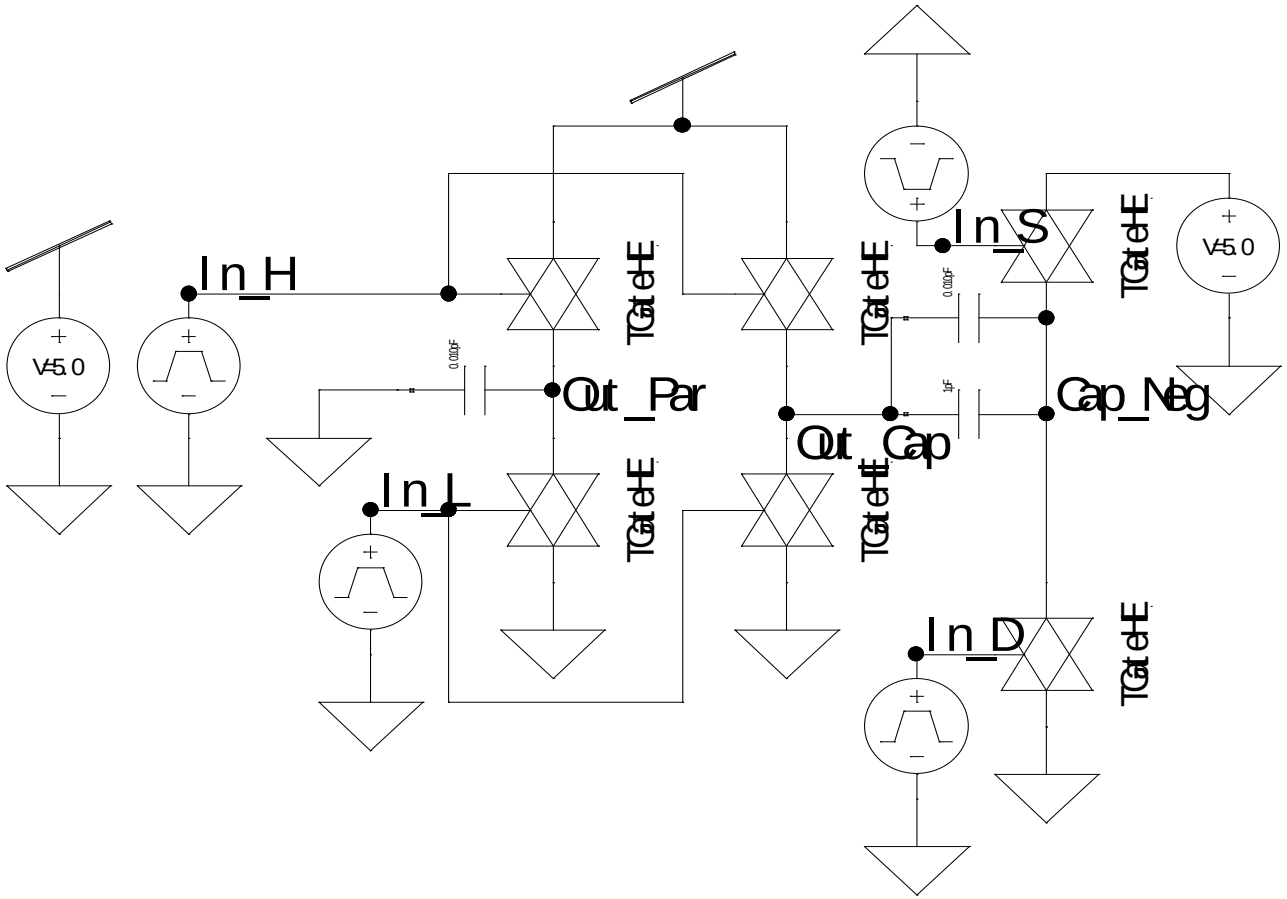
Repeatability is good



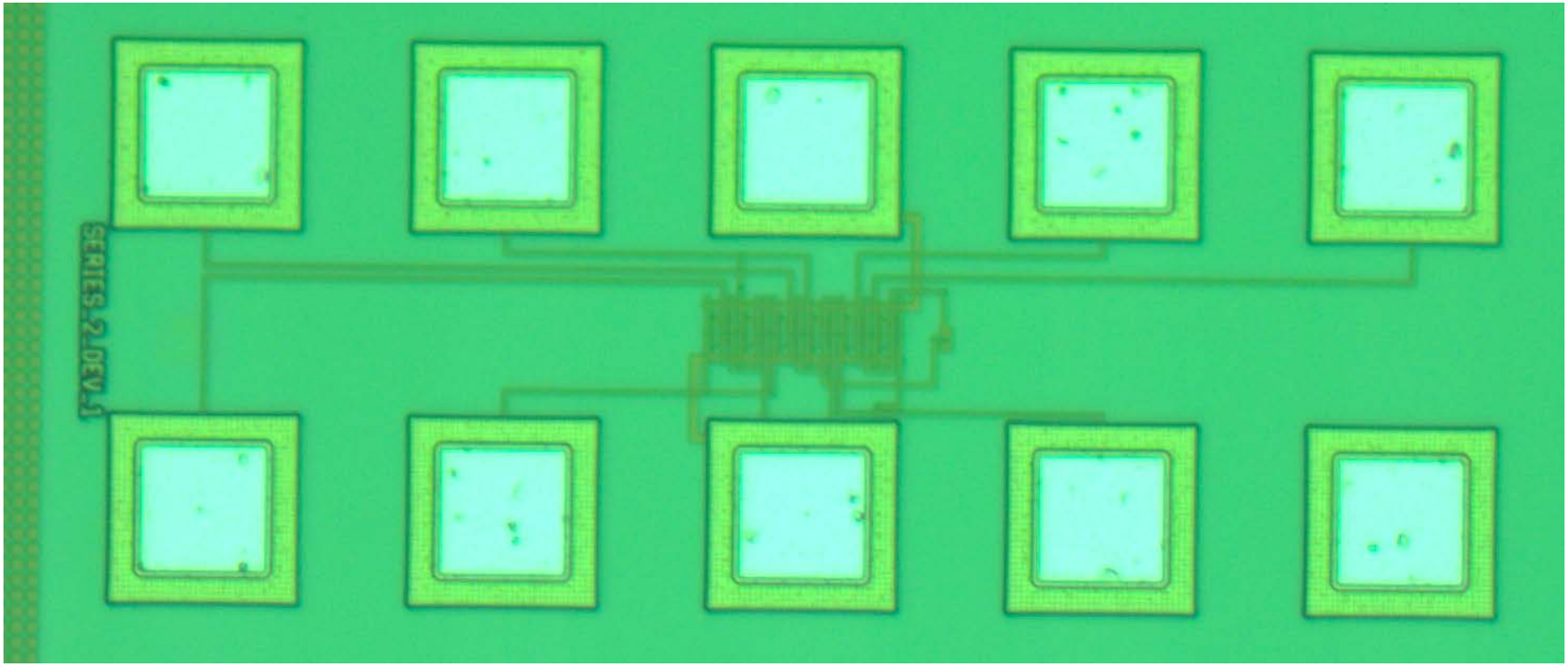
+/- 20 aF Precision



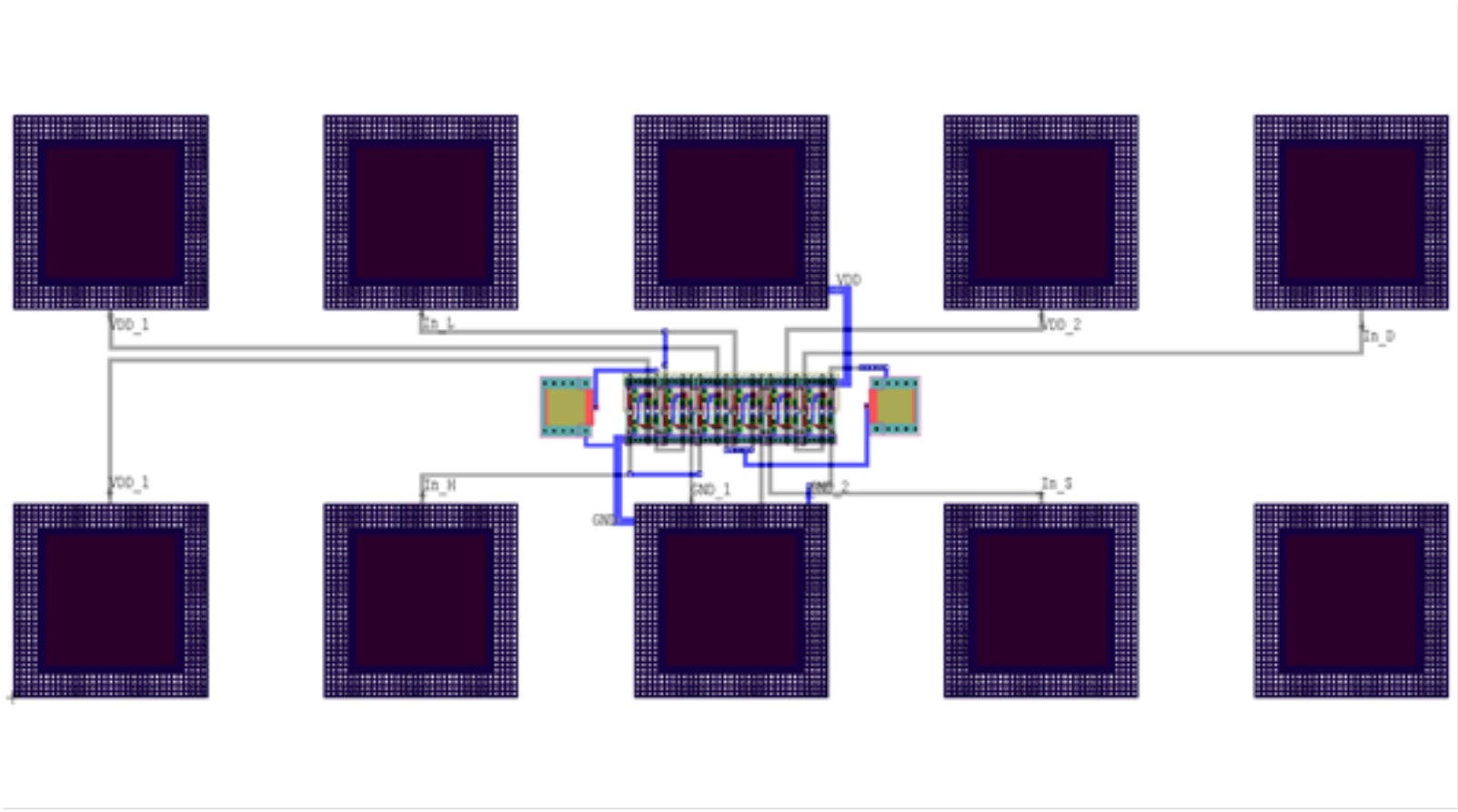
CBCM with Bias: Allows measurement of MOS C-V



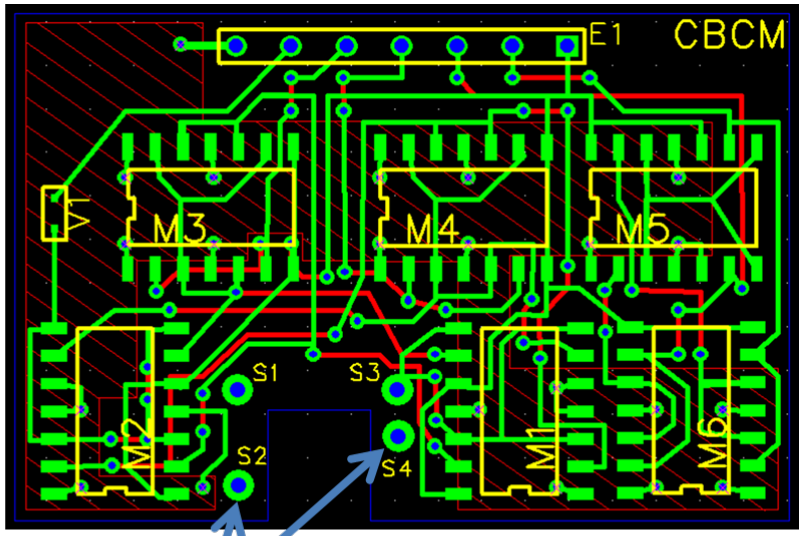
CBCM with capacitance bias control
“SCM on a Chip”



CBCM with bias control and on chip reference capacitors



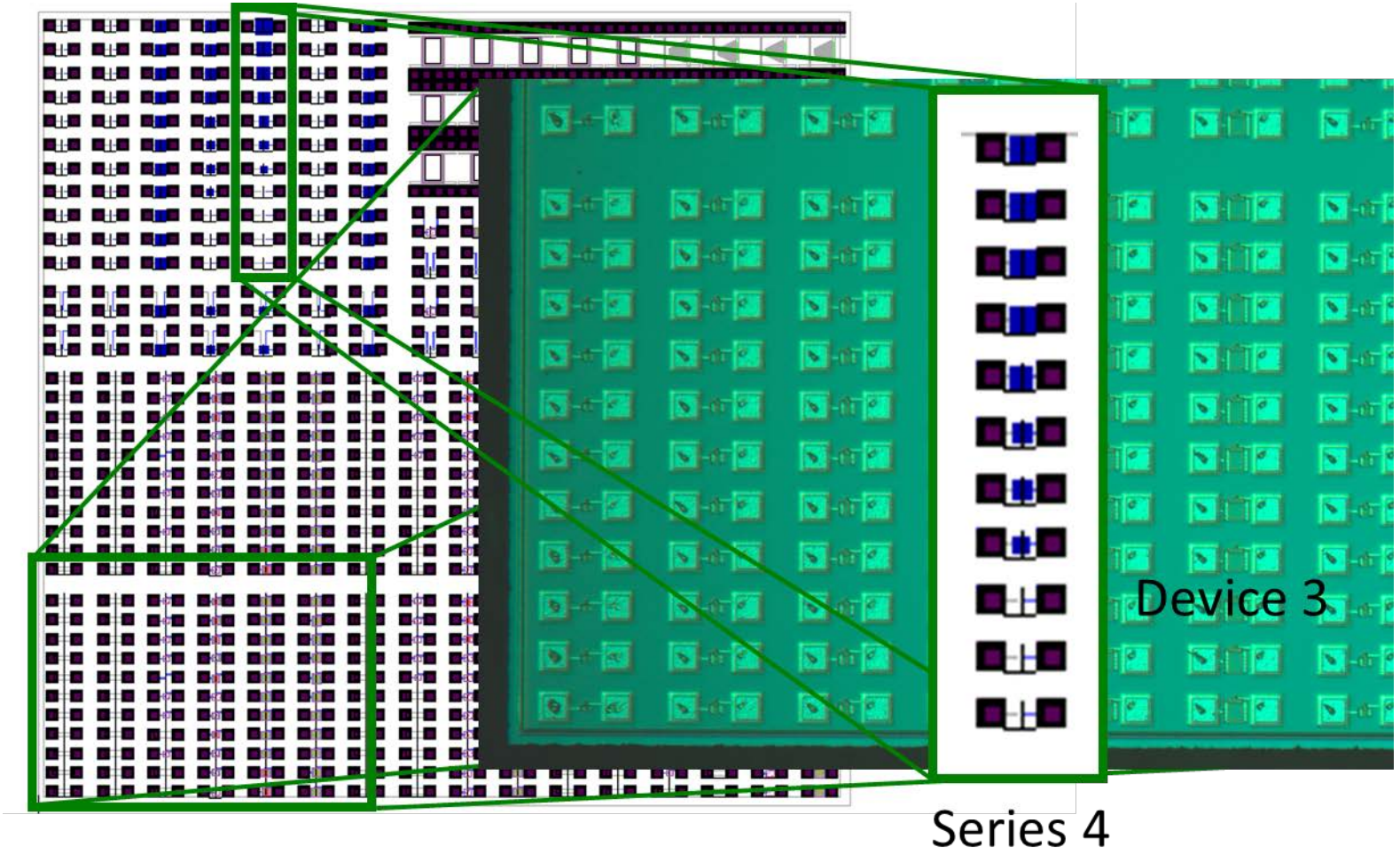
Interface with AFM



AFM mounting holes

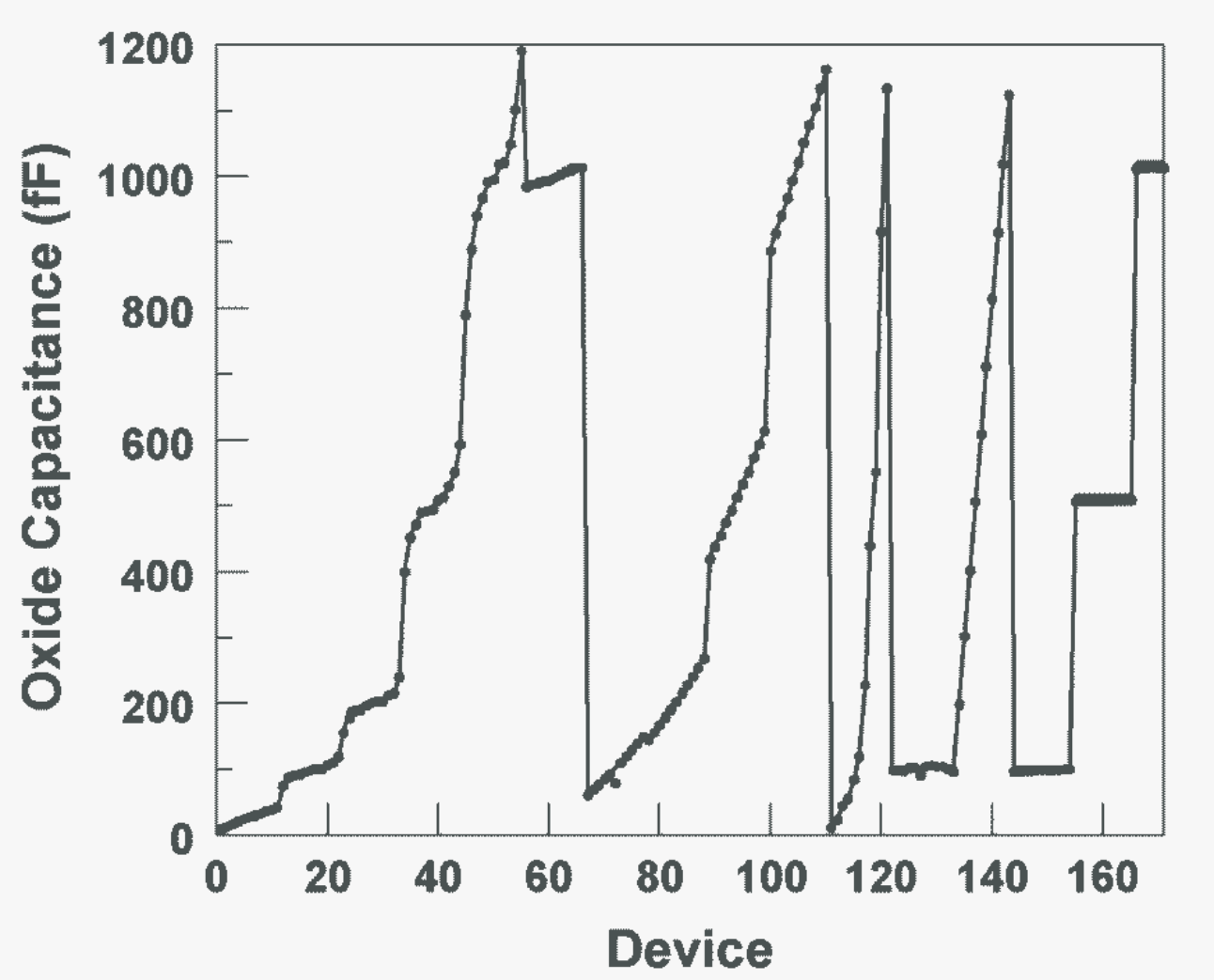
- Simulating and testing proto-type differential current amplifiers.
- Transfer proto-type to miniature circuit board that can clip onto AFM.
- Next chip will integrate differential amplifier and CBCM sensor onto single chip.

Capacitor Test Structure Target



Target for probe based CBCM will be a test chip with a large variety of MOS capacitors from 0.1 to 100 fF.

Capacitor Test Structure Target



Measured with conventional capacitance meter and probe station

Acknowledgements

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