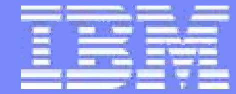

IBM T. J. Watson Research Center

Metrology and Precision for Nanoscale Manufacturing:

Current Trends and Future Directions in Nanoelectronics

Thomas N. Theis,
Director, Physical Sciences, IBM Research

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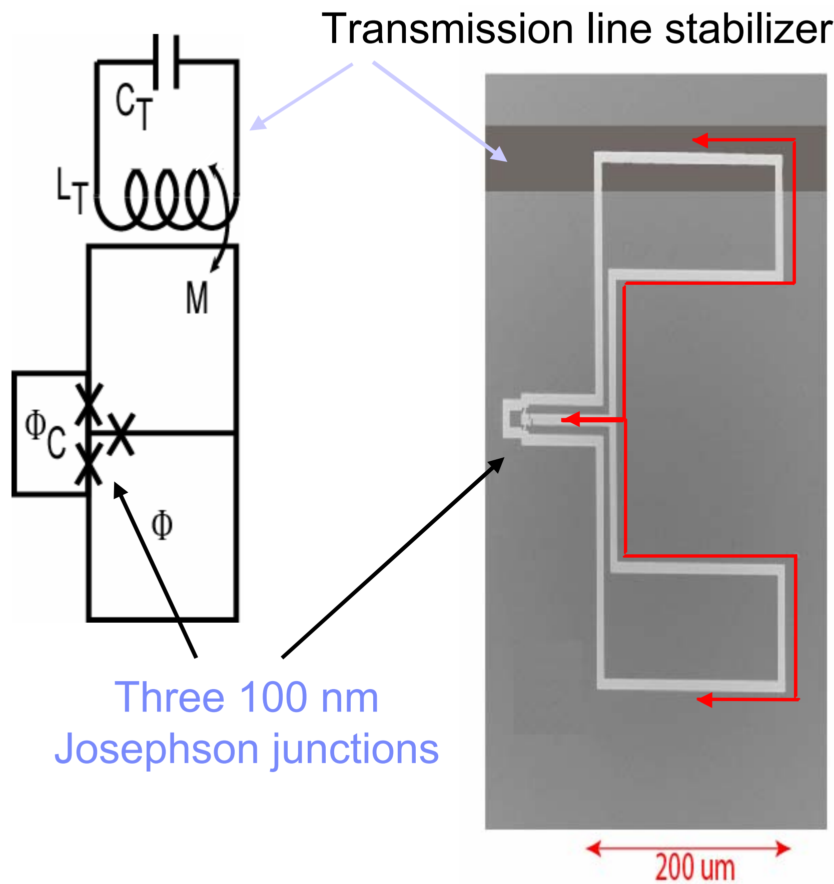
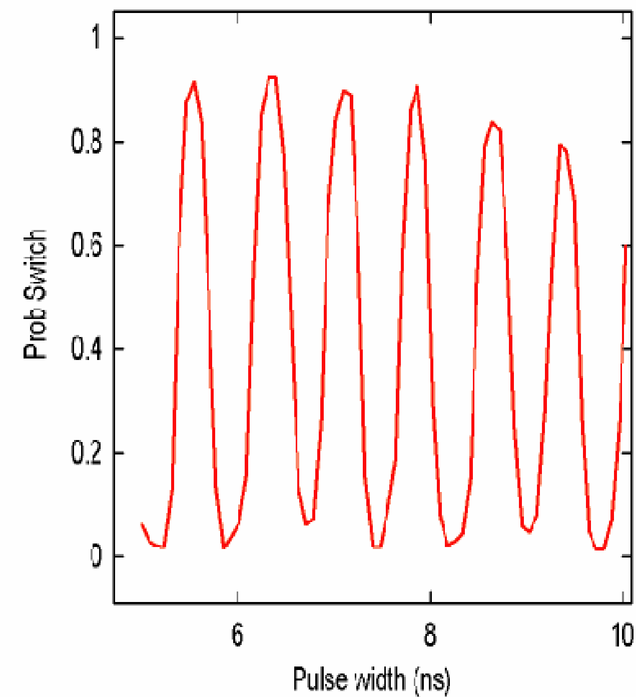
An exploratory quantum device

IBM Josephson Junction Qubit



Three 100 nm Josephson junctions



Measured probability of finding the system in the “current flowing out” state

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5 criteria for building a practical quantum computer
(The DiVincenzo Criteria)

1. Well-defined extendible qubit array (stable memory)
2. Preparable in the “000…” state
3. Long decoherence time (>10^4 operations)
4. Universal set of gate operations
5. Single-quantum measurements (read out)

Meeting these criteria will require

→ unprecedented uniformity of device characteristics

→ extremely precise control of dynamical phase in operation

→ corresponding improvements in metrology

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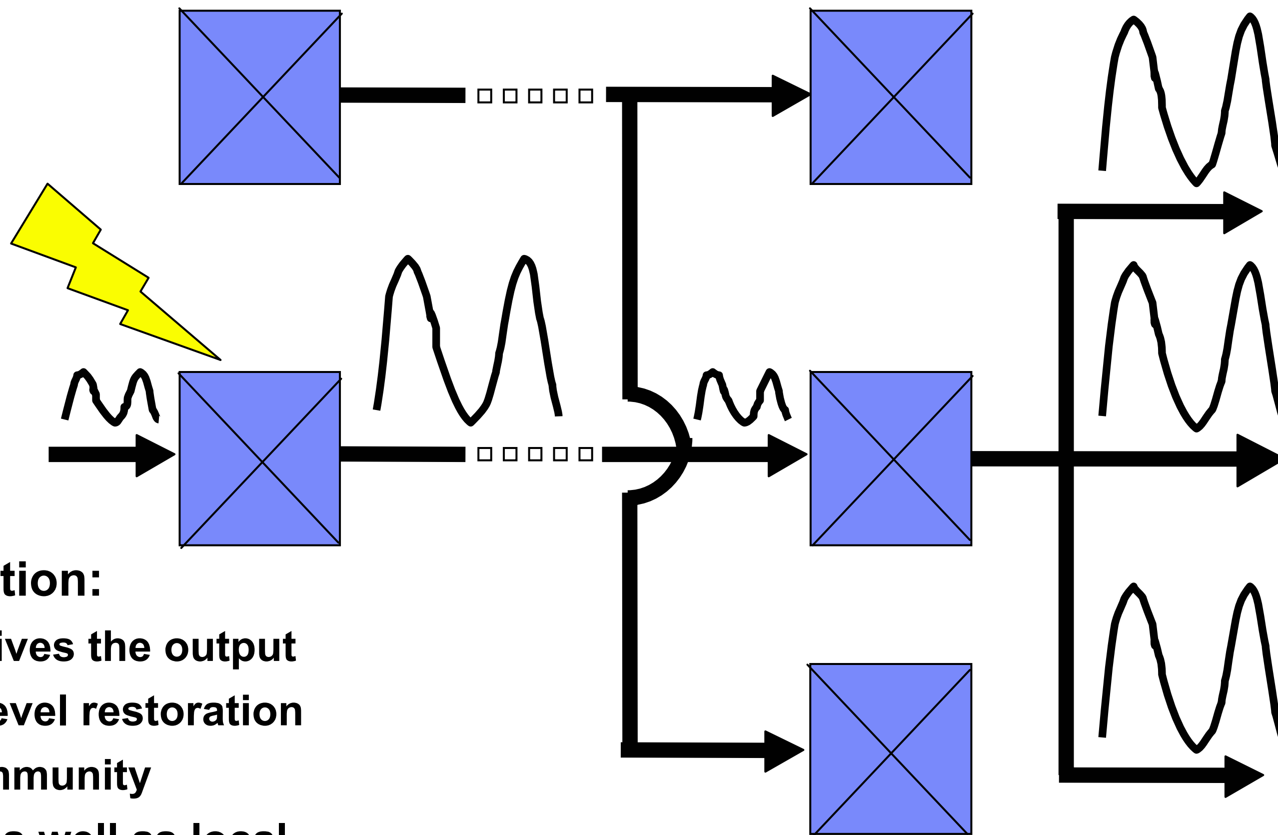
The criteria for historically successful classical logic devices are very different.



Amplification:

- ⇨ Input drives the output
- ⇨ Signal level restoration
- ⇨ Noise immunity
- ⇨ Global as well as local communications

After H.-S. P. Wong, "Novel Device Options" in Sub-100nm CMOS Short Course, *IEDM*, 1999

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Topics

- The extension of silicon CMOS technology
  - Challenges: Device variability and power dissipation
  - Solutions: High-k and other innovations in materials and device structures
- The search for the “ultimate” FET
- Prospects for adiabatic switching and reversible logic
- “Beyond the FET”:
  The Nanoelectronics Research Initiative -- a path for the commercial emergence of quantum devices?

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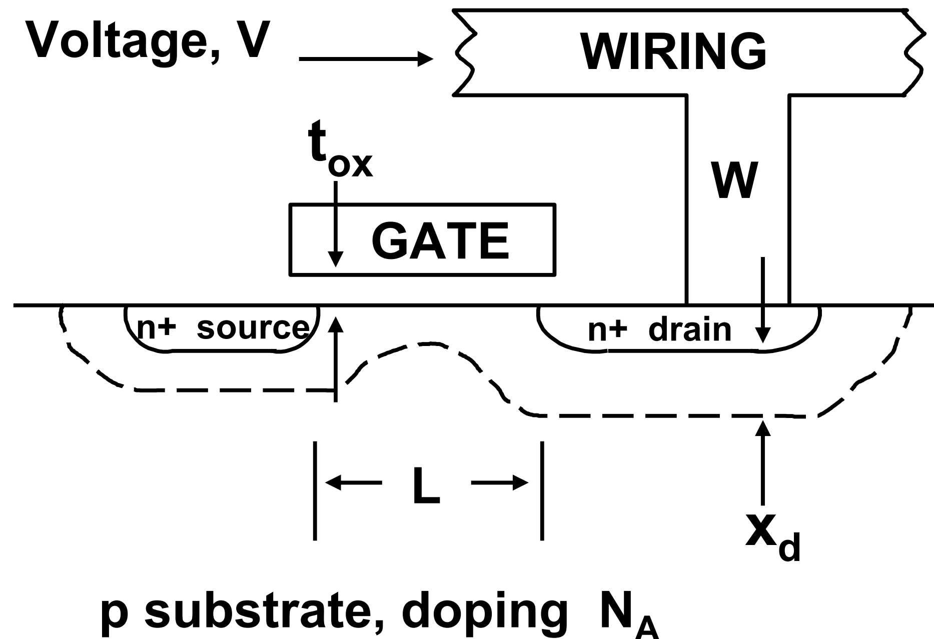
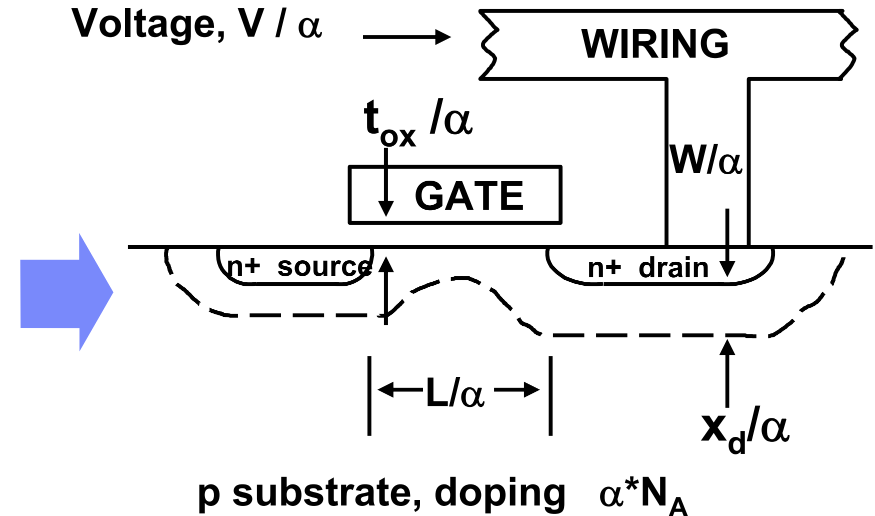
Transistor Scaling

Dennard, et al., 1974





RESULTS:

Higher Density:	α^2
Higher Speed:	α
Lower Power: per circuit	$1/\alpha^2$
Power Density:	**Constant**

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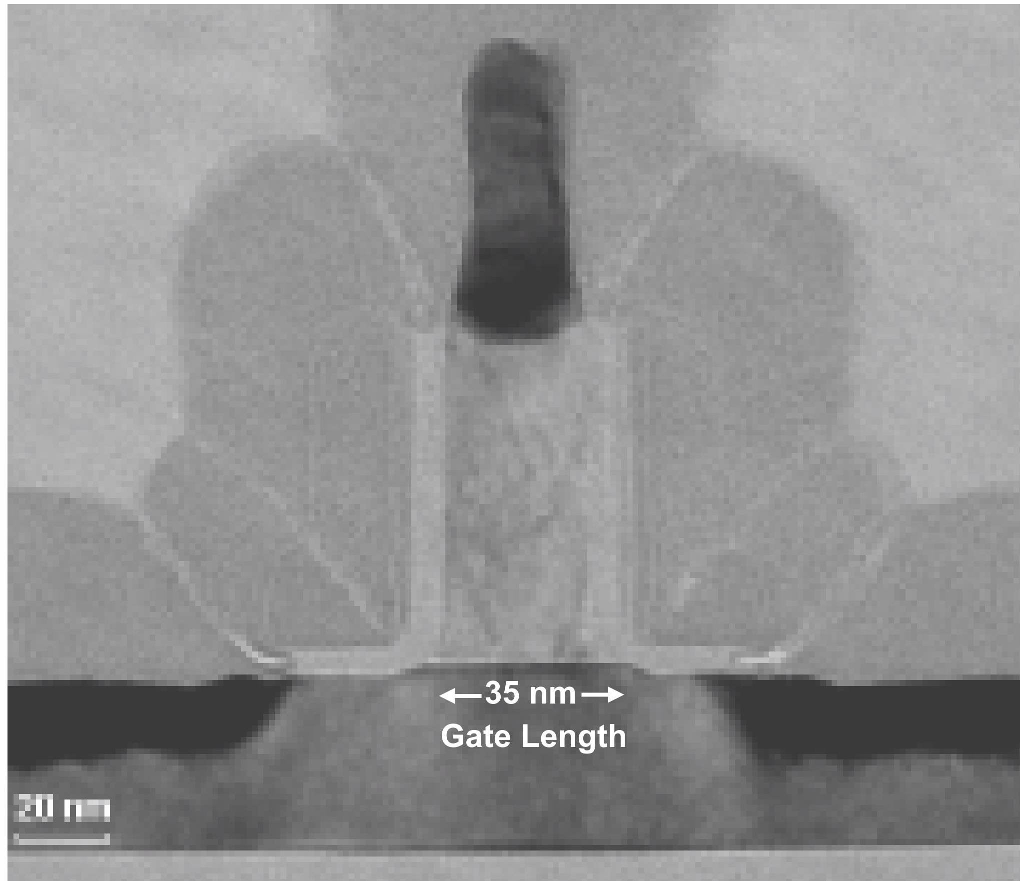
The silicon transistor in manufacturing …



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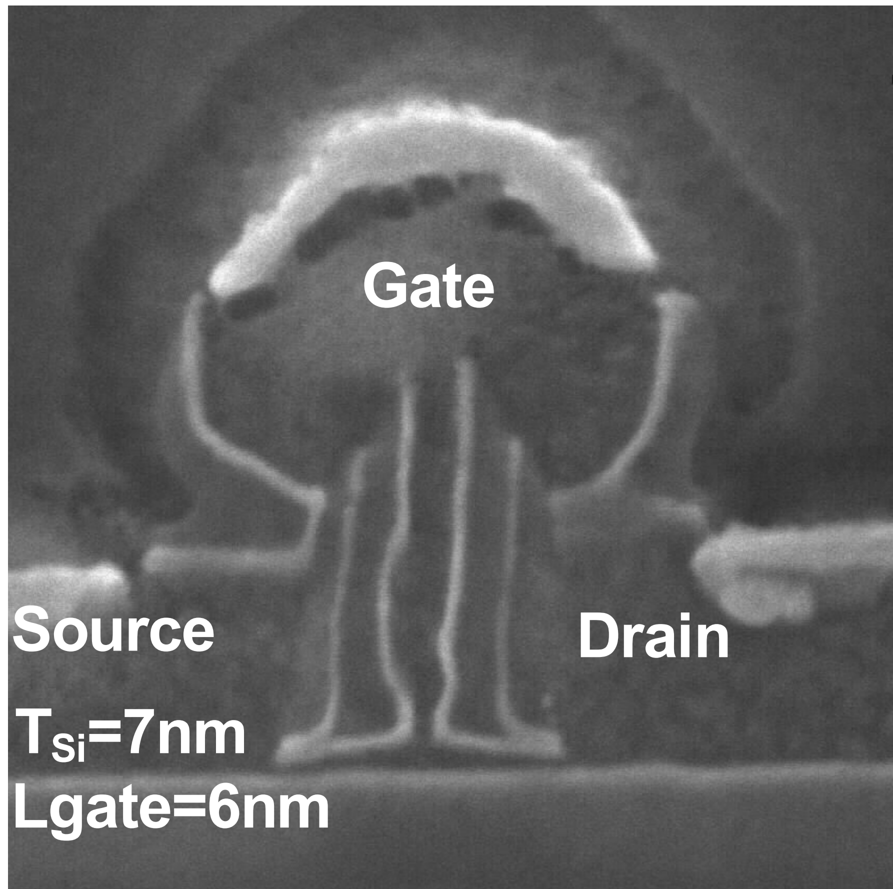
… and in the lab.



B. Doris et al., *IEDM* , 2002

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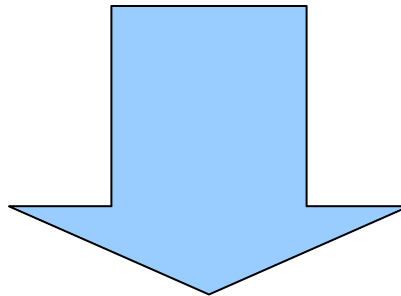
The Problem with Variability

Device-to-device

- Dopant density fluctuations
- Line-edge roughness
- Gate oxide variations
- SOI thickness variations

Across chip

- ACLV
- Process temperature
- Line-edge roughness
- Etch/Deposition rate



Variations in:

- **Intrinsic device parameters**
- **Extrinsic parasitic resistances/capacitances**

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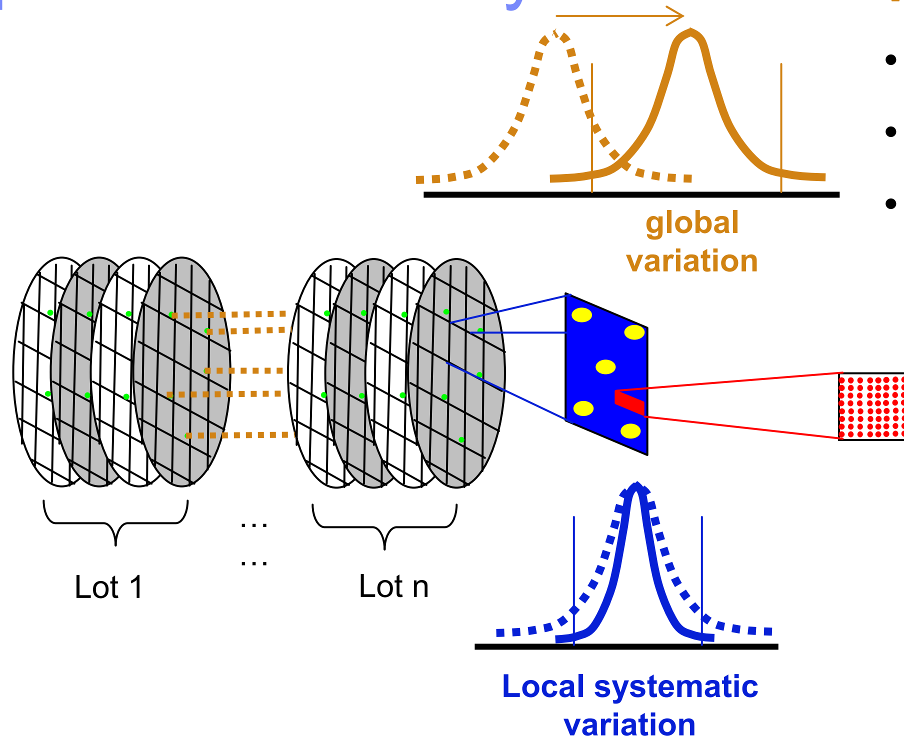
Types of Variability



Wafer/lot uniformity (mean shift)

- Tool/process monitor
- Process control
- SPC control

local random
variation

Across chip systematic variation

- Process characterization
- Process / design interaction
- Design compensation

Local random variations

- Best case σ
- De-convolute from other sources
- Design robustness needed

T. C. Chen, ISSCC 2006

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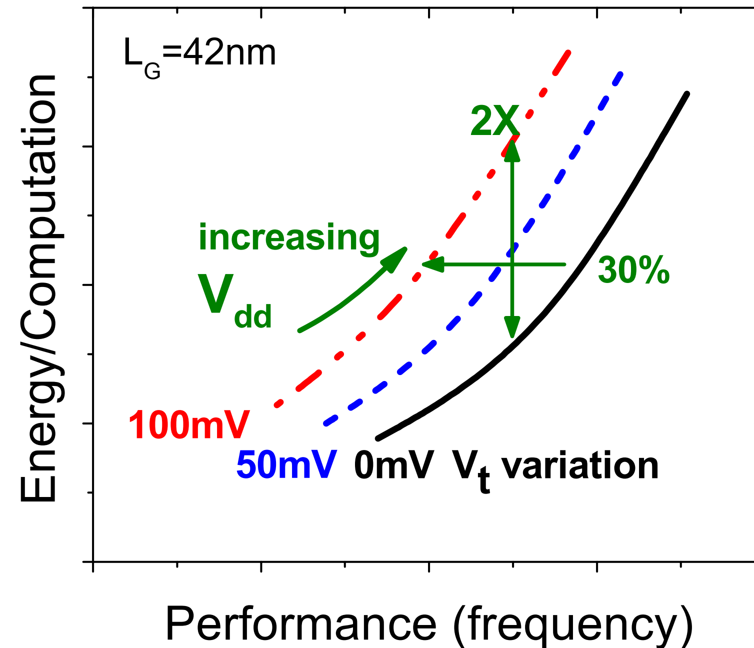
The Impact of Variability on Power and Performance

- **Power consumption dominated by a small fraction of transistors with low threshold**
- **Performance determined by the majority at nominal channel length and Vt**



From J. Cai et al., (IBM).

➢ 30% performance hit or 100% power increase caused by variability

T. C. Chen, ISSCC 2006

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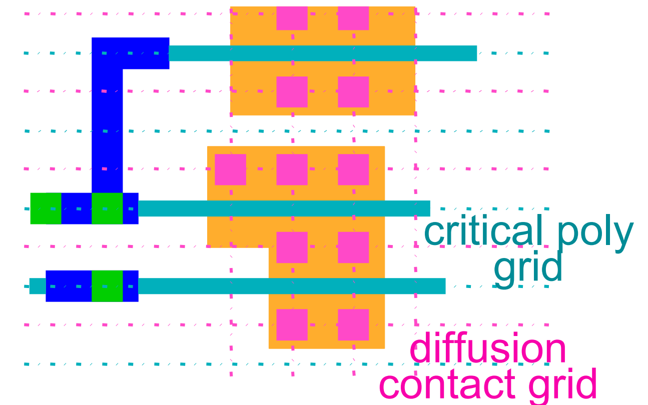
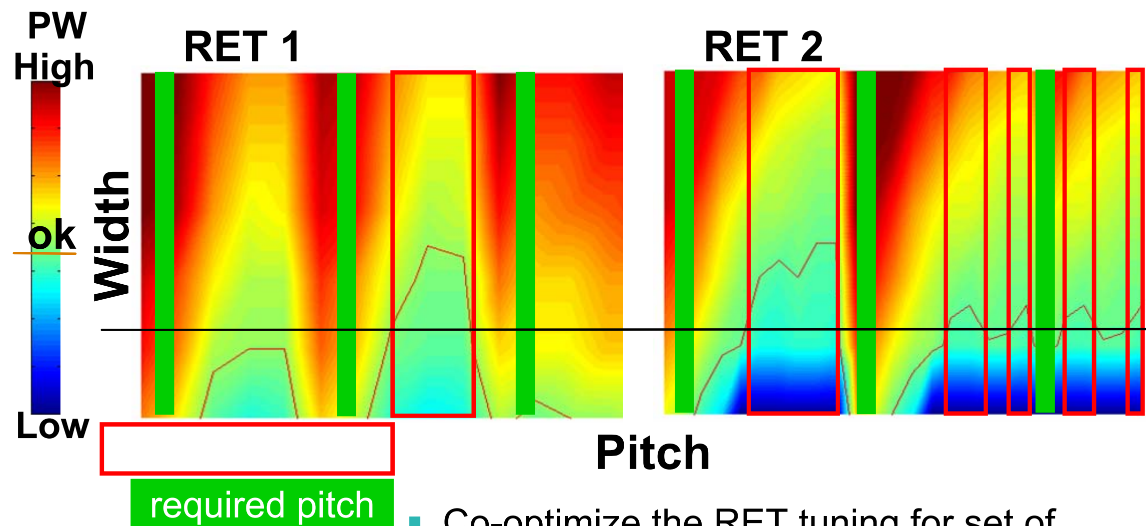
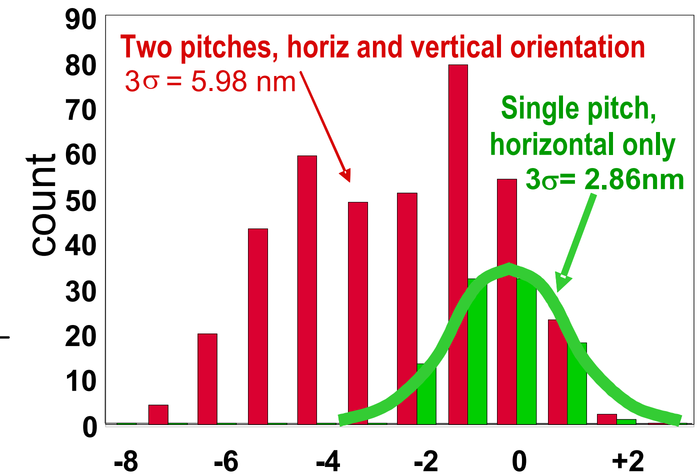
Restricted Design Rules (RDR)

- Narrow features placed on uniform and coarse grid (by macro)
- Single orientation of narrow features (by macro)
- Limit number of pitches and linewidths







- Co-optimize the RET tuning for set of required pitches

T. C. Chen, ISSCC 2006

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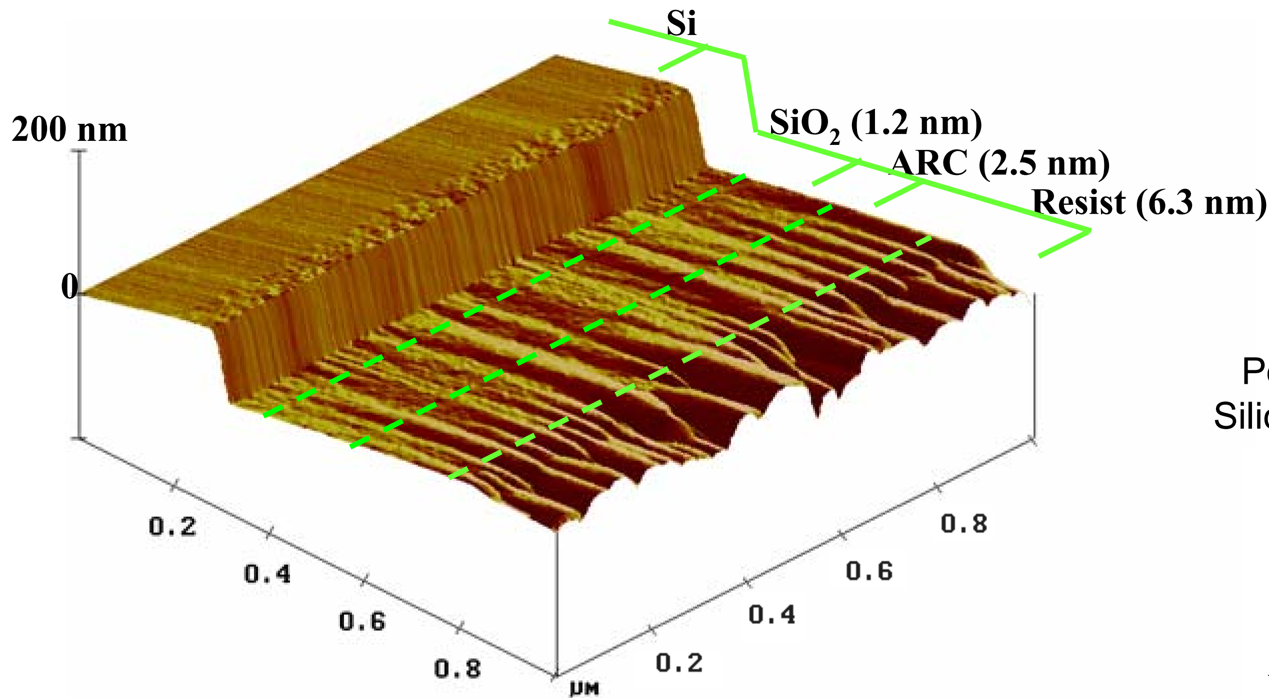
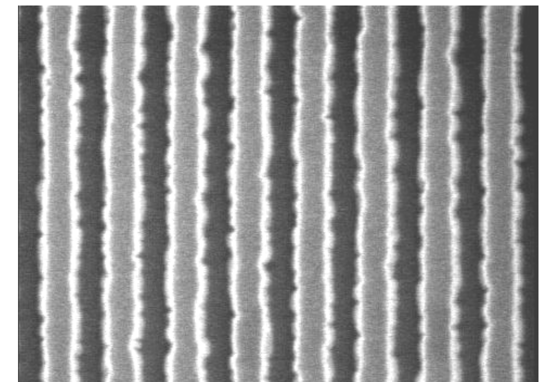
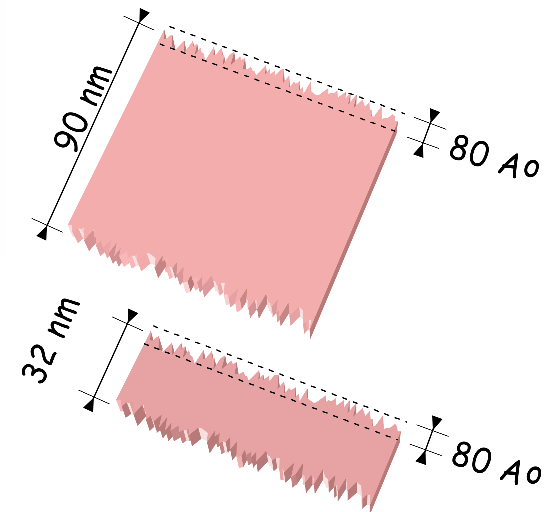
Improved Resist Performance Required for the 32 nm Node



Multilayer stack sidewall roughness from 248nm photoresist transferred into underlayers, measured using AFM



Post-etch Line Edge Roughness on Silicon Oxide Surface after Resist Strip



T. C. Chen, ISSCC 2006

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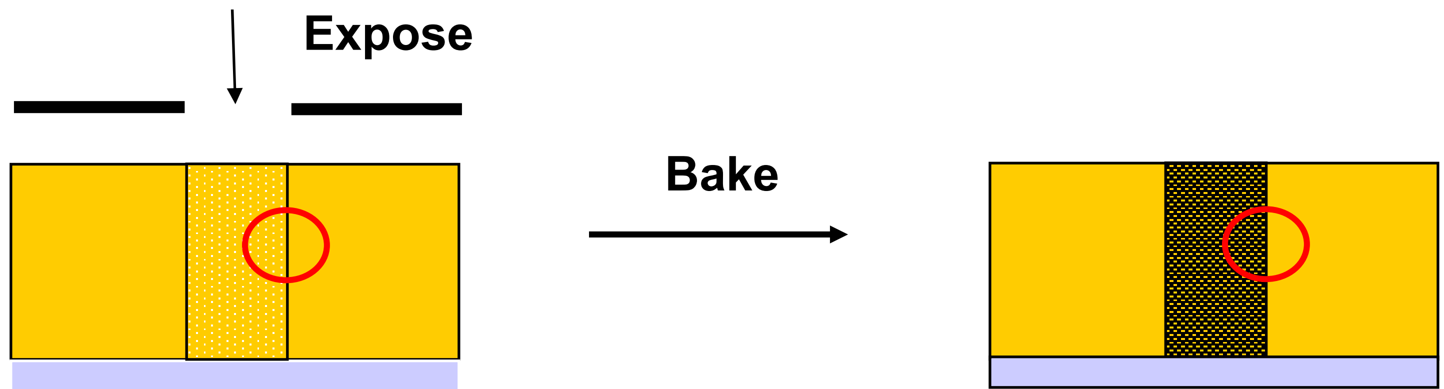
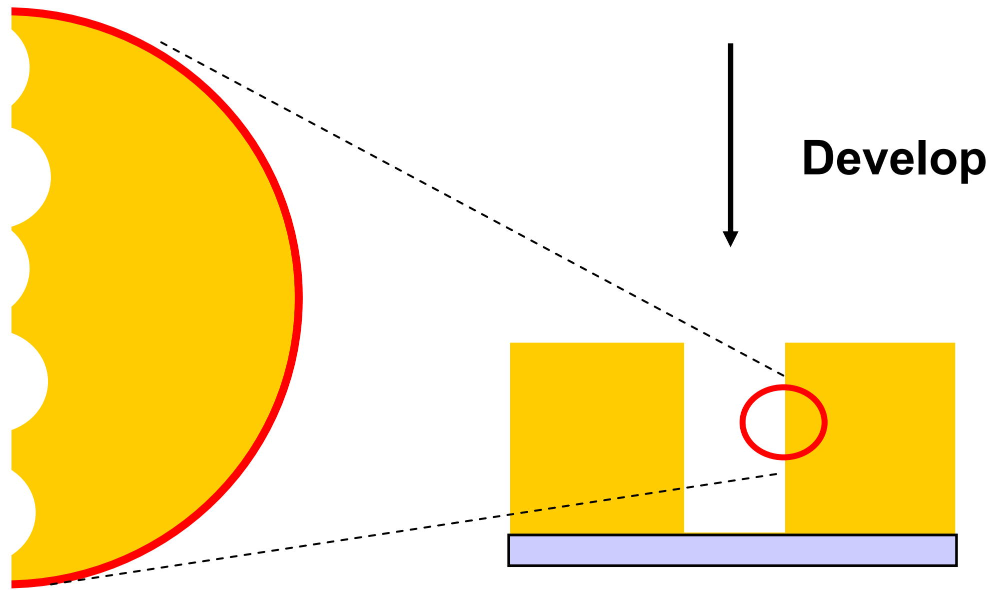
The origin of LER in Chemically Amplified Resists has been carefully studied, and new resists are under development.



Photochemical Generation of Acid (H^+)

Thermal & Chemical Image Blur

Irregular Profile After Development



T.C. Chen, ISSCC 2006

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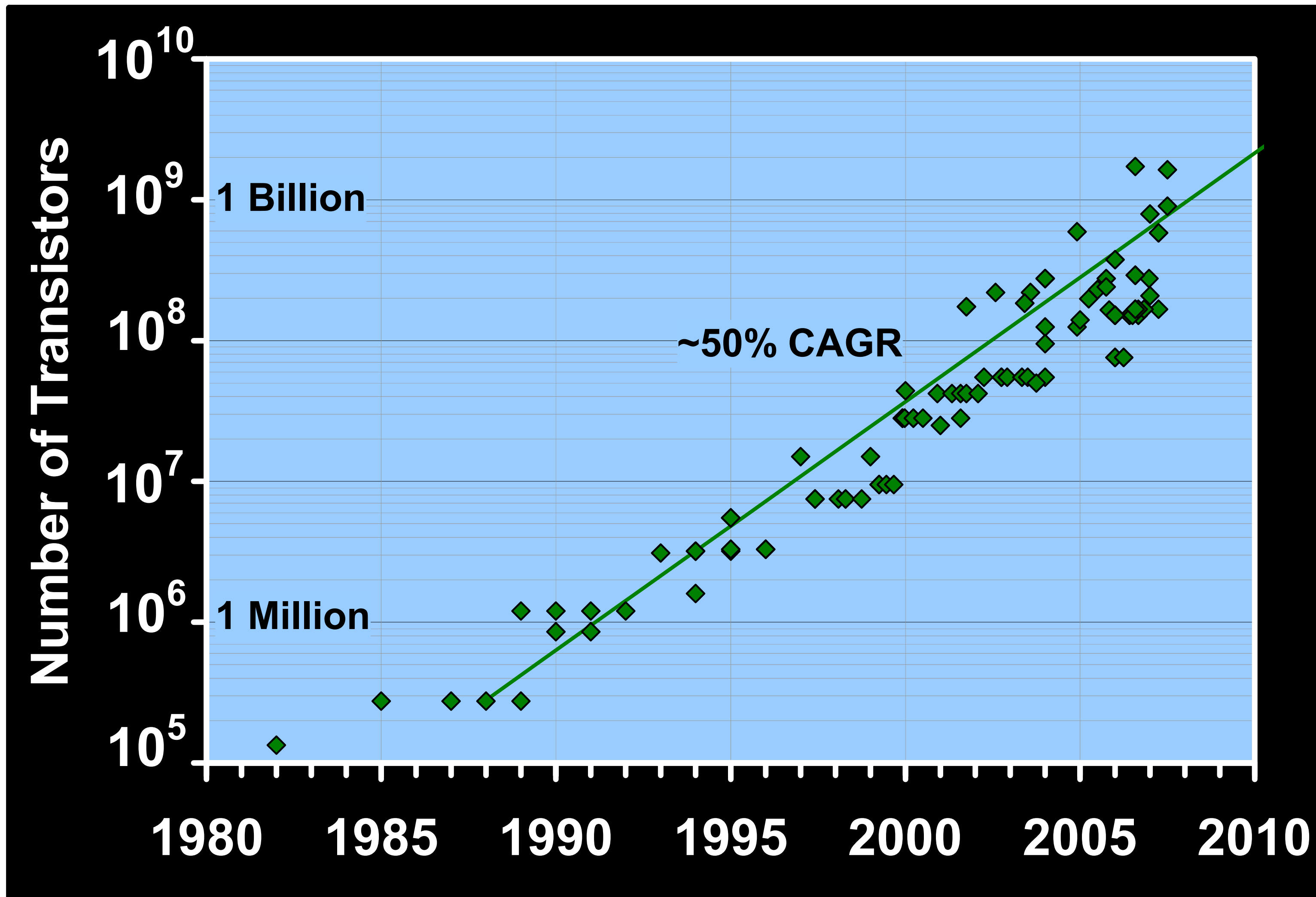
Microprocessor Transistor Count

Lithography continues to deliver density scaling.



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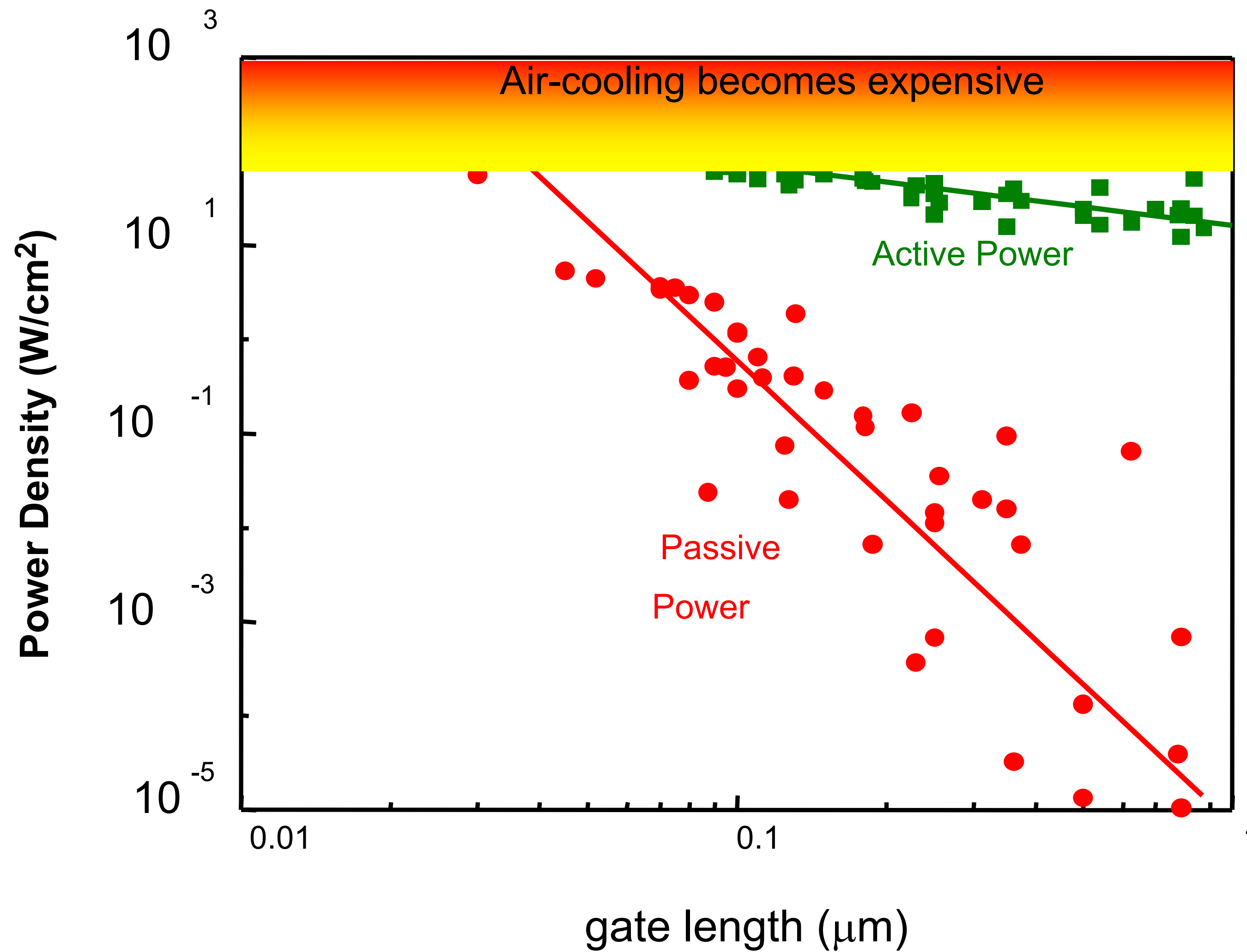
Still, we are approaching some limits.



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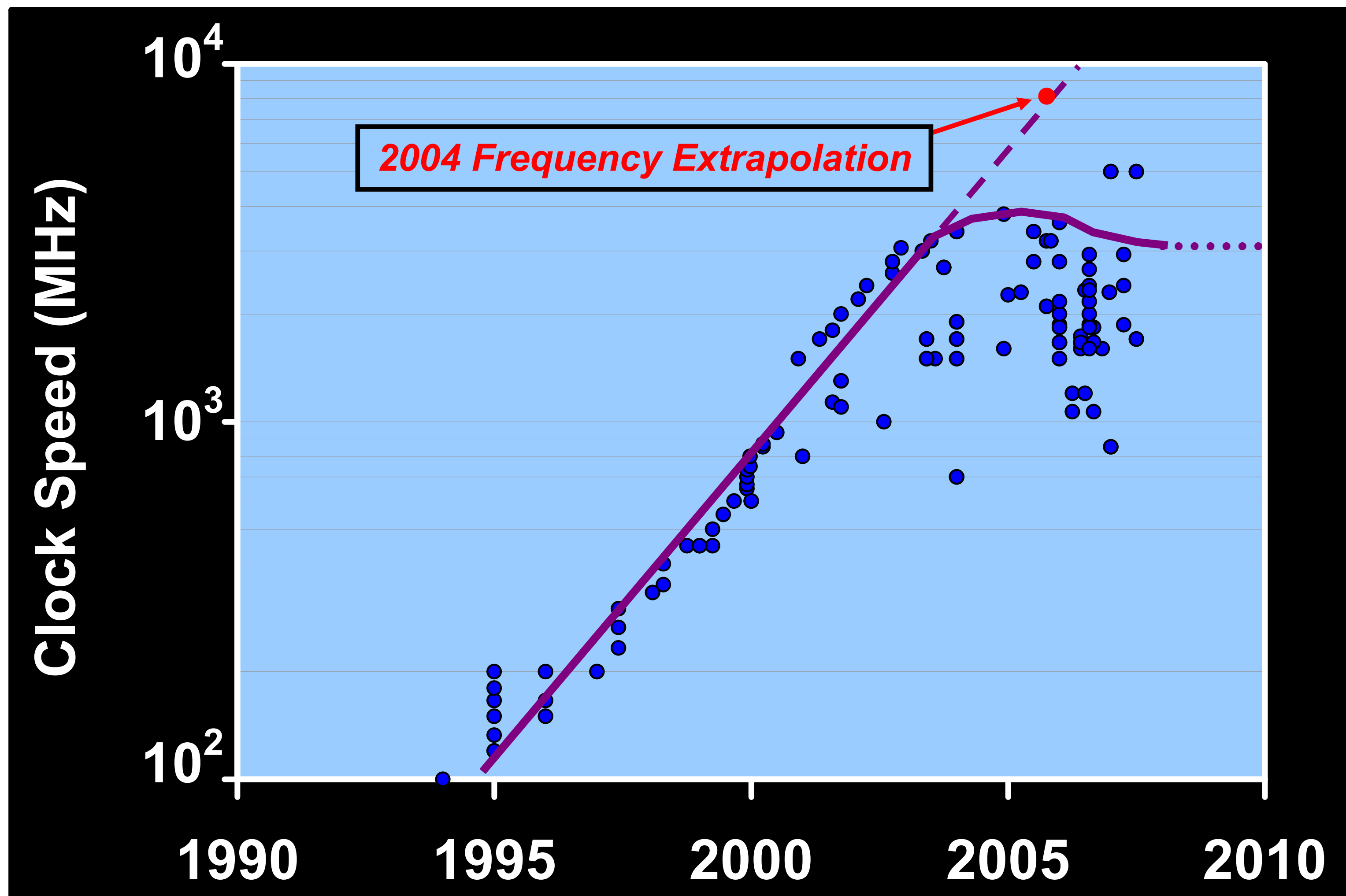
Microprocessor Clock Speed Trends

Cooling costs are limiting clock speeds.



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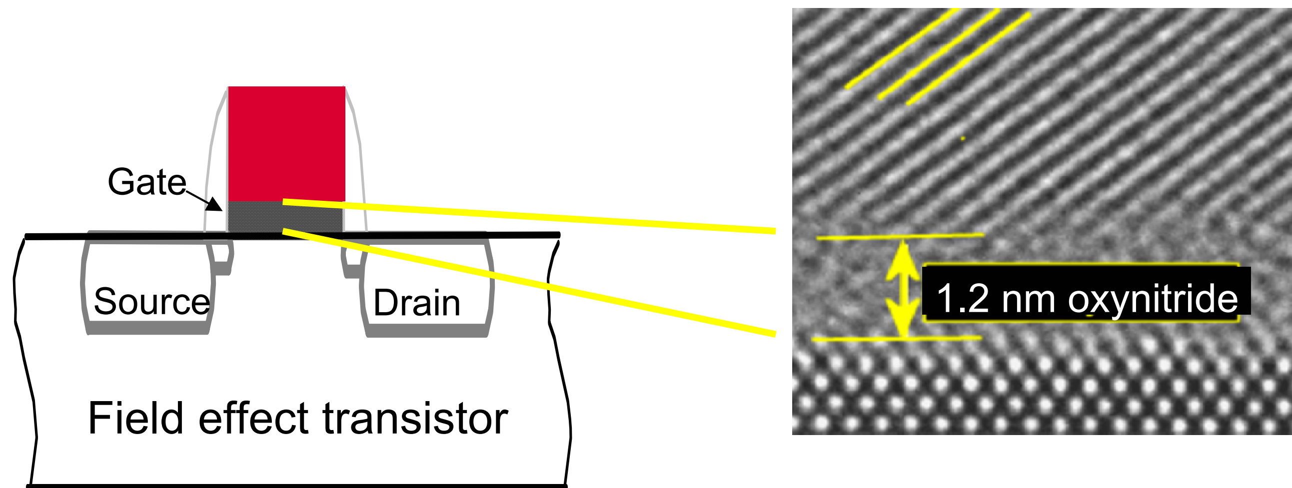
The Problem with Passive Power Dissipation: The Inability to Scale Atoms



- Direct tunneling through the gate insulator will be the dominant cause of static power dissipation.
- Single atom defects can cause local leakage currents 10 – 100x higher than the average current, impacting reliability and generating unwanted variation between devices.

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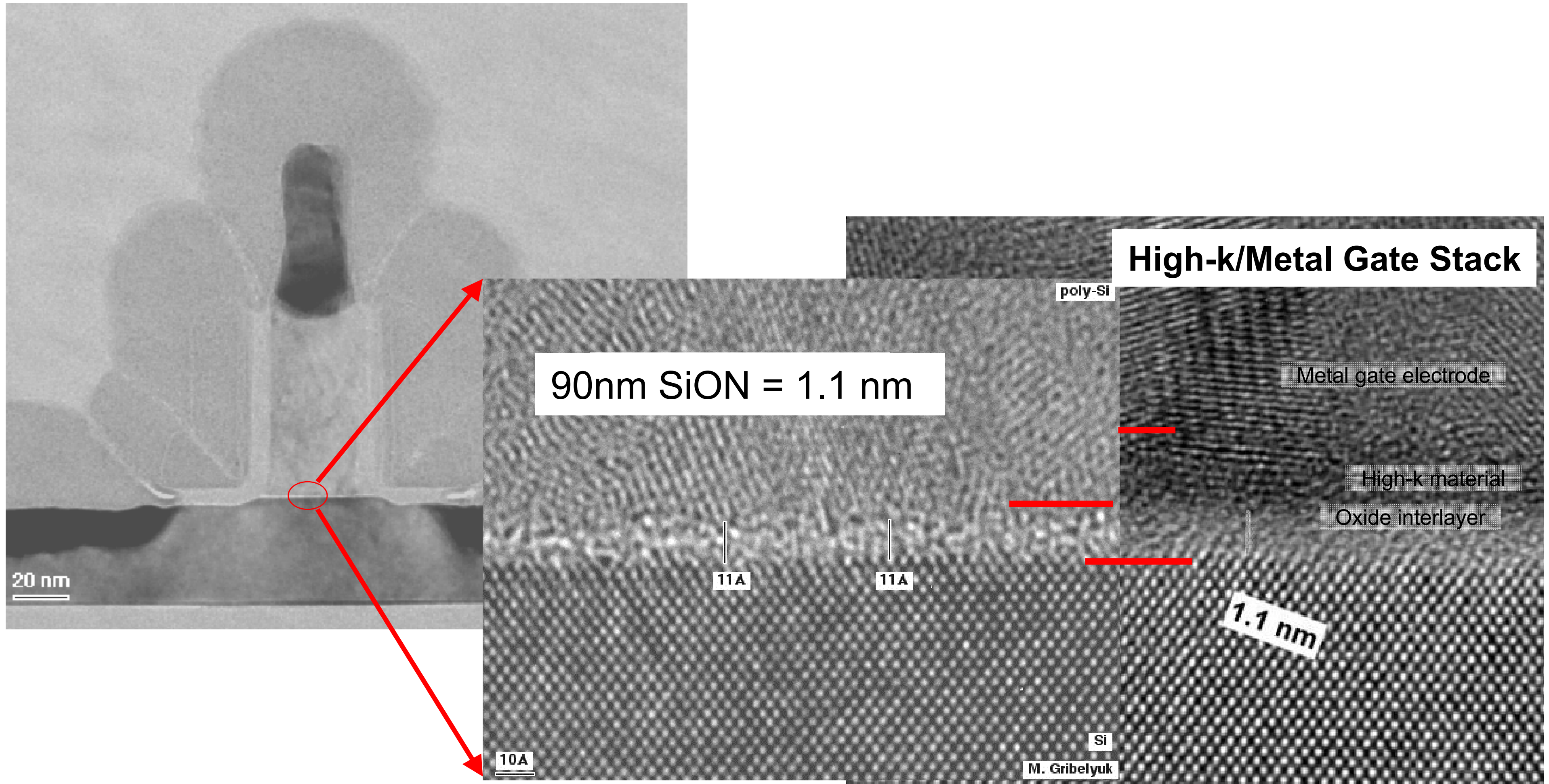
The Work-Around: High-k Insulator / Metal Gate Stack



90nm Gate Dielectric:
Tinv = 19A
ToxGL = 11A

High-k/Metal Gate Stack:
Tinv = 14.5A
ToxGL = 16A

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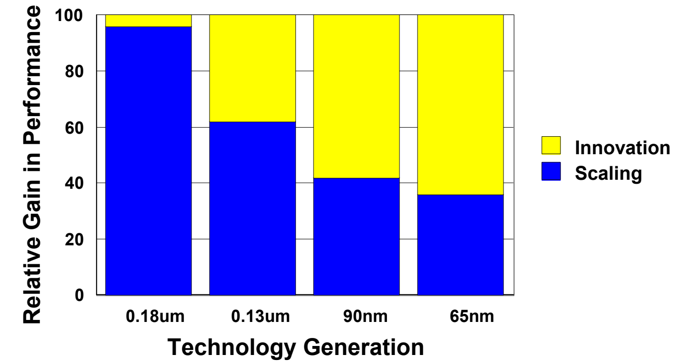
Improving Performance

- No longer possible by scaling alone
  - New Device Structures
  - New Device Design point
  - New Materials



Before the 90's

Since the 90's

Beyond 2005

hydrogen 1 H																		helium 2 He
hydrogen 1 H	beryllium 4 Be												boron 5 B	carbon 6 C	nitrogen 7 N	oxygen 8 O	fluorine 9 F	neon 10 Ne
sodium 11 Na	magnesium 12 Mg												aluminium 13 Al	silicon 14 Si	phosphorus 15 P	sulfur 16 S	chlorine 17 Cl	argon 18 Ar
potassium 19 K	calcium 20 Ca		scandium 21 Sc	titanium 22 Ti	vanadium 23 V	chromium 24 Cr	manganese 25 Mn	iron 26 Fe	cobalt 27 Co	nickel 28 Ni	copper 29 Cu	zinc 30 Zn	gallium 31 Ga	germanium 32 Ge	arsenic 33 As	selenium 34 Se	Bromine 35 Br	krypton 36 Kr
rubidium 37 Rb	strontium 38 Sr		yttrium 39 Y	zirconium 40 Zr	niobium 41 Nb	molybdenum 42 Mo	technetium 43 Tc	Ruthenium 43 Ru	rhodium 45 Rh	palladium 45 Pd	silver 47 Ag	cadmium 48 Cd	indium 49 In	tin 50 Sn	antimony 51 Sb	tellurium 52 Te	iodine 53 I	xenon 54 Xe
caesium 55 Cs	barium 56 Ba	57-70 *	barium 71 Lu	hafnium 72 Hf	tantalum 73 Ta	tungsten 74 W	Rhenium 75 Re	osmium 76 Os	iridium 77 Ir	platinum 78 Pt	gold 79 Au	mercury 80 Hg	thallium 81 Tl	lead 82 Pb	bismuth 83 Bi	polonium 84 Po	astatine 85 At	radon 86 Rn
francium 87 Fr	radium 88 Ra	89-102 **	lawrencium 103 Lr	rutherfordium 104 Rf	dubnium 105 Db	seaborgium 106 Sg	bohrium 107 Bh	hassium 108 Hs	meitnerium 109 Mt	ununnilium 110 Uun	unununium 111 Uuu	ununbium 112 Uub		ununquadium 114 Uuq				

*lanthanoids	lanthanium 57 La	cerium 58 Ce	Praseodymium 59 Pr	neodymium 60 Nd	promethium 61 Pm	samarium 62 Sm	europlum 63 Eu	gadollinium 64 Gd	terbium 65 Tb	dysprosium 66 Dy	holmium 67 Ho	erbium 68 Er	thullium 69 Tm	ytterbium 70 Yb
**actinoids	actinium 89 Ac	thorium 90 Th	protactinium 91 Pa	uranium 92 U	neptunium 93 Np	plutonium 94 Pu	americium 95 Am	curium 96 Cm	berkelium 97 Bk	californium 98 Cf	einsteinium 99 Es	fermium 100 Fm	mendelevium 101 Md	nobelium 102 No

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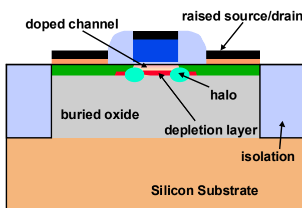
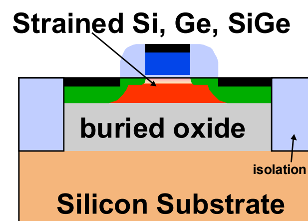
Innovation Will Continue: Transistor Roadmap Options

	2004	2007	2010	2013	2016	2020
Physical Gate	37 nm	25 nm	18 nm	13 nm	9 nm	6 nm

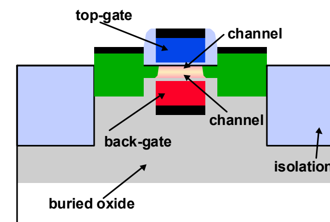
Ultrathin SOI



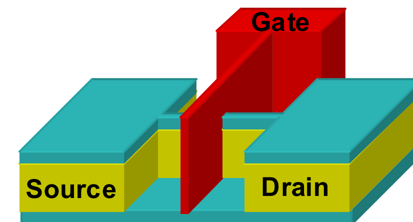
High *k* gate dielectric



Double-Gate CMOS



FinFET



In general, growing power dissipation and increasing process variability will be addressed by introduction of new materials and device structures, and by design innovations in circuits and system architecture.

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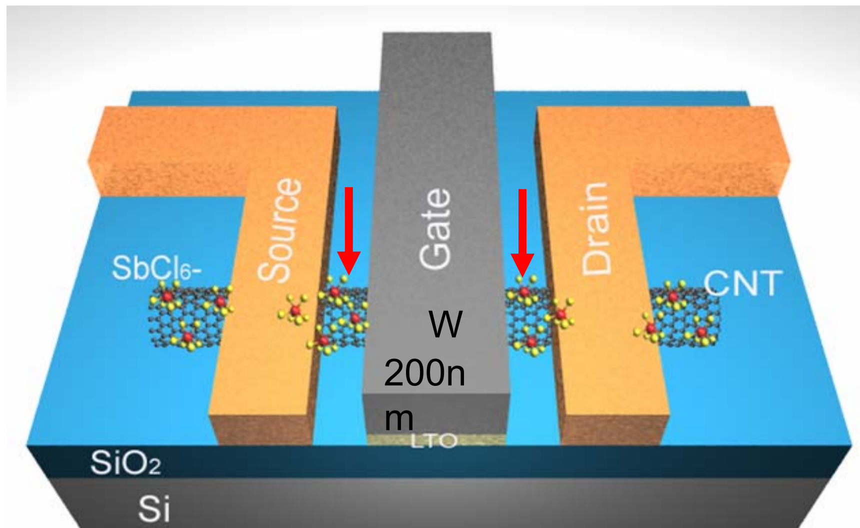
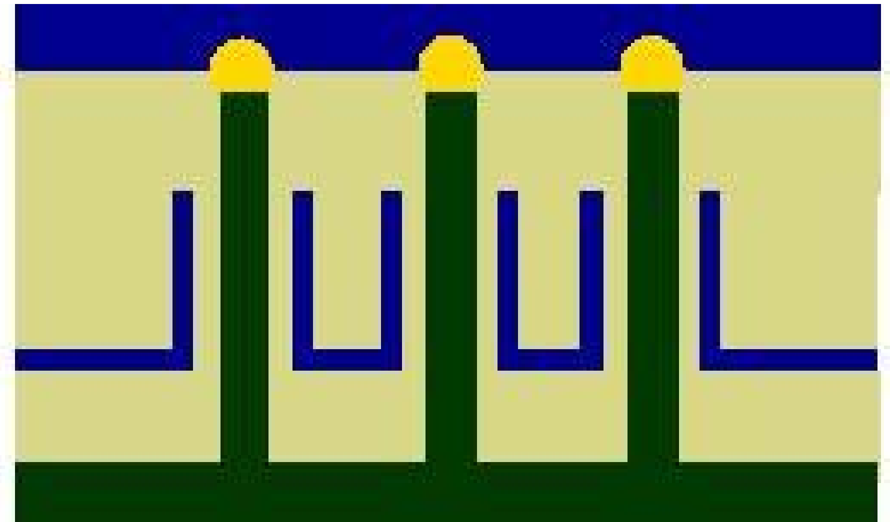
Post-Silicon CMOS: The Quest for the Ultimate FET



Self-Aligned Carbon Nanotube FET:
Extension Contacts Based on
Charge-Transfer Chemical Doping



Vertical Transistor
Based on Semiconductor Nanowires

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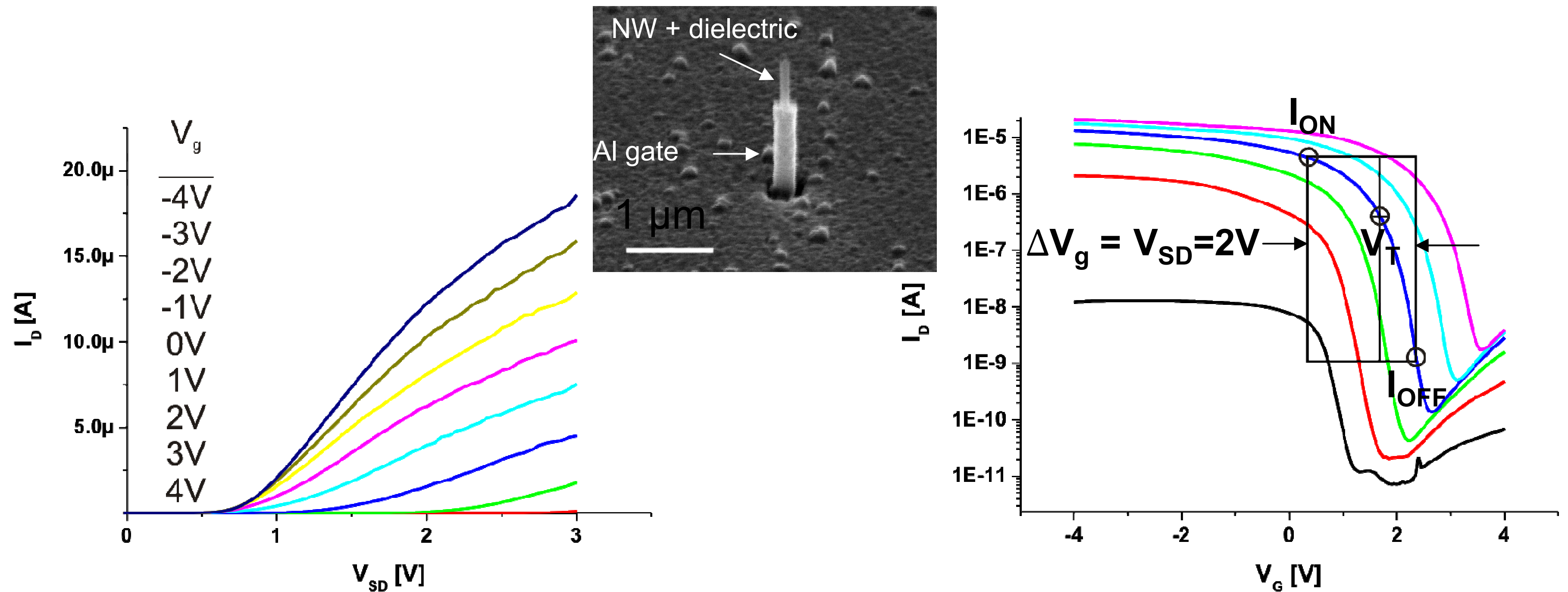
Individual Vertical Surround Gate Si Nanowire FET



- Undoped 60 nm SiNWs on n-Si
- Al bottom contact
  Ni top contact
- 20 nm PECVD SiO_2 dielectric
- Al gate

- Accumulation (p-type)
- Weak inversion
- Large currents (20µA @ V_{sd}=3V)
- No gate leakage (< 1pA @ V_g= 4V)
- Swing ~250 mV/decade
- On/Off ratio ~ 10^4

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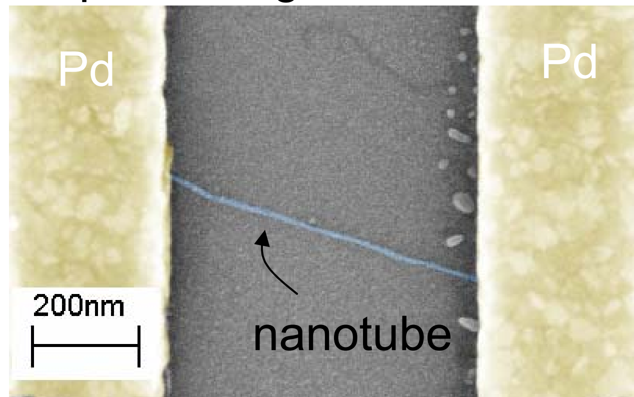
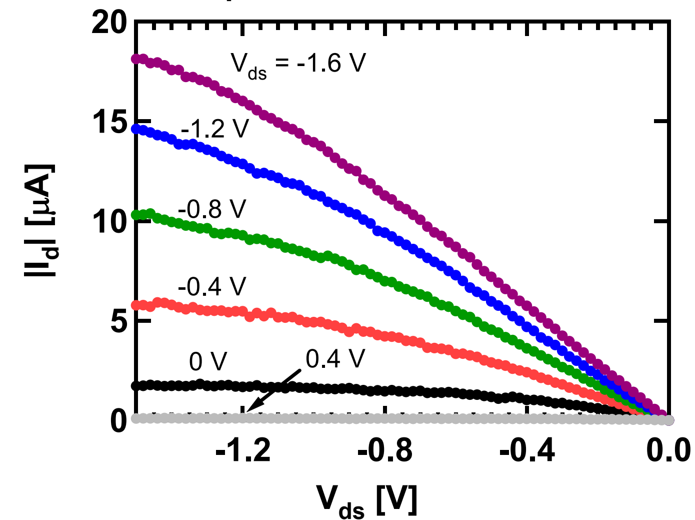
Intrinsic Performance of Carbon Nanotube FETs

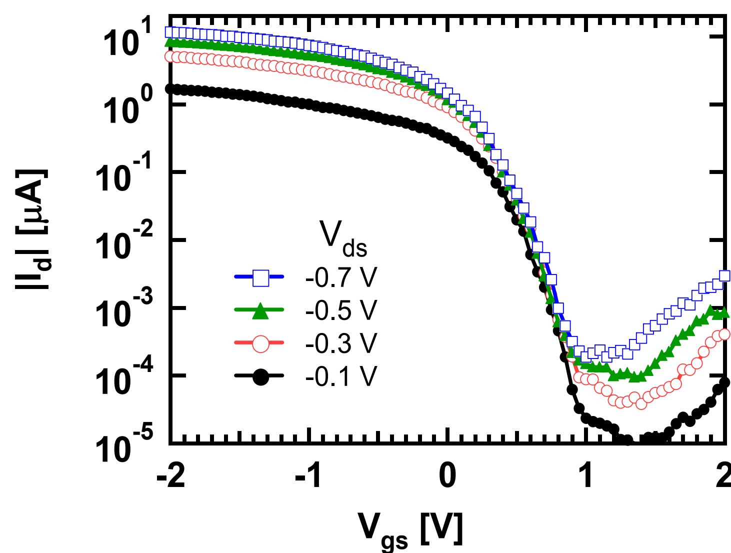
Simple back-gated CNTFET



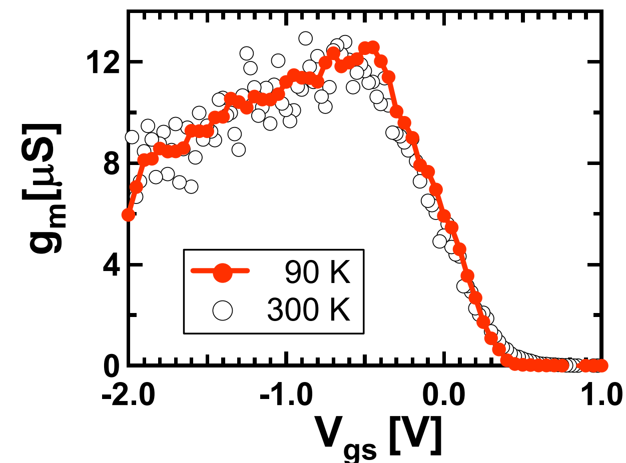
Output Characteristics



Subthreshold Characteristics



Temperature dependence



Yu-Ming Lin *et al.* (IBM), EDL 2005

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Intrinsic Switching Speed of CNFETs

Cut-off Frequency $f_T = \dfrac{g_m}{2\pi C_g}$ C_g : gate capacitance

	Lin et al. (IBM)	Javey et al. (Stanford)	Seidel et al. (Infineon)
Diameter	~ 1.8 nm	~ 1.7 nm	~ 1.1 nm
Gate Dielectric	10-nm SiO_2	8-nm HfO_2	12-nm SiO_2
Maximum g_m	12.5 μS	27 μS	3.5 μS
C_g/L	38 pF/m	120 pF/m	32 pF/m
f_T @ L_g = 65 nm	**800 GHz**	550 GHz	260 GHz

Yu-Ming Lin *et al.* (IBM), EDL 2005

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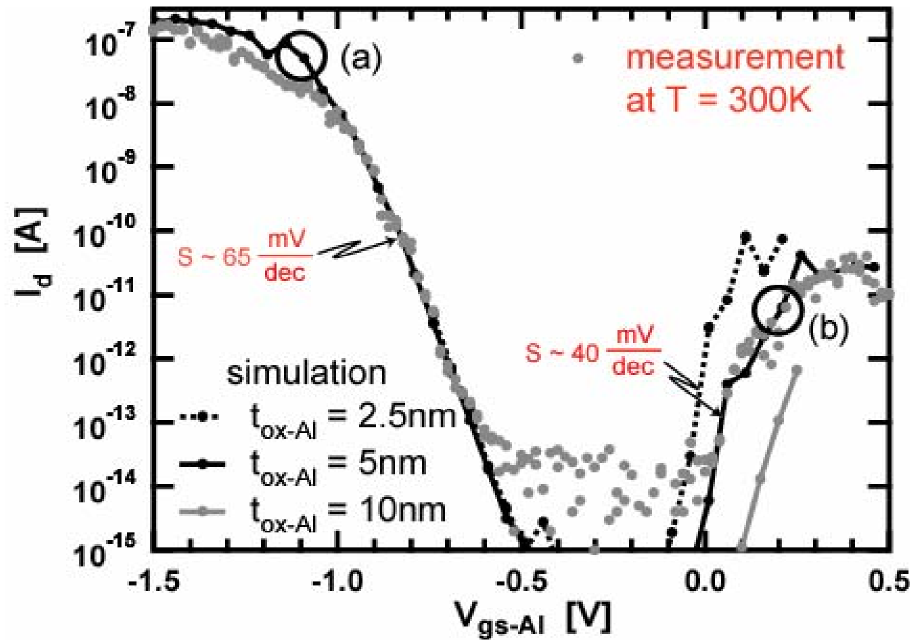
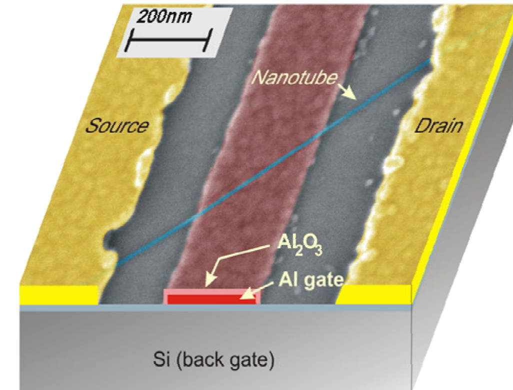
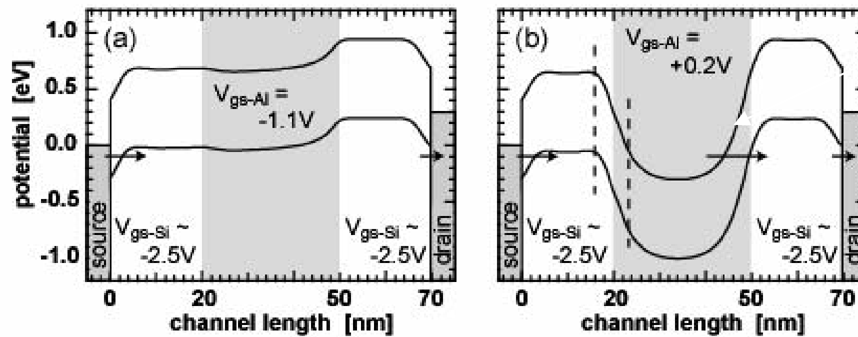
Carbon Nanotube FET:

Potential for greatly improved turn-on characteristics (low-voltage operation)





Dual-Gate CNTFET



J. Appenzeller, Y.-M. Lin, J. Knoch, and Ph. Avouris, Phys. Rev. Lett. **93**, 196805 (2004)

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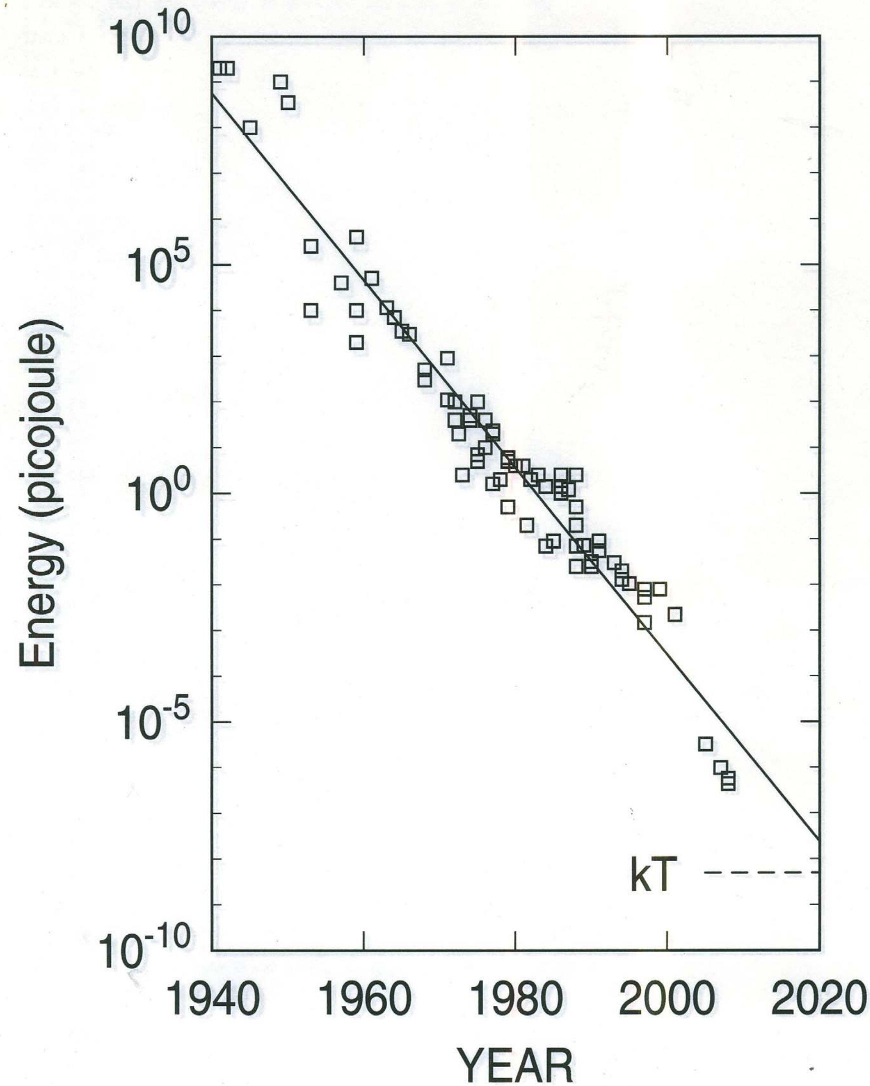
FETs approach the “kT” limit



Data compiled by
R. Keyes,
IBM Research Emeritus

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Can we operate FETs near or below the “kT” limit?

Two paths

1. Conventional Logic:

   Reduce ½CV^2 toward the “kT” limit, accept the reduction in switching speed, and use redundancy and error correction to keep the error rate in bounds. (Refrigeration is allowed, but this makes economic sense only if *total* power dissipation is *reduced*.)

2. Reversible Logic:

   Maintain ½CV^2 well above kT, implement adiabatic switching, energy-conserving reversible logic circuits, and energy-recovering (i.e. resonant circuit) power supply to reduce energy losses per switching event to ~ kT or below.

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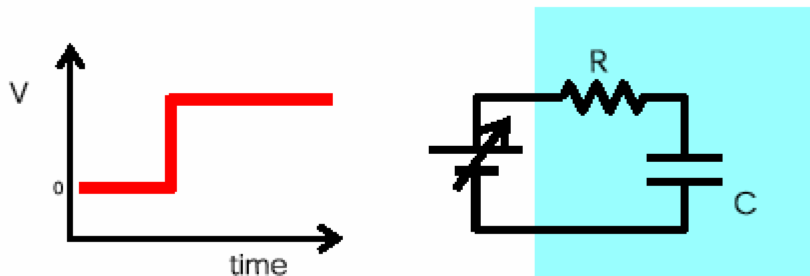
Adiabatic Charging

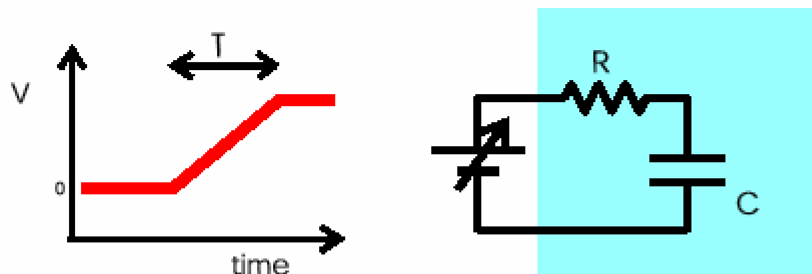
How much energy must be dissipated to charge a capacitor?

Abrupt method



$$E = \frac{1}{2} CV^2$$

Quasi-static Charging



$$E = \frac{1}{2} CV^2 \left(\frac{2RC}{T}\right)$$

(T >> RC)

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Adiabatic Switching

To take advantage of quasi-static charging in logic, there are 2 steps:

First, close switch ($V_{CLK} = V_{CAP}$)

Then, apply clock power (slowly)

Rule 1: never close a switch (turn on an FET) while there is voltage across it.
Rule 2: don't ramp the voltage too quickly.

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Applications of Adiabatic Charging

- Drive specific capacitances which cause large dissipation.
  - Power supplies
  - Energy conserving data bus drivers
- Broadly implement reversible logic.
  - Retractile cascade, reversible pipelines (easy)
  - High-efficiency regenerative power supply (difficult)

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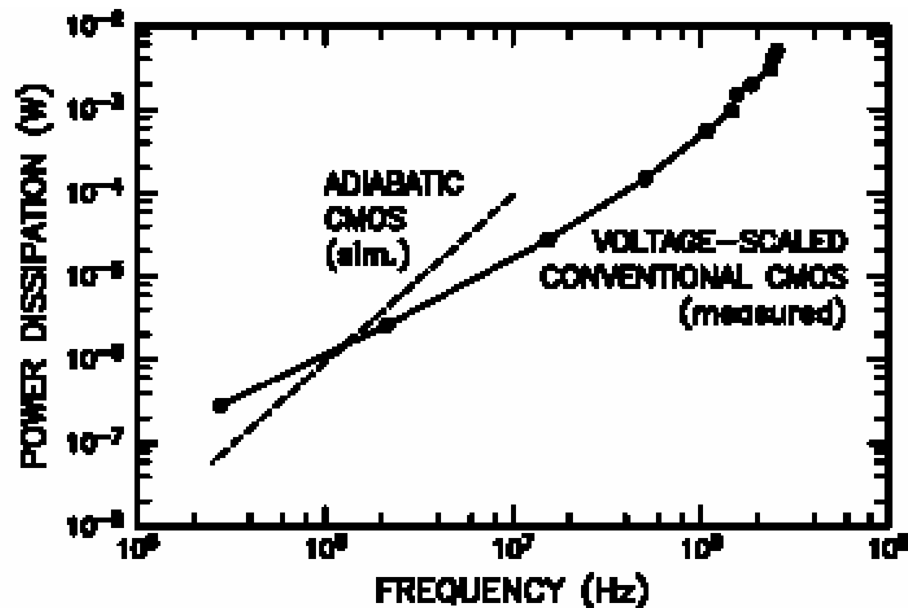
Reversible Logic: Implementation with FETs

- It is conceptually possible to build general purpose reversible computers with energy dissipation per operation going asymptotically to zero as frequency goes to zero.
- But, frequency must be reduced by about 1/1000 to achieve benefits with respect to conventional approaches to CMOS logic.



Dissipation of 4 bit ripple counter (D. J. Frank, 1995)

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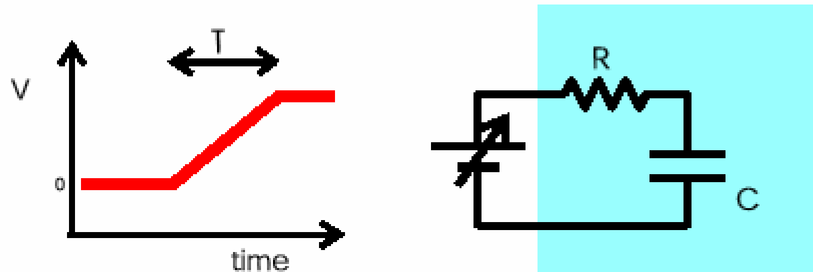
Adiabatic Computing

Energy dissipation depends on the physics of the device!

Quasi-static Charging

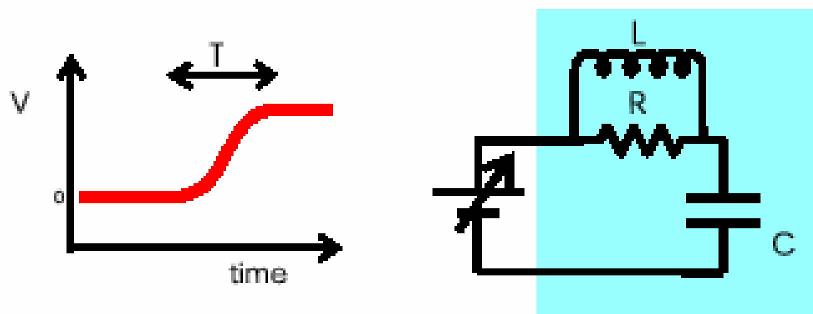


$$E = \frac{1}{2} CV^2 \left(\frac{2RC}{T}\right)$$

This assumes T >> RC.

Energy-time trade-off depends strongly on device physics!

Quasi-static Charging + Superconductivity



Charging through a super-conductor, which behaves as an inductor and resistor in parallel.

$$E = \frac{\pi^4}{8} CV^2 \frac{RC(L/R)^2}{T^3}$$

This assumes T >> RC and T >> L/R.

DJ Frank, MIT Workshop on Reversible Computation, February 14, 2005

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Will there be a successor to the FET?

- Many have written about this subject.

- An article by George Bourianoff ("The Future of Nanocomputing", IEEE Computer 36, pp. 44–53) sparked discussions within the SRC regarding the objectives of a new research program – the Nanoelectronics Research Initiative (NRI) – which would stimulate the exploration of devices "beyond the FET".

→ computational state vectors other than electronic charge

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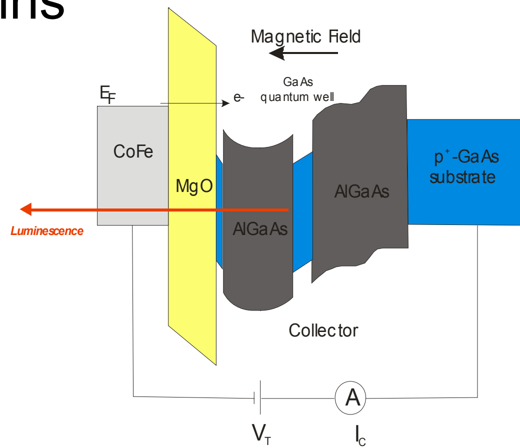
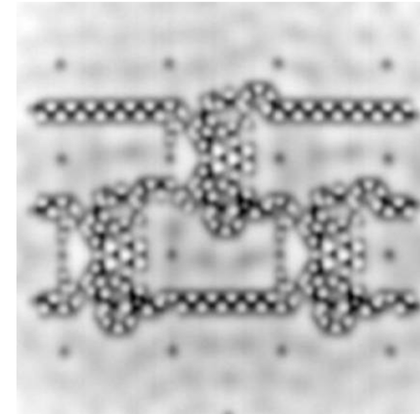
Beyond Charged-Based Logic?

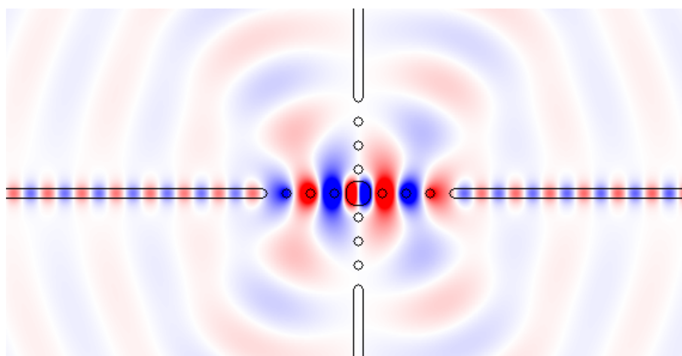
- Spins



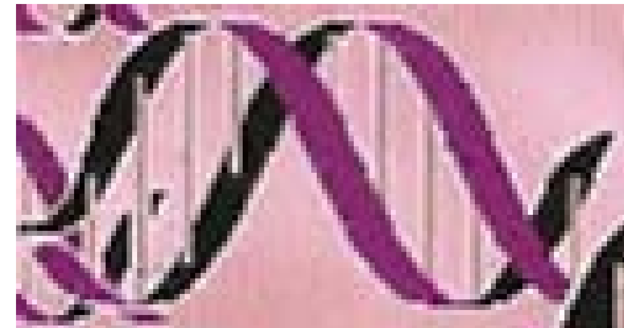
- Nanomechanics



- Photons and Plasmons



- DNA Chemistry



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Nanoelectronics Research Initiative (NRI)

- AMD, Freescale, Micron, TI, IBM, Intel
  → Joint Industry funding of University Research
- Promoting both
  - Invention / Discovery (distributed research, “let many flowers bloom”)
  - Proof of Concept (focused university consortia with outstanding facilities)
- “Extend the historical cost/function reduction, along with increased performance and density … orders of magnitude beyond the limits of CMOS”
  - Computational State Vectors other than Electronic Charge
  - Non-equilibrium Systems
  - Novel Energy Transfer Mechanisms
  - Nanoscale Thermal Management
  - Directed Self-assembly of such structures

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A device that switches much faster than the ultimate transistor must dissipate much less power per switching event than the ultimate transistor.

- Fast, near-adiabatic switching
- Energy-conserving (reversible) logic
- Precise control of dynamical phase over many logical operations
- Fine-grained error correction

A device that can be integrated much more densely that the ultimate transistor will be much smaller than the ultimate transistor.

- "Classical" logical states approximated by small ensembles of quantum states
- Quantum decoherence contributes to error rate
- Fine-grained error correction

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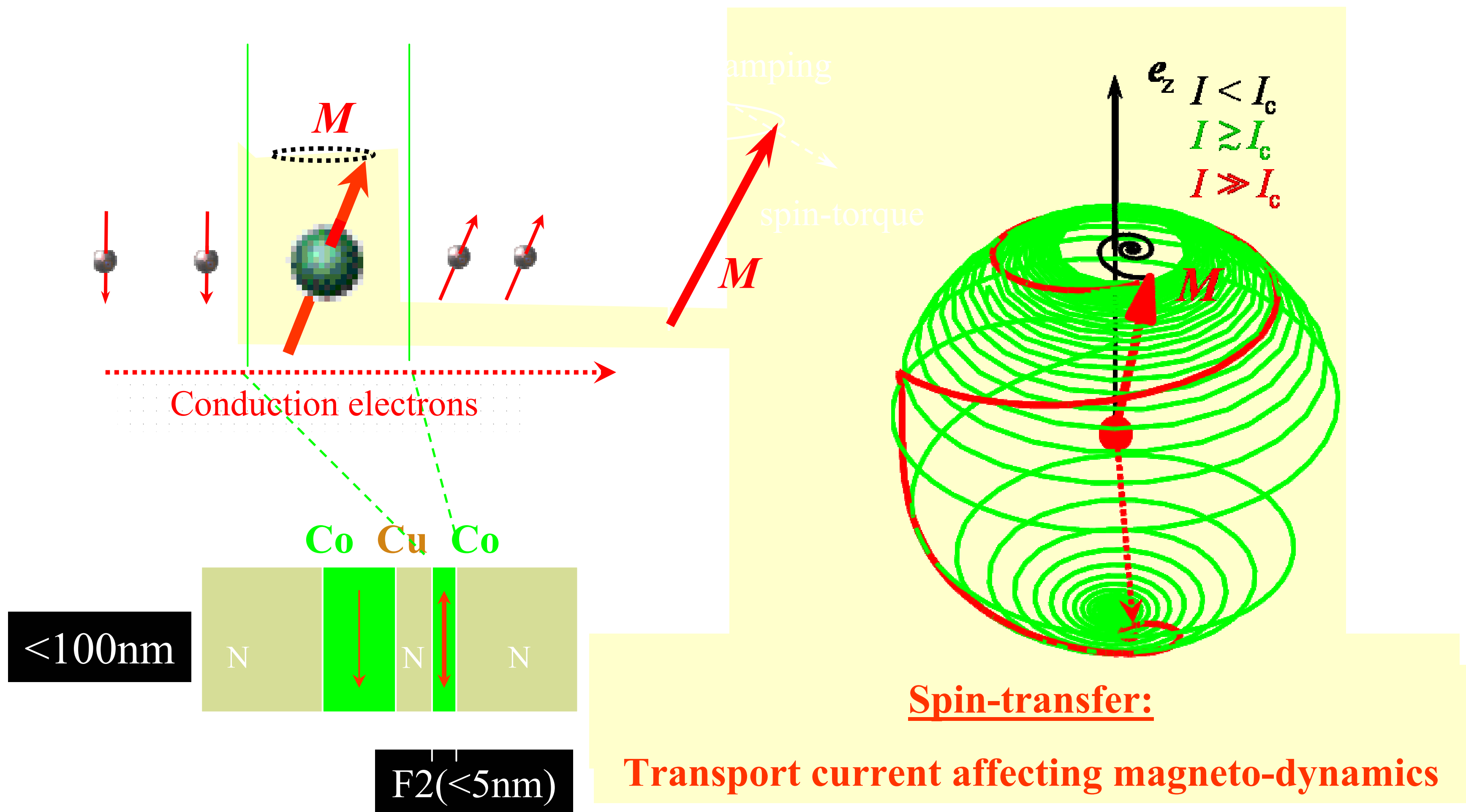
Spin angular momentum transfer and spin-torque:

J. C. Slonczewski, J. Magn. Magn. Mater. **159,** L1 (1996); ibid, **195**, L261 (1999).

J. Z. Sun, J. Magn. Magn. Mater. **202**, 157 (1999); Phys. Rev. B62, 570 (2000) , Nature **425**, 359 (2003).



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Unknowns

- The device
  (So far, nothing smaller or faster than an FET can reliably gate another device.)
- Energy cost of the control system.
  - Analogous to a clock in a conventional circuit?
  - Stringent timing requirements and limits on energy dissipation?
- Energy cost of error correction

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Conclusions

- Silicon CMOS logic will be extended at least another 10 years.
  - New materials and transistor structures
  - Cooperative circuit and device technology co-design
- BUT … we appear to be entering an era in which fundamental physics and truly adventurous electrical engineering will again play a central role in the evolution of information technology.
  - New materials, devices, and circuit architectures …
  - … pushing the physical limits of precision and metrology!

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Thanks to colleagues ...

Paul Solomon

David J. Frank

Charles Bennett

for many discussions, both recent and long past ...

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