An Update on the National Semiconductor Technology Center (NSTC)

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CHIPS for AMERICA | Natcast

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  - Are informational, pre-decisional, and preliminary in nature.
  - Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
  - Are subject in their entirety to any final action by NIST or the Department of Commerce.
- Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or funding opportunities.

CHIPS for America

$39 billion
for incentives

Invest in U.S. production of strategically important semiconductor chips, and assure a sufficient, sustainable, and secure supply of older and current generation chips for national security purposes and for critical manufacturing industries.

$11 billion
for R&D

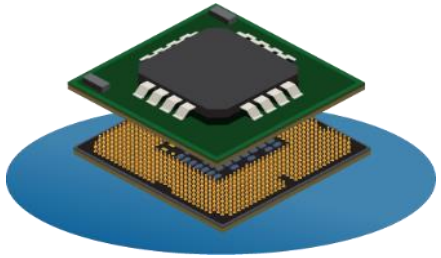
Strengthen U.S. semiconductor research and development (R&D) leadership to catalyze and capture the next set of critical technologies, applications, and industries.

$2 billion
for DoD Microelectronics Commons

A national network that will create direct pathways to commercialization for US microelectronics researchers and designers from “lab to fab.”

Workforce Initiatives

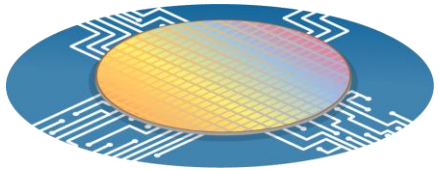
CHIPS R&D Programs



CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast

Natcast is an independent nonprofit organization and operator of the NSTC consortium



CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

Manufacturing USA

CHIPS Manufacturing USA Program

CHIPS Metrology Program

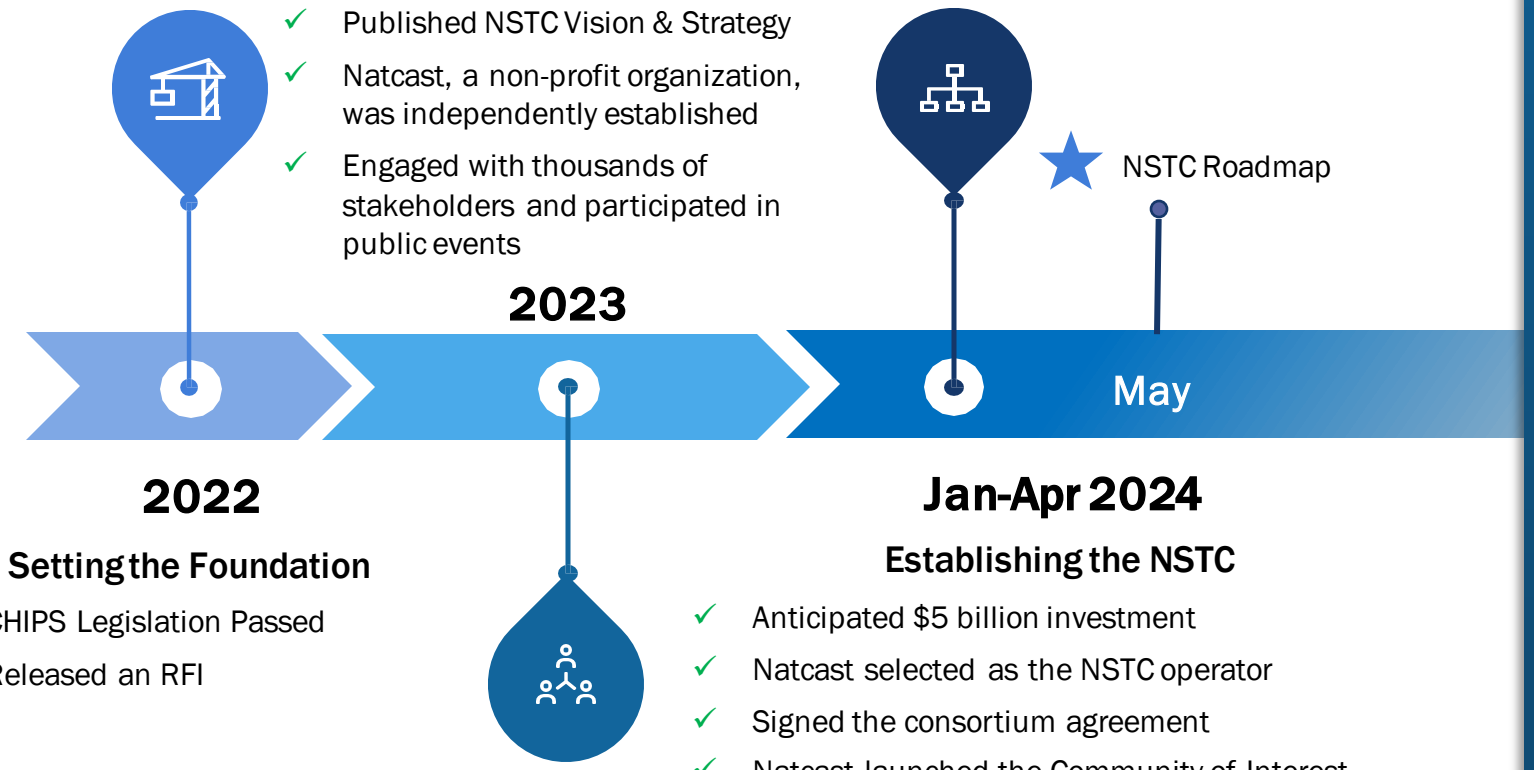
Workforce Initiatives

The National Semiconductor Technology Center

A **public-private consortium**, the National Semiconductor Technology Center (**NSTC**) is where members will have access to facilities, partners, and additional funding opportunities to research, test, investment fund, and scale-up semiconductor technologies and workforce activities.

The NSTC is operated by **Natcast**, a purpose-built, non-profit entity. Natcast works in tandem with the CHIPS NSTC Program, which sits within the U.S. Department of Commerce.

To bring this vision to life, CHIPS for America has moved intentionally.



2022

Setting the Foundation

- ✓ CHIPS Legislation Passed
- ✓ Released an RFI

2023

Engaging the Ecosystem

- ✓ Published NSTC Vision & Strategy
- ✓ Natcast, a non-profit organization, was independently established
- ✓ Engaged with thousands of stakeholders and participated in public events

May

NSTC Roadmap

Jan-Apr 2024

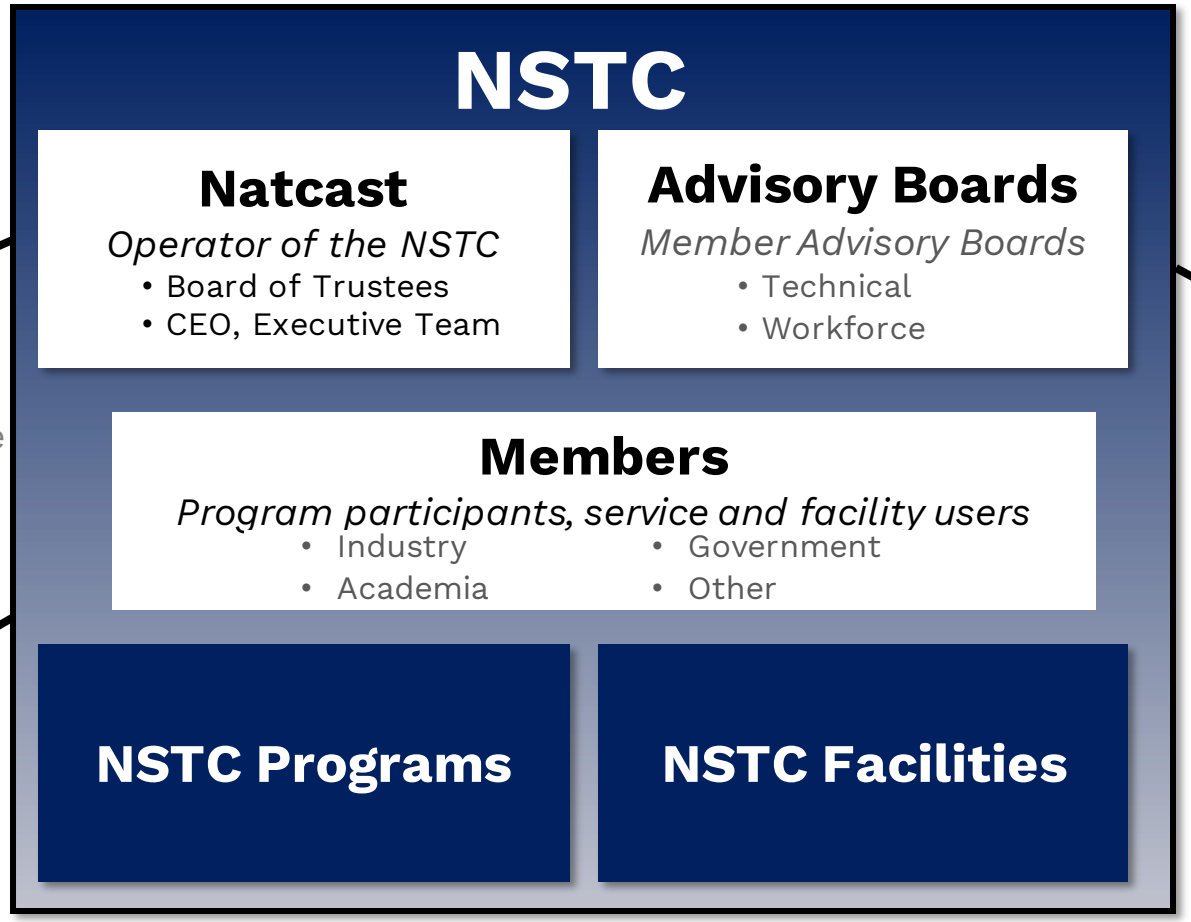
Establishing the NSTC

- ✓ Anticipated $5 billion investment
- ✓ Natcast selected as the NSTC operator
- ✓ Signed the consortium agreement
- ✓ Natcast launched the Community of Interest
- ✓ Hosted two public events with CHIPS & Natcast
- ✓ Natcast released an RFI on Facilities and Capabilities

Coming Up

- *Facilities Model and Selection Process*
- *Workforce Center of Excellence*
- *Initial R&D Funding Opportunities*
- *Opening Membership*

NSTC Operating Structure



Department of Commerce CHIPS NSTC Program

- Funding, oversight, Support, Guide
- Secretary Gina Raimondo, DoC
- Dr. Laurie Locascio, Dir NIST/Under Secretary
- Dr. Jay Lewis, Dir, CHIPS NSTC Program Office

NSTC Steering Committee

- Support, Guide, Coordinate, Strategy
- DoC, DoD, NSF, DoE, Industry

Other CHIPS R&D Programs

- CHIPS NAPMP Program
- CHIPS Metrology Program
- CHIPS MFG USA Program

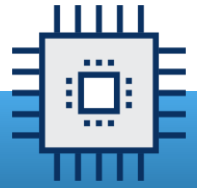
NSTC Focus Areas

Workforce Development

Technicians

Engineers

Researchers



Lower Cost of Design

Design Enablement Gateway

Silicon Aggregation Services

Investment Fund

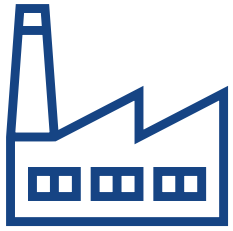
Research

Member-driven TAB

Competitive Awards

Prototyping Facilities

The Road Ahead



Facilities

Workforce Development

Jump Start Projects

Invite Members

Prototyping Strategy: RFI Update

74 RFI responses

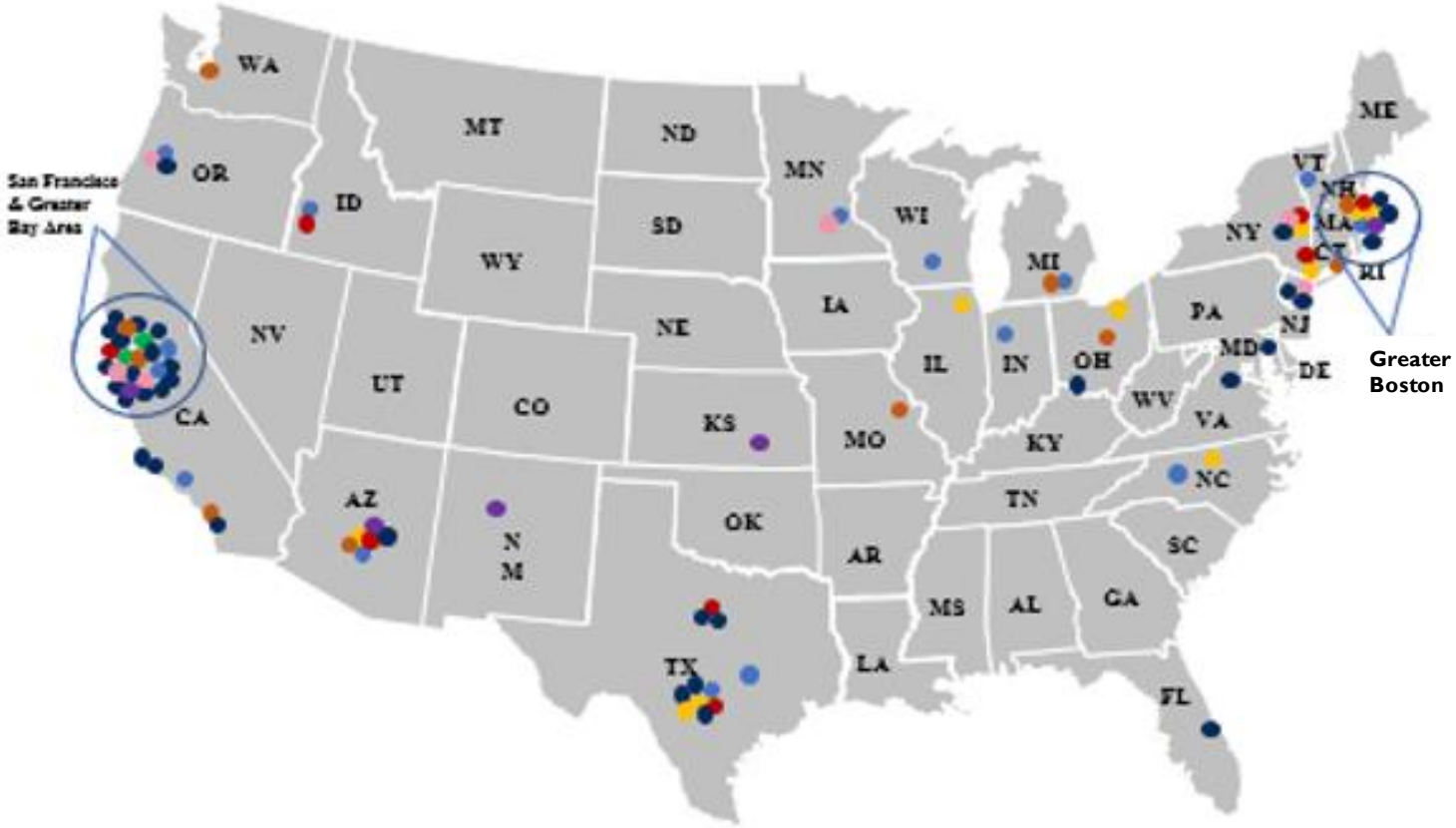
Excellent Participation

Wide Range of Inputs and Direct Engagement

Diverse Set of Technologies and Topics

Ecosystem Mapping of RFI Respondents

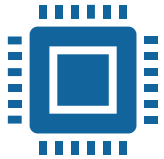
Industry	Partnership & Consortia	Educational Institutions	Government
52	9	17	1



	Ecosystem Mapping	Small	Large
●	Educational Institution	N/A	N/A
●	Partnership/Consortia	N/A	N/A
●	Chip Design – IDM	0	7
●	Chip Design – Fabless	18	8
●	Chip Design – EDA	0	3
●	Wafer Foundry	0	4
●	Capital Equipment & Materials	4	3
●	Assembly, Test, Package, & Other (Industry)	5	0

Note on Map Visual: Respondents' locations were aggregated and mapped based on their HQ, their R&D/Prototyping facilities they mentioned in their RFI responses, and their stated location in their RFI Response. All duplicate locations were then removed. There is a subset of respondents that received multiple marks on the map based on this aggregation.

Ecosystem Feedback Emerging Themes

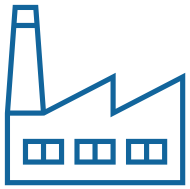


High Interest in Packaging:

- Nearly all respondents indicated interest in advanced packaging access and increasing US competitiveness

Need for Full-Flow (End-to-End) Wafer Processing Capabilities:

- Full-flow, foundry-like production capabilities and services, in addition to the ability to run short-loop experiments for unit-process development and earlier-stage R&D.



At least three distinct process lines called out:

1) A specialized '300mm CMOS+X' flow with end-to-end capability and flexibility to add new materials and features into a baseline CMOS flow.
2) A wide-bandgap material line.
3) A 300mm advanced CMOS flow leveraging EUV lithography and next-generation device structures.

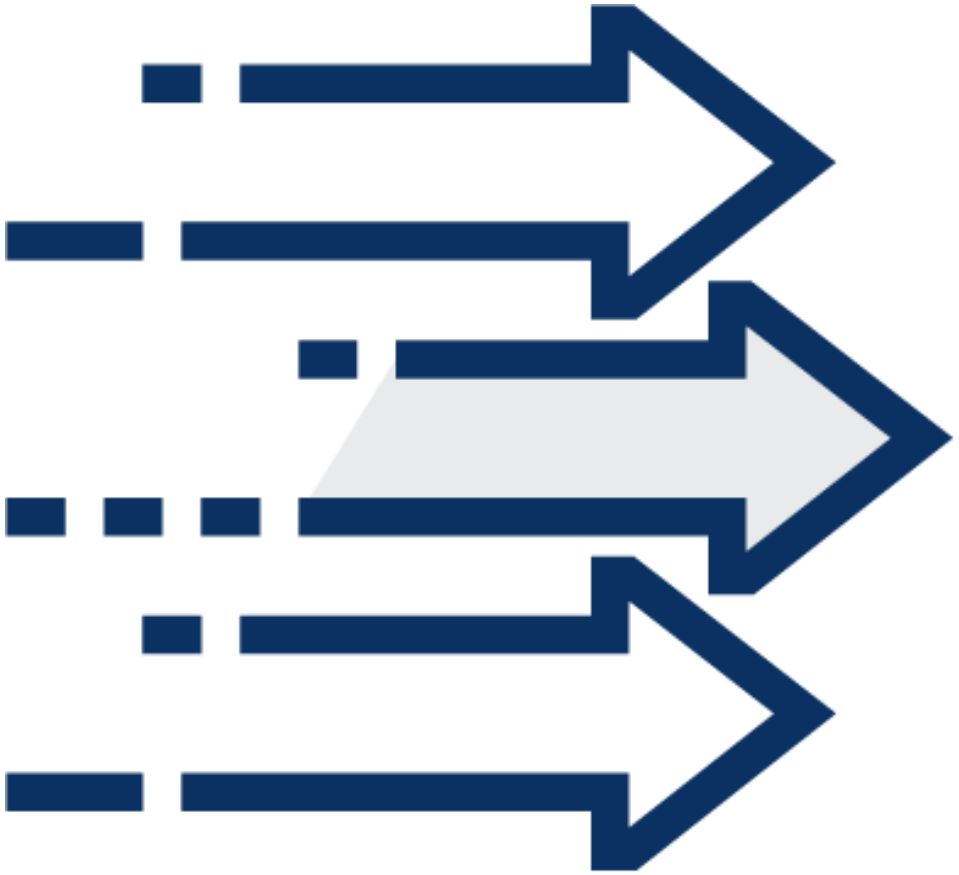
Workforce Development

NSTC Workforce Center of Excellence

"The Workforce Center of Excellence will be the definitive, trusted hub for workforce development for semiconductor companies doing business in America."

- Secretary Gina Raimondo

- **Engage** industry, researchers, educational institutions, government, nonprofit and labor stakeholders to identify critical needs
- **Scale up** proven programs
- **Expand access** to relevant educational programs
- **Grow interest** in the industry
- **Accelerate** adoption of best practices



Jump Start Projects

Initial R&D Project Topic Selection

- At least $100 million
- High Impact
- Quick turn around
- Broad ecosystem engagement
- Does not require new capabilities/infrastructure

Funding competitions for the first two topics are **expected to launch in early summer 2024** with a second competition expected to be released later in the summer.

First Project: Artificial Intelligence Driven RF Integrated Circuit Design Enablement (AIDRFIC)

Challenge: Lack of experienced Radio Frequency Integrated Circuit (RFIC) designers and limited improvements in RFIC design productivity

Goal: Enablement of domestically developed AI-based Electronic Design Automation (EDA) tools for RFIC design

Objectives

- 30-month effort to mature tools, integrate into a flow, and demonstrate on example Si/SiGe and GaAs circuits
- Fabrication and testing of physical exemplars
- Diverse teams representing TRL/MRL 3-7 pipeline

Program

- Lower the experience barrier
- Increase RFIC design productivity
- Optimize RFIC designs
- Generate unique, non-intuitive RFIC designs
- Enable continuous machine learning

Key Dates

- Info Webinar: June 21, 2024
- Proposers' Day: 2nd week of July 2024
- Proposals Due: August 16, 2024
- Projects to start by the end of the year

Please Note: A previous version of this slide listed the due date as September 6, 2024.

Second Project: Test Vehicles

Challenge: Lack of sophisticated Test Vehicles (test chip designs, advanced test chip processing, automated testing hardware) limiting efficient domestic TRL advancement

Goal: Democratize access and promote standardization of results

Objectives

- Reduce the time, cost and risk of process development and improvement
- Increase R&D learning cycles
- Allow research organizations to focus their limited resources and actual R&D value-add

Program

- Test Vehicle with clearly defined specifications and needs, such as non-volatile Memory; materials and unit process development; FEOL and BEOL development
- Convene user meetings to verify sufficient need, potential providers, and form teams addressing a broad range of topics

Key Anticipated Dates

- Info Webinar: August 2024
- Proposers Day: September 2024
- Proposal Due Date: Nov 2024
- Projects to start in February 2025

Topic under consultation: PFAS Abatement

Challenge: The semiconductor industry is a contributor of PFAS release to the environment, but PFAS uses are essential to semiconductor manufacturing

In the short-term, solutions to abate PFAS must be evaluated

Jump Start Program - *in consultation*: Demonstrate prototyping of solutions to capture and destroy PFAS in relevant conditions, without disrupting existing process technology

Membership

NSTC: Building **enduring value** through a membership program that drives innovation to commercialization, maximizes collaboration, and contributes to the long-term financial sustainability

NSTC to be a member-driven consortium that brings together a diverse ecosystem

Design	Academia	Professional Services
Manufacturers	End Customers	Workforce Organizations
Investors	Govt. Organizations	Suppliers

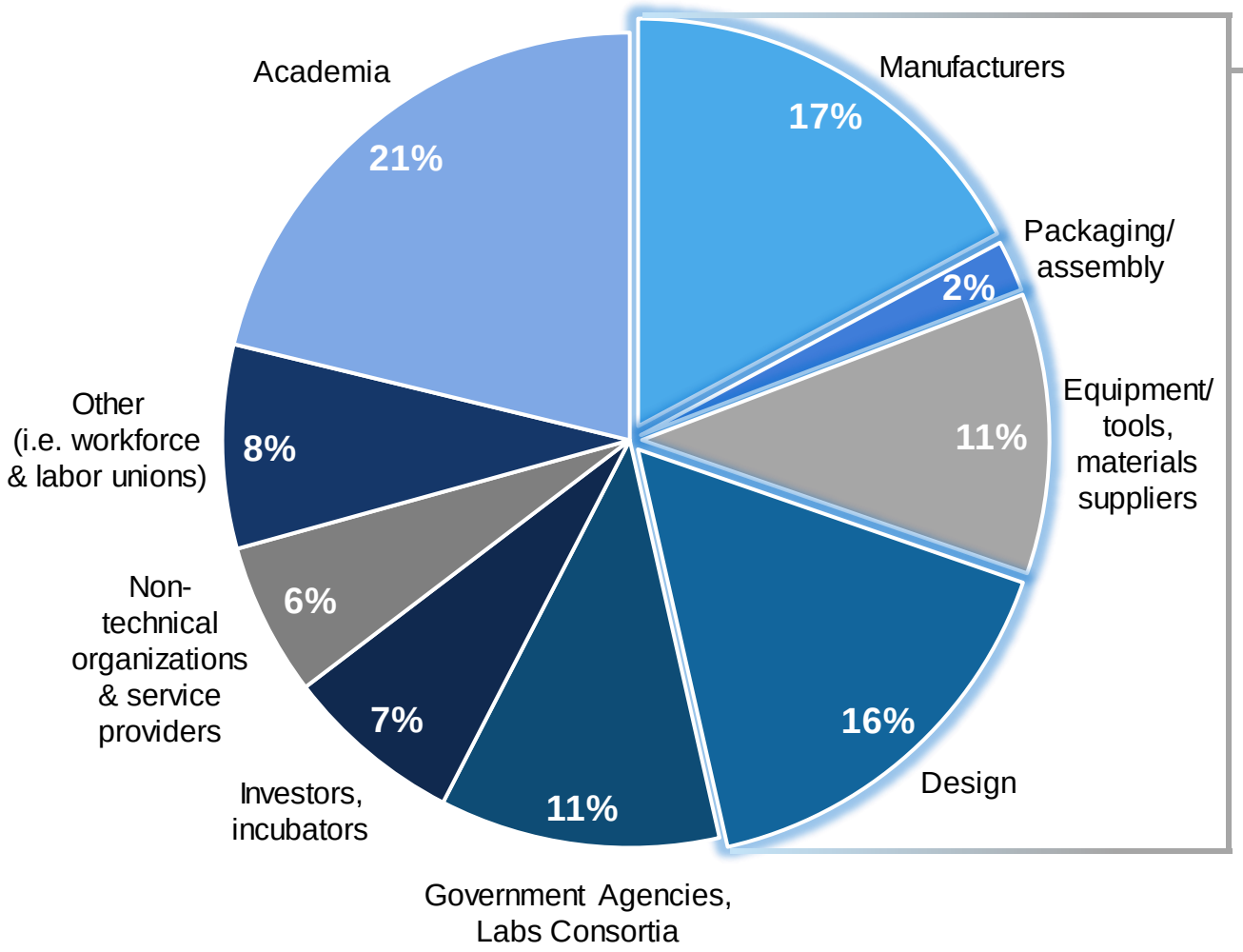
Guiding Principles

- Accessible
- Valuable
- Simple
- Connected

Membership Open Fall 2024

Community of Interest from Natcast

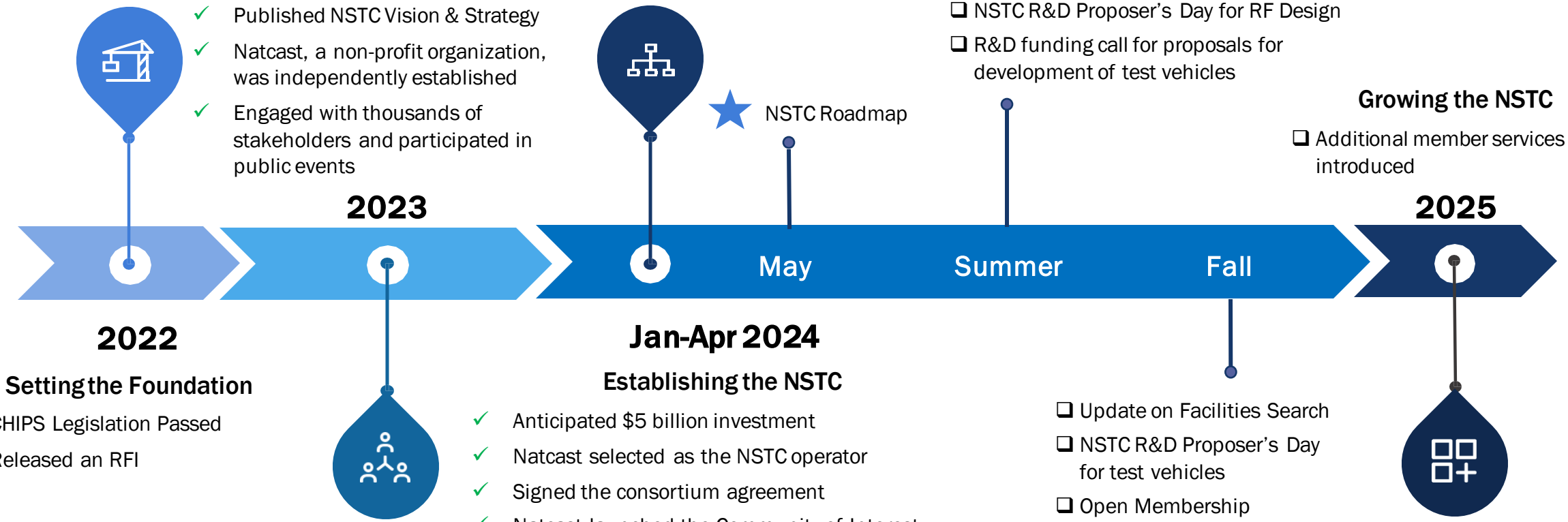
250+ Respondents



46%

Join Today

NSTC Roadmap: 4 Year View



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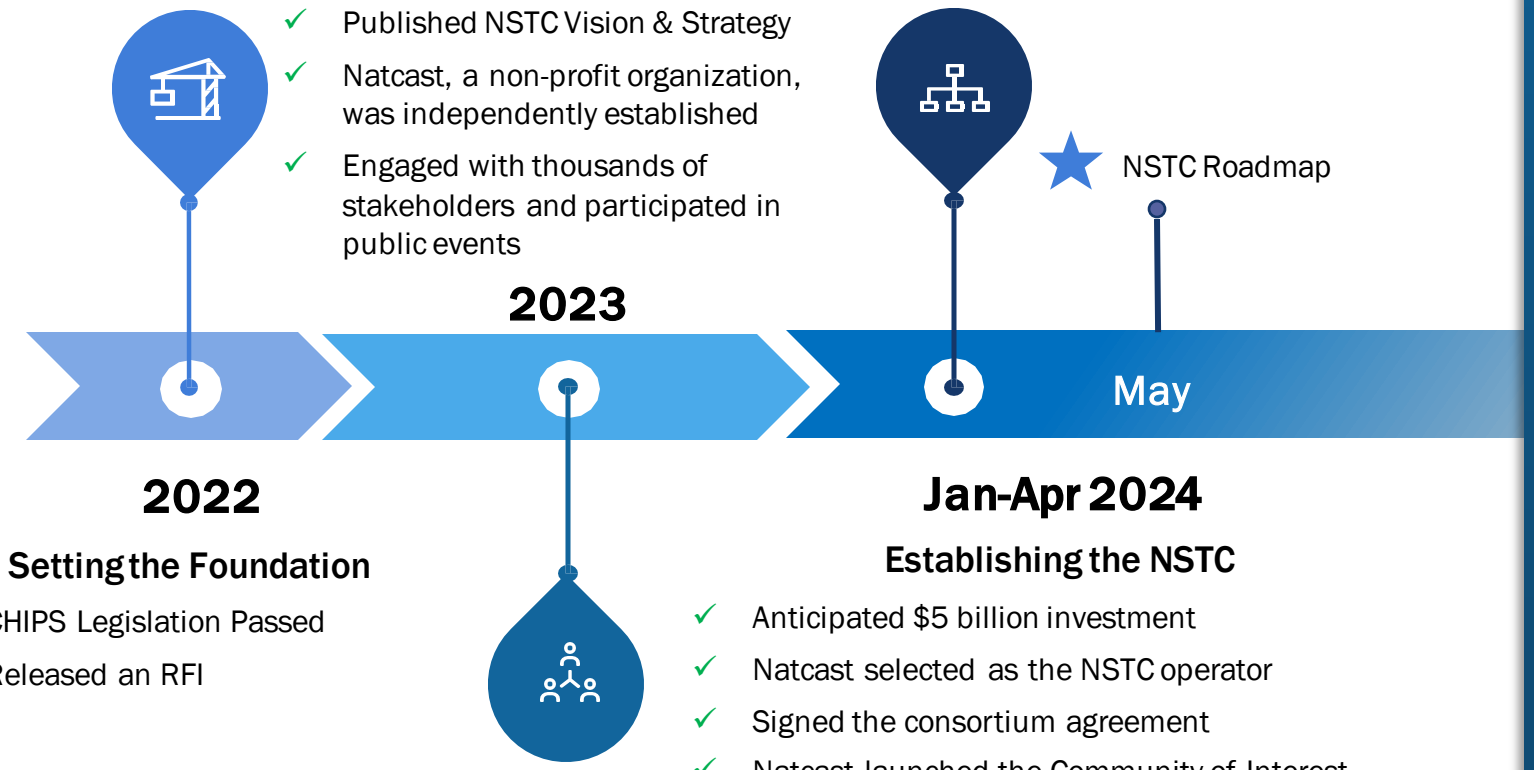

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Get Engaged

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  - Natcast: Natcast.org
- Get in contact:
  - CHIPS for America: askchips@chips.gov
  - Natcast: info@natcast.org

Join the Natcast Community of Interest


Thank you