

Issues with Electrical Characterization of Graphene Field Effect Transistors

Eric M. Vogel

Professor, Georgia Institute of Technology
Adjunct Professor, University of Texas at Dallas

Acknowledgments

- **Corey Joiner, Dr. Tania Roy, Dr. Zohreh Hesabi (Georgia Tech)**
- **Dr. Archana Venugopal¹ (now with T.I.), Dr. Jack Chan¹ (now with Micron),**
- **Dr. Luigi Colombo²**
- **Prof. Robert M. Wallace,¹ Dr. Adam Pirkle¹ (now with Intel), David Hinojos¹,**
- **Dr. Stephen McDonnell¹,**
- **Prof. Rodney Ruoff³, Dr. Carl Magnuson³**

¹University of Texas at Dallas

²Texas Instruments Incorporated

³University of Texas at Austin

Funding

- Center for Low Energy Systems Technology (LEAST), one of six centers supported by the STARnet phase of the Focus Center Research Program
- NSF MRSEC: The Georgia Tech Laboratory for New Electronic Materials
- Texas Instruments Diversity Fellowship
- SRC-NRI Southwest Academy for Nanoelectronics (completed)

Outline

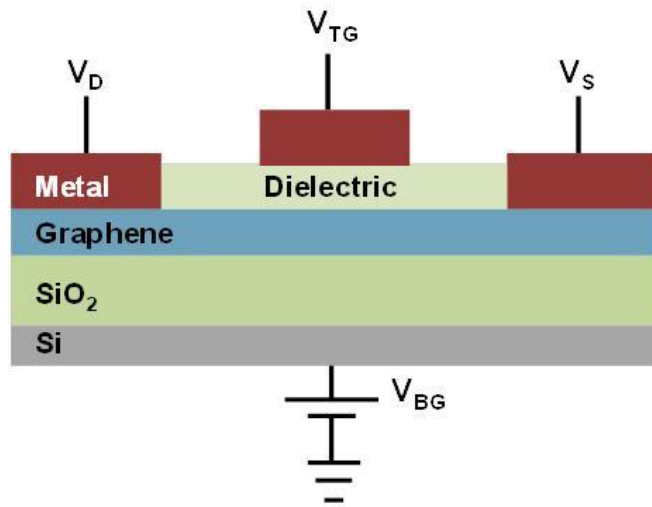
- Motivation
- A Simple “Universal” Model for Transport in Single Layer Graphene
- Effect of Device Dimensions on Mobility
- Effect of Contacts
- CVD Graphene Vertical Tunnel Transistors
- Conclusions

Outline

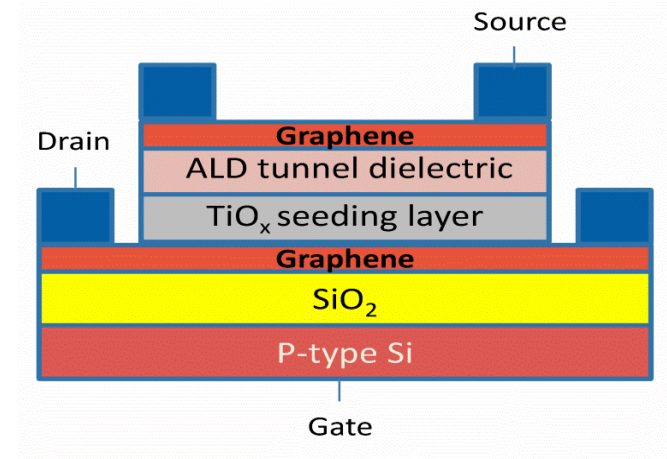
- Motivation
- A Simple “Universal” Model for Transport in Single Layer Graphene
- Effect of Device Dimensions on Mobility
- Effect of Contacts
- CVD Graphene Vertical Tunnel Transistors
- Conclusions

Motivation

Tunnel FETs or SymFET



Graphene FET



- While the use of the FET test structure is common, there have been few investigations to systematically determine whether assumptions associated with characterizing the transport properties of graphene using this test structure are valid.

R. M. Feenstra, et al., Journal of Applied Physics, vol. 111, Feb 2012.
J.J Su et al., Nat. Phys., 4, 799 (2008)

Outline

- Motivation
- A Simple “Universal” Model for Transport in Single Layer Graphene
- Effect of Device Dimensions on Mobility
- Effect of Contacts
- CVD Graphene Vertical Tunnel Transistors
- Conclusions

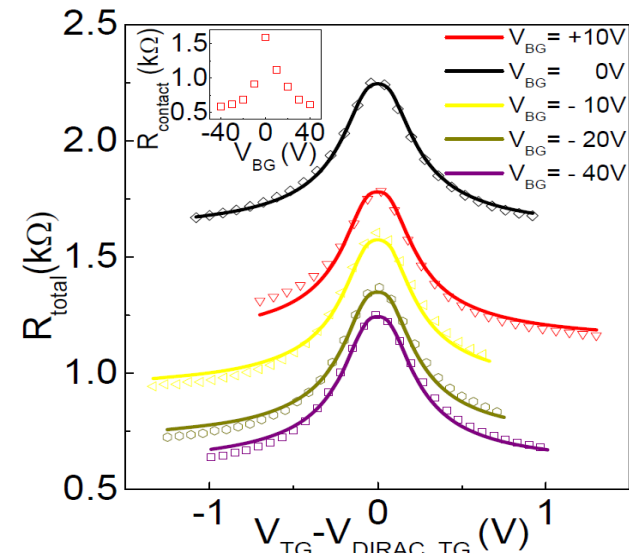
Mobility Extraction – Constant Mobility Model

- Two Point Probe measurement setup. Contact Resistance extracted from the model.

$$R_{total} = R_{contact} + R_{channel} = R_{contact} + \frac{N_{sq}}{n_{total} e \mu} = R_{contact} + \frac{N_{sq}}{\sqrt{n_0^2 + n[V_{TG}^*]^2} e \mu}$$

- Mobility extracted from R - V_{bg} measurements using the model proposed Kim et al.
- Also extracted is the intrinsic carrier concentration n_0 .
- The model assumes that the mobility is carrier concentration independent.

S. Kim et al., *Appl. Phys. Lett.* 94, 062107(2009)

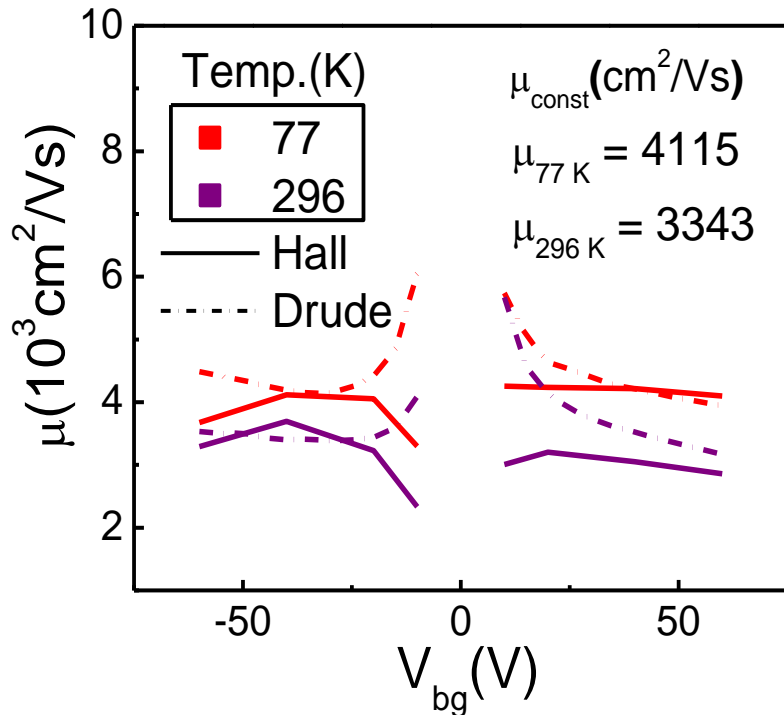


Question

Is this model for transport calculations and extraction consistent with other methods?

Plot shows R_{total} vs. $V_{TG - Dirac}$
Symbols – Data
Lines – modeling results

Comparison of Mobility Models



μ_{const} without R_c

$\mu_{const(296 \text{ K})} \sim 2342 \text{ cm}^2/\text{Vs}$
 $\mu_{const(77 \text{ K})} \sim 2931 \text{ cm}^2/\text{Vs}$

- Observed μ_H vs. n trend agrees with reported trend for exfoliated graphene in literature

W. Zhu et al., Phys. Rev. B, 80, 235402 (2009)

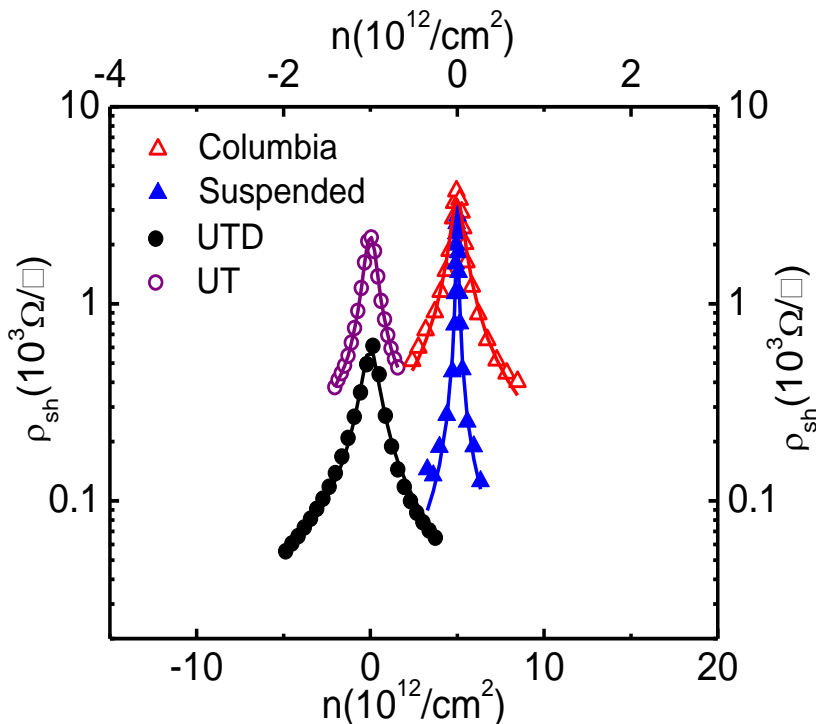
- Mobility values from all models comparable at high bias.

- Difference in mobility at low bias attributed to the use of intrinsic carrier conc. n_0 in the constant mobility model.

- Extracted mobility is seen to have a significant dependence on the contact resistance

A. Venugopal et al., Journal of Appl. Phys. 109, 104511 (2011)

Comparison of Mobility Models



Sample	Description	Reported Mobility (cm ² /Vs)	Extracted Mobility (cm ² /Vs)
UTD	Back-gate, measurement at ~300K	X	24381
Ref. 2	Top gate (Al ₂ O ₃ dielectric), measurement at ~300 K	8600	8407
Ref. 1-1	Back-gate, measurement at ~5 K	30000	26134
Ref. 1-2	Back-gate, measurement at ~5 K	230000	201634

- Mobility reported in literature and mobility extracted using constant mobility model compared.

- Extracted and reported mobilities seen to be consistent
- Trends in sheet resistance at a given carrier concentration follow the trend in extracted mobilities as expected.

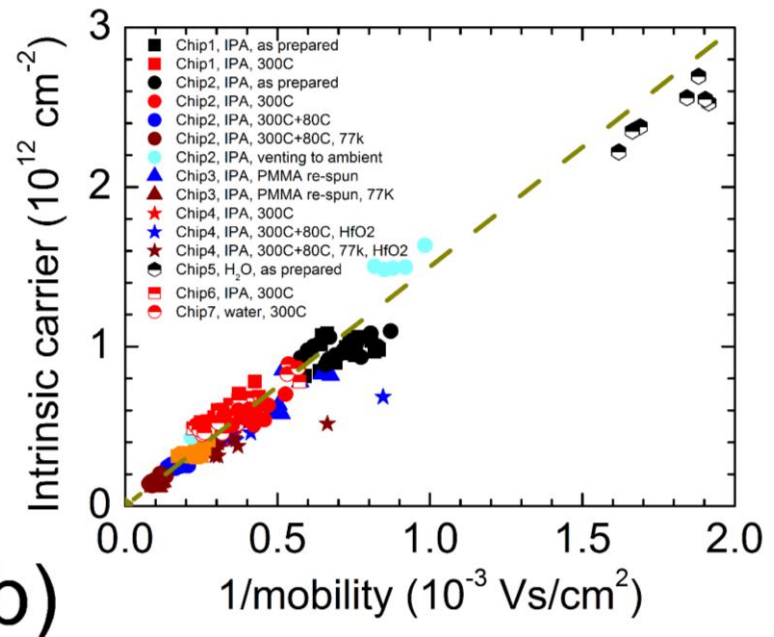
¹Bolotin K.I. et al., *Solid State Communications*, 146, 351-355(2008)

²S. Kim et al., *Appl. Phys. Lett.* 94, 062107(2009)

Mobility and Impurities

It is found that the product of mobility and impurity density is a constant for a wide variety of interfacial conditions, annealing conditions, top dielectrics and measurement temperatures.

$$\mu \times n_0 \approx 1.15 \times 10^{15} / \text{Vs}$$



- Adam, S.; Hwang, E. H.; Galitski, V. M.; Das Sarma, S., A Self-consistent Theory for Graphene Transport. *Proc. Natl. Acad. Sci.* **2007**, *104*, 18392-18397.
- Chen, J. H.; Jang, C.; Adam, S.; Fuhrer, M. S.; Williams, E. D.; Ishigami, M., Charged-impurity Scattering in Graphene. *Nat. Phys.* **2008**, *4*, 377-381.
- J. Chan, A. Venugopal, A. Pirkle, S. McDonnell, D. Hinojos, C. W. Magnuson, R. S. Ruoff, L. Colombo, R. M. Wallace, and E. M. Vogel, "Reducing Extrinsic Performance-Limiting Factors in Graphene Grown by Chemical Vapor Deposition," *ACS Nano*, **2012**, *6* (4), pp 3224–3229

A Simple “Universal” Model for SLG Transport

$$R = R_c + R_{ch}$$
$$R_{ch} = \frac{L/W}{n(V_{bg})q\mu}$$

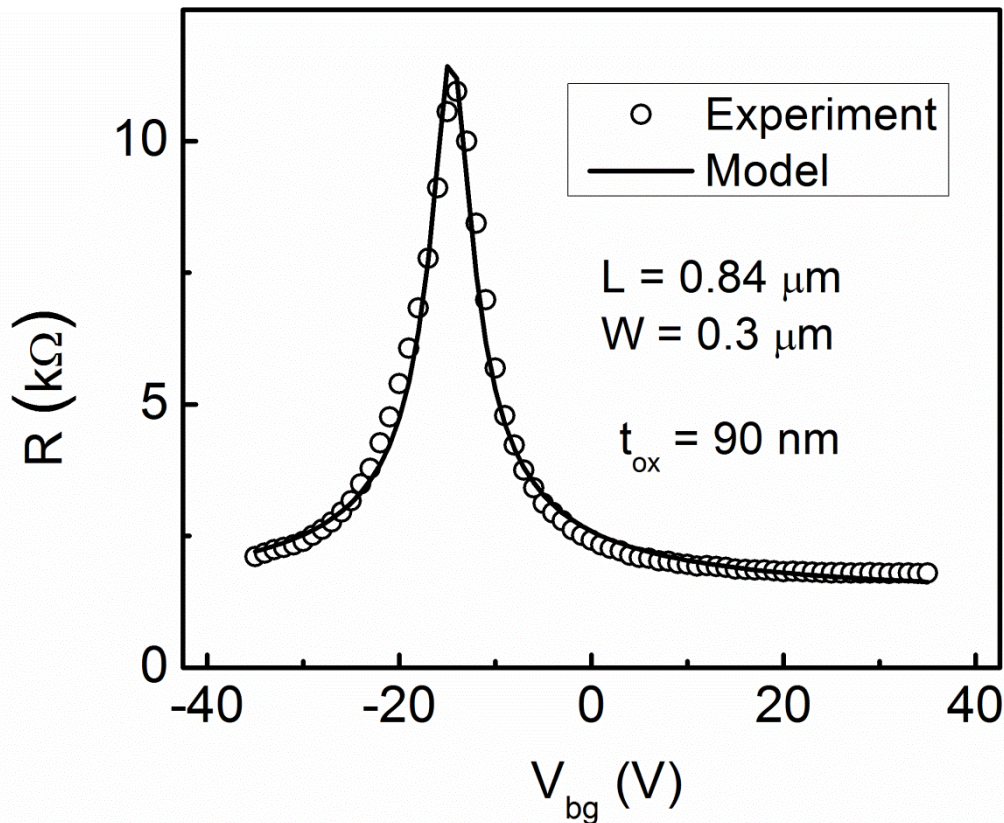
$$\rho_{sh} = \frac{R_{ch}}{L/W}$$

$$n(V_{bg}^*) = \sqrt{n_{ind}(V_{bg}^*)^2 + n_0^2}$$

$$n_{ind}(V_{bg}^*) = \frac{C_{ox}V_{bg}^*}{q}$$

$$V_{bg}^* = V_{bg} - V_{Dirac}$$

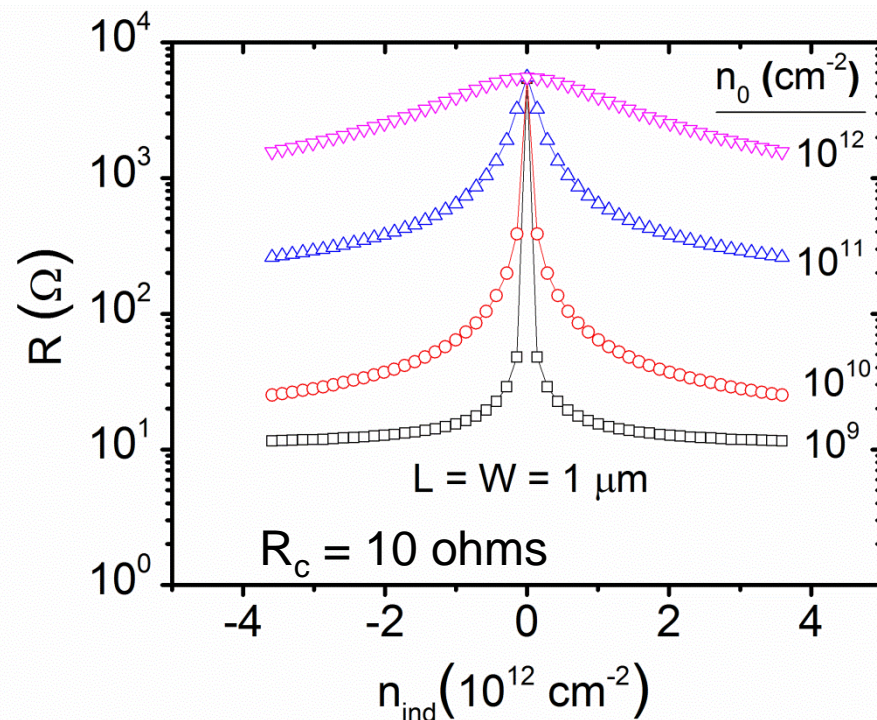
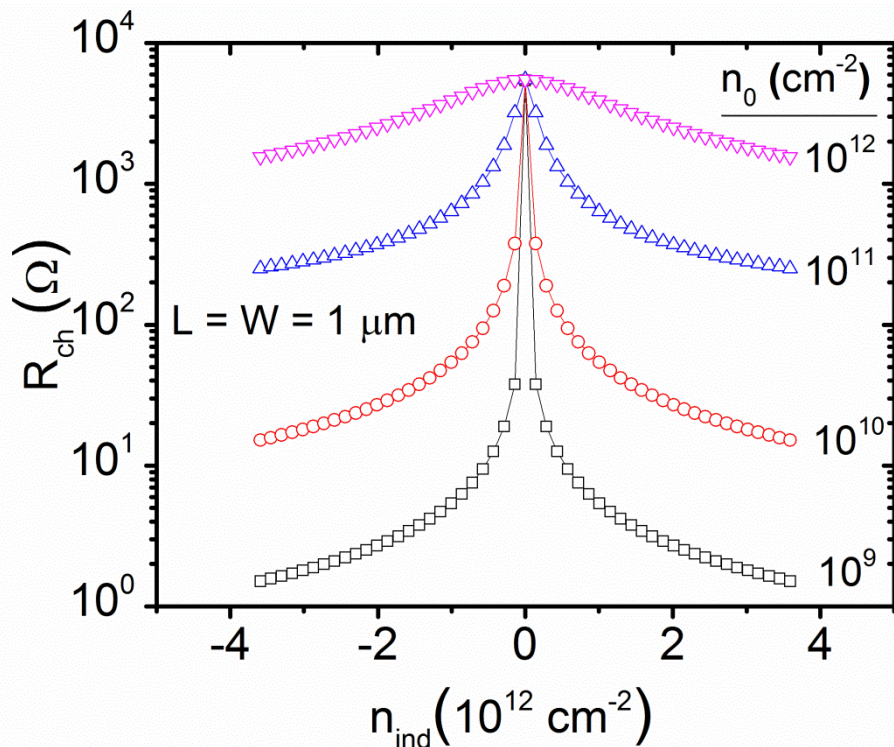
$$\mu \times n_0 \approx 1.15 \times 10^{15} /Vs$$



S. Kim et al., *Appl. Phys. Lett.* 94, 062107(2009)

A. Venugopal et al., *accepted Solid-State Communications* (2012)

A Simple “Universal” Model for SLG Transport



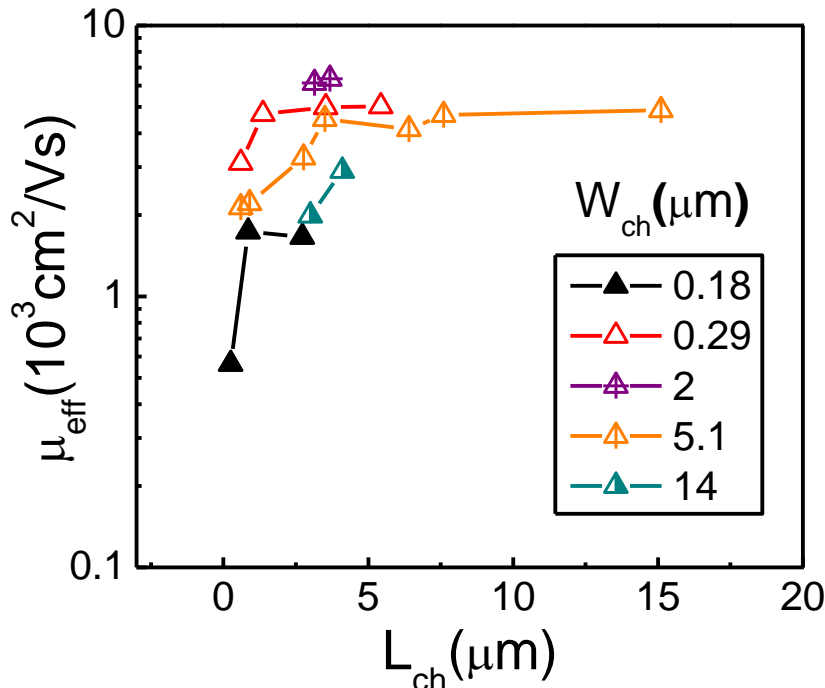
- The maximum resistance of a single layer graphene device cannot be strongly changed.
- The minimum resistance for high quality (low n_0) graphene is limited by R_c . As n_0 increases and μ decreases, the influence of R_c on the minimum R is less important.

Outline

- Motivation
- A Simple “Universal” Model for Transport in Single Layer Graphene
- **Effect of Device Dimensions on Mobility**
- Effect of Contacts
- CVD Graphene Vertical Tunnel Transistors
- Conclusions

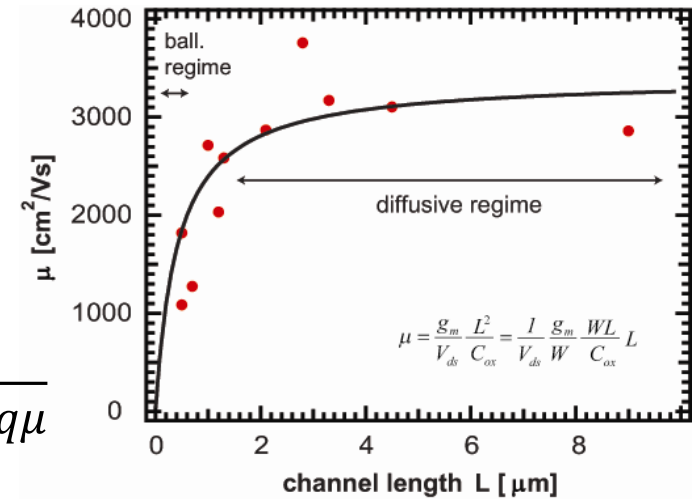
Dependence of μ_{eff} on L_{ch}

A. Venugopal et al., *Journal of Appl. Phys.* 109, 104511 (2011)



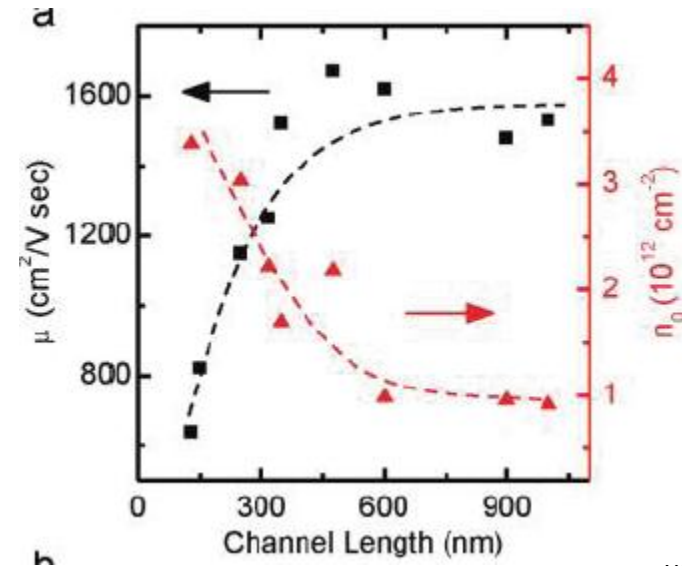
$$R_{ch} = \frac{L/W}{n(V_{bg})q\mu}$$

Z. Chen et al., *IEDM* (2008)

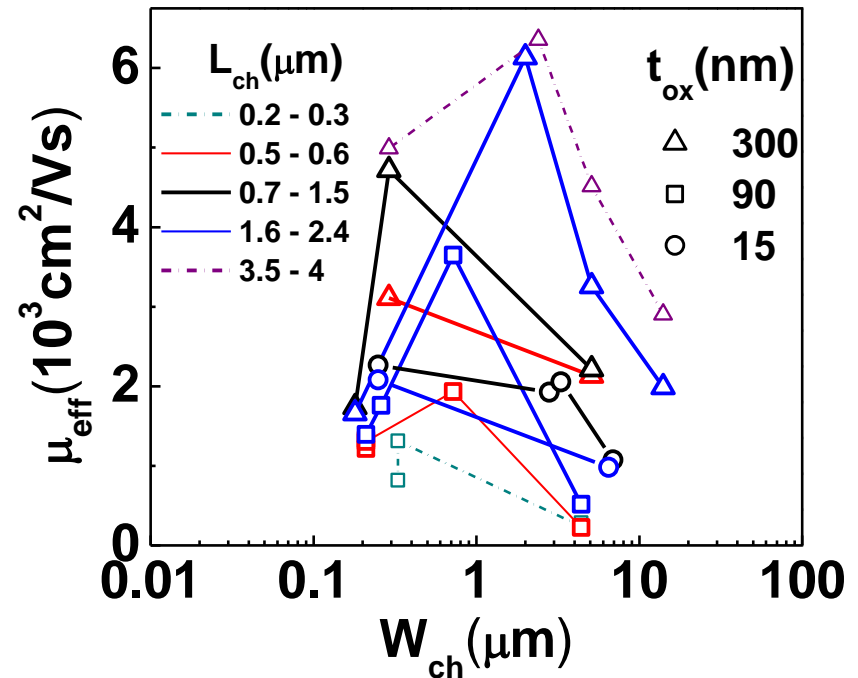
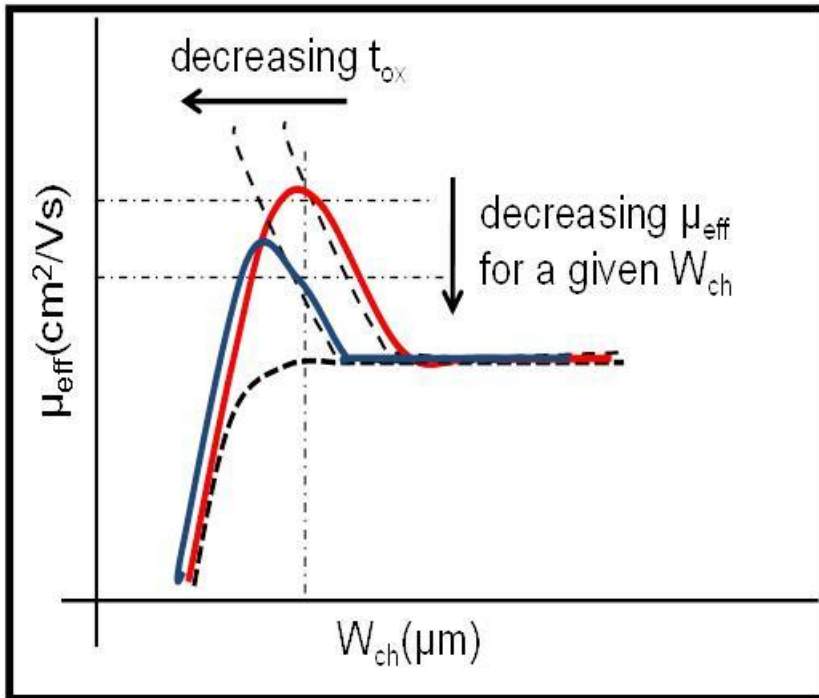


- Mobility determined to be dependent on channel length
- L_{ch} dependence previously attributed to
 - device operating partially in the ballistic and diffusive regime
 - damage from e beam lithography

I. Meric et al., *Nanoletters* 11, 1093(2011)



$\mu_{\text{eff}}(L_{\text{ch}}, W_{\text{ch}}) - \text{Dependence on } t_{\text{ox}}$

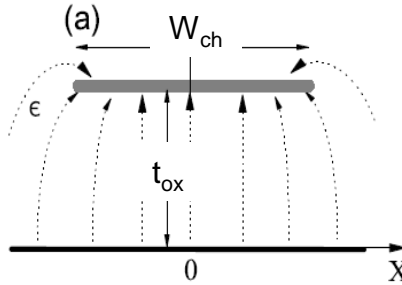


- Extracted μ_{eff} plotted as a function of channel length (L_{ch}), width (W_{ch}) and underlying oxide thickness (t_{ox}).
- For comparable L_{ch} and W_{ch} , mobility is seen to decrease with decreasing oxide thickness t_{ox} .

A. Venugopal et al., *Journal of Appl. Phys.* 109, 104511 (2011)

Graphene on 300 nm SiO₂ – Strip Capacitor

F.T. Vasko et al., *Appl. Phys. Lett.* 97, 092115 (2010)

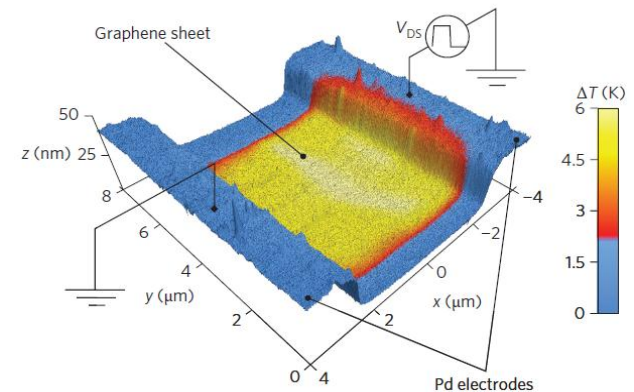
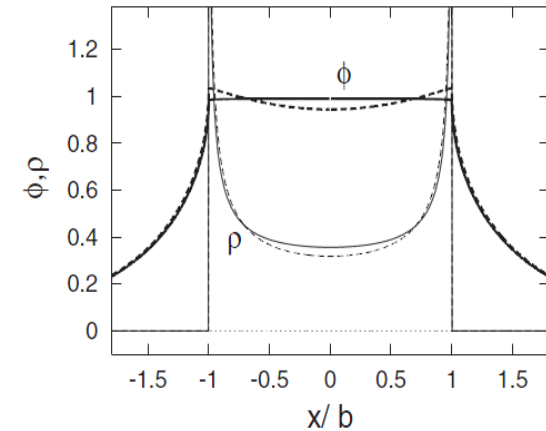


- Uniformity of charge density distribution in the channel region depends on the aspect ratio, W_{ch}/t_{ox} (ratio of the device width and the thickness of the dielectric).
- Comparable W_{ch} and t_{ox} results in enhanced charge density at the edges.

Nishiyama et al., *IEEE Trans. on Components, Hybrids and Manufacturing Technology*, 13, 417(1990)

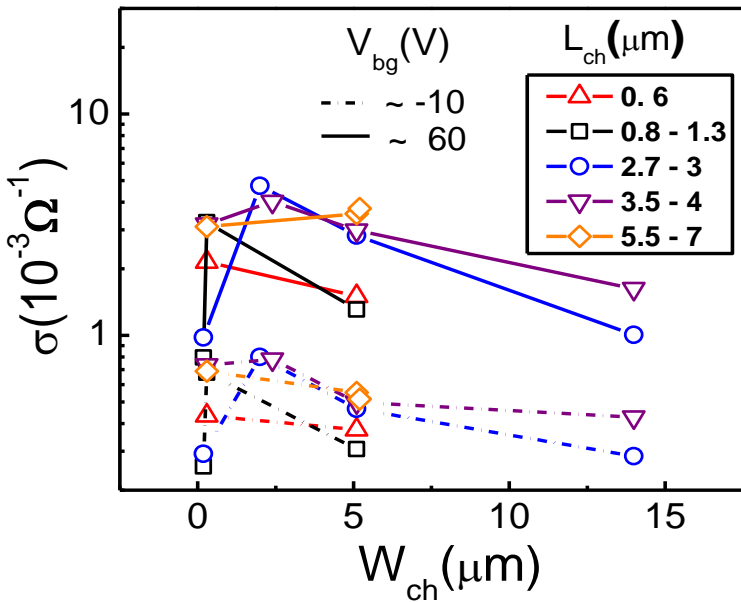
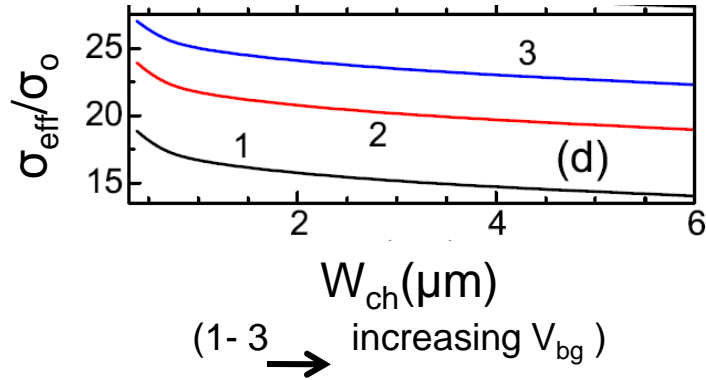
P. G. Silvestrov et al., *Phys. Rev. B*, 77, 155436(2008)
K.L. Grosse et al., *Nature Nano.* (2011)

Charge density distribution in a graphene strip

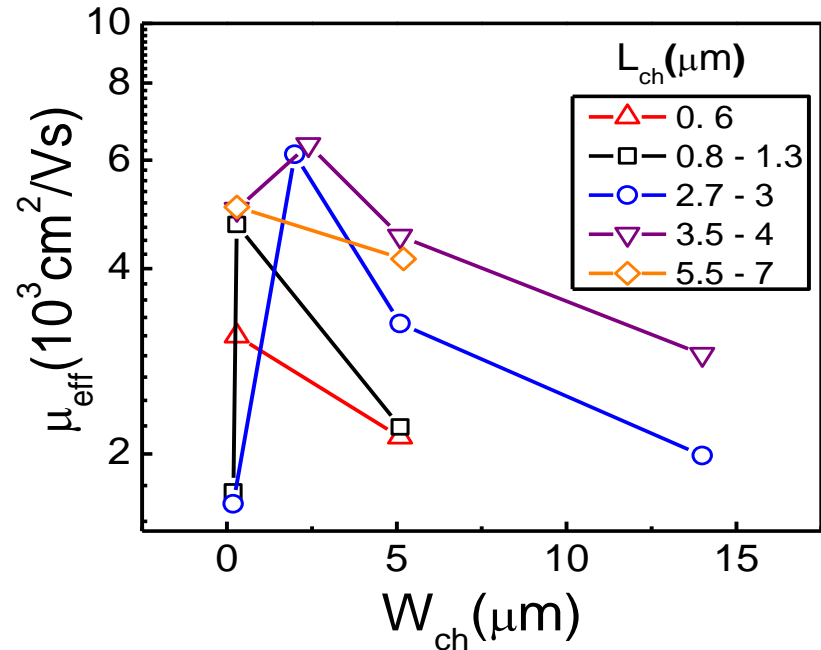


Graphene on SiO_2 – Strip Capacitor

F.T. Vasko et al., *Appl. Phys. Lett.* 97, 092115 (2010)



- Charge accumulation at the edges results in enhanced conductivity in the channel.
- Trend seen in conductivity vs. channel width manifests itself in the extracted mobility



A. Venugopal et al., *Journal of Appl. Phys.* 109, 104511 (2011)

Mobility Values

Reference	Dielectric Type	tox (nm)	L (μm)	W (μm)	Temp. (K)	Mobility (cm^2/Vs)
[1]	SiO ₂ (BG)	300	~5	~0.5	5-300	3000-10000
[25]	SiO ₂ (BG)	300	2-4	0.5-4	4.2	3500
[25]	SiO ₂ (BG)	300	2-4	0.5-4	350	2500
[26]	SiO ₂ (BG)	300	5	5	1.7	10000
[27]	SiO ₂ (BG)/HfO ₂ (TG)	300	5	3	1.5	10000-17000
[21]	SiO ₂ (BG)/NFC HfO ₂ (TG)	300	17	1.5	300	8500
[18]	SiO ₂ (BG)	300	10-15	5-10	300	25000
[4]	SiO ₂ (BG)	300	3	1.5	5	25000
[4]	Suspended	300	3	1.5	5	200000
[13]	SiO ₂ (BG)/Al ₂ O ₃ (FG)	300	2.4	10	300	8500
[28]	SiO ₂ (BG)	300	7.3	0.4	300	4780
[29]	h-BN (BG)	14	~3.5	~1.5	4	60000
[30]	SiO ₂ (BG)	300	4	7	300	4500
[31]	SiO ₂ (BG)	300	3-20	3-20	1.6	2000-20000
[32]	SiO ₂ (BG)	300	3-5	1-3	300	8200
[32]	Al ₂ O ₃ (BG)	72	3-5	1-3	300	7400

A. Venugopal, L. Colombo, and E. M. Vogel, "Issues with Characterizing Transport Properties of Graphene Field Effect Transistors," *Solid State Communications* **152**, 1311–1316 (2012)

- [1] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, Y. Zhang, S.V. Dubonos, I.V. Grigorieva, A.A. Firsov, *Science*, 306 (2004) 666-669.
- [4] K.I. Bolotin, K.J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, H.L. Stormer, *Solid State Communications*, 146 (2008) 351-355.
- [13] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, S.K. Banerjee, *Applied Physics Letters*, 94 (2009) 062107-062103.
- [18] J.-H. Chen, C. Jang, S. Xiao, M. Ishigami, M.S. Fuhrer, *Nat Nano*, 3 (2008) 206-209.
- [21] D.B. Farmer, H.-Y. Chiu, Y.-M. Lin, K.A. Jenkins, F. Xia, P. Avouris, *Nano Letters*, 9 (2009) 4474-4478.
- [25] W. Zhu, V. Perebeinos, M. Freitag, P. Avouris, *Physical Review B*, 80 (2009) 235402.
- [26] Y. Zhang, Y.-W. Tan, H.L. Stormer, P. Kim, *Nature*, 438 (2005) 201 - 204.
- [27] K. Zou, X. Hong, D. Keefer, J. Zhu, *Physical Review Letters*, 105 (2010) 126601.
- [28] M.C. Lemme, T.J. Echtermeyer, M. Baus, H. Kurz, *IEEE Electron Device Letters*, 28 (2007) 282-284.
- [29] C.R. Dean, A.F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K.L. Shepard, J. Hone, *Nat Nano*, 5 (2010) 722-726.
- [30] V.E. Dorgan, M.-H. Bae, E. Pop, *Applied Physics Letters*, 97 (2010) 082112-082113.
- [31] Y.W. Tan, Y. Zhang, K. Bolotin, Y. Zhao, S. Adam, E.H. Hwang, S. Das Sarma, H.L. Stormer, P. Kim, *Physical Review Letters*, 99 (2007) 246803.
- [32] L. Liao, J.W. Bai, Y.Q. Qu, Y. Huang, X.F. Duan, *Nanotechnology*, 21 (2010).

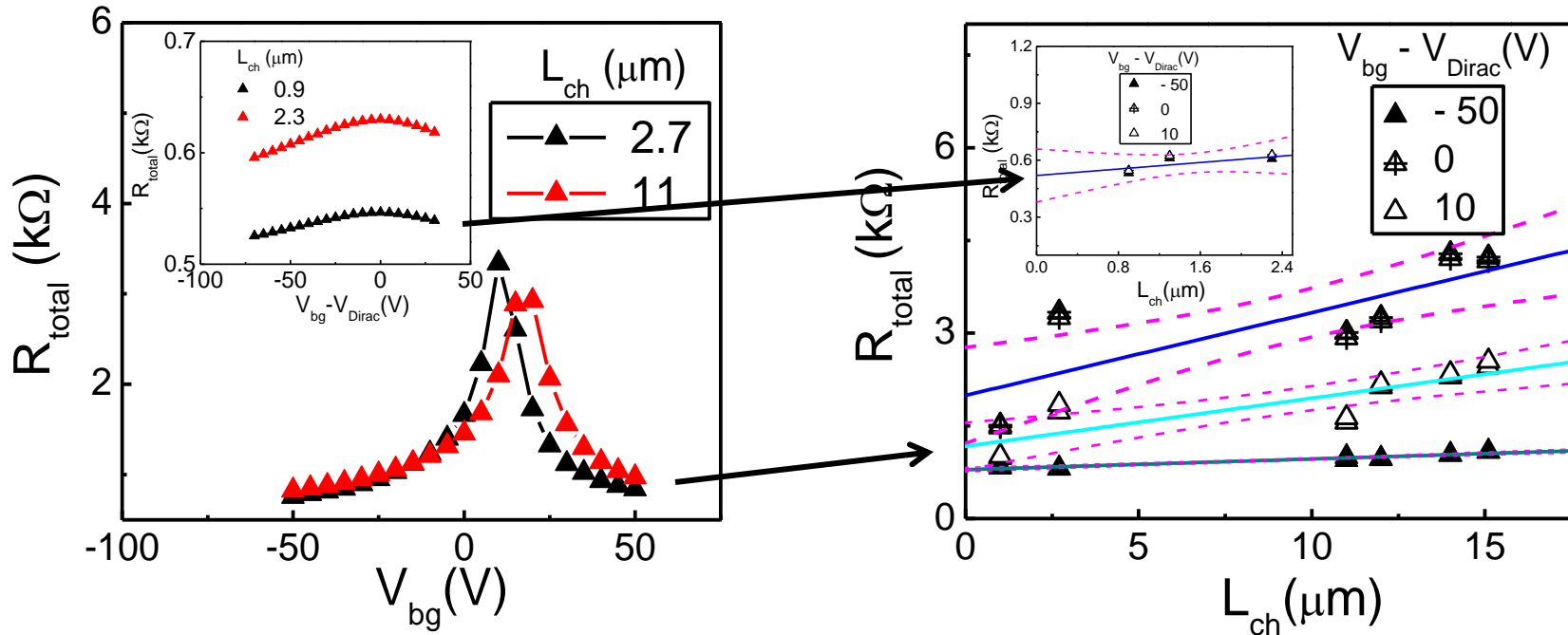
Outline

- Motivation
- A Simple “Universal” Model for Transport in Single Layer Graphene
- Effect of Device Dimensions on Mobility
- **Effect of Contacts**
- CVD Graphene Vertical Tunnel Transistors
- Conclusions

Comparison of TLM and $R - V_{bg}$

$$R_{tot} = 2R_{con} + R_{ch}$$

Main Plot: Monolayer Graphene
Inset: Three Layer Graphene



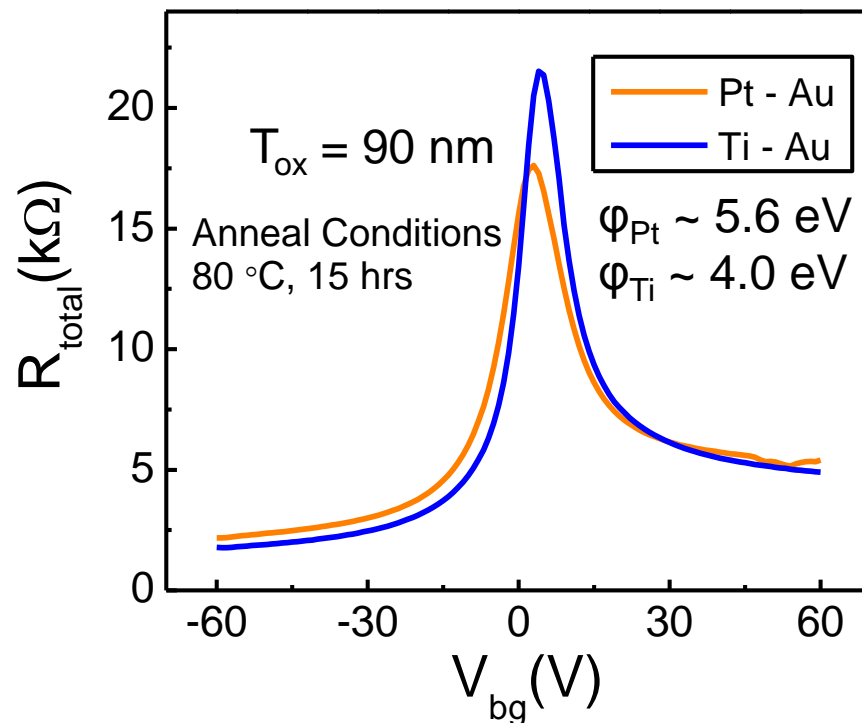
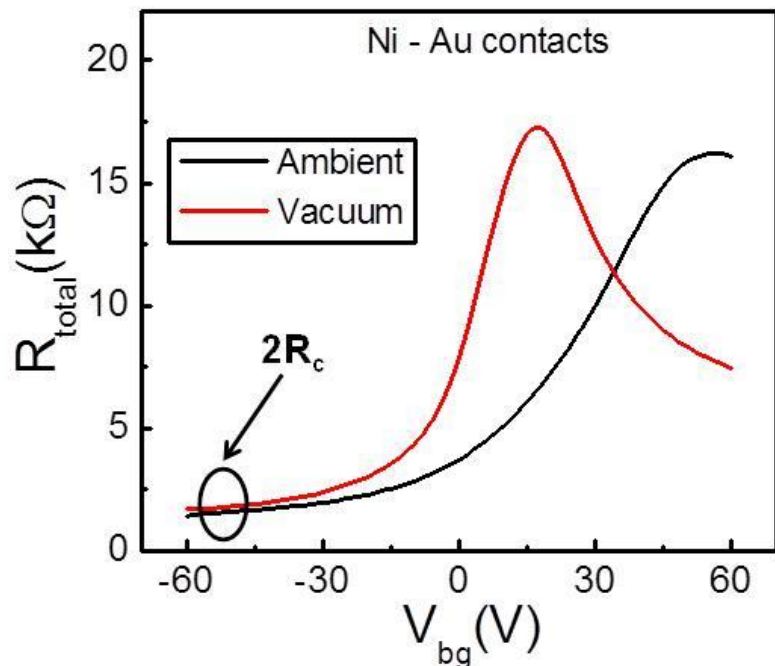
- Scatter in data reduces with increasing carrier concentration
- The contact resistance obtained using TLM is equivalent to the total resistance at high V_{bg} .

A. Venugopal et al., *Appl. Phys. Lett.* 96, 013512 (2010)

A. Venugopal et al., *Appl. Phys. Lett.* 96, 013512 (2010)

Contact Resistance as a Function of Metal Type

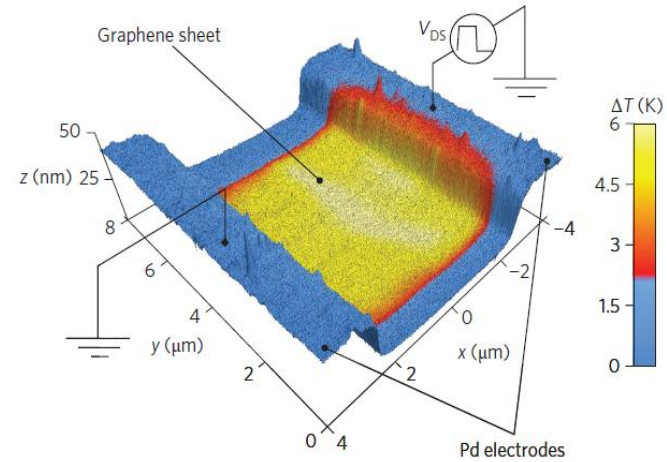
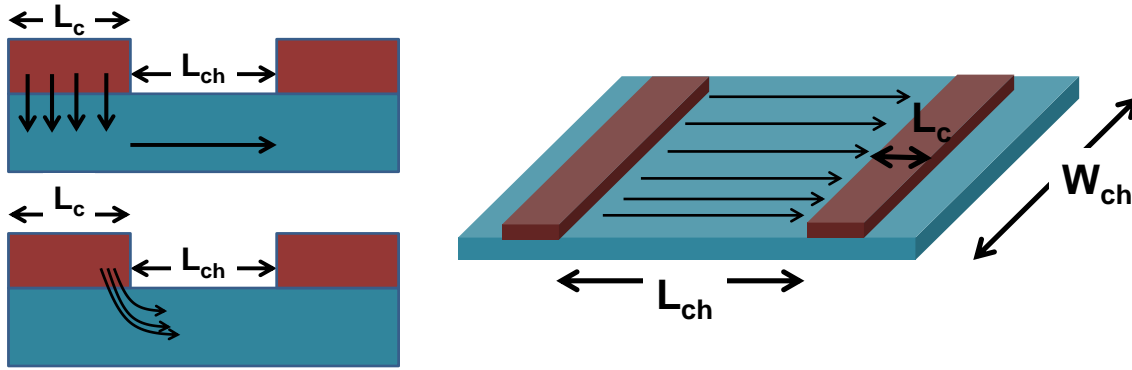
CVD Graphene - *Non-optimized Transfer Process



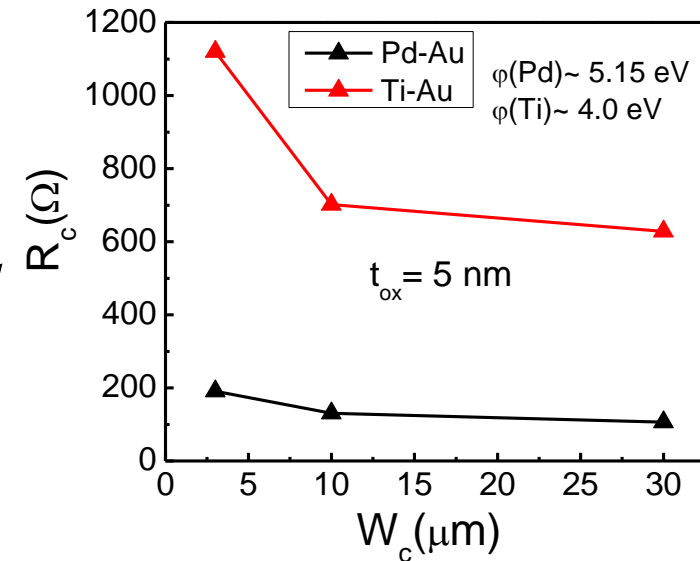
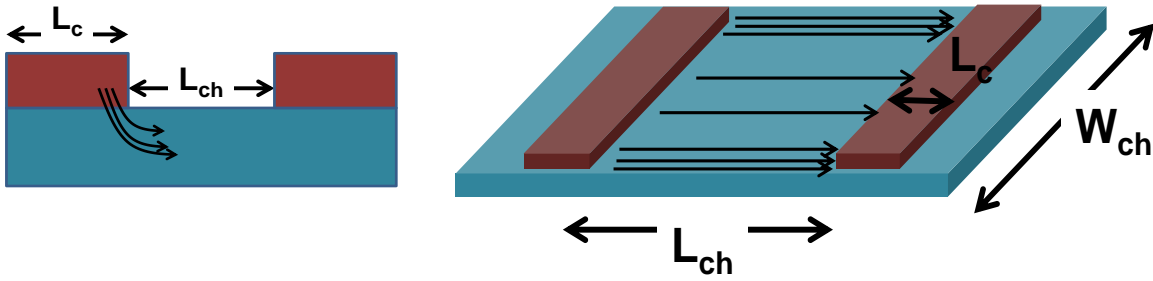
- No appreciable difference between R_c measured in air vs. R_c measured in vacuum
- **No dependence** on metal work function
- Possible reasons:
 - residue at the interface dominates any difference that metal type might have
 - charge transfer does not contribute appreciably to the contact resistance (R_c)

Dependence of R_c on W_c

Typical current flow paths



Current flow path in a graphene device (assumption)



Contact Resistance Values

Reference	Metal	Pre-/Post Process Conditions	Measurement Conditions	Contact Resistance
[44]	Ti/Au	N/A	TLM at 0.25-4.2 K	800 $\Omega\text{-}\mu\text{m}$
[15]	Ni	N/A	TLM at room temp	800-2000 $\Omega\text{-}\mu\text{m}^2$
[41]	Cr/Au	PMA (H ₂ /Ar, 300 °C, 1 hr)	CBKR at room temp	10 ³ -10 ⁶ $\Omega\text{-}\mu\text{m}$
[41]	Ti/Au	PMA (H ₂ /Ar, 300 °C, 1 hr)	CBKR at room temp	10 ³ -10 ⁶ $\Omega\text{-}\mu\text{m}$
[41]	Ni	PMA (H ₂ /Ar, 300 °C, 1 hr)	CBKR at room temp	500 $\Omega\text{-}\mu\text{m}$
[45]	Pd/Au	N/A	TLM at room temp	230 $\Omega\text{-}\mu\text{m}$
[45]	Pd/Au	N/A	TLM at 6 K	90-130 $\Omega\text{-}\mu\text{m}$
[46] (CVD)	Ti/Pd/Au	N/A	I-V at room temp	2000-2500 $\Omega\text{-}\mu\text{m}$
[46] (CVD)	Ti/Pd/Au	5 nm Al followed by etch	I-V at room temp	200-500 $\Omega\text{-}\mu\text{m}$
[42] (Epi)	Ti/Au, Ni/Au, Pt/Au, Cu/Au, Pd/Au	PMA (Forming Gas, 450 °C, 15 min)	TLM at room temp	>1000 $\Omega\text{-}\mu\text{m}^2$
[42] (Epi)	Ti/Au, Ni/Au, Pt/Au, Cu/Au, Pd/Au	O ₂ Plasma Clean and PMA (Forming Gas, 450 °C, 15 min)	TLM at room temp	~7.5 $\Omega\text{-}\mu\text{m}^2$
[47] (Epi)	Cr/Au	N/A	TLM at room temp	0.005 $\Omega\text{-}\mu\text{m}^2$
[47] (Epi)	Cr/Au	N/A	TLM at 673 K	0.003 $\Omega\text{-}\mu\text{m}^2$
[47] (Epi)	Ti/Au	N/A	TLM at room temp	0.06 $\Omega\text{-}\mu\text{m}^2$
[47] (Epi)	Ti/Au	N/A	TLM at 673 K	0.05 $\Omega\text{-}\mu\text{m}^2$

A. Venugopal, L. Colombo, and E. M. Vogel, "Issues with Characterizing Transport Properties of Graphene Field Effect Transistors," *Solid State Communications* **152**, 1311–1316 (2012)

[15] A. Venugopal, L. Colombo, E.M. Vogel, Applied Physics Letters, 96 (2010) 013512-013513.

[41] K. Nagashio, T. Nishimura, K. Kita, A. Toriumi, Applied Physics Letters, 97 (2010) 143514.

[42] J.A. Robinson, M. LaBella, M. Zhu, M. Hollander, R. Kasarda, Z. Hughes, K. Trumbull, R. Cavalero, D. Snyder, Applied Physics Letters, 98 (2011) 053103-053103.

[44] S. Russo, M.F. Craciun, M. Yamamoto, A.F. Morpurgo, S. Tarucha, Physica E: Low-Dimensional Systems and Nanostructures, 42 (2010) 677-679.

[45] F. Xia, V. Perebeinos, Y.-m. Lin, Y. Wu, P. Avouris, Nat Nano, 6 (2011) 179-184.

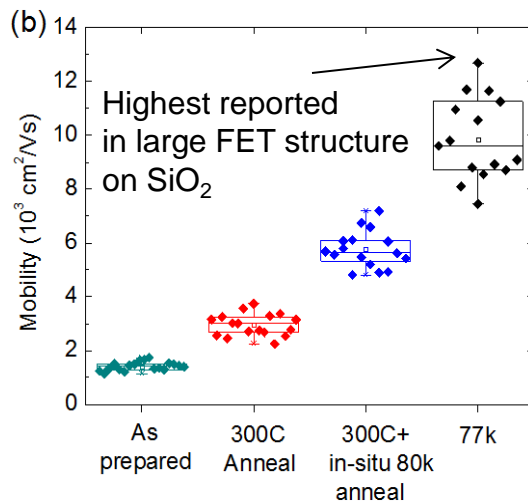
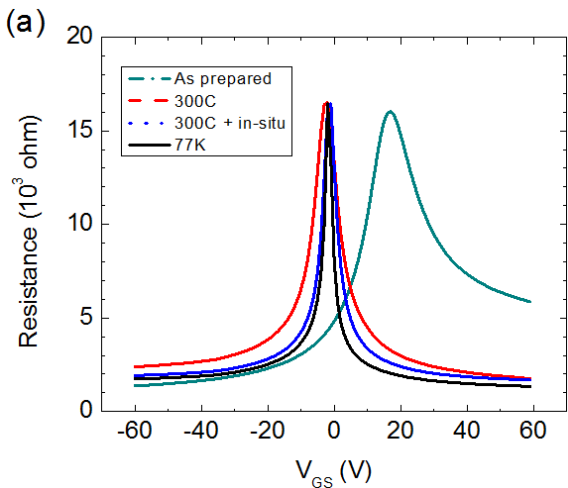
[46] A. Hsu, W. Han, K. Ki Kang, K. Jing, T. Palacios, Electron Device Letters, IEEE, 32 (2011) 1008-1010.

[47] V.K. Nagareddy, I.P. Nikitina, D.K. Gaskill, J.L. Tedesco, R.L. Myers-Ward, C.R. Eddy, J.P. Goss, N.G. Wright, A.B. Horsfall, Applied Physics Letters, 99 (2011) 073506.

Outline

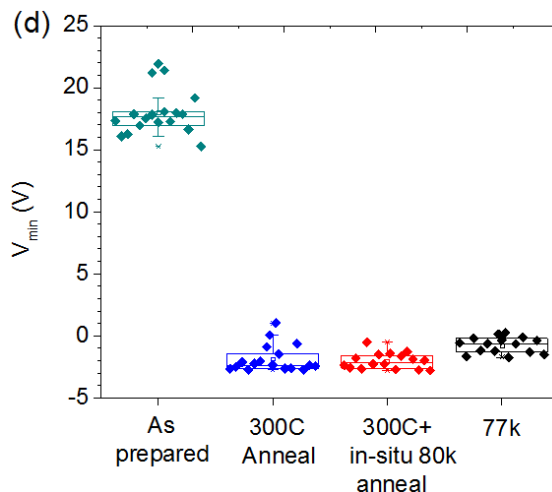
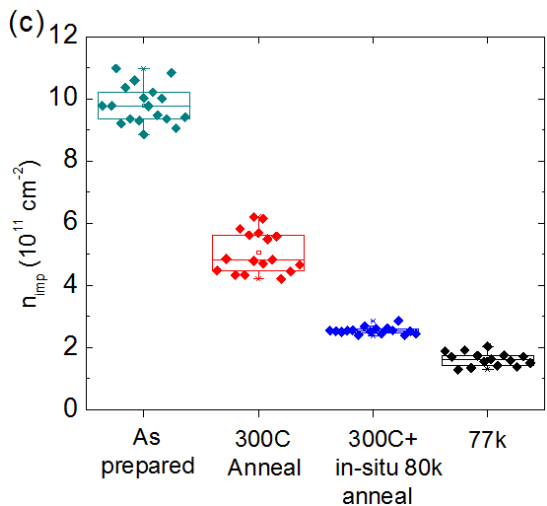
- Motivation
- A Simple “Universal” Model for Transport in Single Layer Graphene
- Effect of Device Dimensions on Mobility
- Effect of Contacts
- CVD Graphene Vertical Tunnel Transistors
- Conclusions

Optimized CVD Graphene Transfer Process



Improved performance by 80 °C *in-situ* anneal

- Mobility as high as 7200 cm²/Vs at room temperature (65 x 15 μm²)
- Mobility as high as 12700 cm²/Vs at 77K, highest reported CVD graphene with FET structure

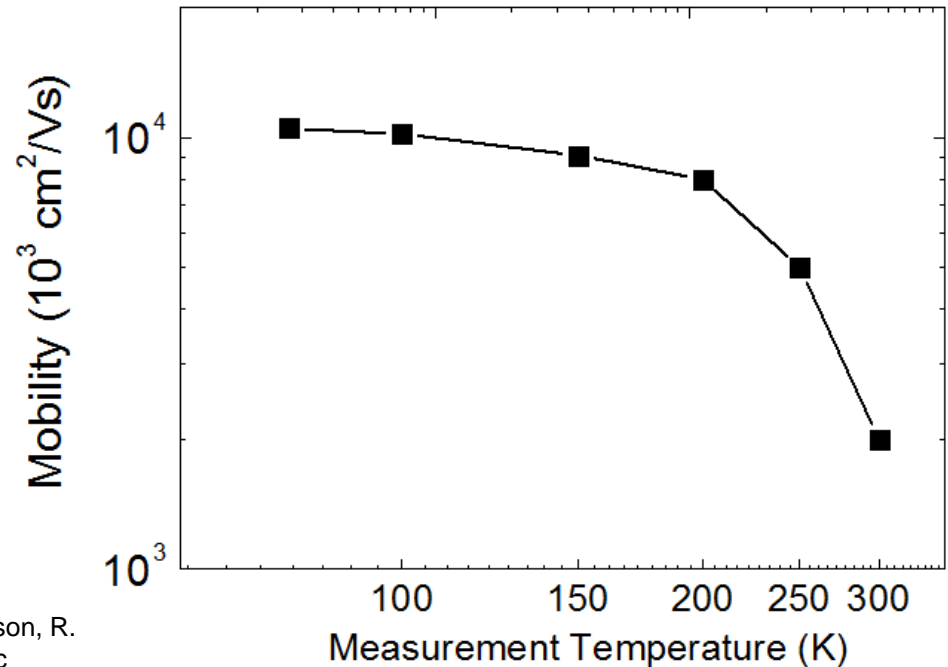


Approaching Exfoliated Graphene

- Electrical behavior of CVD graphene is similar to that of exfoliated graphene on SiO₂ substrate
- Mobility approaches the limit (~10,000 cm²/Vs) of graphene reported on SiO₂*
- The mobility is by impurity scattering at low temperature and both phonons and impurities at room temperature.

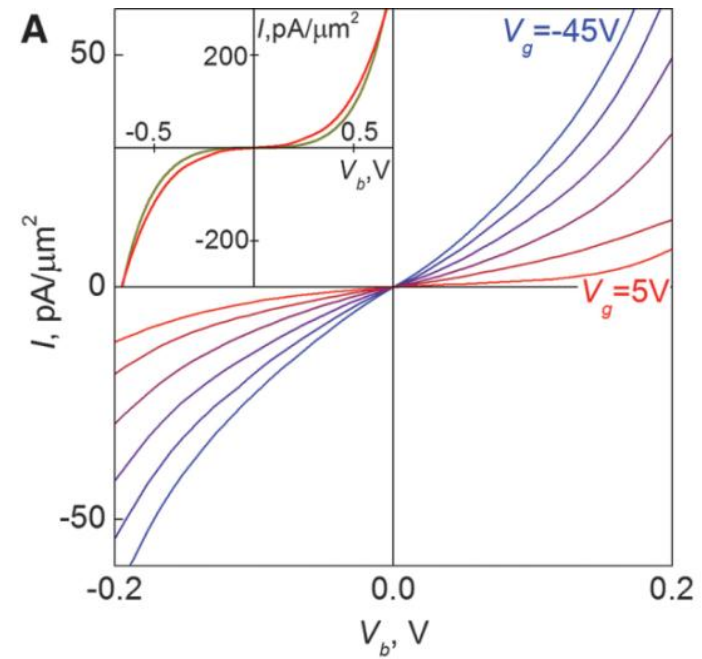
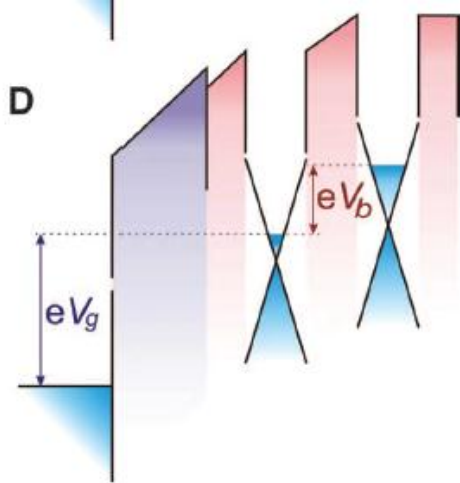
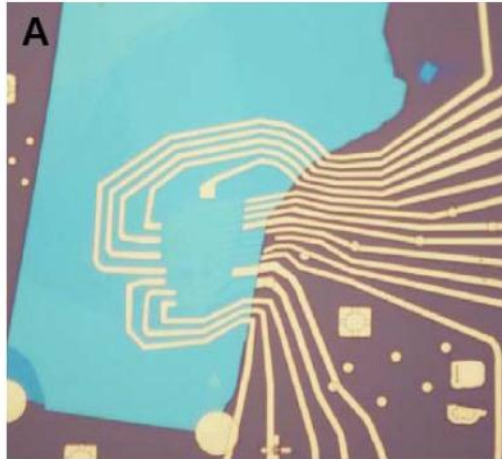
*S. Adam et. al., *A self-consistent theory for graphene transport*, *PNAS*. 104, 18392–18397 (2007).

J. Chan, A. Venugopal, A. Pirkle, S. McDonnell, D. Hinojos, C. W. Magnuson, R. S. Ruoff, L. Colombo, R. M. Wallace, and E. M. Vogel, "Reducing Extrinsic Performance-Limiting Factors in Graphene Grown by Chemical Vapor Deposition," *ACS Nano*, **2012**, 6 (4), pp 3224–3229



Vertical Graphene Tunnel FET Literature

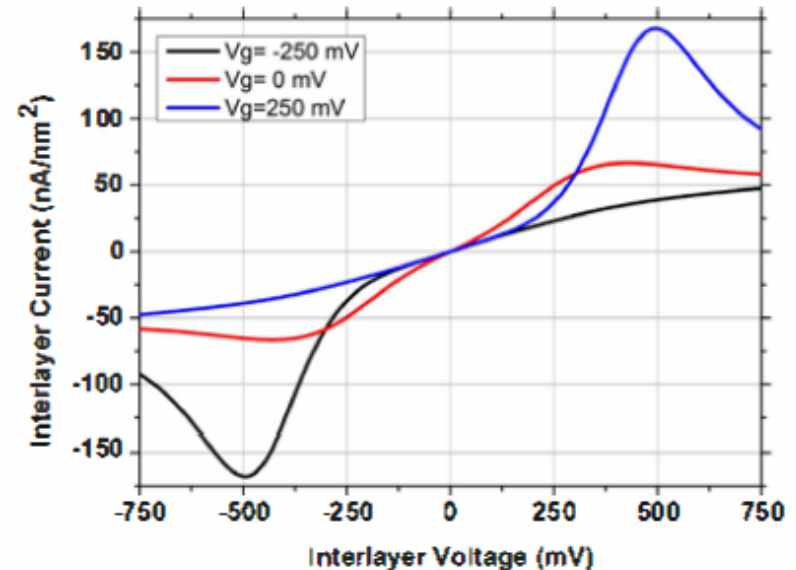
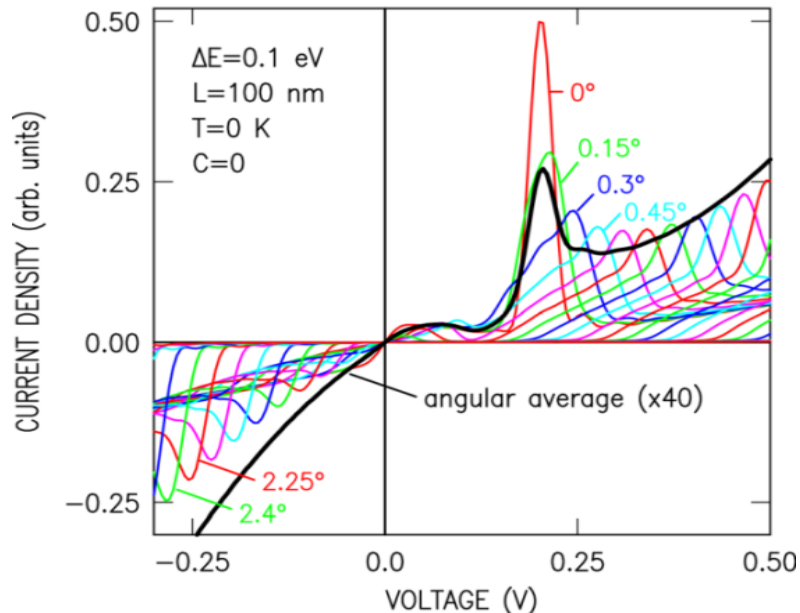
- Tunneling for a graphene-hBN device with 6 ± 1 layers of hBN as the tunnel barrier.
- Room temperature switching ratio:
 - ≈ 50 with h-BN
 - ≈ 10000 with MoS_2 ^[1]



^{1]}Britnell et al., *Science*, 335 (2012)

Vertical Graphene Tunnel FET Literature

- Negative differential resistance can be observed when Dirac points of two graphene layers line up^[2-3]



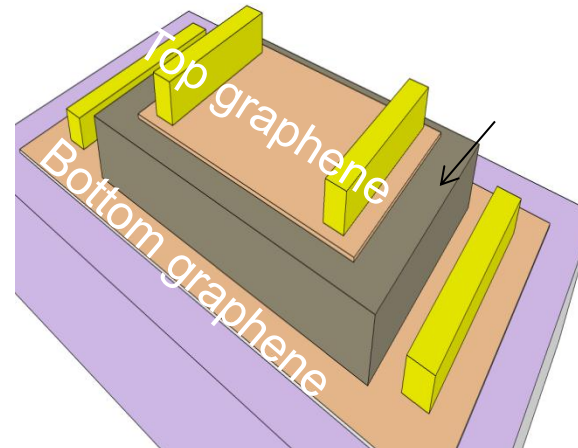
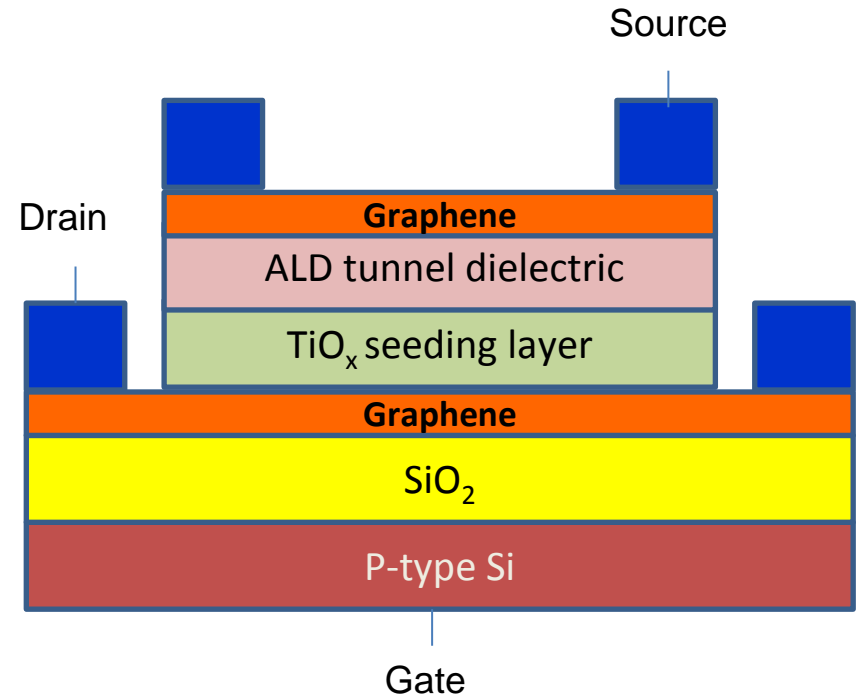
[2]Feenstra et al., *J. Appl. Phys.*, 111 (2012)

[3]Reddy et al., *IEEE Dev. Res. Conf.* (2012)

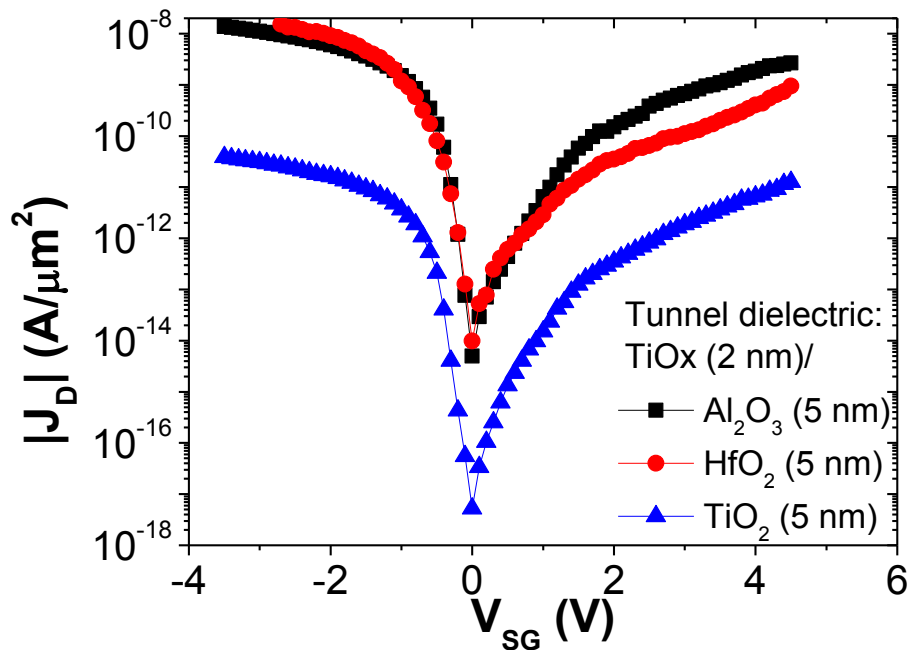
Device Structure

Fabrication process and sample preparation:

- Thermal growth of SiO_2 on p-doped Si
- Wet transfer of CVD graphene
- CVD graphene anneal in 2% forming gas
- Graphene etch in oxygen plasma
- Lift-off of Ni/Au drain metal contacts
- E-beam evaporation of Ti seeding layer on graphene
- Atomic layer deposition of dielectric
- Wet transfer of top graphene layer
- Graphene etch in oxygen plasma
- Lift-off of Ni/Au source metal contacts
- Anneal of top graphene layer in 2% forming gas
- 80 °C anneal of devices in vacuum prior to measurement



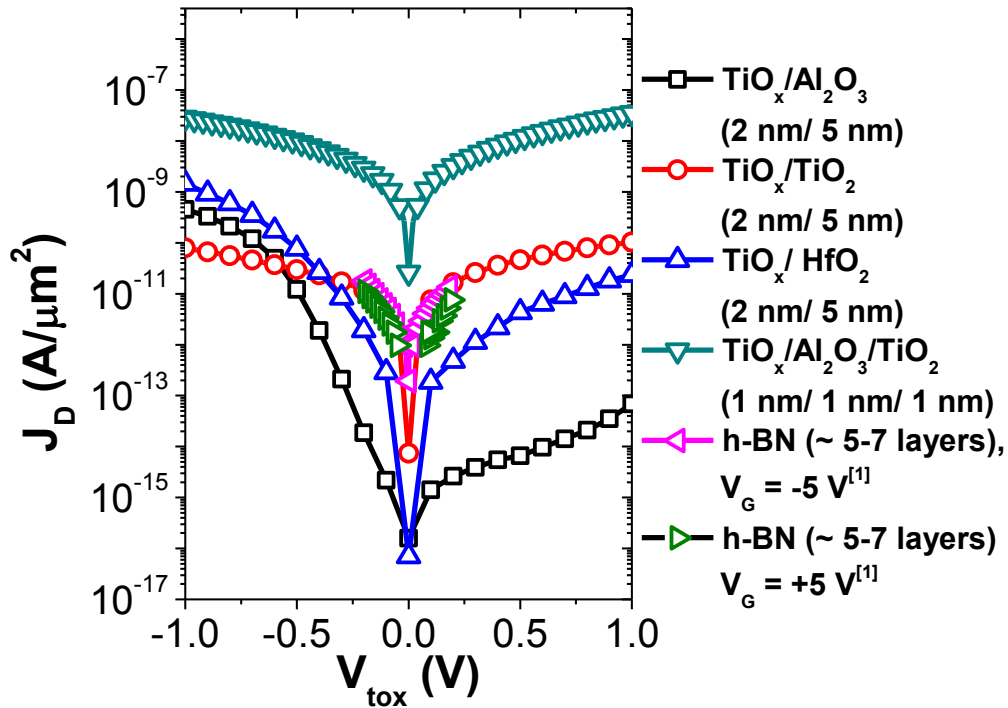
Gate Voltage Dependence of Current



$$S = \frac{dI_D}{dV_G} = \frac{\partial I_D}{\partial V_D} \frac{\partial V_D}{\partial V_G}$$

- Subthreshold swing for TiO_x/Al₂O₃ – 120 mV/dec
- Subthreshold swing for TiO_x/TiO₂ – 70 mV/dec
- $I_{ON}/I_{OFF} \approx 10^6$

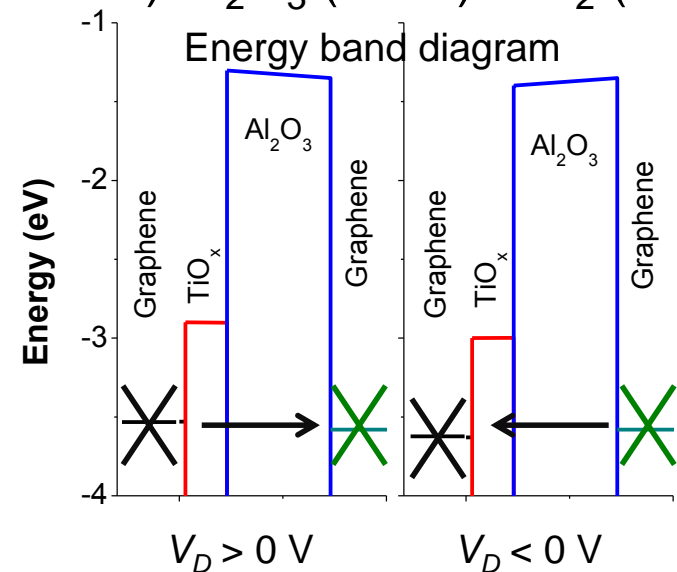
Drain Voltage Dependence of Current



- Symmetric current for symmetric barrier
- Drive current extremely low

$$S = \frac{dI_D}{dV_G} = \frac{\partial I_D}{\partial V_D} \frac{\partial V_D}{\partial V_G}$$

- Upon decoupling gate oxide capacitance
 - “subthreshold swing” $(\partial I_D / \partial V_D)^{-1} \approx 27$ mV/dec for TiO_x (2 nm)/ TiO_2 (5 nm)
 - 10 mV/dec for TiO_x (1 nm)/ Al_2O_3 (1 nm)/ TiO_2 (1 nm)



Outline

- Motivation
- A Simple “Universal” Model for Transport in Single Layer Graphene
- Effect of Device Dimensions on Mobility
- Effect of Contacts
- CVD Graphene Vertical Tunnel Transistors
- **Conclusions**

Conclusions

- A simple model for the total device resistance indicates that the maximum graphene resistance is approximately independent of mobility and that the minimum resistance is limited by the contact resistance.
- Mobility depends on both the device length and width. Large device dimensions should be used when extracting mobility.
- Current saturation at large fields is due to the contact resistance.
- The width dependence of contact resistance suggests preferential injection at the edges of graphene.
- A transfer process for CVD graphene has been developed which achieves mobility consistent with exfoliated graphene.
- Vertical tunnel FETs have been fabricated using bilayers of CVD graphene.