2007 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics
March 27-29, 2007 Gaithersburg, MD National Institute of Standards and Technology (NIST)

Advanced CMOS and Related Characterization in MIRAI project

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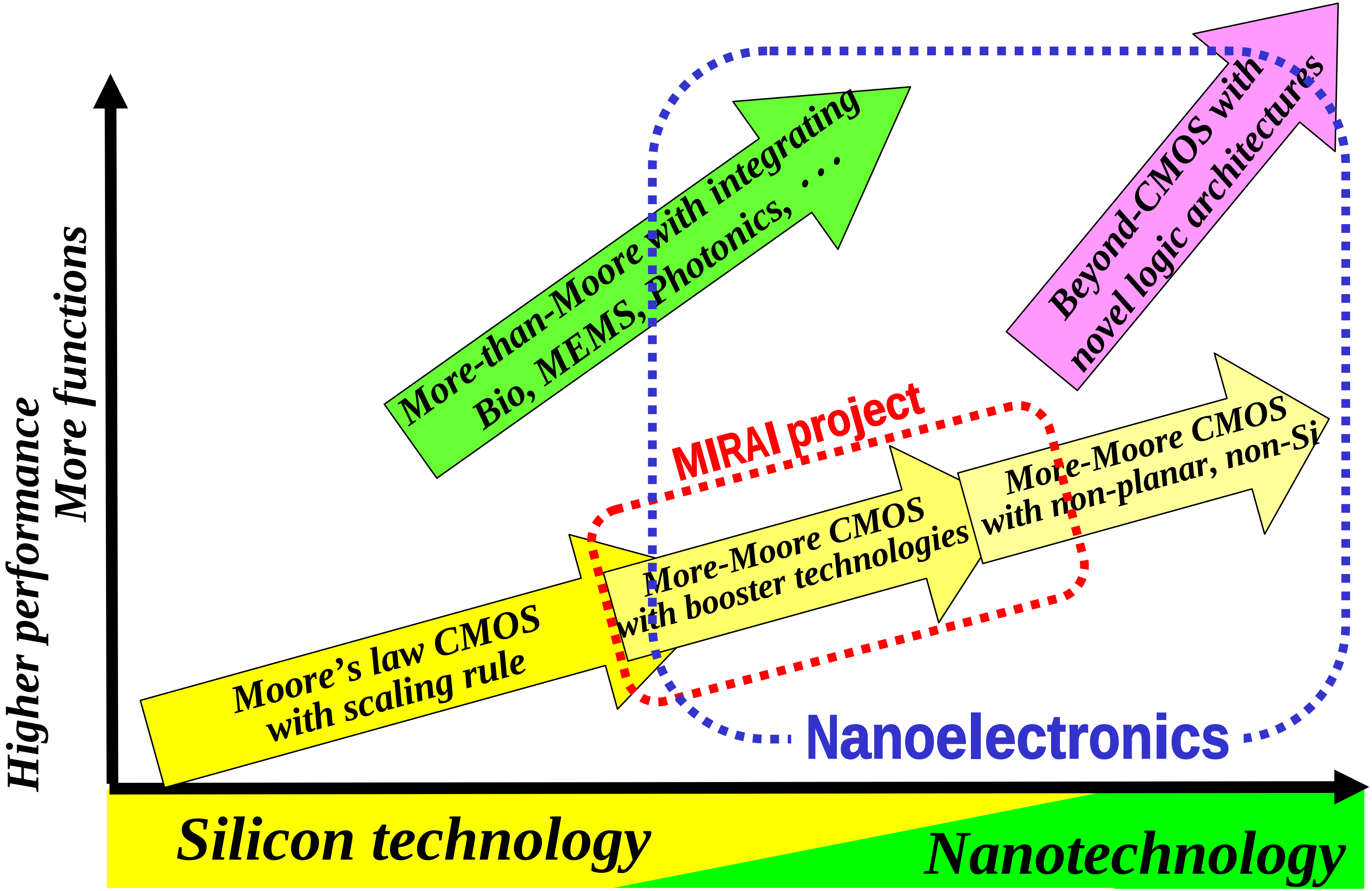
MIRAI, Semiconductor Leading Edge Technologies (Selete)

The MIRAI project is supported by NEDO, Japan

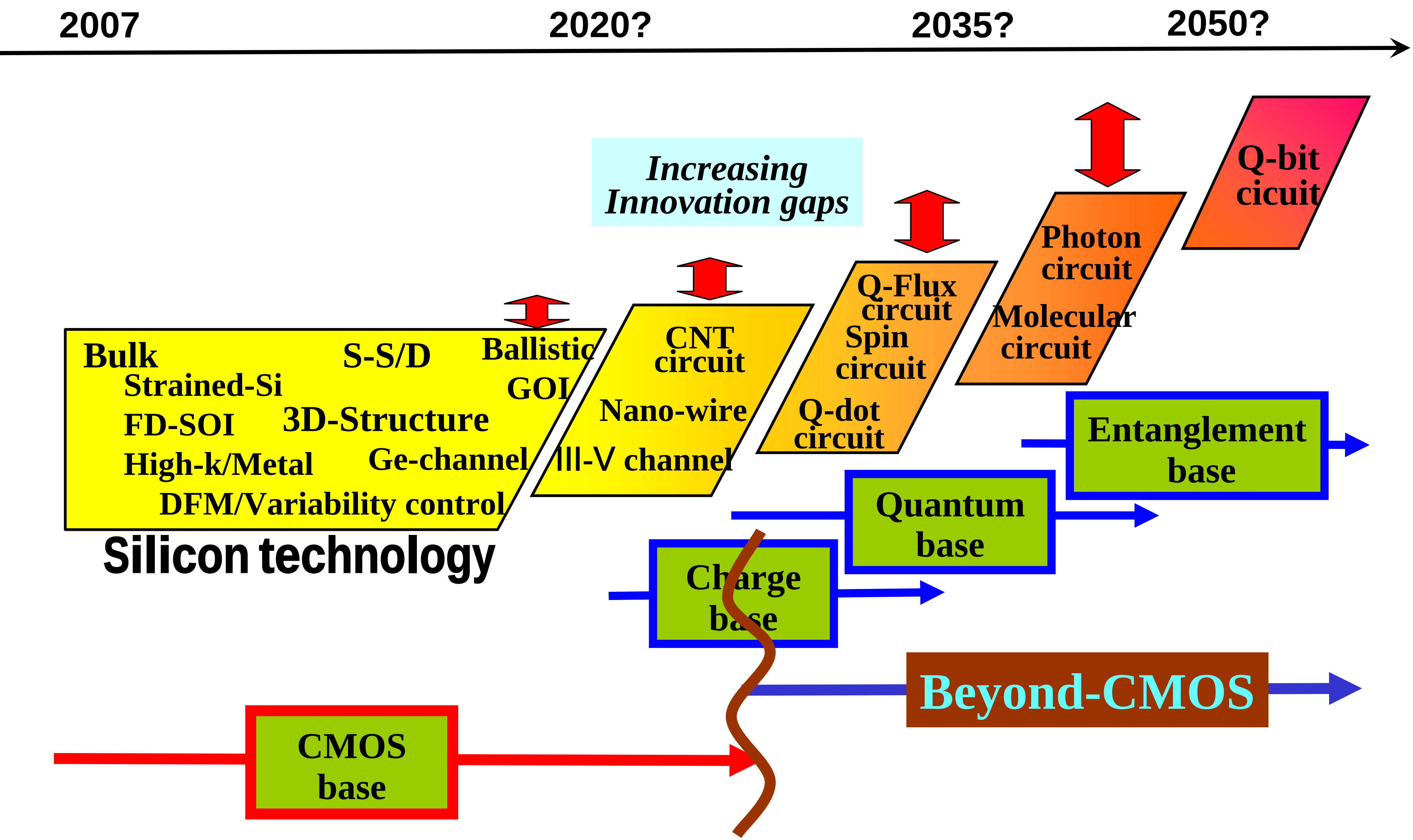
Contents

- Introduction (Nanoelectronics)
- MIRAI project and TSC (Selete)
- MIRAI activities
- Advanced CMOS
- Conclusion

More-Moore, More-Than-Moore, Beyond CMOS

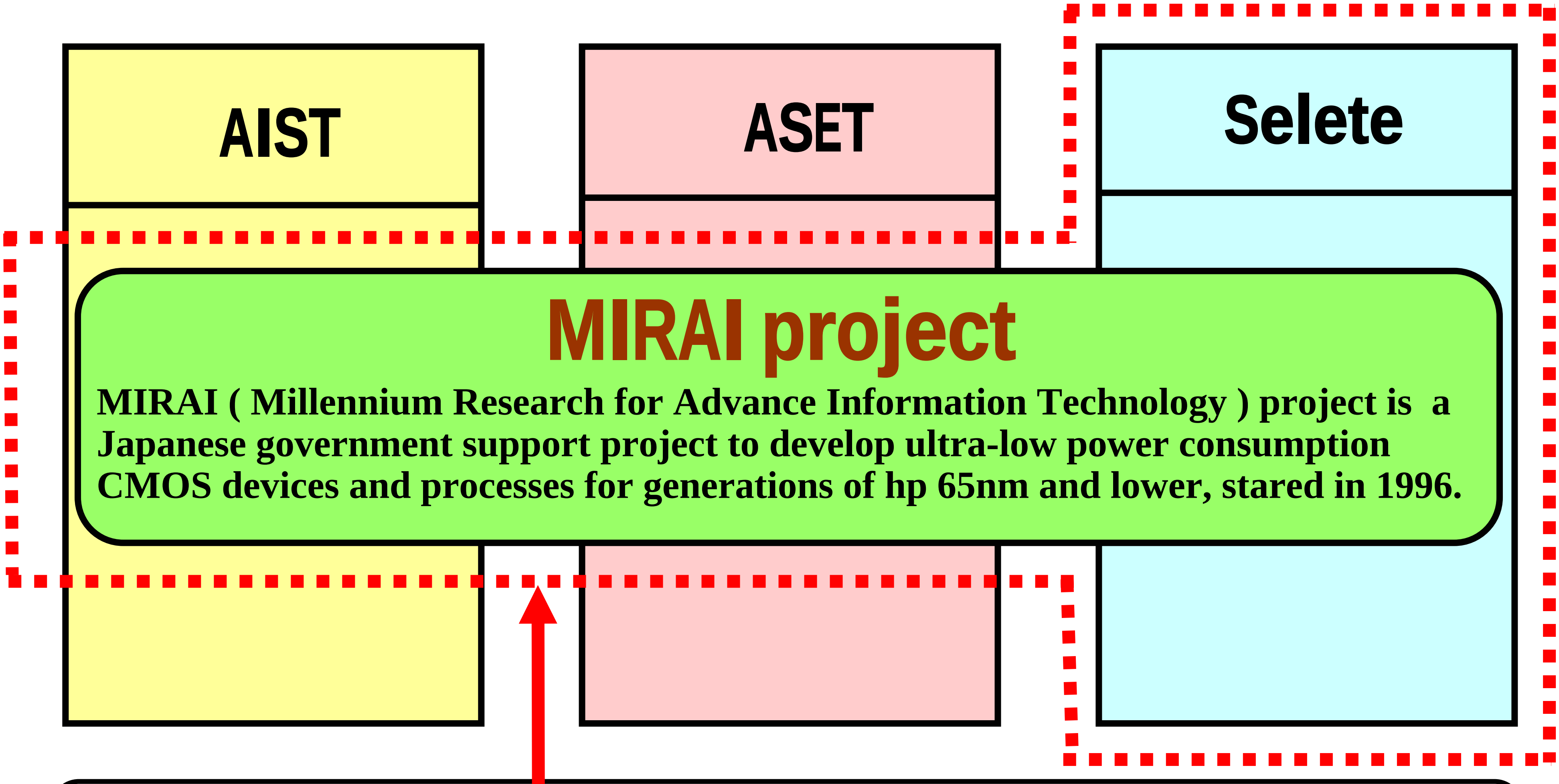


Beyond-CMOS devices with novel architectures



MIRAI project and TSC

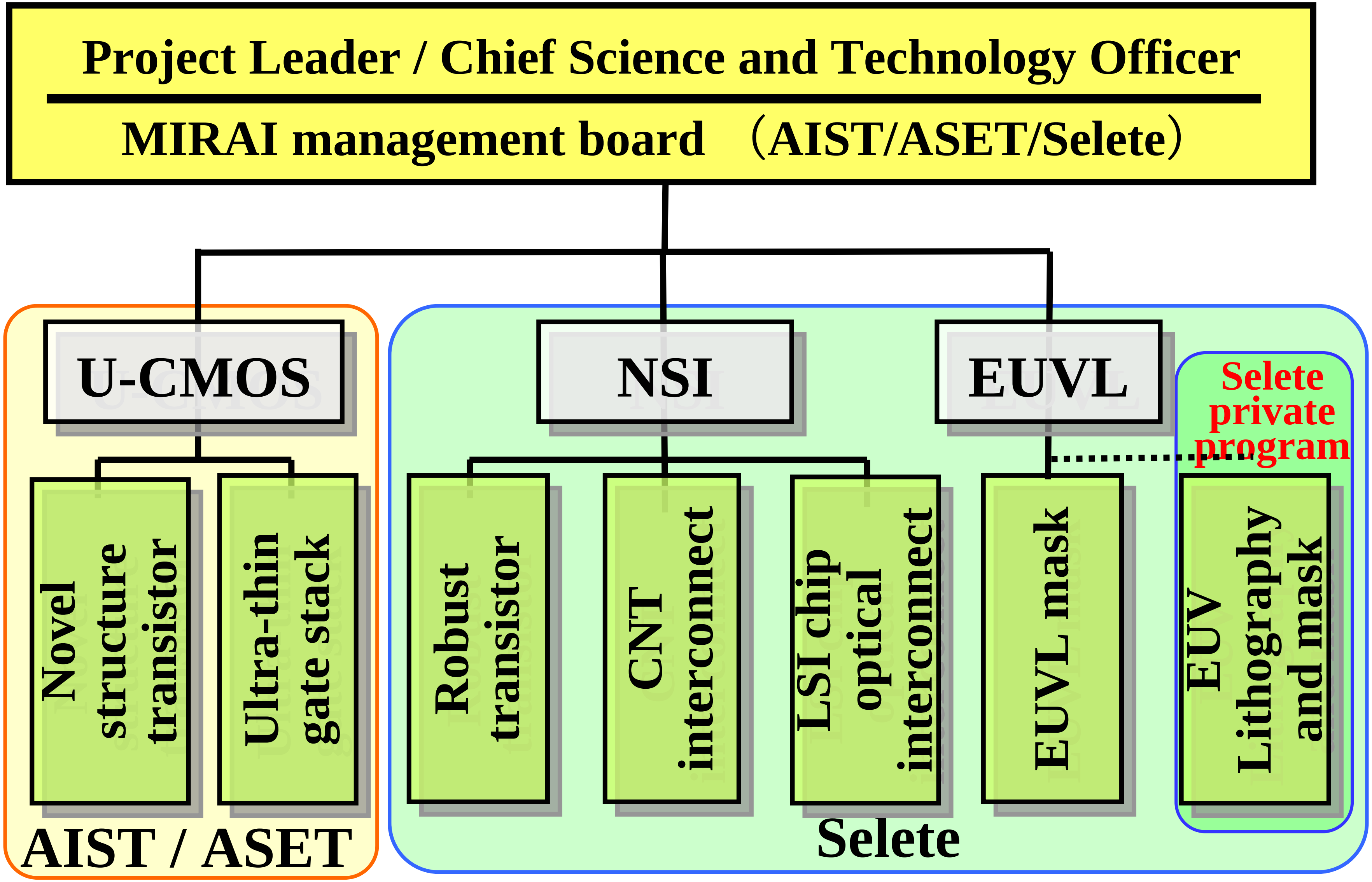
MIRAI project consists of parts of three organizations.



TSC (Tsukuba Semiconductor Consortium) is a virtual organization to enhance collaborative works between Selete and MIRAI.

TSC (MIRAI project and Selete)

Organization of MIRAI



NSI : Nano-Silicon Integration

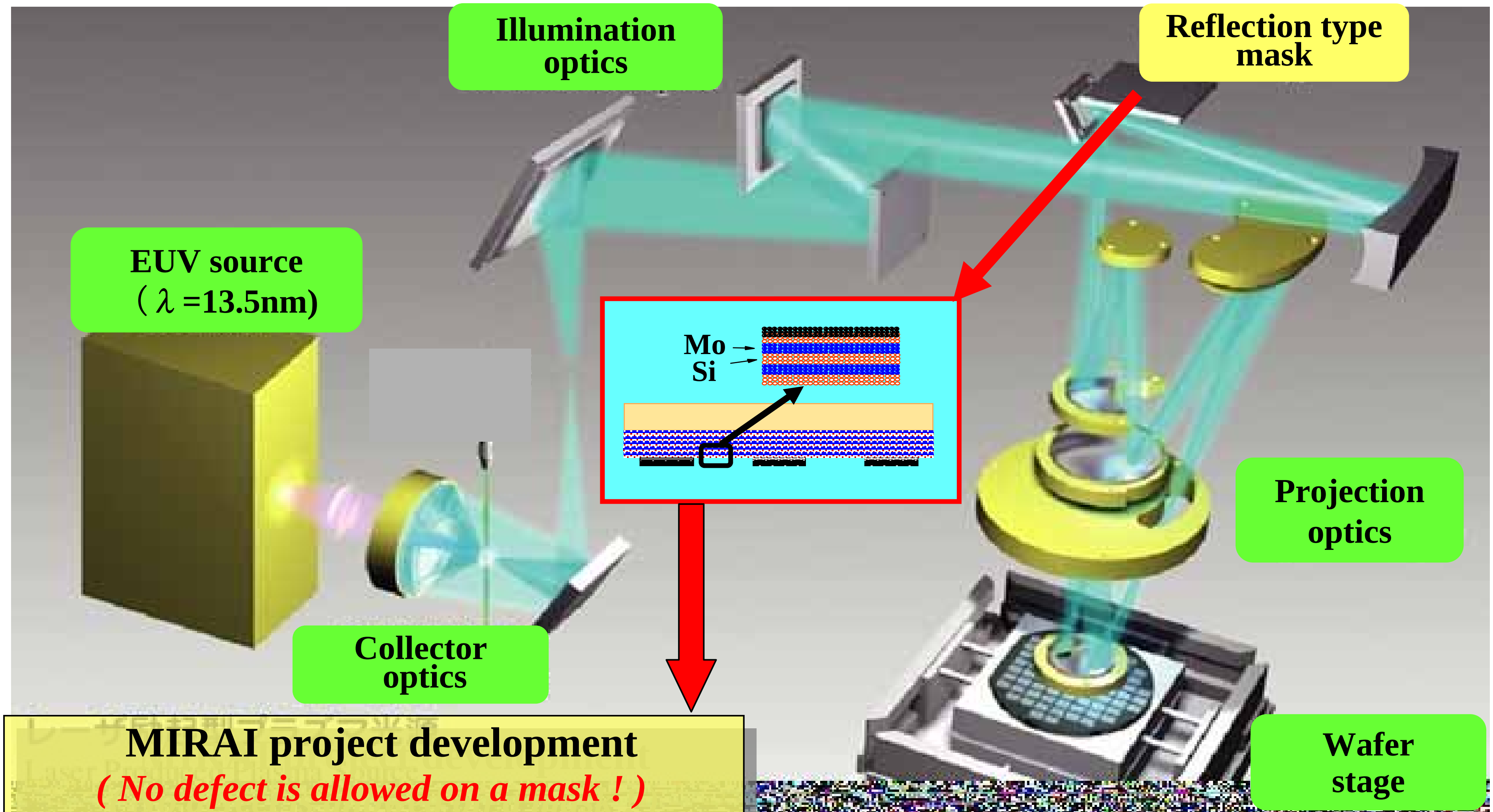
Rough sketch of TSC R&D Targets

Advanced CMOS (Ultra scaled CMOS)	High-k Gate →	Higher-k Gate →	3D channel →	Nanostructured channel
Interconnect (Novel concept)	Low-k Cu →	Lower-k Cu →	Lower-k CNT →	Wireless Interconnection
Variability (Robust transistor)	Individual variabilities →	Combined variabilities →	Robust LSI →	Dependable LSI
Production system (SoC line)	Bottle-neck analysis →	SOC-oriented CMOS line architecture		
Lithography (EUVL)			EUVL	
Half pitch (SoC)	65nm	45nm	32nm	22nm

2005 2010 2015 2020

Year of production start

EUVL system



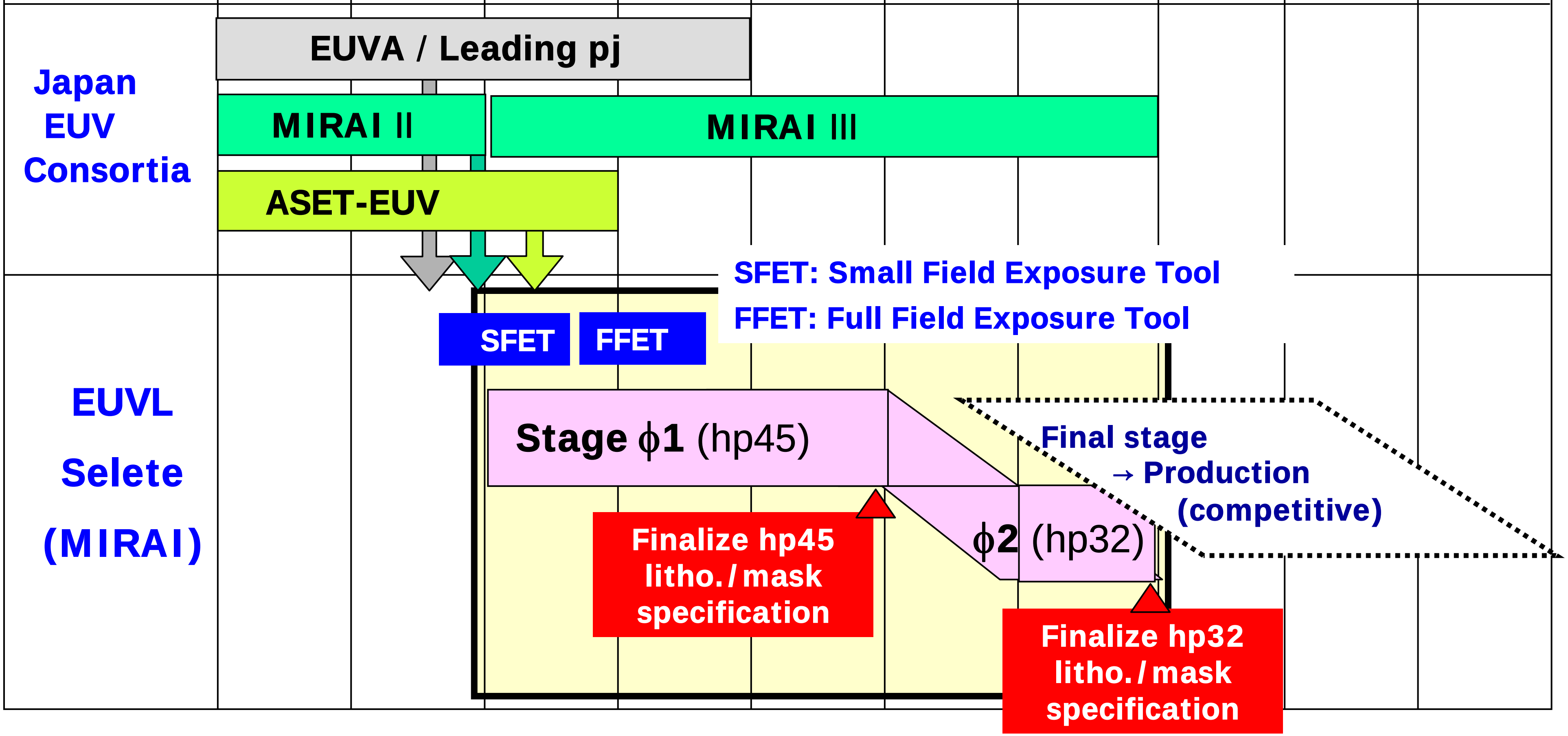
MIRAI project development

(No defect is allowed on a mask !)

- Quality check and control by 13.5nm
- Phase defect detection and control
- Pattern defect detection and control
- Contamination-free carrier

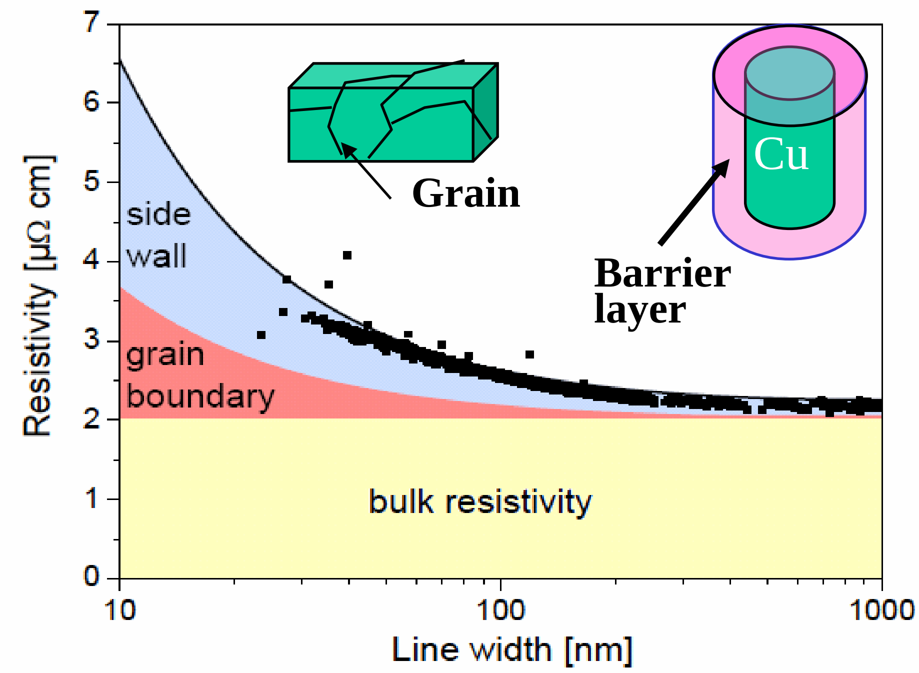
EUVL Program schedule

FY	04	05	06	07	08	09	10	11	12	13
Technol. node	hp90			hp65			hp45			hp32
Business code		65		45		32		22		



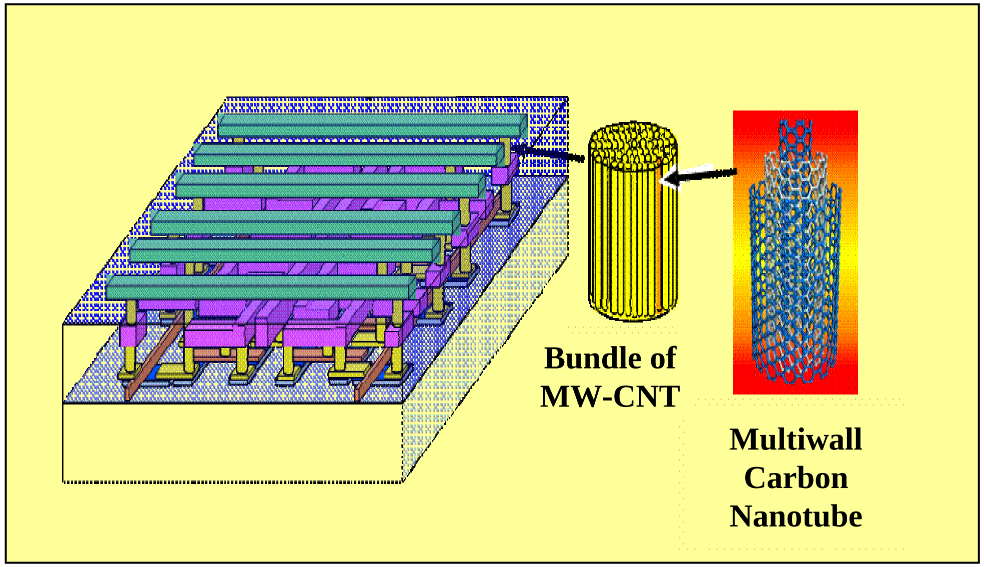
Post-Cu interconnect

Future issues of Cu/Low-k interconnect



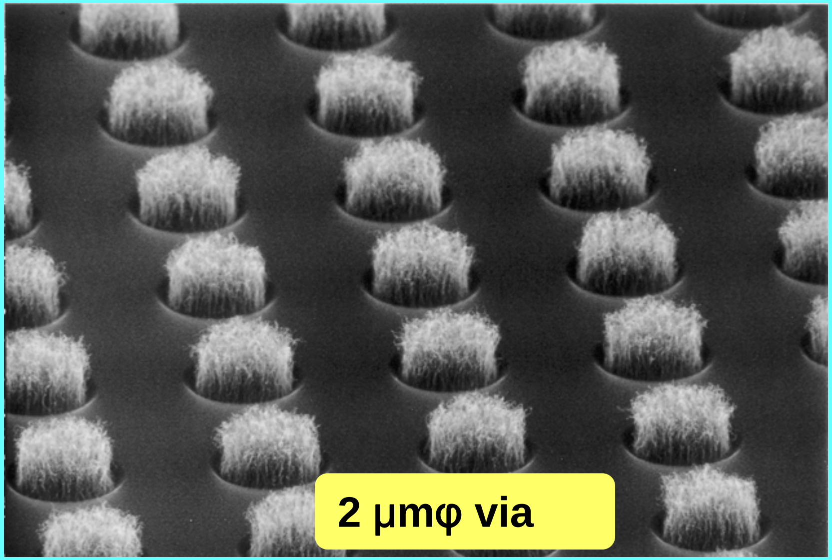
- Resistivity
- Reliability (EM)
- Process complexity

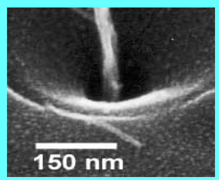
CNT via in low-k as a post-Cu via



- **Max. current density is 1,000 times larger than Cu.**
- **Thermal conductivity is 10 times higher than Cu.**
- **Mechanical strength is 100 times larger than steel.**
- **Ballistic carrier transport along the tube (300K)**
- **Self-organizing growth mechanism (A/R>1000)**

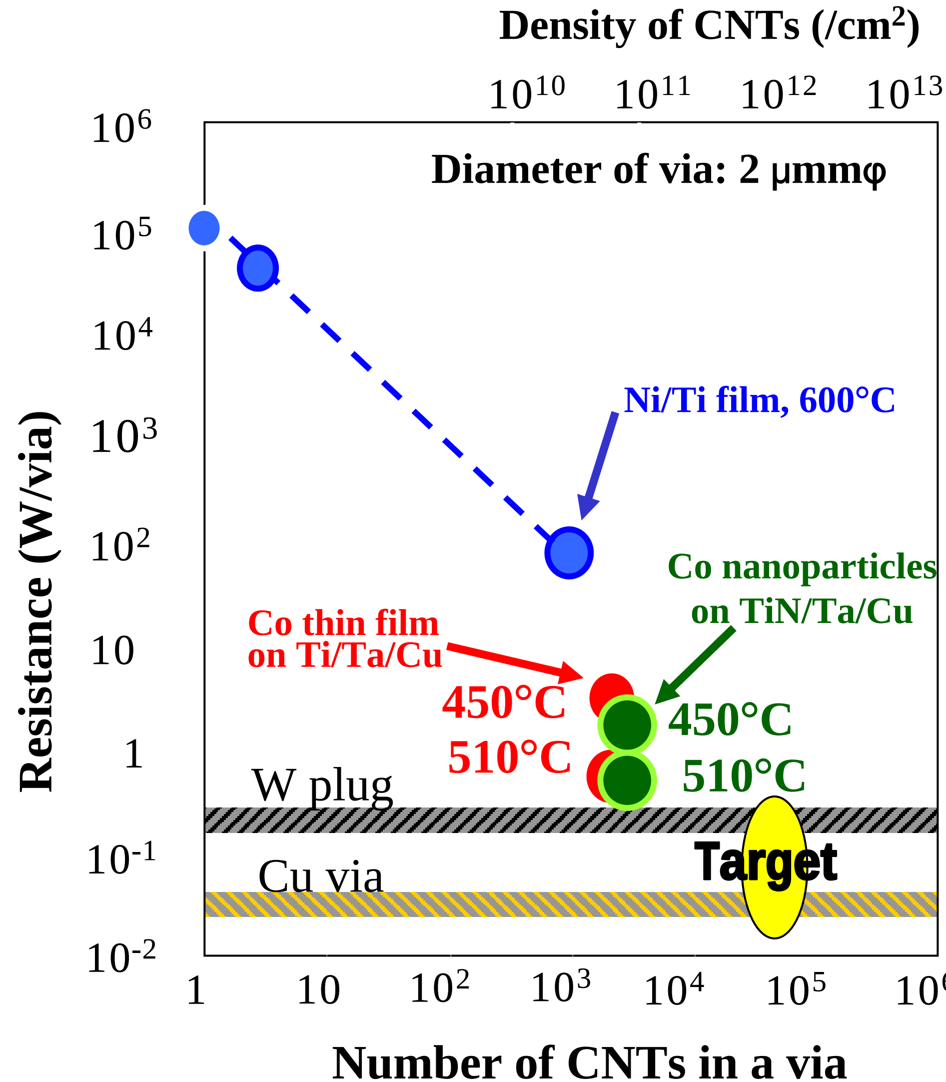
CNT via using cobalt catalyst





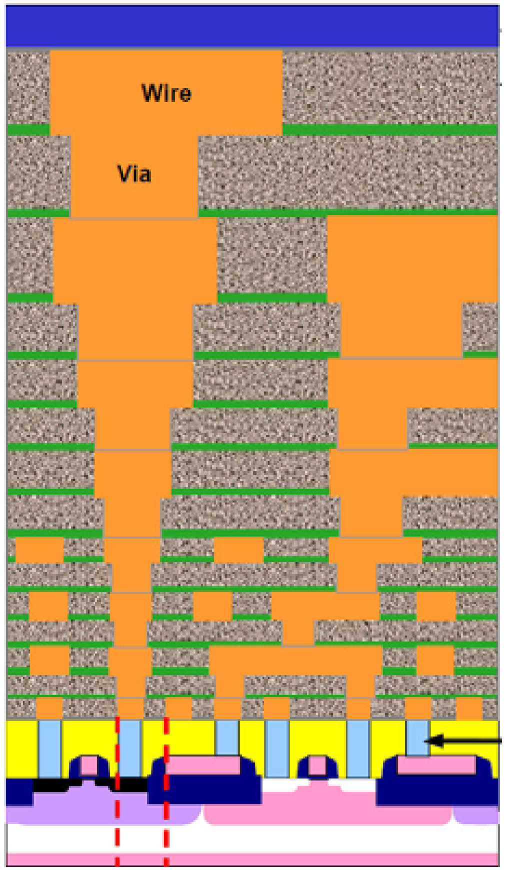
40 nmφ via

CNT via grown at 450 ℃ using cobalt nanoparticle catalyst on TiN/Ta/Cu

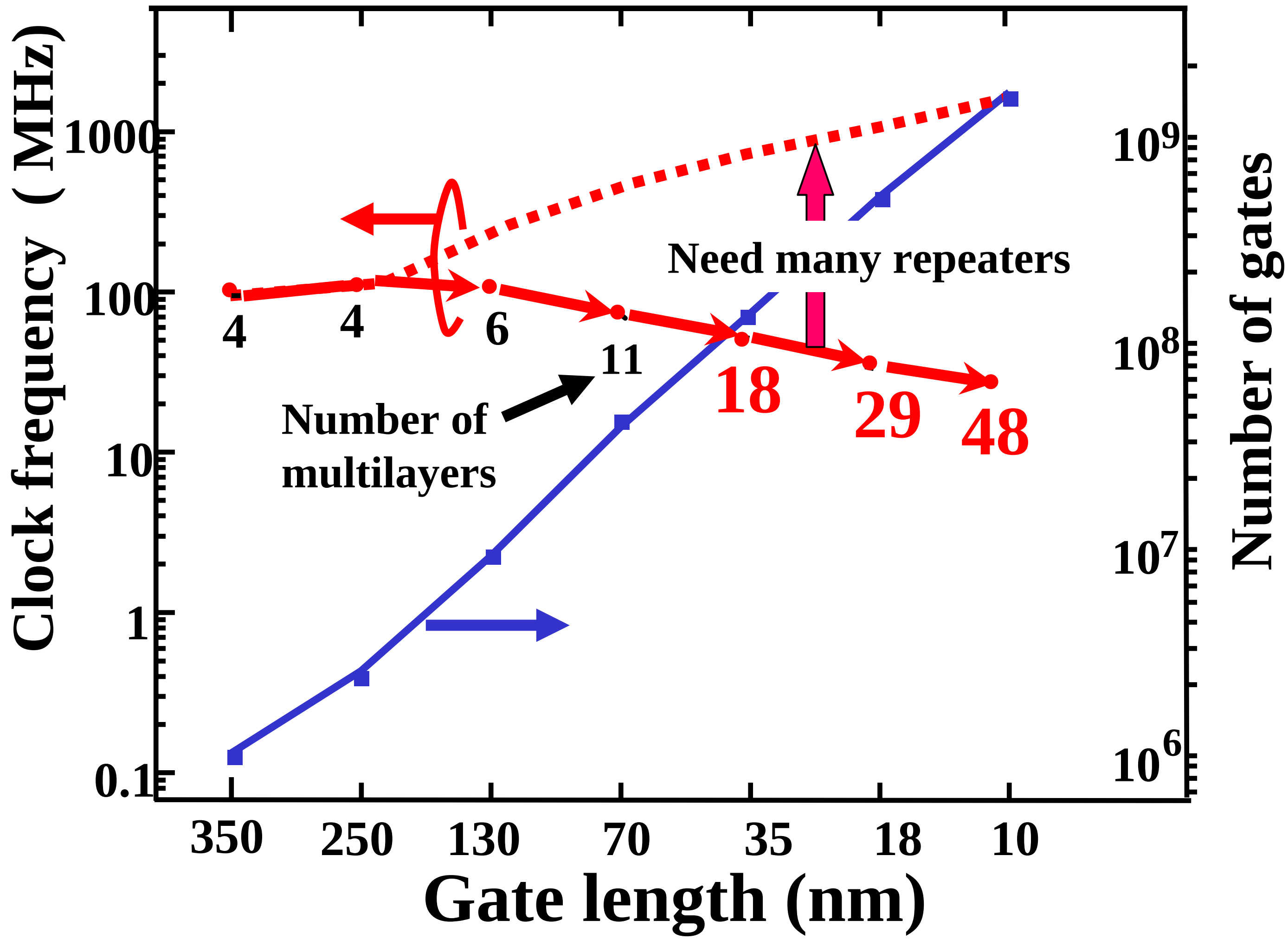


A detail will be reported at this conference tomorrow pm, by Dr. Y. Awano of MIRAI project

Number of mutilayers of interconnect



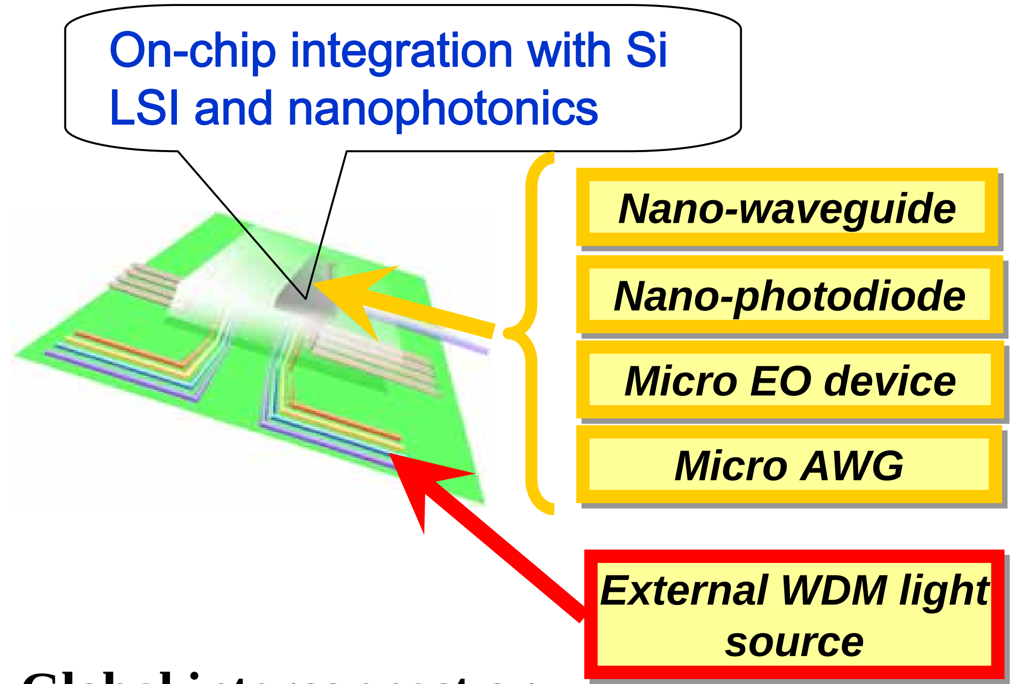
Multilayer interconnect



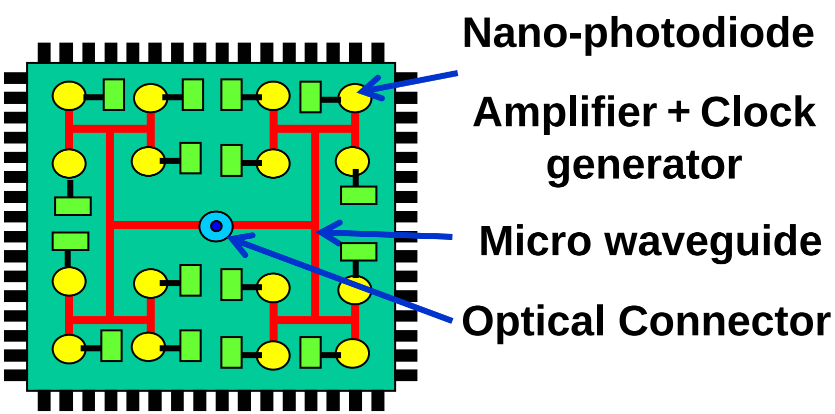
M.Yamashina's simulation (0.01μm Si LSI Symposium in Tokyo 1997)

On-chip optical interconnect

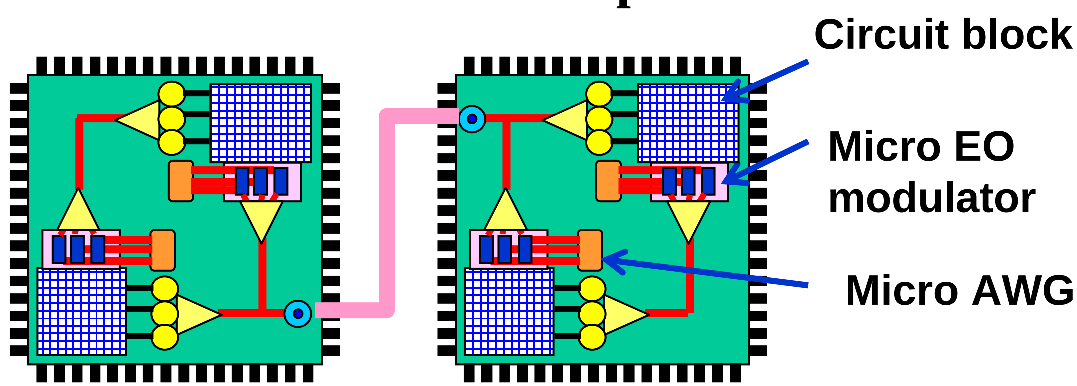
- On-chip high speed clock sharing with less skew and low noise.
- High speed communication by wavelength multiple optical transmission within blocks and chips. (>100Gbps)



1. Clock sharing

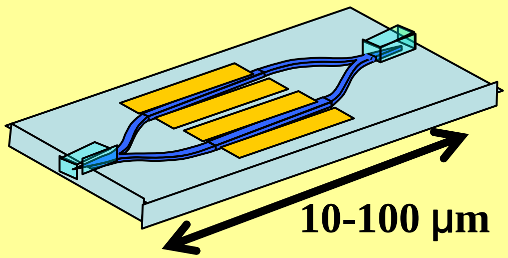


2. Global interconnect or interconnect between chips

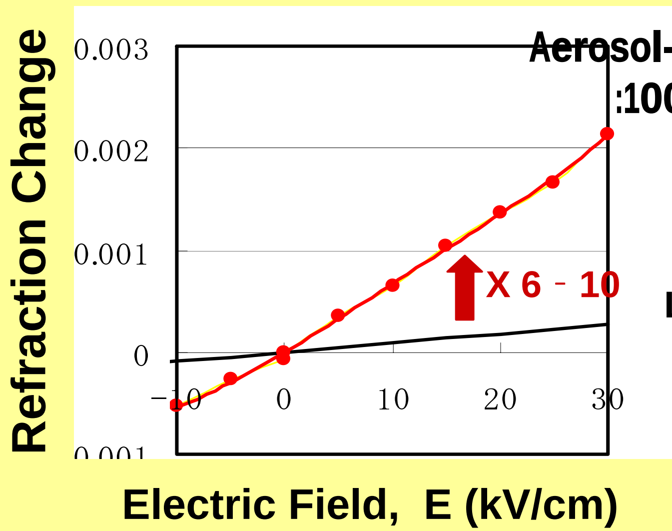


Optical micro devices for on chip interconnect

Micro EO Modulator

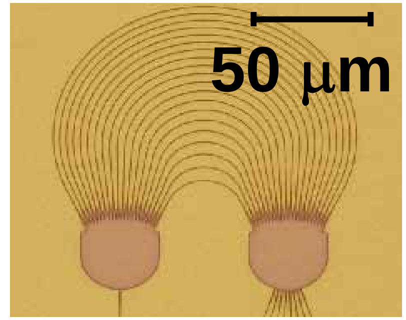


Low Voltage : ~1V
Speed Response: >20GHz

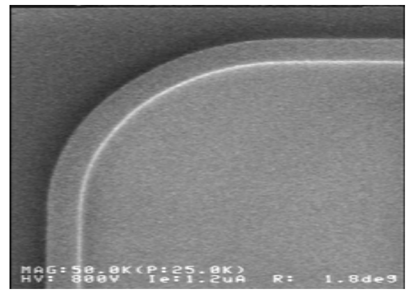


K. Ohashi, ISSCC 2006

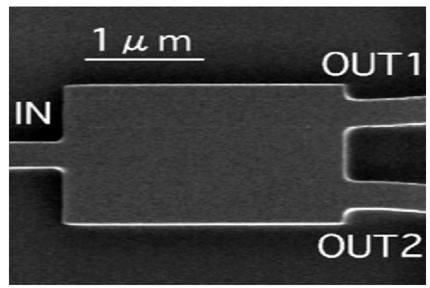
Arrayed waveguide gratings (AWG)



Sharp bending (loss<0.1 dB)

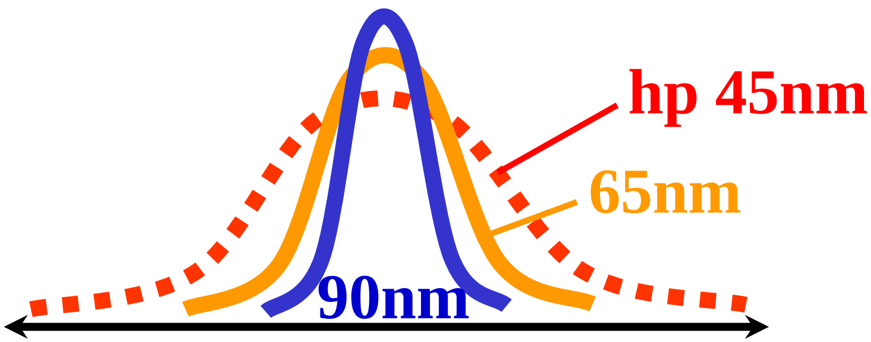


Branching

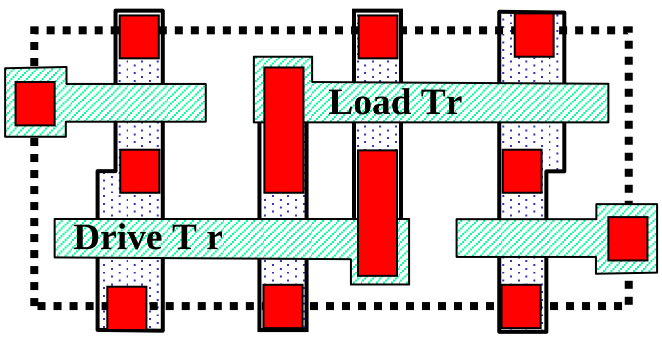


Need for Vth variability control in SRAM

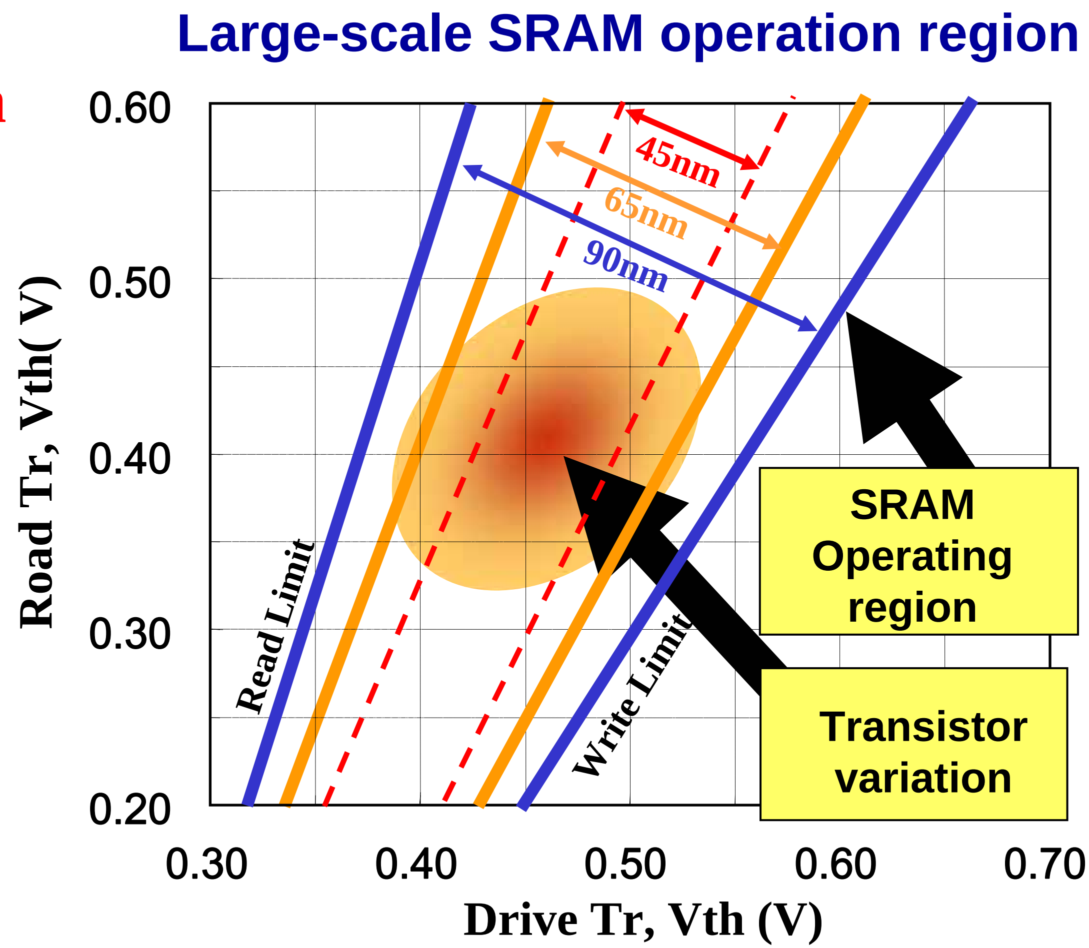
- Variability science and control : an urgent issue of SRAM in SoC
- Decreasing SRAM operation margin with lowering supply voltage



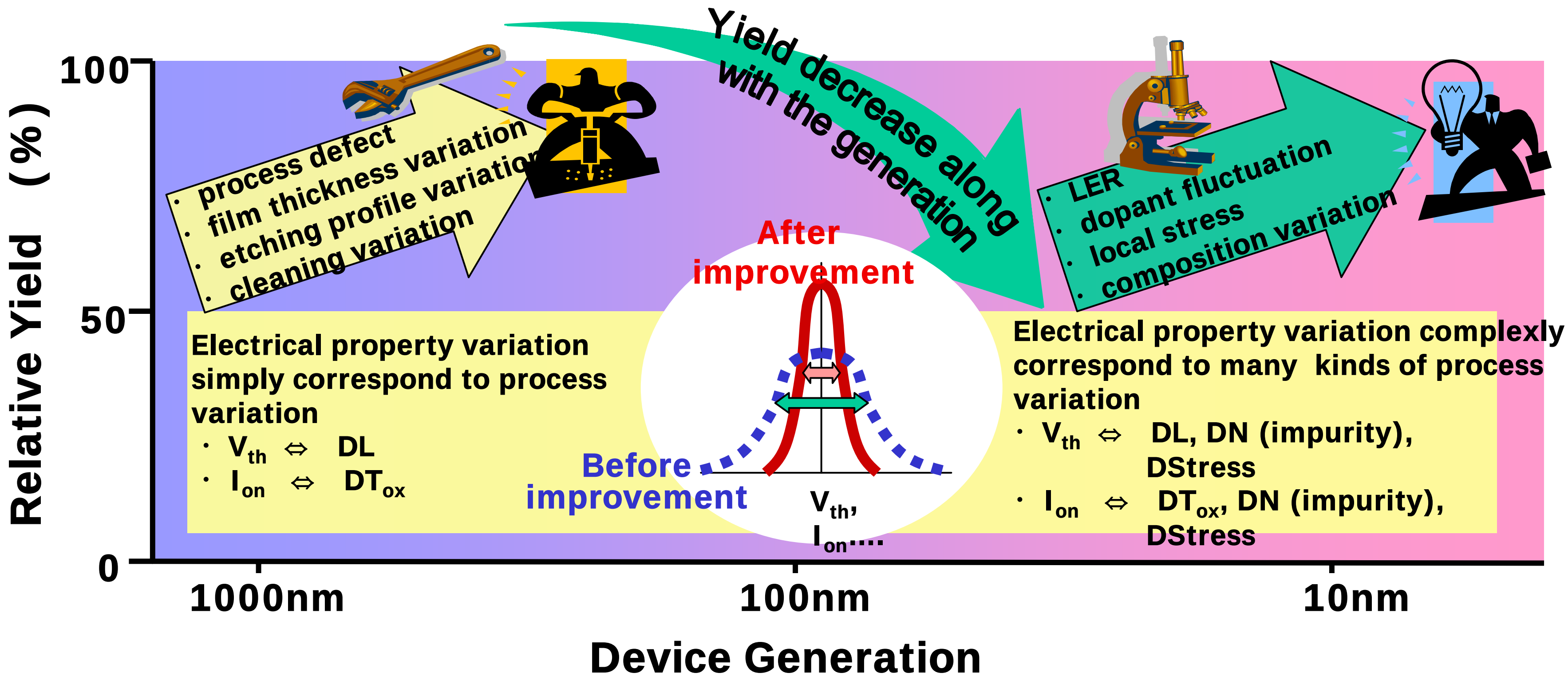
Vth variation of SRAM



SRAM layout



Variability issue in future LSI



>100nm Process generation

Yield improvement strategy

- Process improvement by one-by-one analysis

<100nm Process generation

Yield improvement strategy

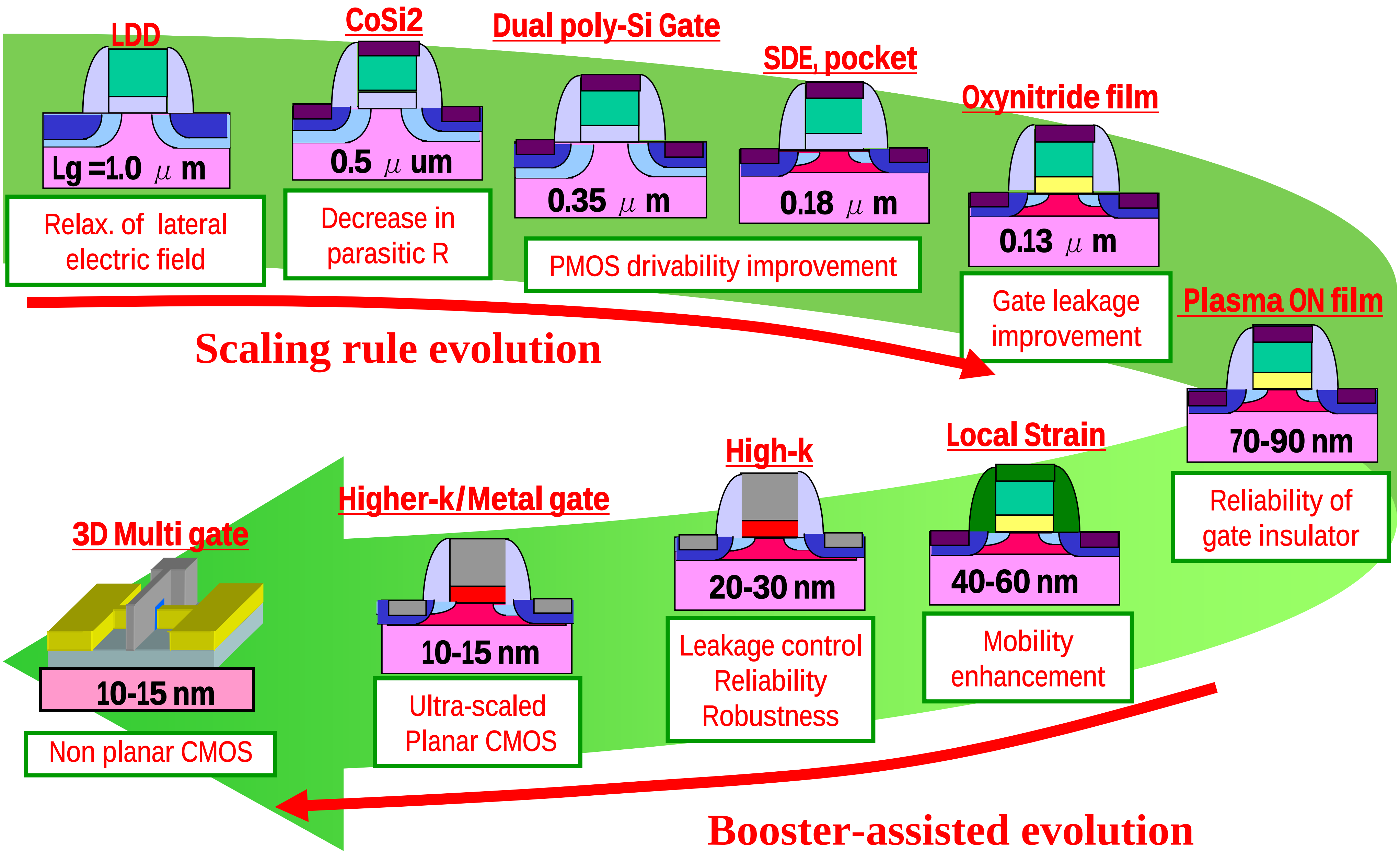
- Device structure improvement
- Circuit design improvement
- Process improvement by analyzing combined reasons

Variability-robust transistors and LSI

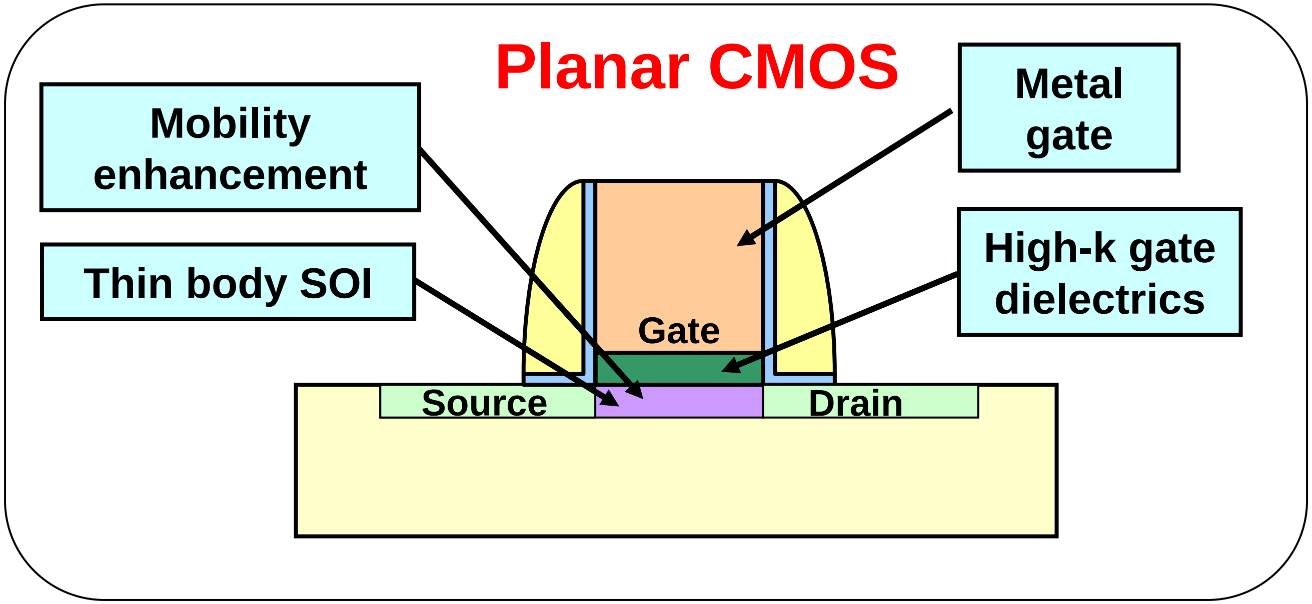
IRAI

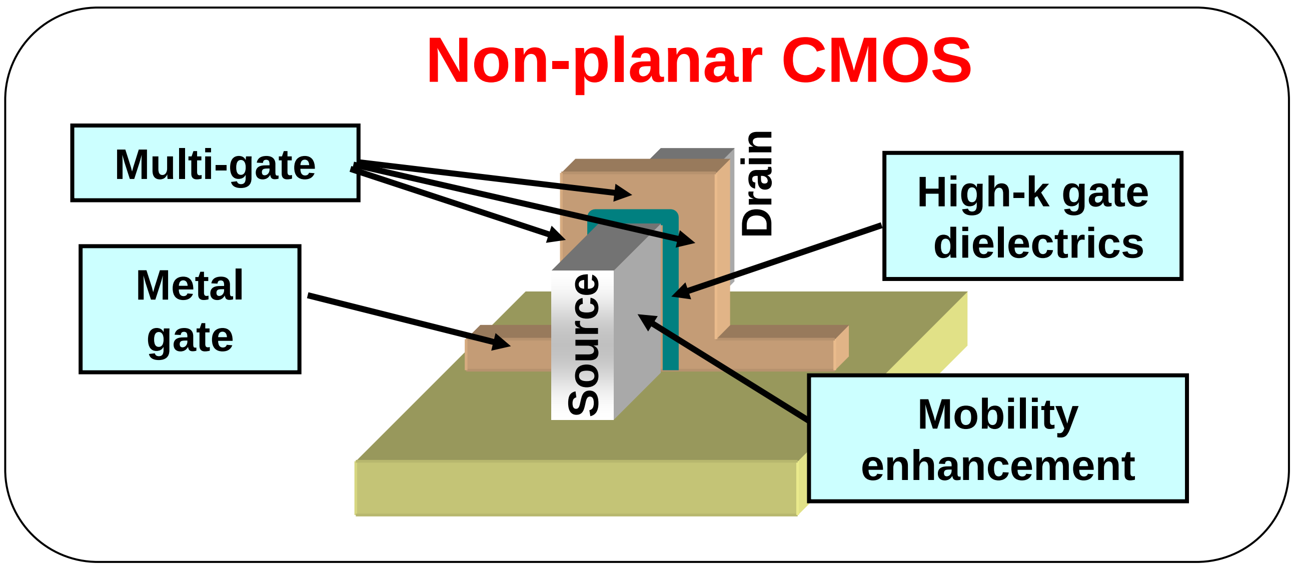
Evolution of CMOS miniaturization

T.Eimori, SFJ2006
Modified by H.W.



CMOS booster technologies

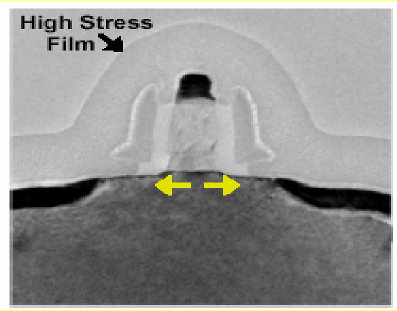


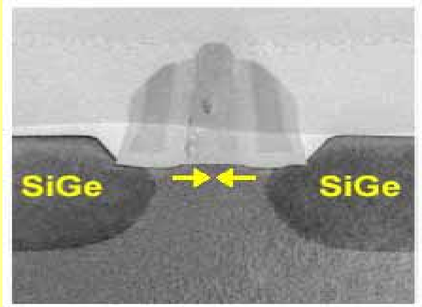


Mobility Enhancement Technologies

Strain Control

SiN Stressor & SD Stress

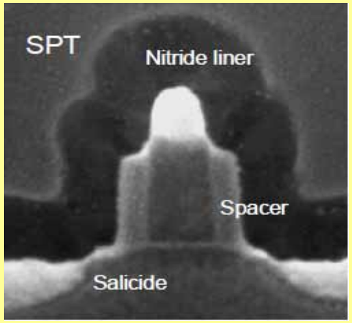




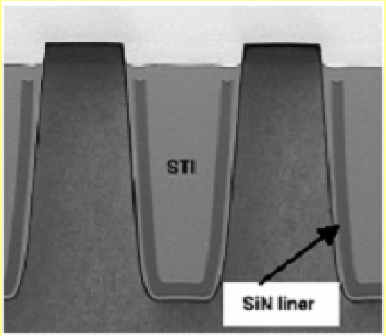
NMOS PMOS

T. Ghani, IEDM' 03

Strained Channel



Si/SiGe Channel

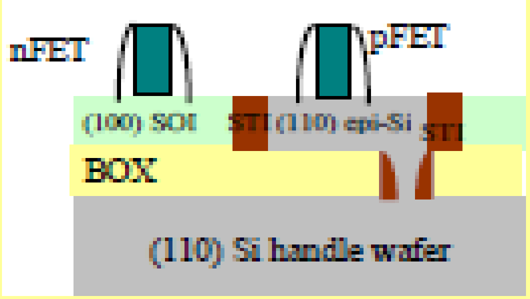


STI Stress

Others

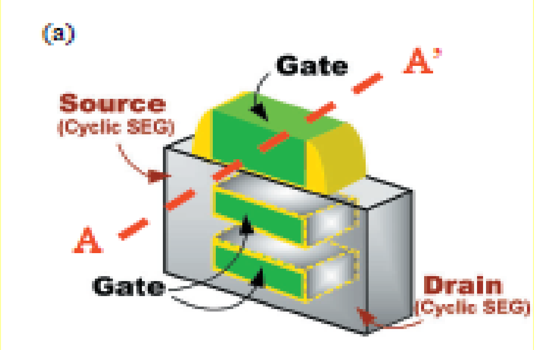
Crystal Orientation

Hybrid Orientation Technology (HOT)



Multi channel

Multi-bridge channel

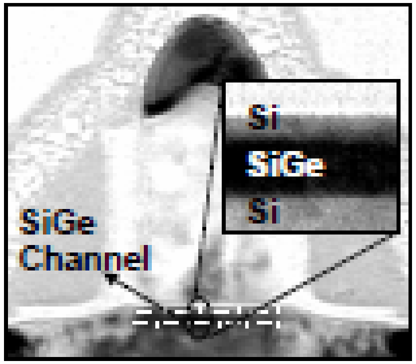


High-μ Materials

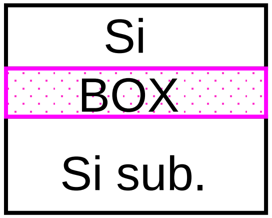
SiGe channel/(110)Si

GOI (Ge on Insulator)

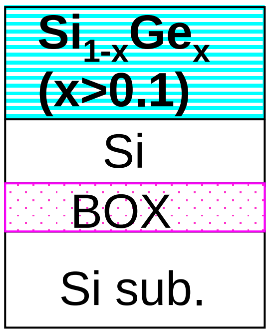
III-V



Formation of strained Si SOI substrate



Commercially available SOI substrate



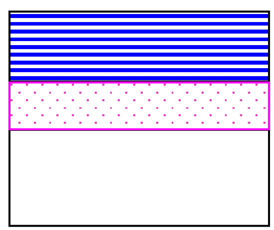
SiGe epitaxial growth

N. Hirashita et al., Proc. SOI conference (2004) p.141

High temperature oxidization

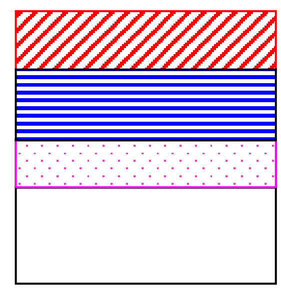
$Si_{1-x}Ge_x$ (x > 0.3)

SiO_2 removal

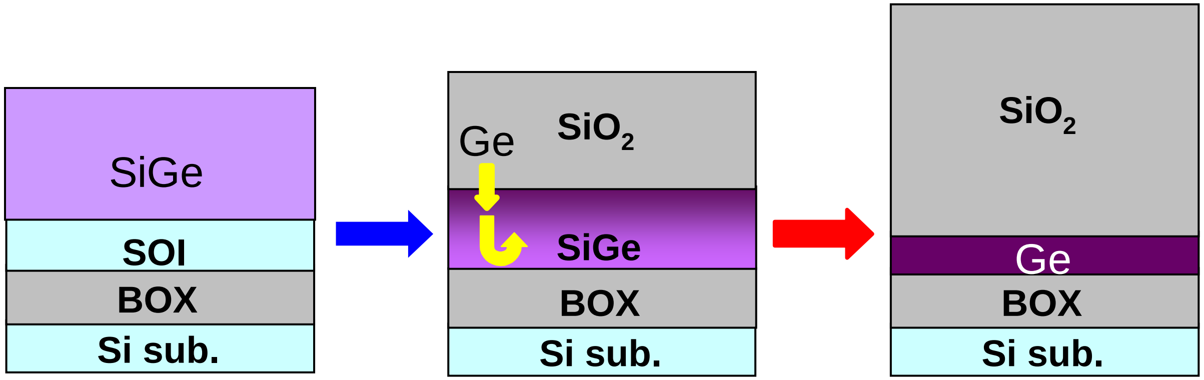


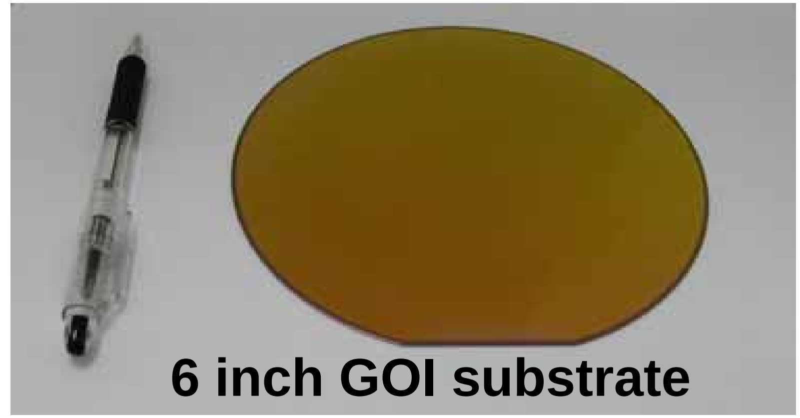
Si epitaxial growth

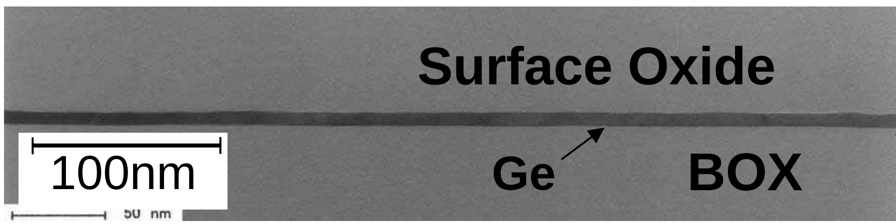
Strained Si

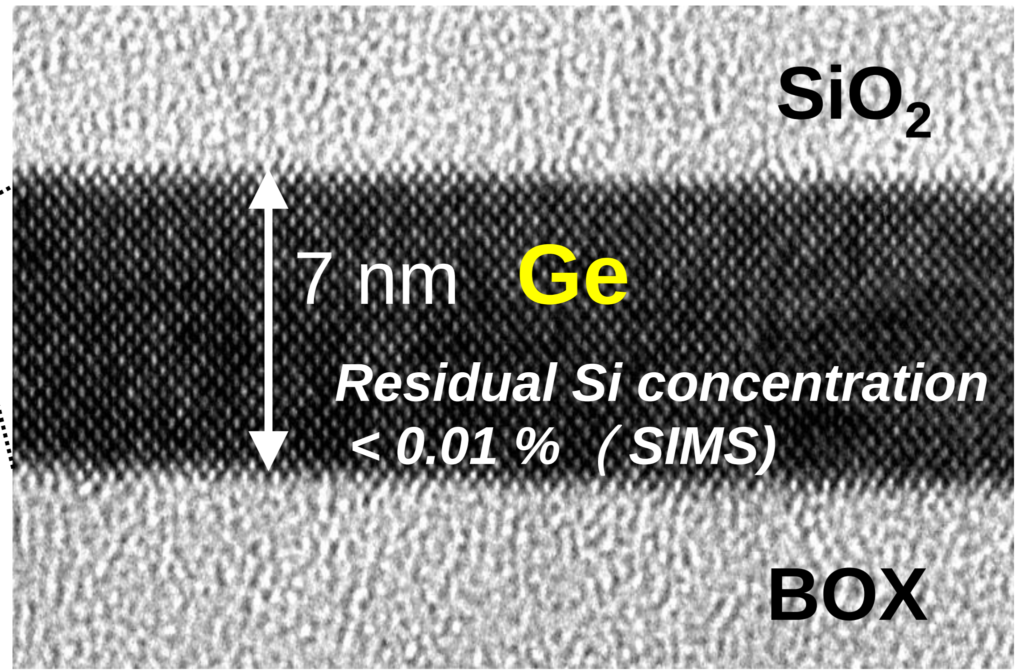


Formation of GOI (Ge-On-Insulator) substrate









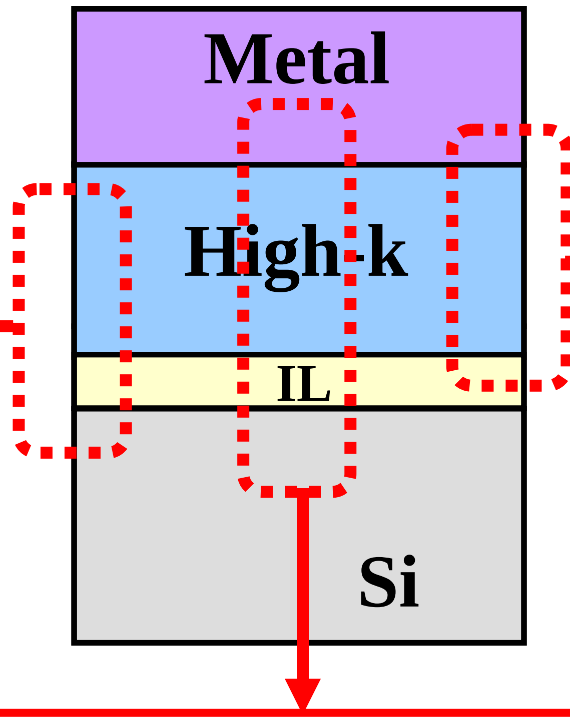
GOI thickness can be controlled in the range of 35nm ~ 2nm by adjusting Ge concentration of initial SiGe epitaxial growth

Gate stack management

Gate stack structure management is dependent on applications (LSI makers)
High performance (HP), Low operation power (LOP) or Low stand-by power (LSTP), with a resultant choice of single-or-dual high-k, single-or-dual metal, on bulk-or-SOI and gate-first or gate-last process

J_g control

- ◆Higher-k
- ◆Less defect
- ◆Interface flatness



V_{th} control

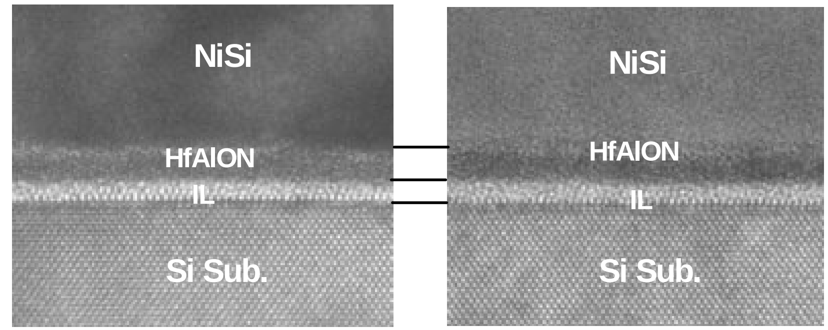
- ◆ WF adjustment (FLP control)
- ◆ Symmetric Vth
- ◆ Interface charge control

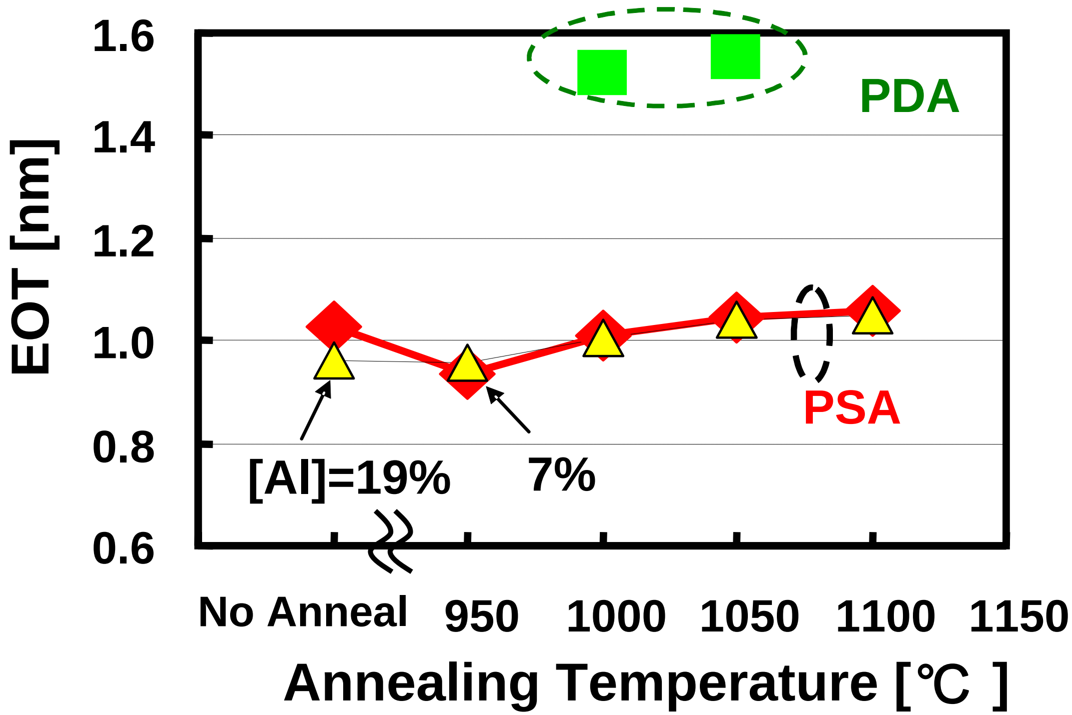
- **High mobility and high reliability are must after total integration process.**

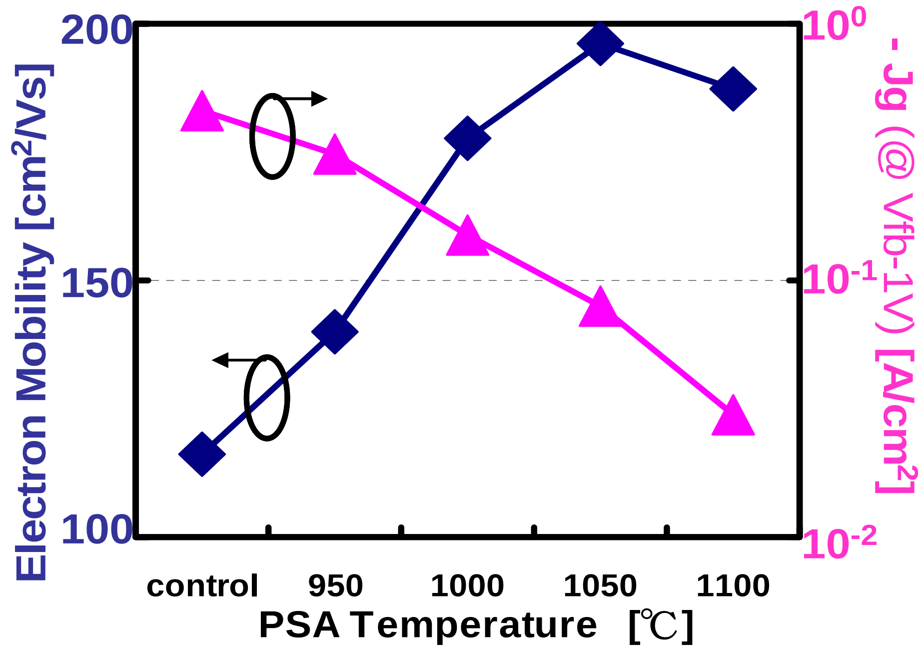
Quality control by annealing process

High-k deposition
PDA
Si deposition
PSA
Matal (Ni) deposition

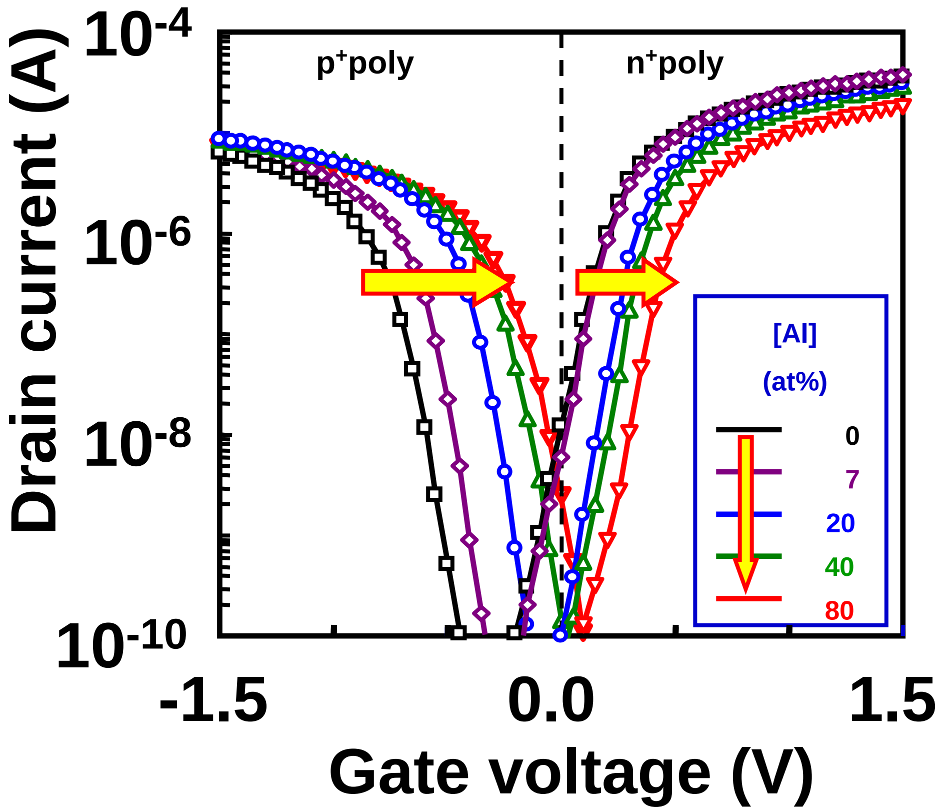
No Anneal | PSA (1050 ℃)



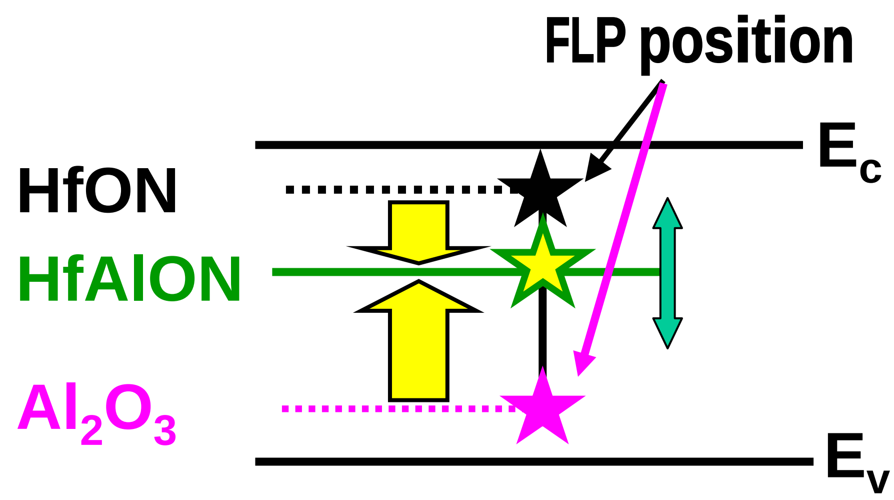




Control of FLP by changing Al content in HfAlON



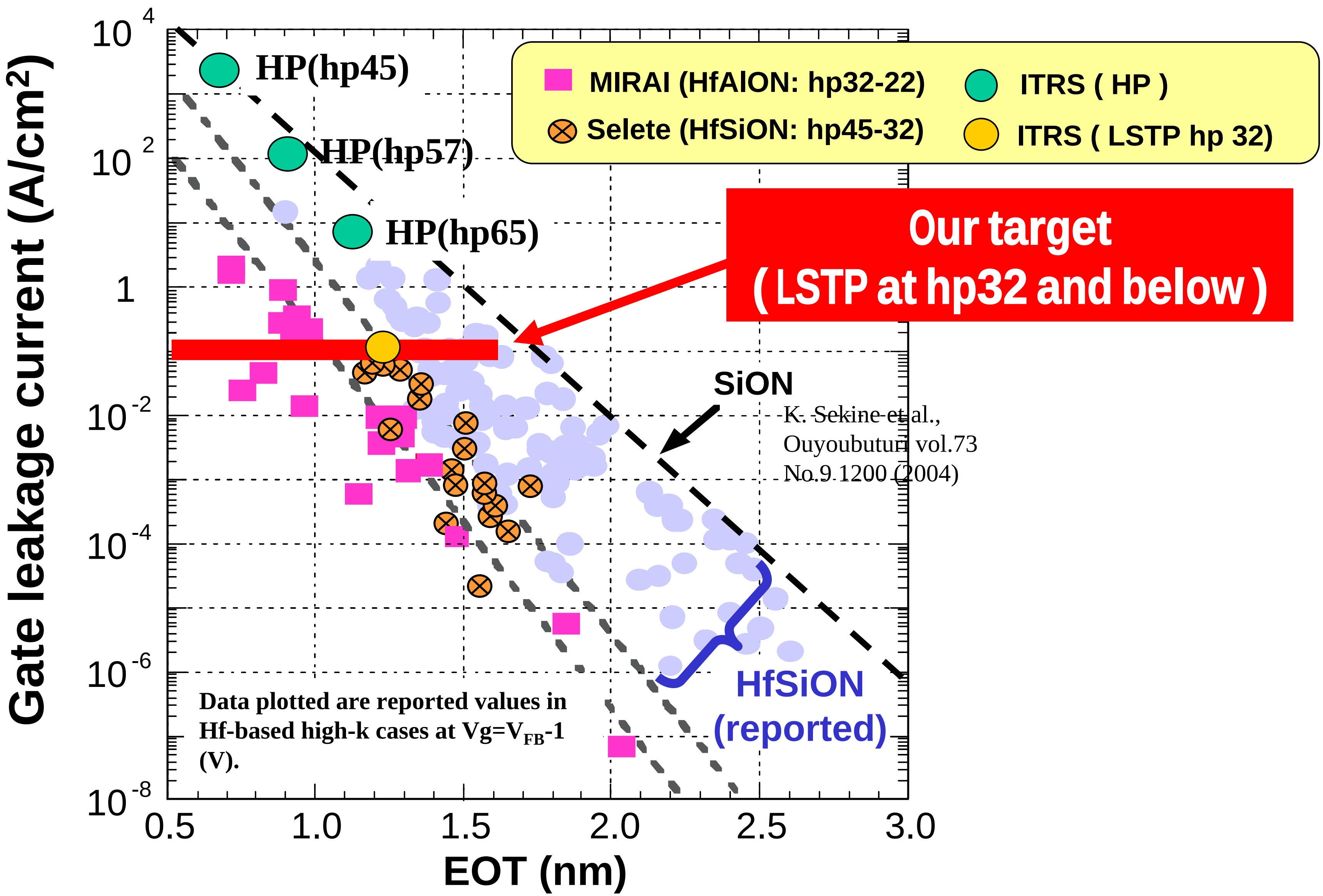
- Symmetric V_{th} can be obtained at [Al] 25 at.% for poly-Si.



HfAlON is an attractive material because it can obtain a symmetric Vth of NMOS and PMOS by controlling Al concentration.

M. Kadoshima et al., VLSI Symp. 2005 p.70

Targets of Hf-based gate stack leakage current



Modified from the figure reported by A. Toriumi et al. (Microelectronic Engineering 80 (2005) 190)

IRAI

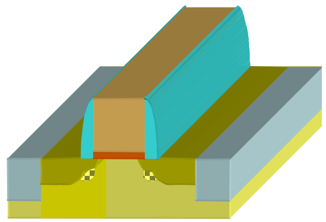
Metal-gate / High-k gate stack management

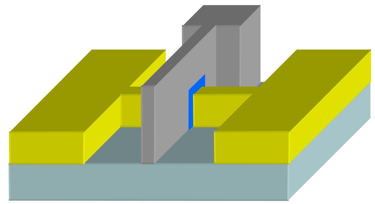
	nMOS	pMOS
Metal (Ω↓)	W, poly-Si	
Metal (Vth↕) (WFM)	TaC, NiSi, HfSi, Ta(Tb, Er, Yb)N, (Ta, Hf, Mo)SiN	Pt, Ru, Re, $PtSi_x$, Ni_3Si, MoN_x, TiSiN, TiCN,
High-k (Dipole charge)	HfLaO; La_2O_3	Al_2O_3,AlN; HfAlO
High-k (Jg↓)	HfLaO; HfSiON, HfO_2 ,HfAlON	HfSiON, HfO_2 ,HfAlON; HfAlO
IL (μ↑)	SiO_2, SiON	
Si (channel)	N I/I; Non I/I	Non I/I; F I/I

◆ All materials and elements shown here are reported at VLSI2005, VLSI2006, IEDM2004 and IEDM2005.

◆ More material combinations are proposed in world-wide patents.

Metrology and characterization by MIRAI project



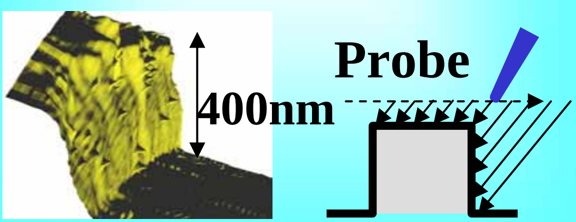


- CD
- Edge roughness
- Strain
- Impurity position

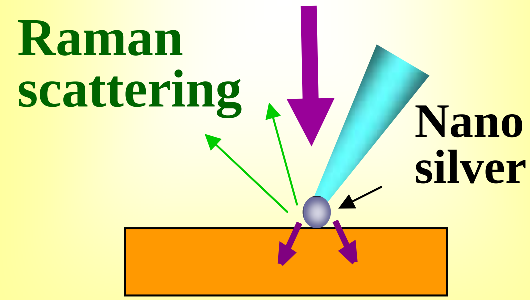
Scanning probe metrology

A detail will be reported at this conference on March 29 pm, by Dr. T. Kanayama of MIRAI project

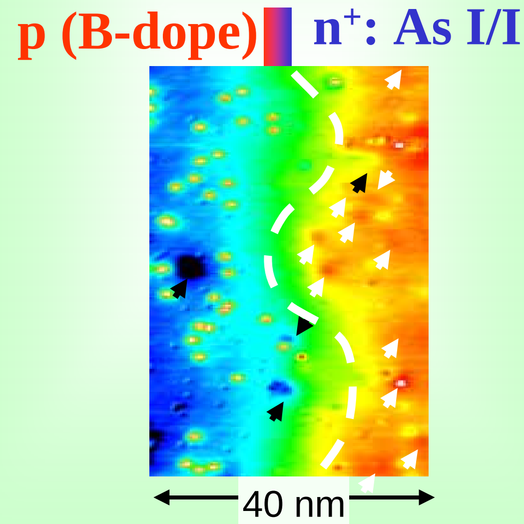
LER 3D measurement by laser interference CD-AFM



Strain distribution measurement by AFM probe near-field Raman scattering

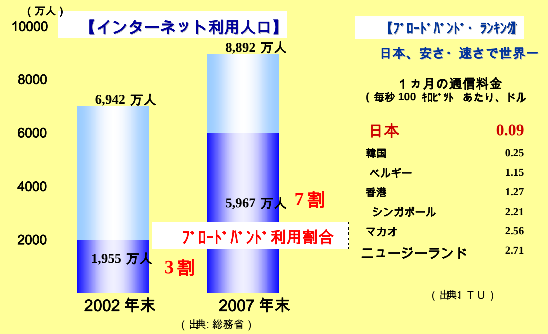


Surface potential and impurity position measurement by STM

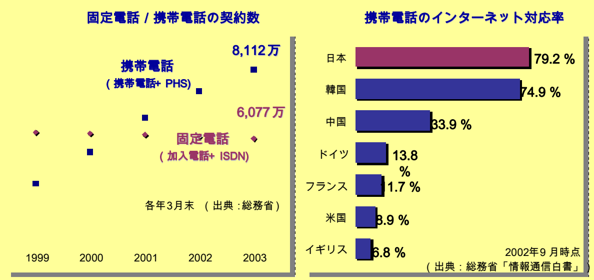


Huge semiconductor applications grown in Japan

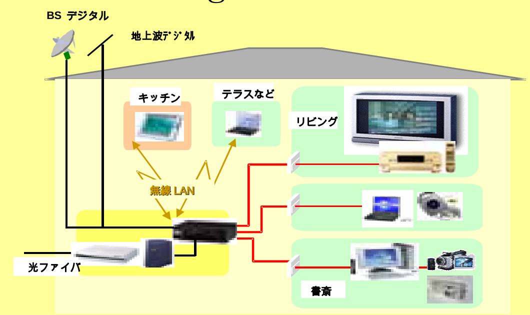
Broadband communication



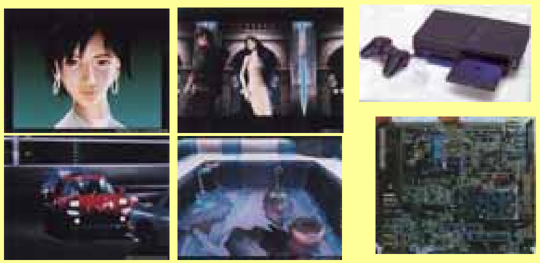
Mobile communication



Digital home



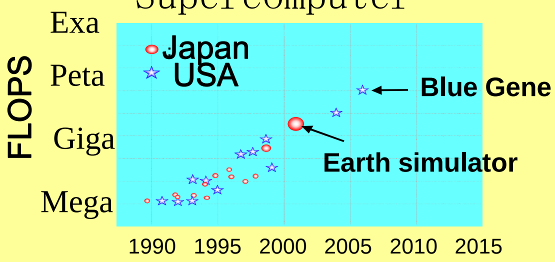
Digital entertainment



Partner Robot

Eco/digital car

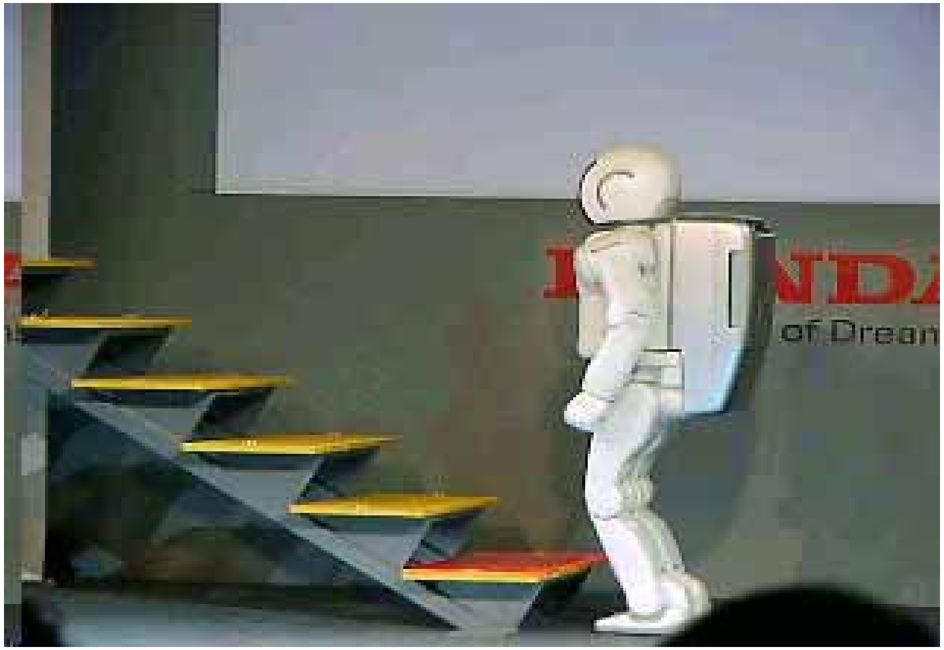
Supercomputer



- ◆ Various semiconductor devices are key components for their performances.
- ◆ Ultra-low power consumption of LSIs is a strong demand in all these applications.

Japan's next semiconductor market ; Partner robot

Honda



AIST

Sony

NEC

- Any kind of next generation semiconductor applications including partner robots or supercomputers needs high performance with extremely low power consumption.
- MIRAI project is focusing on low power CMOS technologies in the nanoelectronics era.

Thank you for your attention !