Semiconductor Research Corporation

PIONEERS IN COLLABORATIVE RESEARCH®

The Semiconductor Industry's Nanoelectronics Research Initiative

NRI

anoelectronics RESEARCH INITIATIVE

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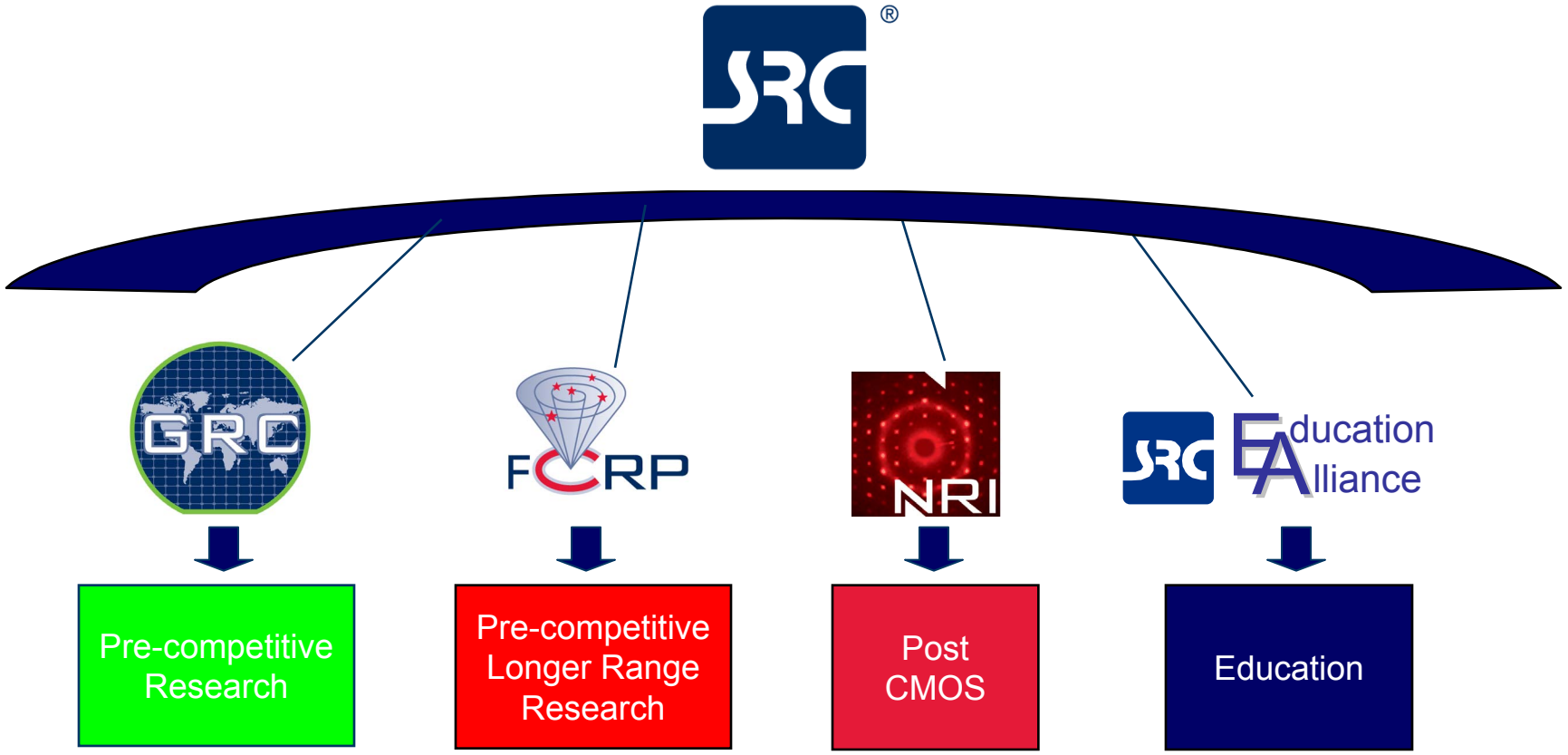
Semiconductor Research Corporation: Collaboratively Sponsored University Research

- Strong university research is critical for continuing rapid pace of technology
  - Research in new concepts, breakthrough ideas and solutions to problems for which no currently known solutions exist
  - Development of talent pool of scientists and engineers
- The Semiconductor Industry Association (SIA) members have recognized that collaboration among industry, government and academia is the most efficient means of advancing university research capabilities
- Semiconductor Research Corporation (SRC) has been established as one of the key initiatives to facilitate collaboratively sponsored university research
- SRC manages a full spectrum of research related to CMOS and beyond CMOS technologies under various program entities

SRC Global Research Collaboration



GRC – Global Research Collaboration

FCRP – Focus Center Research Program

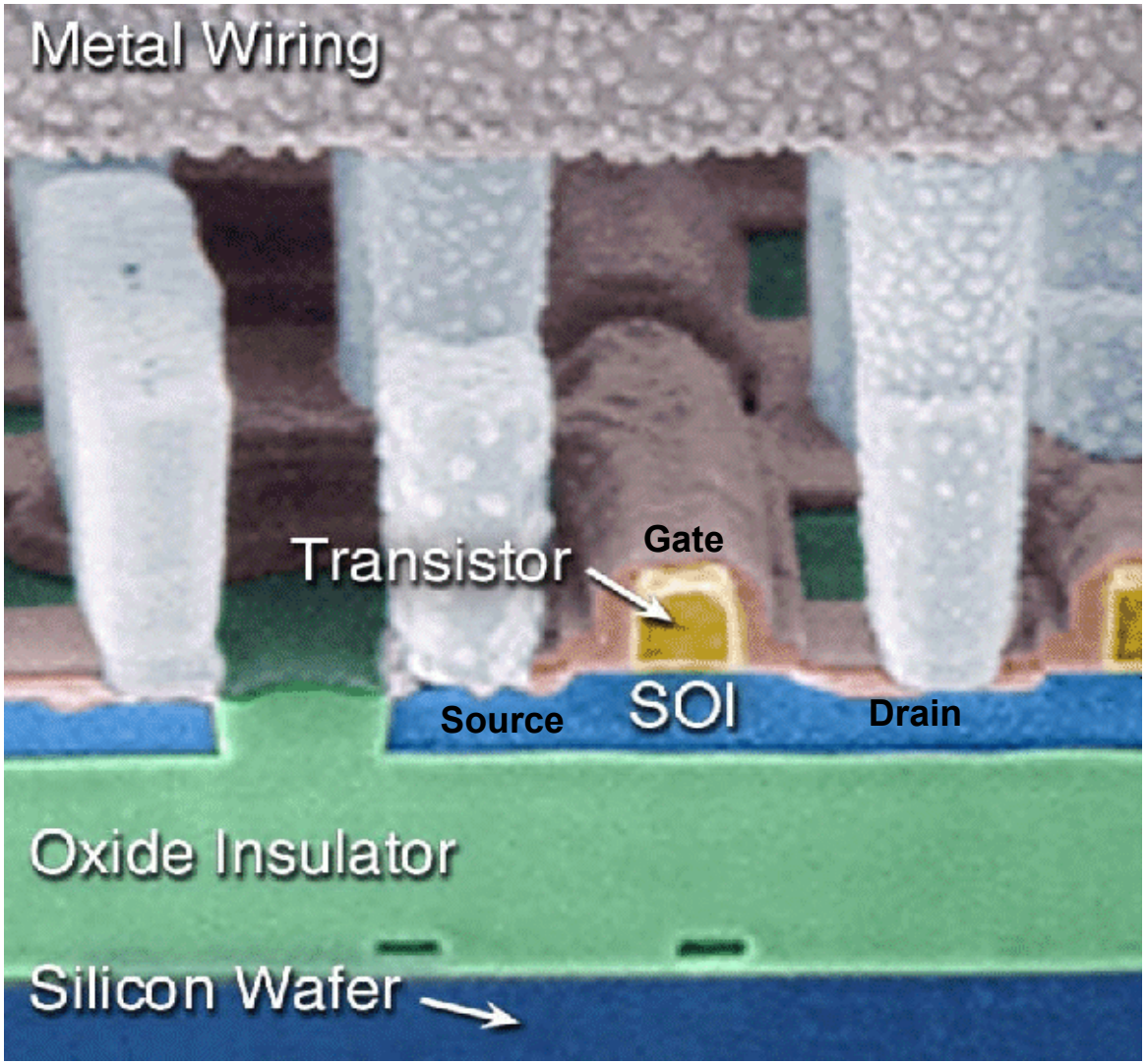
NRI – Nanoelectronics Research Initiative

EA – Education Alliance

SRC: Research Program Differentiators

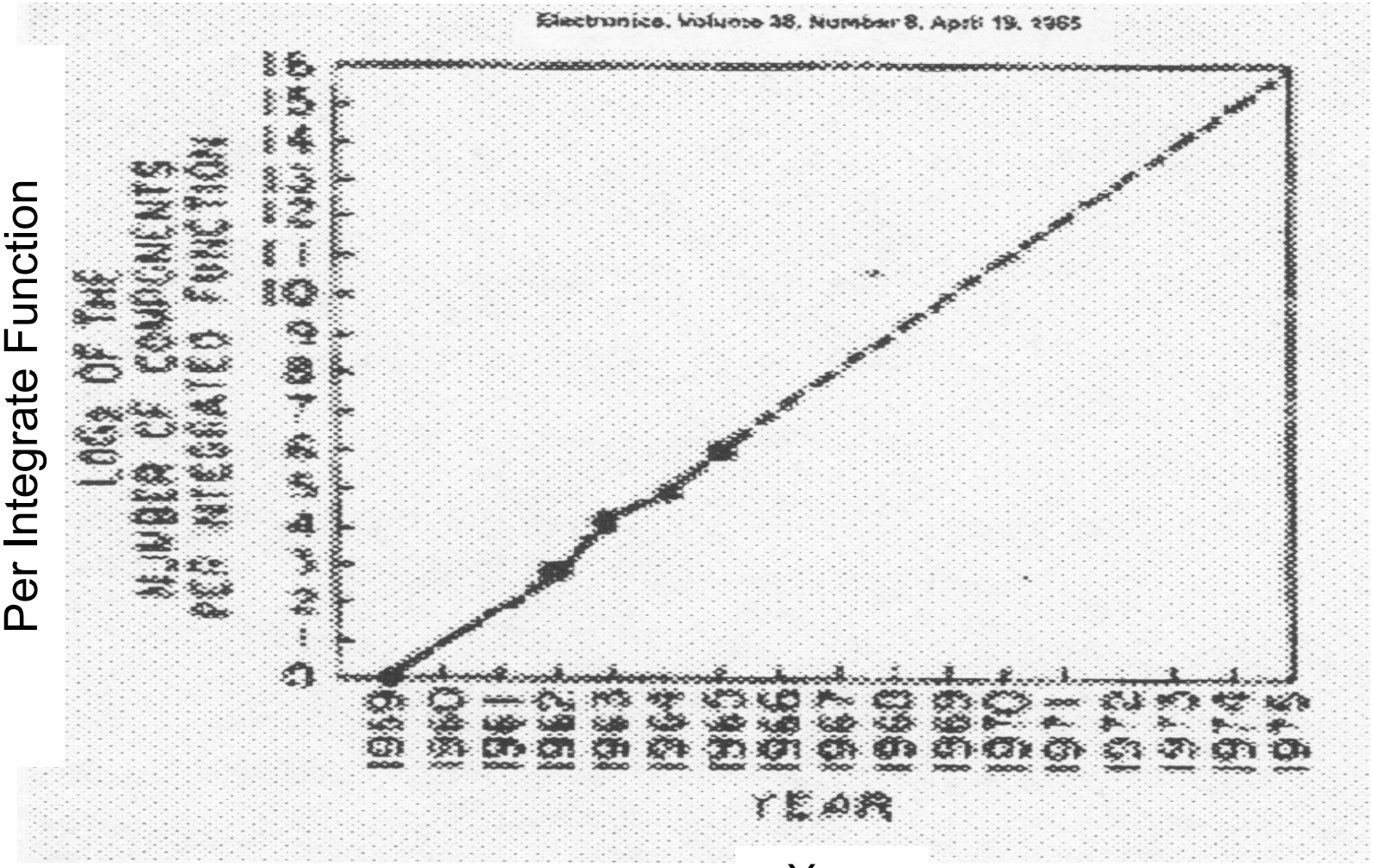
	SRC-GRC	SRC-FCRP	SRC-NRI
Nature of Research	Narrowing options	Creating Options	Next Information Element
Technology Spectrum	CMOS and Scaling Independent Research	CMOS + Hooks to beyond CMOS	Beyond CMOS
Industry Involvement	Strategic and in execution	High level strategic	Influence through highly leveraged co-investment
Government Involvement	Limited; leverage funding	Significant funding; 50:50 with DOD	Major funding – State and federal
University Autonomy	Limited	Significant	Significant
Membership	Global	U. S. only	U. S. only

High Performance Silicon-On-Insulator CMOS

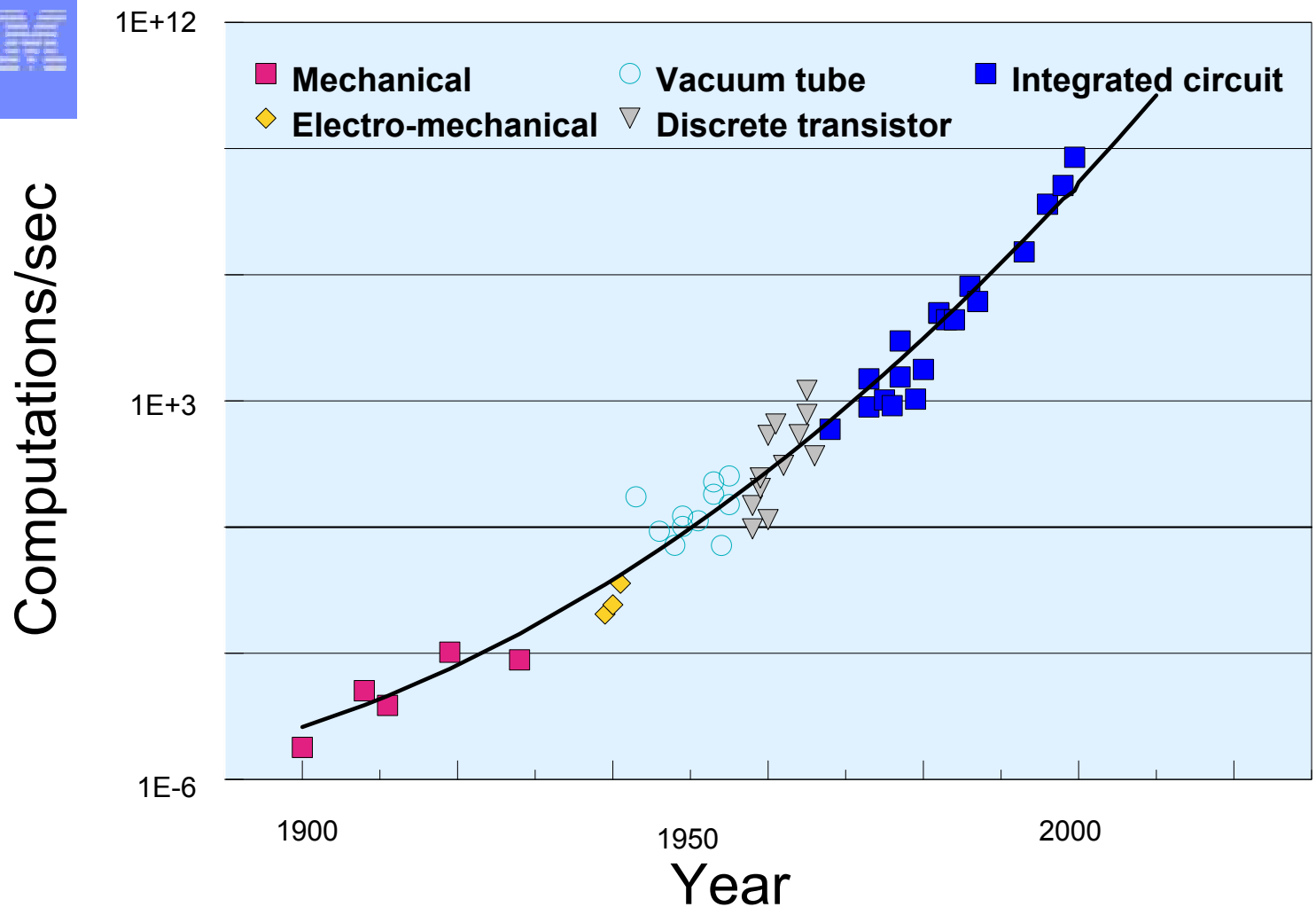


Moore's Law

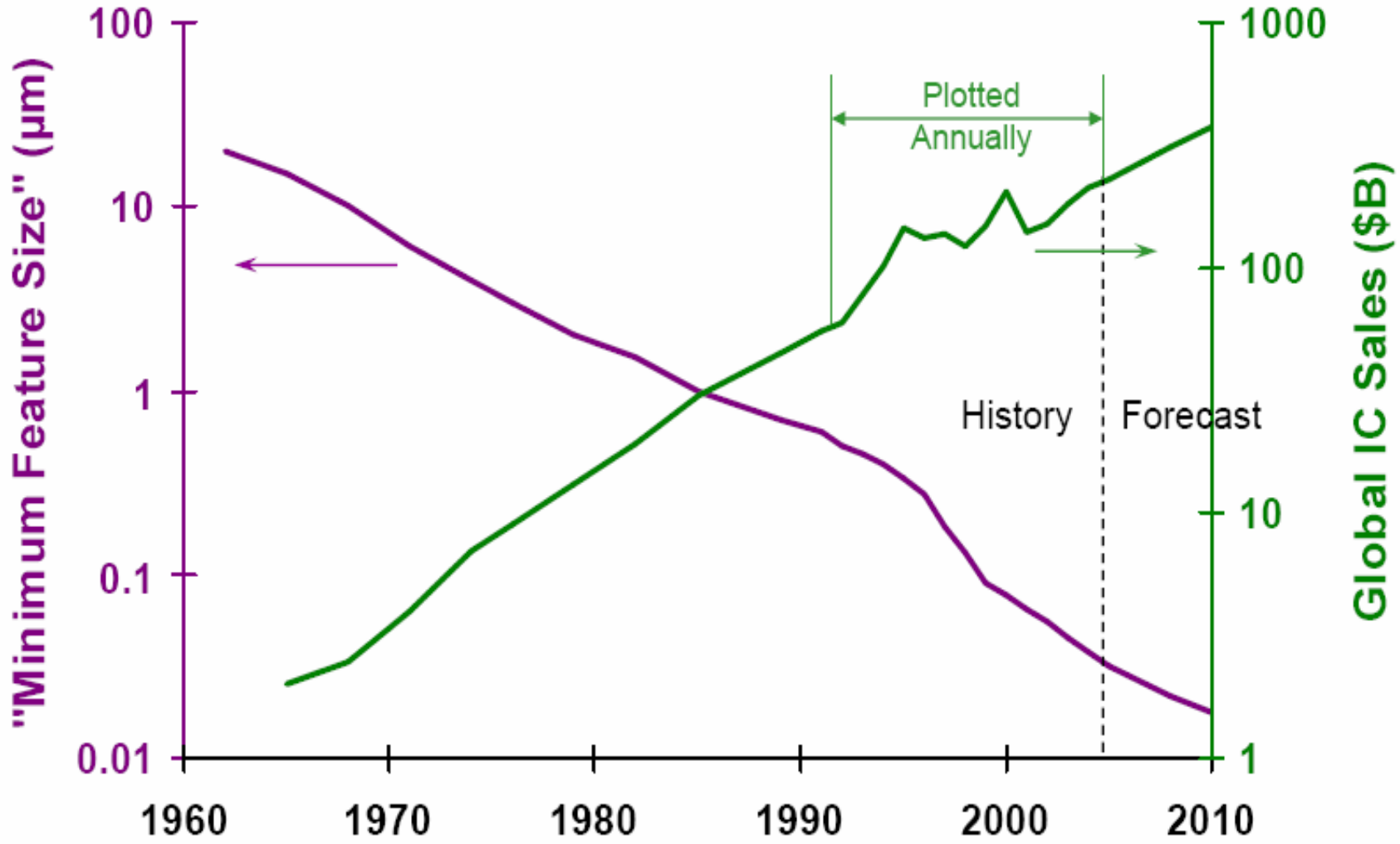
Electronics, Volume 38, Number 8, April 19, 1965



1000 $ Buys


1E+12
1E+3
1E-6
Computations/sec
Mechanical
Electro-mechanical
Vacuum tube
Discrete transistor
Integrated circuit
1900
1950
2000
Year

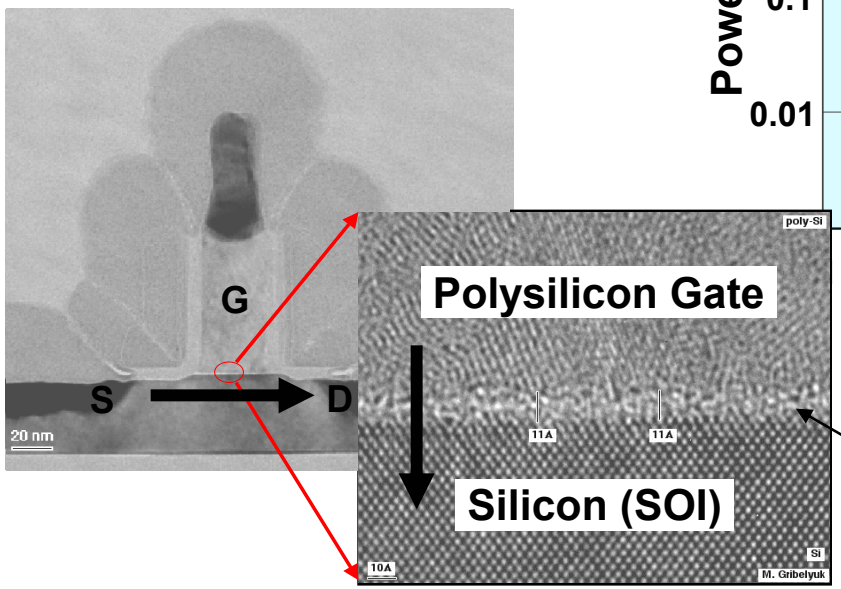
Scaling = Progress in Electronics

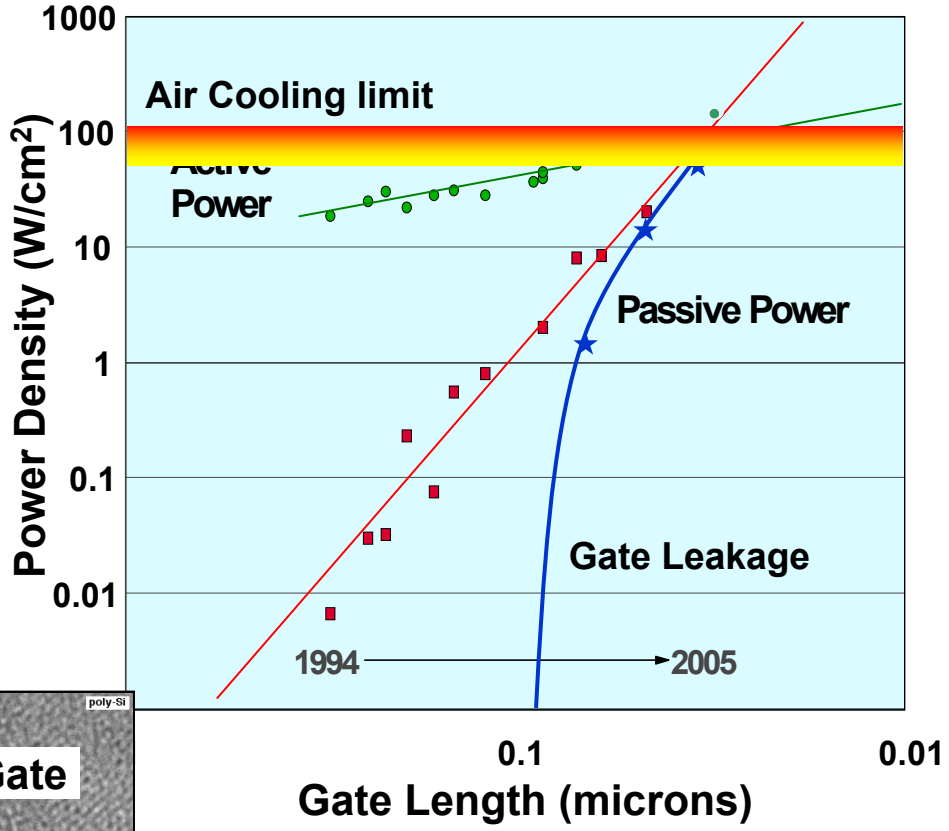


Smaller features → Better performance & cost/function
→ More apps → Larger market

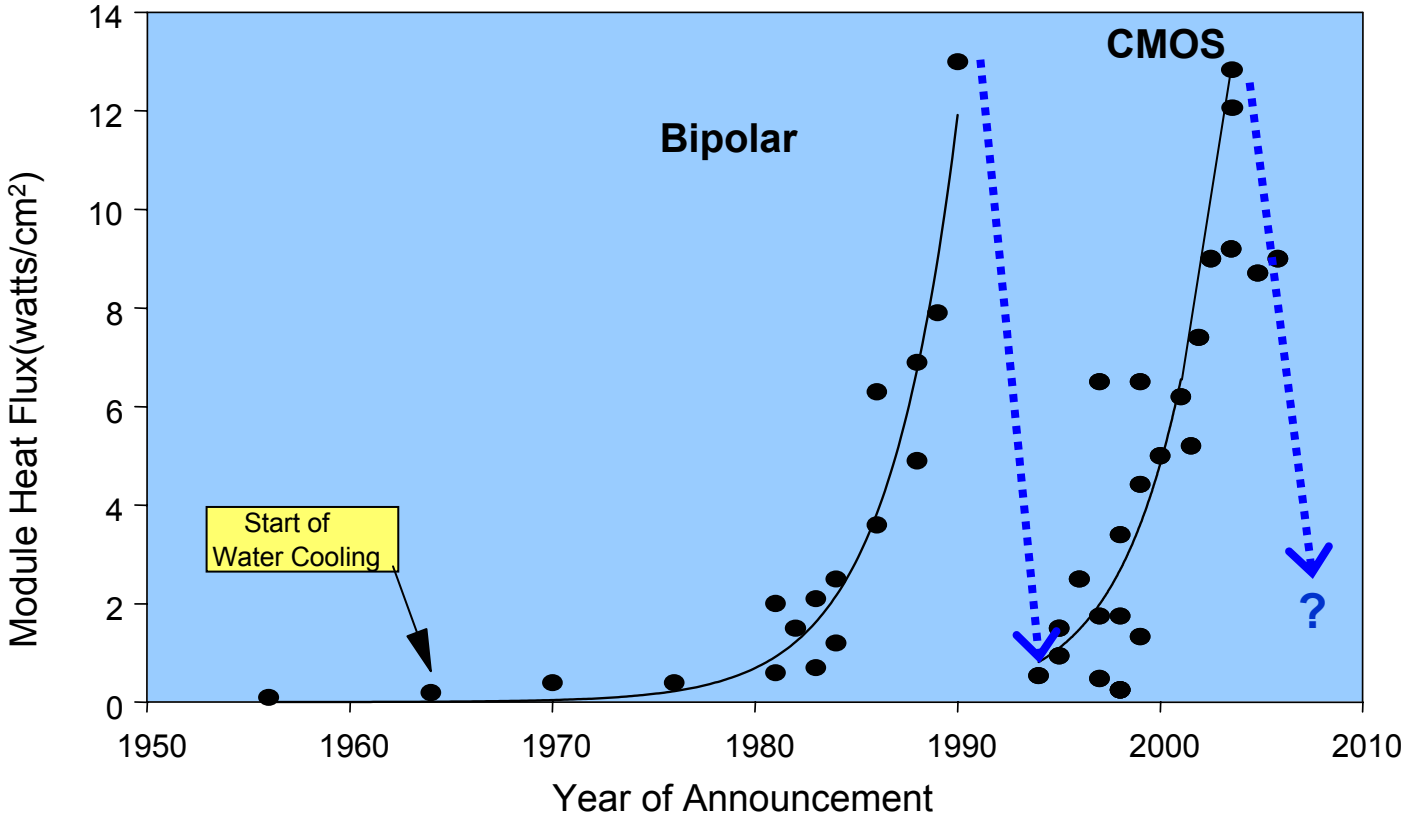
CMOS Power Issue: Active vs. Passive Power

- Power components:
  - Active power
  - Passive power
    - Gate leakage
    - Source - Drain leakage





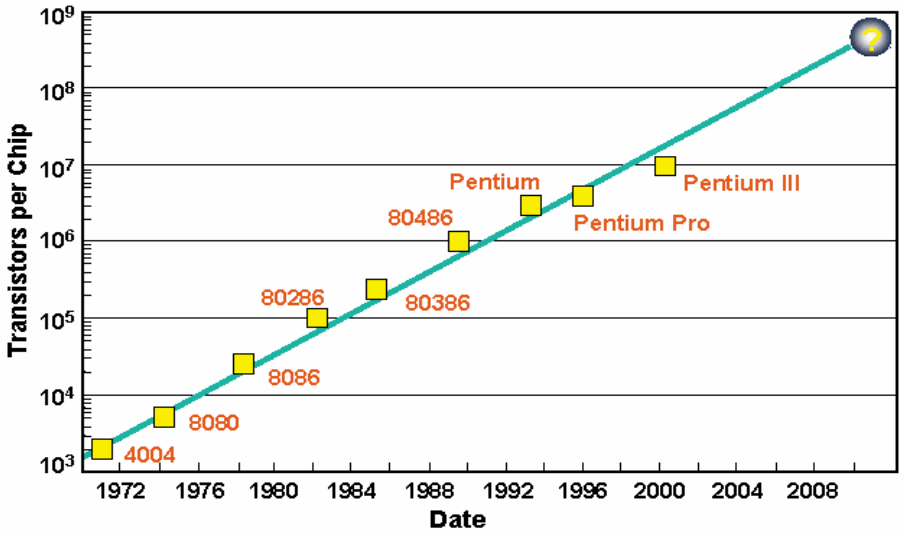
Has This Ever Happened Before?



2005 ~ 2015: New utilization of technology

> 2015?: New technology

Moore's Law: Transistors per chip



Source: Stan Williams, Hewlett Packard

What is the ultimate number of binary transitions per second in a 1cm^2 chip area?

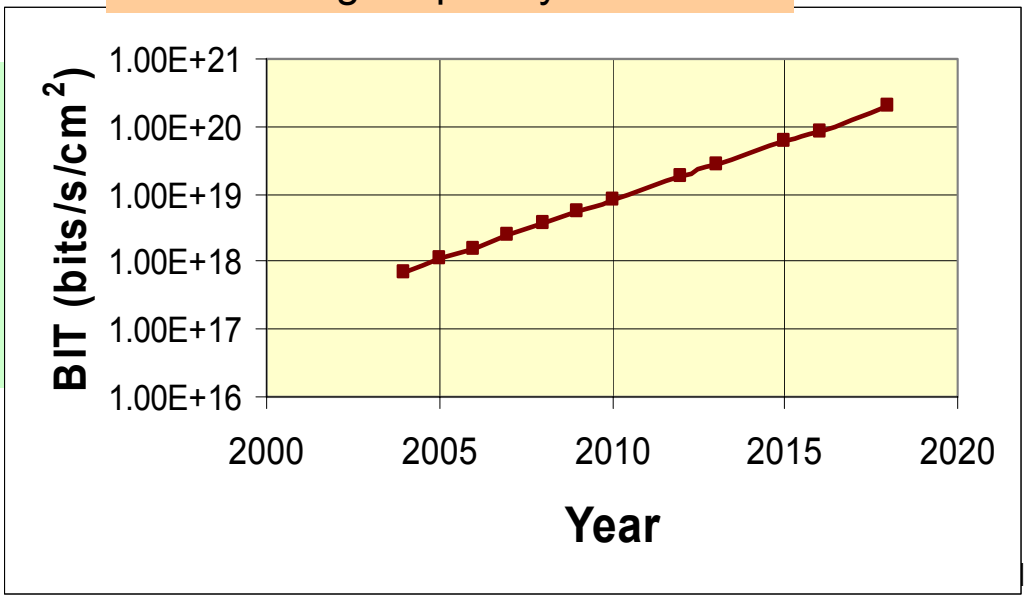
$$BIT = n_{bit} f$$

- a measure of computational capability on device level

n_{bit} – the number of binary states

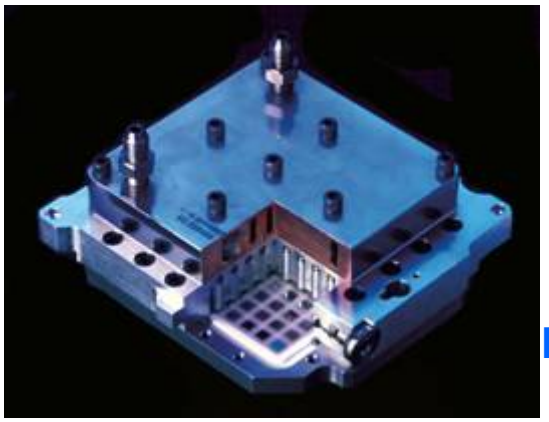
f – switching frequency

Why scaling? – To increase the *Binary Information Throughput* (BIT)



Key Systems Transitions

Bipolar
Frequency

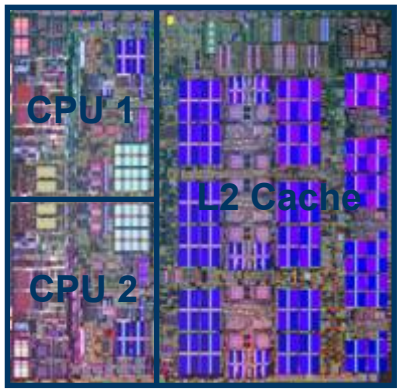


Multi-Chip Module (MCM)

1980's

Cost
Power

CMOS
Frequency & density

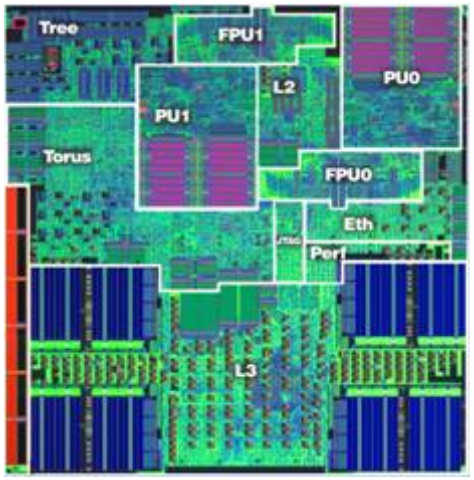


Power 5

1990's – 2000's

Cost
Power

CMOS SoC
Integration & density



Blue Gene L

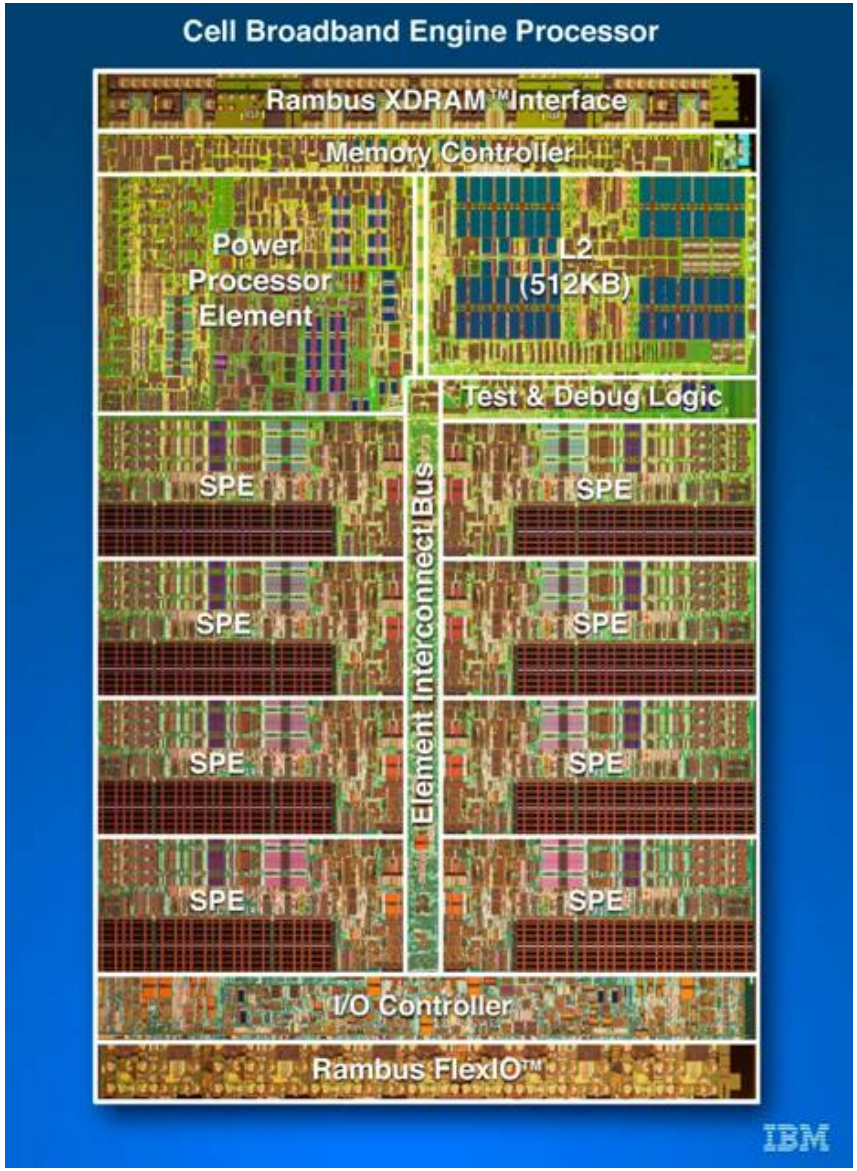
- Multi-core microprocessor, ASIC library, design tools

2004 & Beyond

(Note: Figures not to scale)

Cell Processor

- ~250M transistors
- ~235mm2
- Top frequency >4GHz
- 9 cores, 10 threads
- > 256 GFlops (SP) @4GHz
- > 26 GFlops (DP) @4GHz
- Up to 25.6GB/s memory B/W
- Up to 75 GB/s I/O B/W
- Large design investment (time & money)



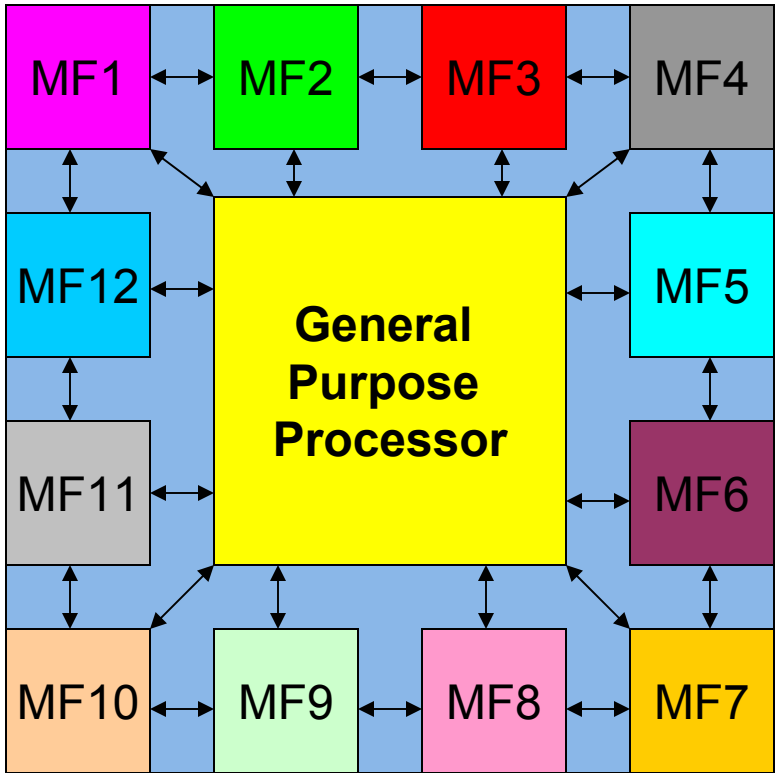
Heterogeneous Multi-Core Architectures

A possible ultimate evolution of **on-chip** architectures is Asynchronous ***Heterogeneous*** Multi-Core with Flexible Processors Organization

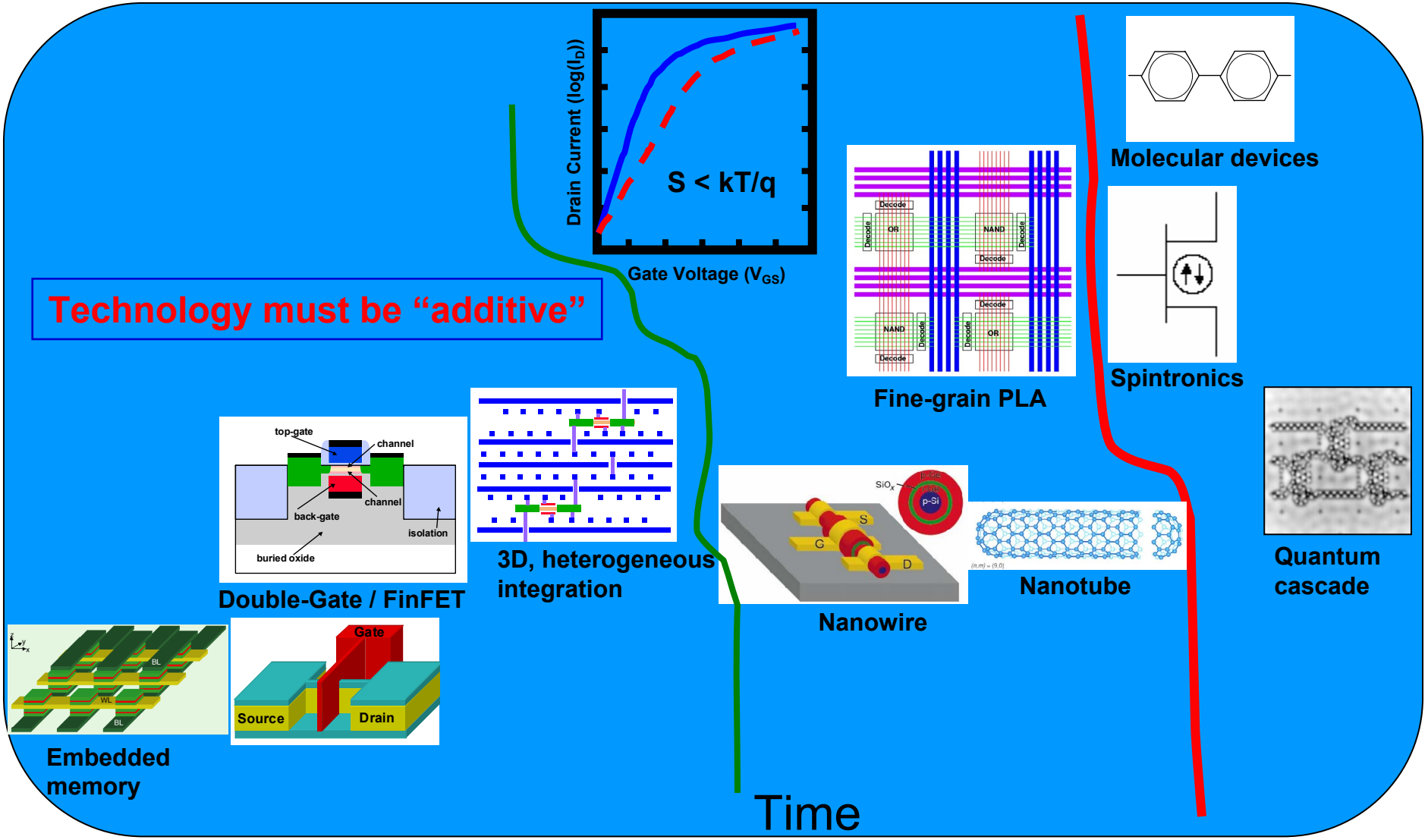
- General-purpose CMOS CPU
- Several application-specific processors/systems
  - May be CMOS hybrids and/or
  - Operate in multiple physical domain

Key Challenge: Software

MF(n) – application-specific processor implementing a specific macro-function (*may need specialized devices)*



What about a New Device?



2005 ITRS Risk Assessment of Potential Future Memory Devices

Table 64 Performance Evaluation for Emerging Research Memory Device Technologies (Potential)

Memory Device Technologies (Potential)	Scalability [A]	Performance [B]	Energy Efficiency [C]	OFF/ON "1"/"0" Ratio [D1]	Operational Reliability [E]	Operate Temp [F] ***	CMOS Technological Compatibility [G] **	CMOS Architectural Compatibility [H] *
Nano Floating Gate Memory	2.5	2.5	2.5	2.5	2.2	2.7	2.7	3.0
Engineered Tunnel Barrier Memory	2.2	2.3	2.3	2.3	2.4	2.8	2.8	3.0
Ferroelectric FET Memory	1.9	2.3	2.5	2.2	2.0	3.0	2.6	3.0
Insulator Resistance Change Memory	2.5	2.5	2.0	2.2	1.9	2.8	2.6	2.8
Polymer Memory	2.1	1.5	2.3	2.2	1.6	2.9	2.3	2.5
Molecular Memory	2.3	1.5	2.4	1.6	1.4	2.6	1.9	2.3

2005 ITRS Risk Assessment of Potential Future Logic Devices

Logic Device Technologies (Potential)	Scalability [A]	Performance [B]	Energy Efficiency [C]	Gain [D2]	Operational Reliability [E]	Room Temp Operation [F] ***	CMOS Technological Compatibility [G]**	CMOS Architectural Compatibility [H]*
1D Structures (CNTs & NWs)	2.4	2.5	2.3	2.3	2.1	2.8	2.3	2.8
Resonant Tunneling Devices	1.5	2.2	2.1	1.7	1.7	2.5	2.0	2.0
SETs	1.9	1.5	2.6	1.4	1.2	1.9	2.1	2.1
Molecular Devices	1.6	1.8	2.2	1.5	1.6	2.3	1.7	1.8
Ferromagnetic Devices	1.4	1.3	1.9	1.5	2.0	2.5	1.7	1.7
Spin Transistor	2.2	1.3	2.4	1.2	1.2	2.4	1.5	1.7

> 20	>16 - 18
>18 - 20	≤ 16

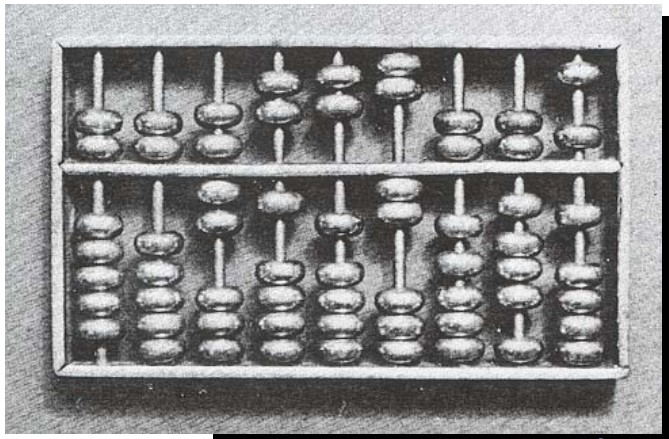
For each Technology Entry (e.g. 1D Structures, sum horizontally over the 8 Criteria
Max Sum = 24
Min Sum = 8

For a new technology, it must either . . .

- Reduce power density
  - Smaller size, more current alone don't help
  - Better sub-Vt slope, better Ion/Ioff, lower leakage do
- Control variability
  - Dopant placement, gate length variation, S0I / oxide thickness variation
- Reduce parasitics
  - Capacitance, resistance
  - New wiring would be great!
- Offer potential for continued scaling
- (Change atomic size limits, elementary charge value, speed of light, etc.)

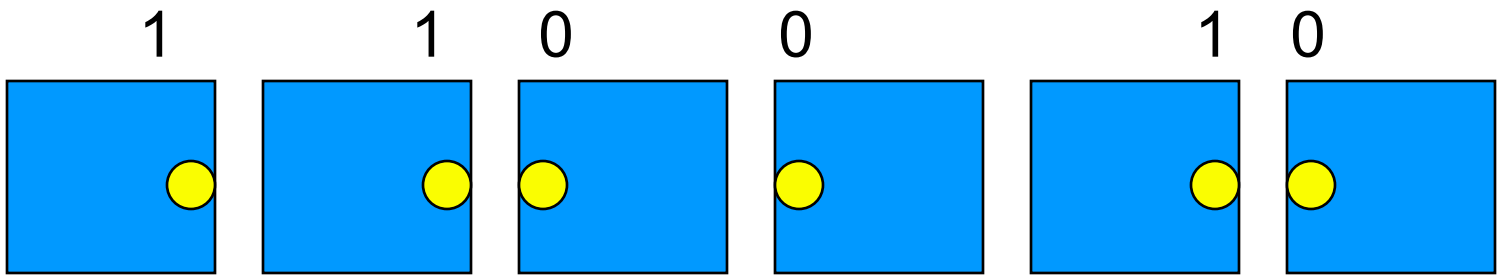
. . . Or it doesn't solve the problem!

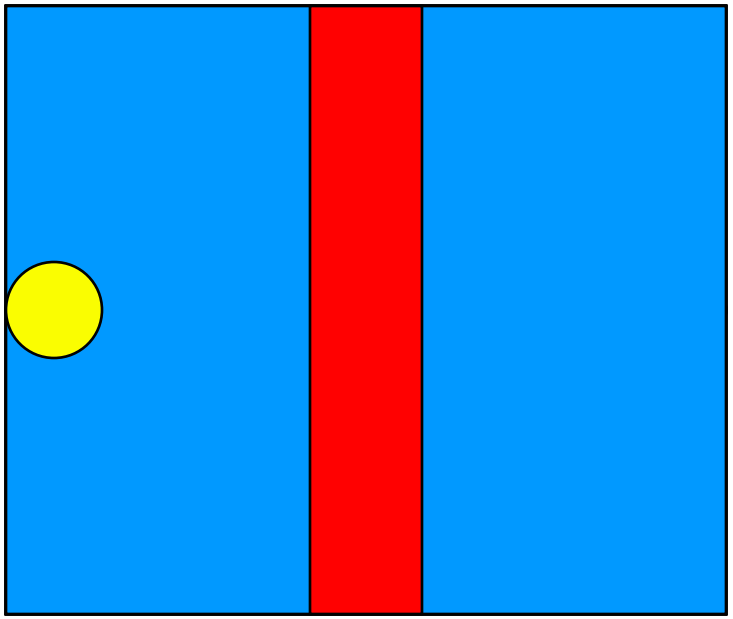
What is Information?



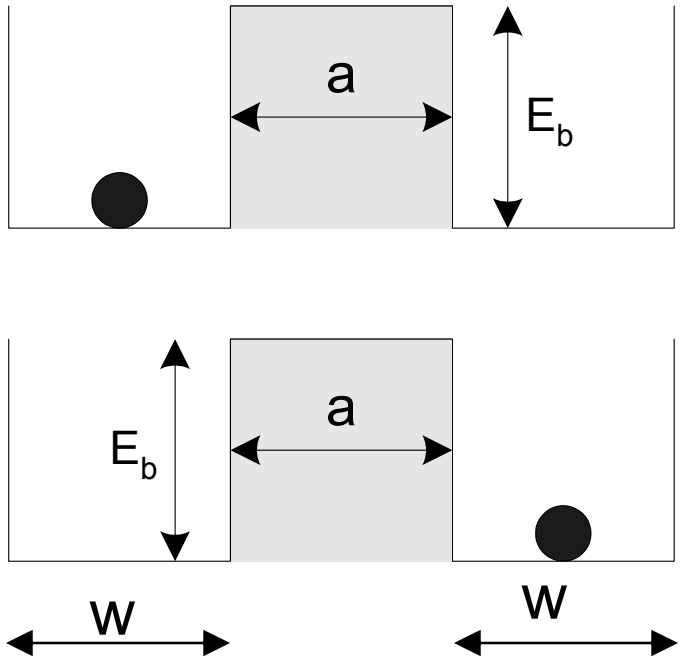
Information is measure of distinguishability manifested in physical form

Particle Location is an Indicator of State

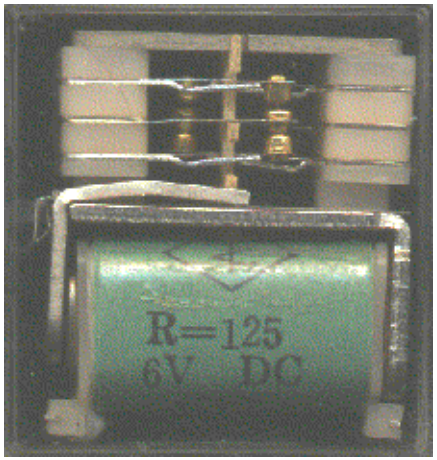


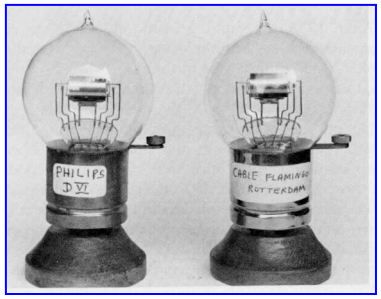


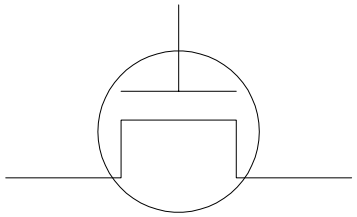
Two-well bit

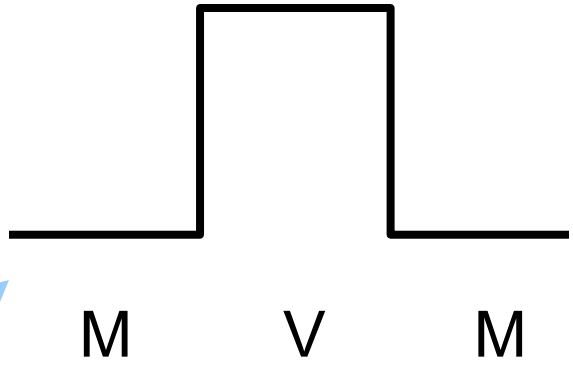


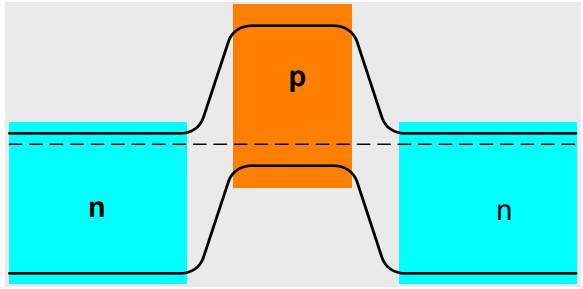
Electronic switches can be of different nature, but they all have similar fundamentals

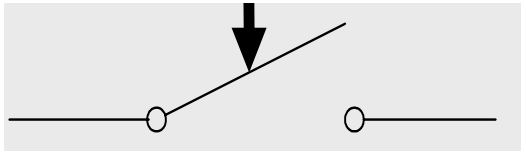


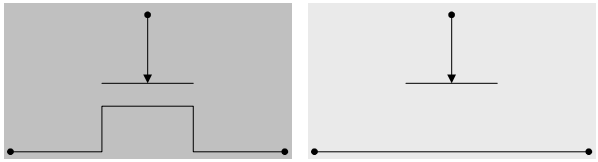




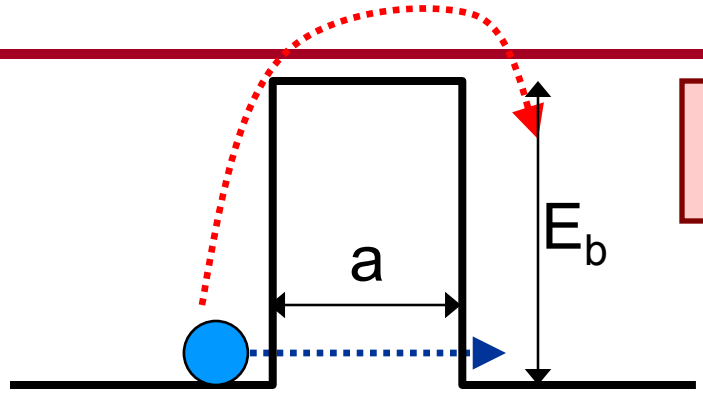




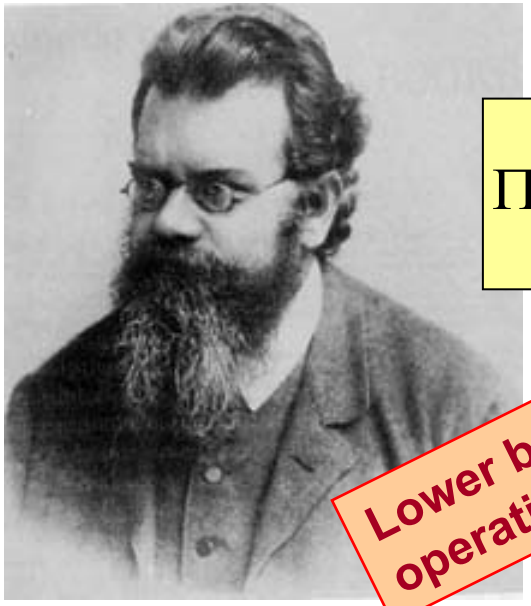




Basic Equations of Two-well Bit



What are the requirements/limitations on the height and width the barrier?



$$\Pi_B = \exp\left(-\frac{E_b}{k_B T}\right)$$

Lower bound on operation energy

"Boltzmann constraint" on minimum barrier height

$$\Delta x \Delta p \geq \hbar/2$$

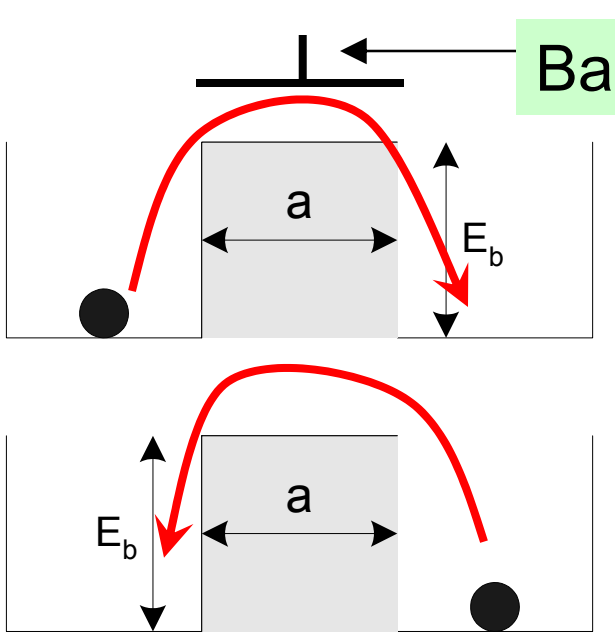
$$\Delta E \Delta t \geq h/2$$

Lower bound on device size

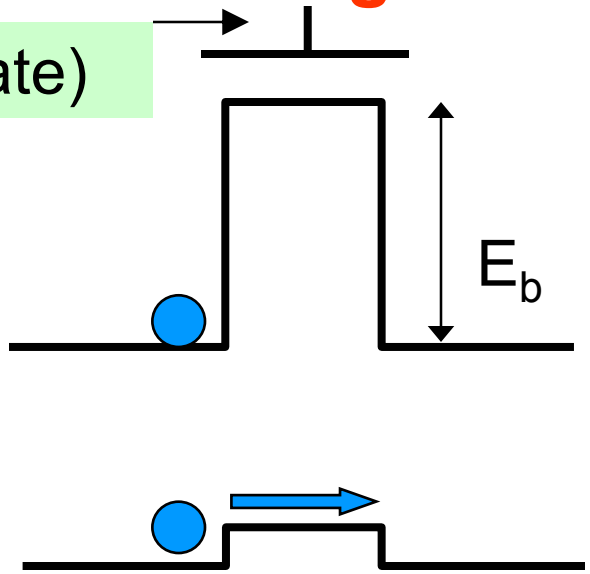
"Heisenberg constraints" on minimum barrier width

Classic Distinguishability:
The Boltzmann constraint

How small could the energy barrier height be ?



OR



$$E_{bit}^{\min} = E_b$$

Distinguishability requirement: The probability of spontaneous transitions(errors) Π_{error}<0.5 (50%)

Energy to "deform" the barrier

$$\Pi_{error} = \exp(\frac{E_b}{k_B T})$$

$$0.5 = \exp(-\frac{E_b}{k_B T})$$

$$E_b^{\min} = k_B T \ln 2$$

Size and Time: The Heisenberg Constraint

$$\Delta x \Delta p \geq \hbar$$

$$\Delta E \Delta t \geq \hbar$$

$$E_b = kT\ln 2$$

$$a_{crit} \sim \frac{\hbar}{\sqrt{2mE_b}}$$

$$t_{\min} \sim \frac{\hbar}{E_b}$$

At this size, tunneling will destroy the state

Minimal time of dynamical evolution of a physical system

N. Margolus and L. B. Levitin, Physica D 120 (1998) 188

Summarizing, what we have learned so far from fundamental physics

1) Minimum energy per binary transition → Boltzmann

$$E_{bit}^{\min} = k_B T \ln 2$$

---

2) Minimum distance between two distinguishable states

$$\Delta x \Delta p \geq \hbar$$ → Heisenberg

$$x_{\min} = a = \frac{\hbar}{\sqrt{2mkT \ln 2}} = 1.5nm(300K)$$

---

3) Minimum state switching time

$$\Delta E \Delta t \geq \hbar$$ → Heisenberg

$$t_{st} = \frac{\hbar}{kT \ln 2} = 4 \times 10^{-14} s(300K)$$

---

4) Maximum gate density

$$n = \frac{1}{x_{\min}^2} = 4.6 \times 10^{13} \frac{gate}{cm^2}$$

Total Power Dissipation (@E_{bit}= $kT\ln(2)$) - A Catastrophe!

$$P_{chip} = \frac{n \cdot E_{bit}}{t} = 4.6 \cdot 10^{13}[cm^{-2}] \cdot \frac{3 \cdot 10^{-21}[J]}{4 \cdot 10^{-14}[s]}$$

$$E_{bit} = k_B T \ln 2 \approx 3 \cdot 10^{-21} J$$

$$P_{chip} = 4.74 \times 10^{6} \frac{W}{cm^2}$$ T=300 K

The circuit would vaporize when it is turned on!

Implications for Nanoelectronics Circuits

- **Circuit heat generation is the main limiting factor for scaling of device speed and switch circuit density**

- Scaling to molecular dimensions may not yield performance increases
  - We will be forced to trade-off between speed and density
- Optimal dimensions for electronic switches should range between 5 and 50 nm
  - Likely achievable with Si – easily within the scope of ITRS projections
- Going to other materials for FETs will likely achieve only "one-time" percentage gains
  - Need a new device mechanism or computational architecture for new scaling path

2005 ITRS Taxonomy for Processing

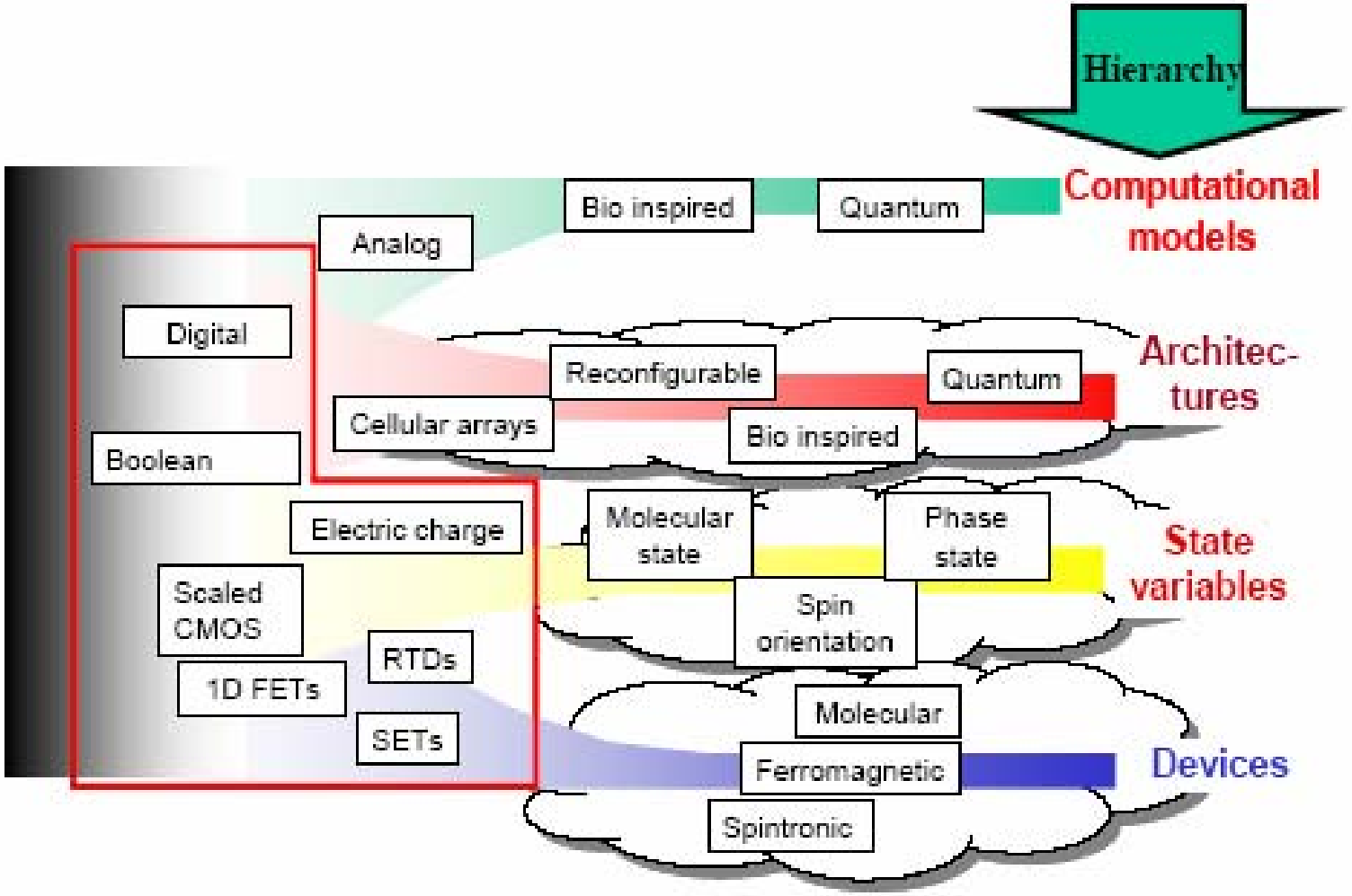


Figure 51 A Taxonomy for Nano Information Processing

NRI Mission Statement

- **NRI Mission: Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.**
  - These devices should show significant advantage over ultimate FETs in power, performance, density, and/or cost to enable the semiconductor industry to extend the historical cost and performance trends for information technology.
  - To meet these goals, NRI is focused primarily on research on devices utilizing new computational state variables beyond electronic charge. In addition, NRI is interested in new interconnect technologies and novel circuits and architectures, including non-equilibrium systems, for exploiting these devices, as well as improved nanoscale thermal management and novel materials and fabrication methods for these structures and circuits.
  - Finally, it is desirable that these technologies be capable of integrating with CMOS, to allow exploitation of their potentially complementary functionality in heterogeneous systems and to enable a smooth transition to a new scaling path.

Five Research Vectors

- Computational State Vector other than Electronic Charge
  (e.g. "bits" represented by spins)
  - New scaling path
- Non-equilibrium Systems
  - Lower power, less heat
- Novel Data Transfer Mechanisms
  - Overcome RC limits
- Nanoscale Thermal Management
  - Cooler operation, manage power density
- Directed Self-assembly of such structures
  - Less variability, higher density, more reliable, lower cost

➢ ***Strong Focus in NRI on the first Research Vector***

NRI Milestones

- March 2004:
  - SIA White Paper on Post-CMOS presented to SIA Board
  - SIA Board Resolution for formation of **NRI**
- March 2005:
  - Six Companies sign NRI Participation Agreement
    - AMD, Freescale, IBM, Intel, Micron, TI
  - **NERC** incorporated to manage NRI
  - Governing Council (GC) and Technical Programs Group (TPG) formed with one representative per participating company
    - Advisors from NIST, NSF, and DARPA
- September 2005: NRI and NSF Solicitations released
- December 2005: NSF and NRI Awards announced
- January 1, 2006: Research Programs started
- November 16-17, 2006: First Annual NRI Review in San Francisco, CA

NRI Sponsored Nanoelectronics Research Institutes

- NRI Mission: Demonstrate novel computing devices to enable the semiconductor industry to extend Moore's Law beyond the limits of CMOS
- Leverage industry, university, and both state & fed government funds, and use to drive university fabrication infrastructure

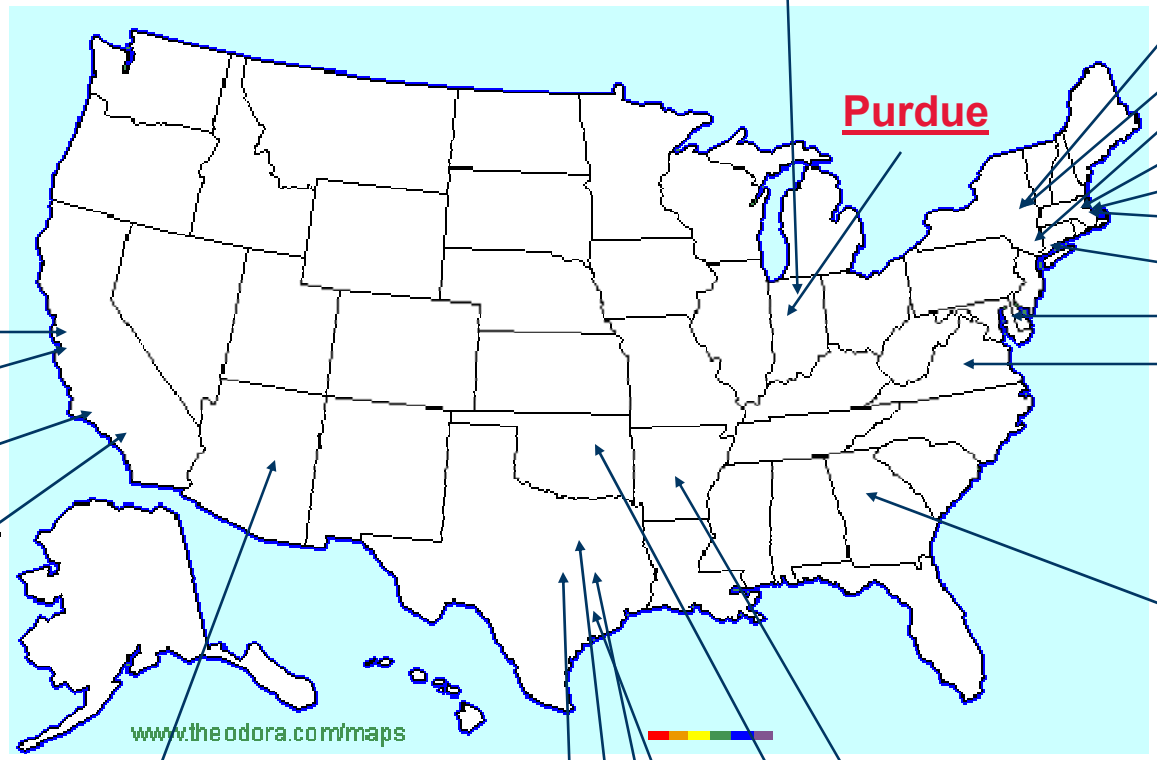
WIN Western Institute of Nanoelectronics	**INDEX** Institute for Nanoelectronics Discovery & Exploration	**SWAN** SouthWest Academy for Nanoelectronics	**NSF NSEC & MRSEC** Supplemental Funding
UCLA, UCSB, Berkeley, Stanford	Albany, GIT, Harvard, MIT, Purdue, RPI, Yale	UT-Austin, UT-Dallas, TX A&M, Rice, ASU, Notre Dame, U of MD	Various schools – funding ~6 centers per year
Theme 1: Spin devices Theme 2: Spin circuits Theme 3: Benchmarks & metrics	Task I: Novel state-variable devices Task II: Fab & Self-assembly Task III: Modeling & Arch Task IV: Theory & Sim Task V: Roadmap	Task 1: Logic devices with new state-variables Task 2: Materials & structs Task 3: Self-assembly & thermal mgmt Task 4: Interconnect & Arch Task 5: Nanoscale characterization	Broad work on various topics – also leverages other work in the centers

NRI Funded Universities

INDEX INSTITUTE FOR NANOELECTRONICS DISCOVERY AND EXPLORATION

WIN Western Institute of Nanoelectronics

SWAN



Notre Dame

SUNY Albany

RPI

Columbia

U Mass

MIT

Harvard

Yale

U of MD

U of Virginia

Purdue

UC Berkeley

Stanford

UC Santa Barbara

UC Los Angeles

GIT

Rice

U of Arkansas

Arizona State

TX A&M

U of Oklahoma

UT Dallas

UT Austin

INDEX

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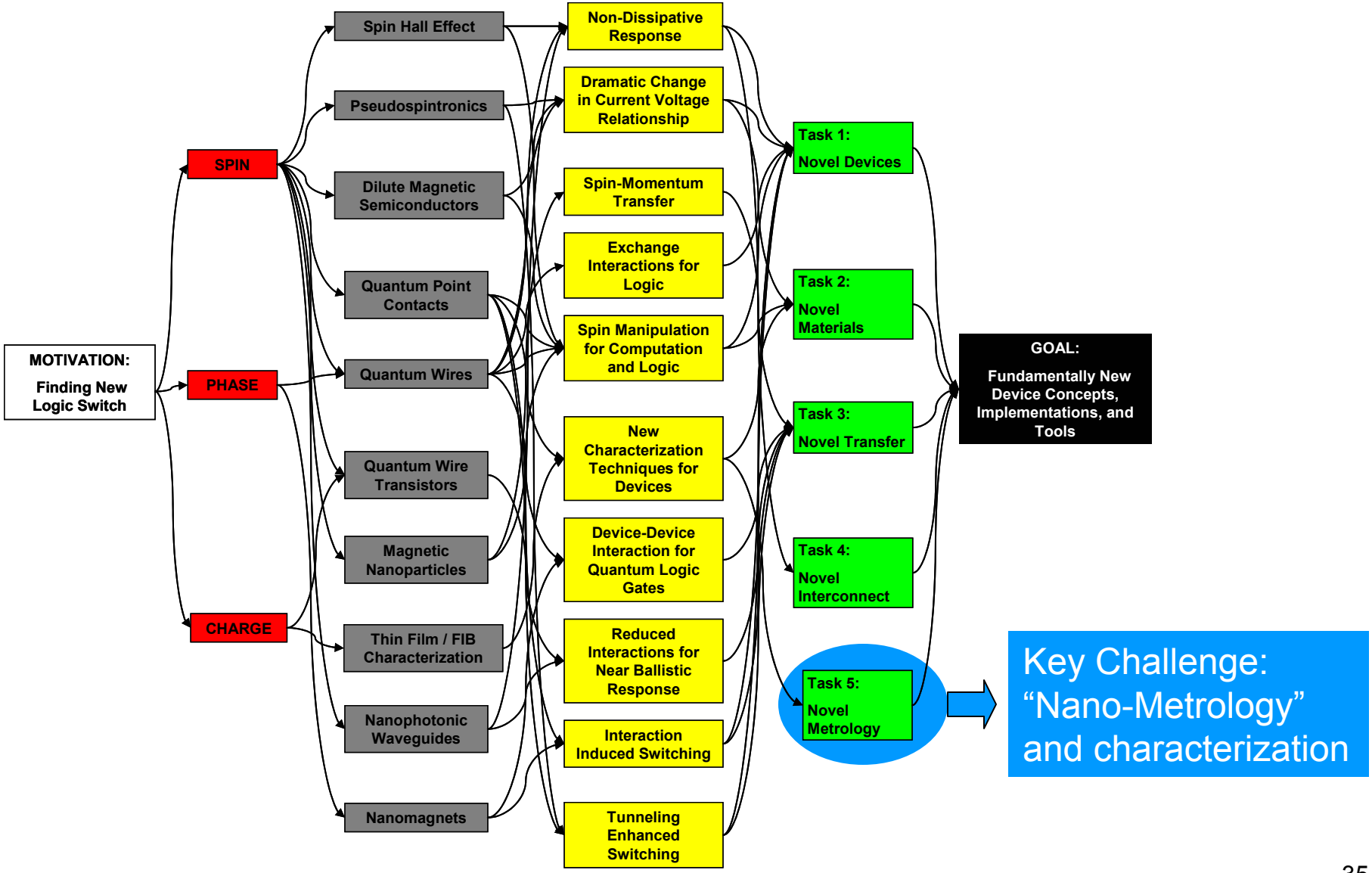
NSF-NRI

SWAN Novel Transistor Research



2005 ITRS Energy / Cost / Area / Delay

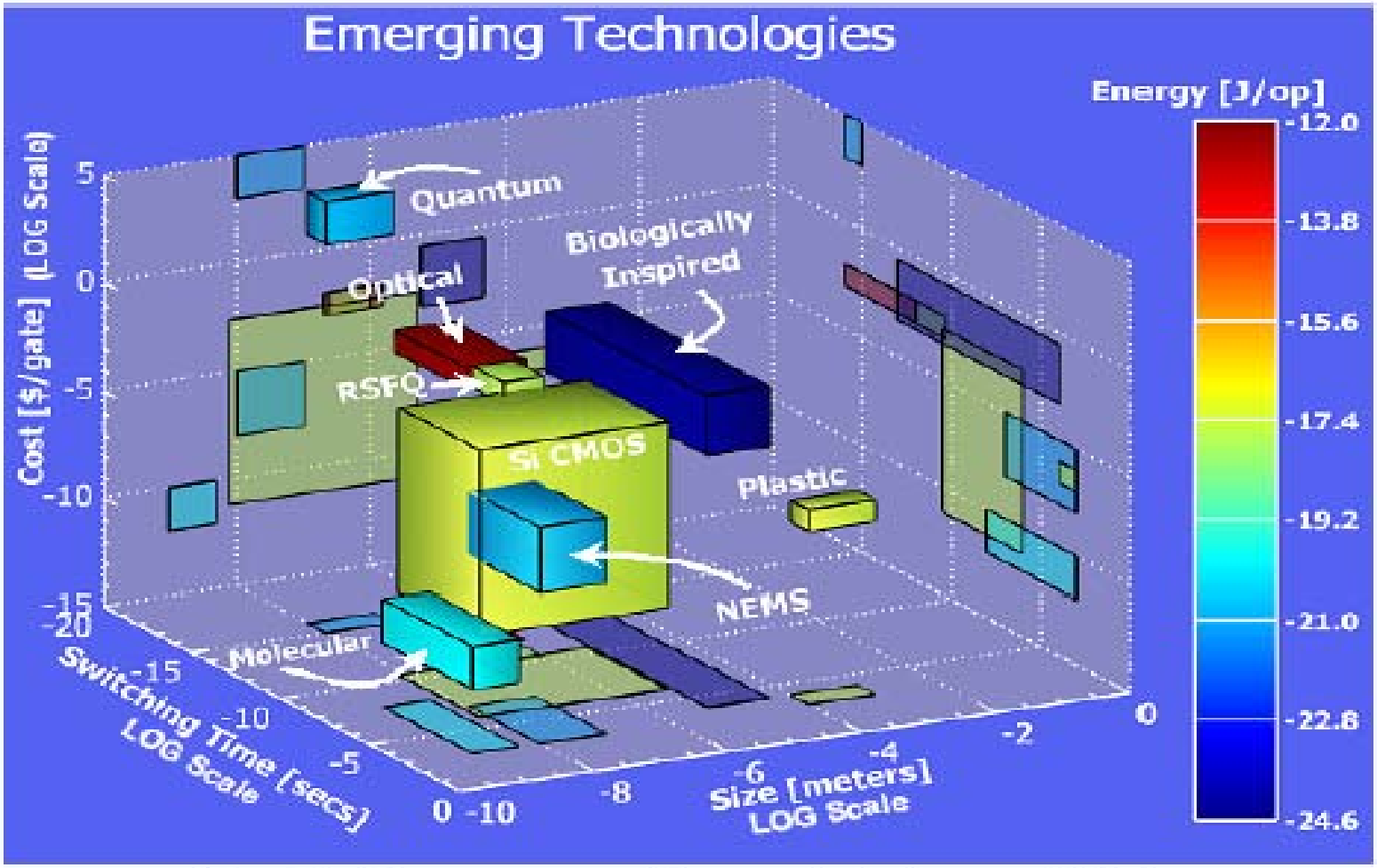


Figure 52 Parameterization of Emerging Technologies and CMOS—Speed, Size, Cost, and Switching Energy

Summary

- Power will continue to be the principal concerns facing the semiconductor industry
  - CMOS will continue to scale and improve over at least the next decade, with emphasis on utilizing increasing transistor density over increasing frequency
- Any new device / technology to replace CMOS must overcome the power / performance limits of a charge-based FET, and enable a new scaling path for the industry
- NRI is specifically focused on finding a new logic device to scale beyond CMOS in 2015-2020
  - Three main centers and joint work at several NSF centers already under way – will continue to expand
  - Continuing to be interested in additional novel devices and state variables (beyond spin)