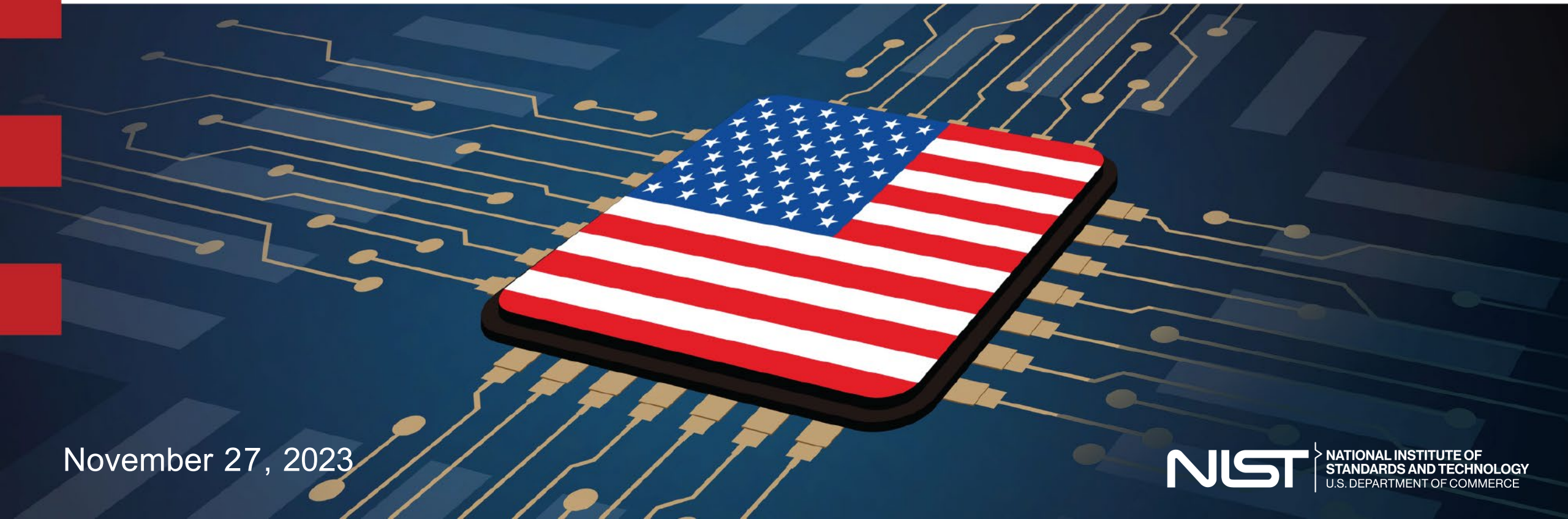
The Vision for the National Advanced Packaging Manufacturing Program

CHIPS for AMERICA



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NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

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Today's Speakers

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Director, NAPMP

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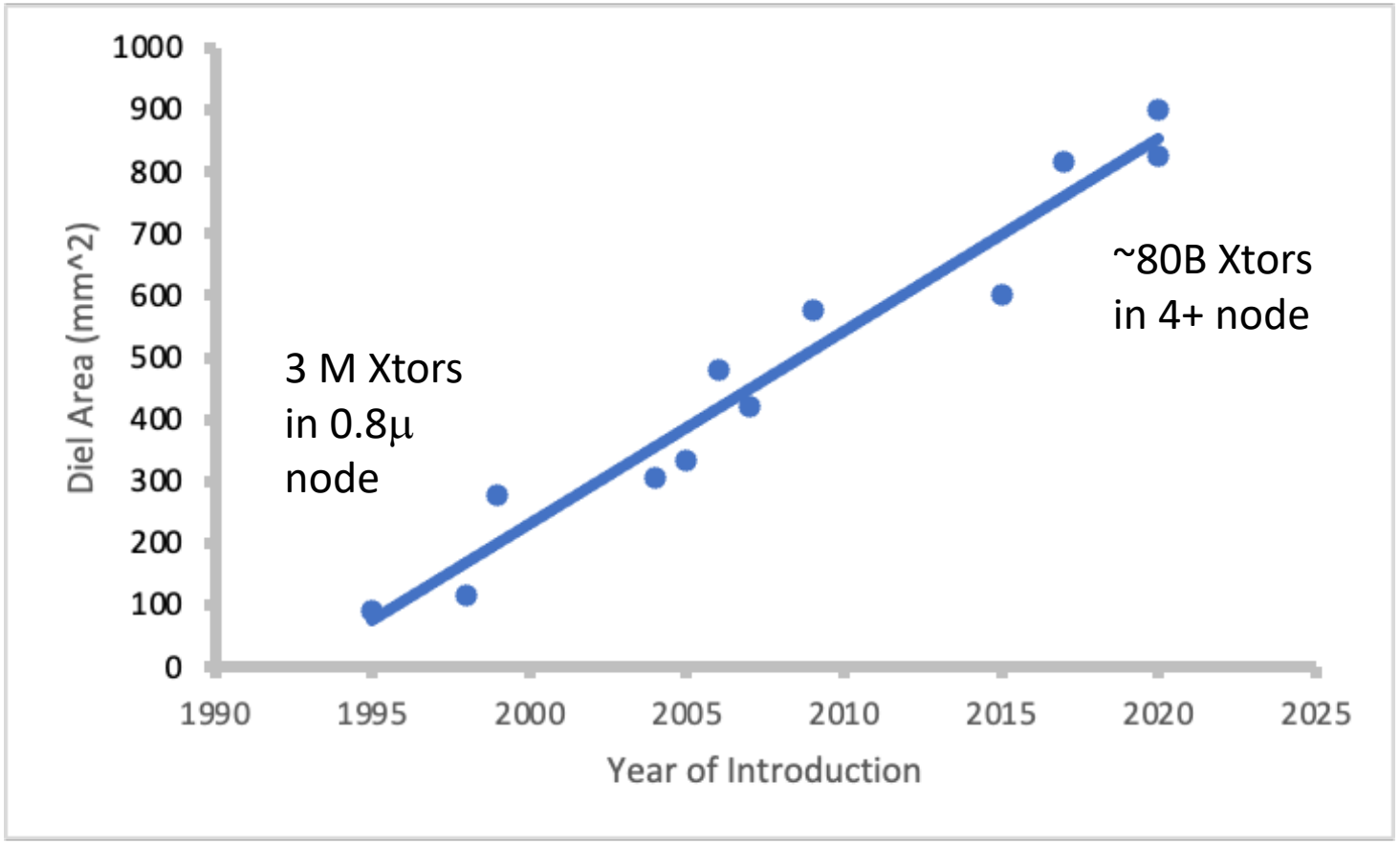
Agenda and Webinar Goals

- Opportunities in Advanced Packaging
  - Context
  - Background
- NAPMP vision, mission, and outcomes
- NAPMP investment areas
- Next steps

Even though transistors have scaled dramatically, die sizes have grown larger



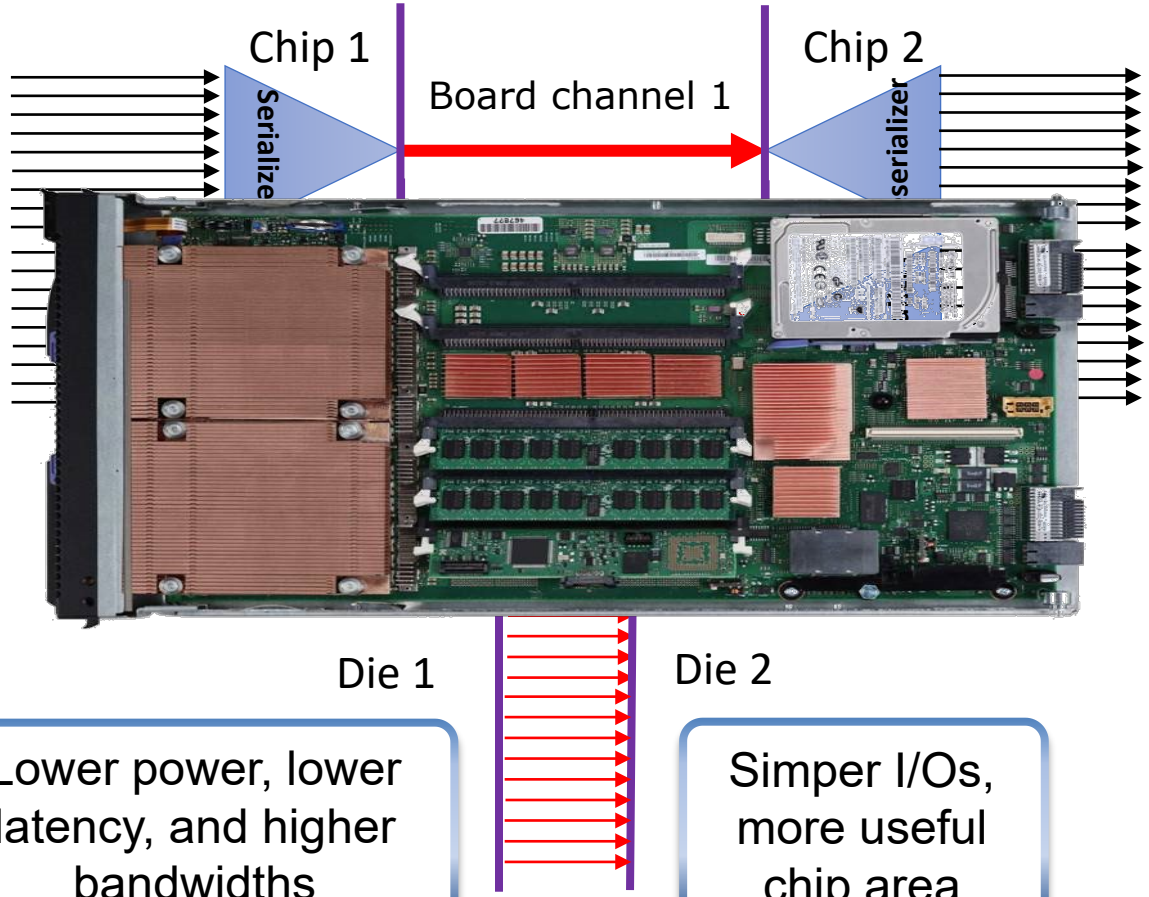
This chart shows past and current die size scaling trend

- Monolithic dies still outperform multi-chip packaged assemblies
  - Because packaging scaling has not kept up with silicon scaling (~10X Vs 10^6 X)
  - But high-performance dies have reached reticle limits
- Packaging is evolving to emphasize system integration rather than single chip packaging with the increasing adoption of silicon processing techniques

**Die size data from commercial product spec sheets*

Heterogeneous integration is not new

The difference now is scale:



Lower power, lower latency, and higher bandwidths

Simper I/Os, more useful chip area

- More channels on the package
  - Finer ”bump/pillar” pitch
  - Approach on-chip via pitches (<1 µm)
- Finer trace pitch
  - Approach on-chip wiring pitches
- Shorter inter-die distance
  - ~ µm

Scale Down

- Significantly more intimately connected silicon

Scale Out

Advanced packaging blurs the line between a monolithic chip and a packaged assembly of heterogeneous chips

Scaling down features on the package:

- Making the features on the package approach those at the top level on a monolithic CMOS chip
- Connecting the dies to the package at pitches approaching the final via pitches on a chip
- Reducing the distance between dies that are assembled on a multi-chip package to approach the distance between IP blocks on a monolithic chip

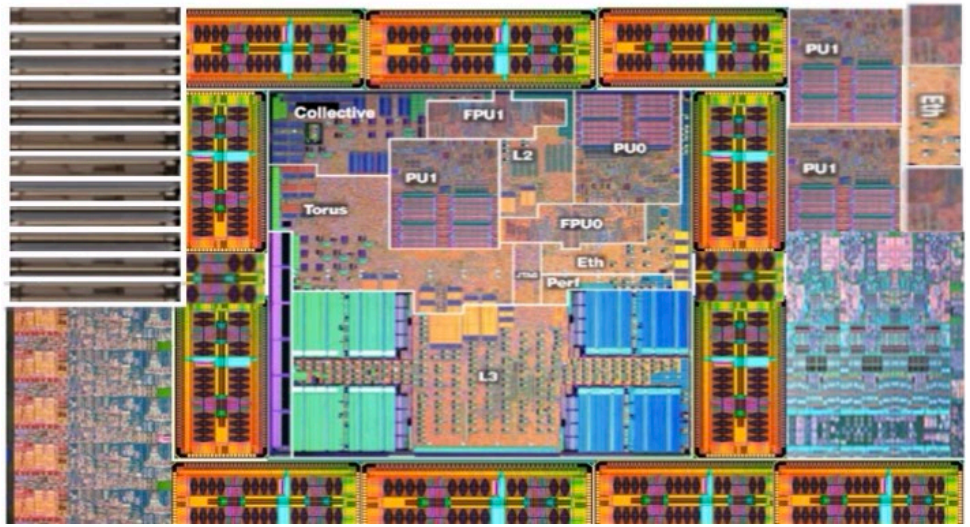
Scaling out the package

- Accommodate a larger number of closely packed heterogeneous dies
- Address the power delivery, thermal dissipation, and external connection challenges
- Develop standards and protocols to accommodate this large and diverse set of chips (chiplets)

Advanced packaging allows us to change the way we put complex systems together[1]

Adapting SoC methods to packaged systems

- IP blocks transformed into hardware verified dielets (chiplets)
  - Chiplets are IP designs
  - Chiplets are not small chips but need to be connected to complementary chiplets to function
  - Dielets are hardware instantiated chiplets
- Bare dielets are stacked (3D) or integrated side by side at fine pitch on an interconnect fabric (substrate)
- Dielets are heterogeneous
- A simpler and flatter hierarchy is possible



Chiplet discovery, disaggregation, and dielet reintegration

[1]S.S. Iyer T-CPMT (2016)

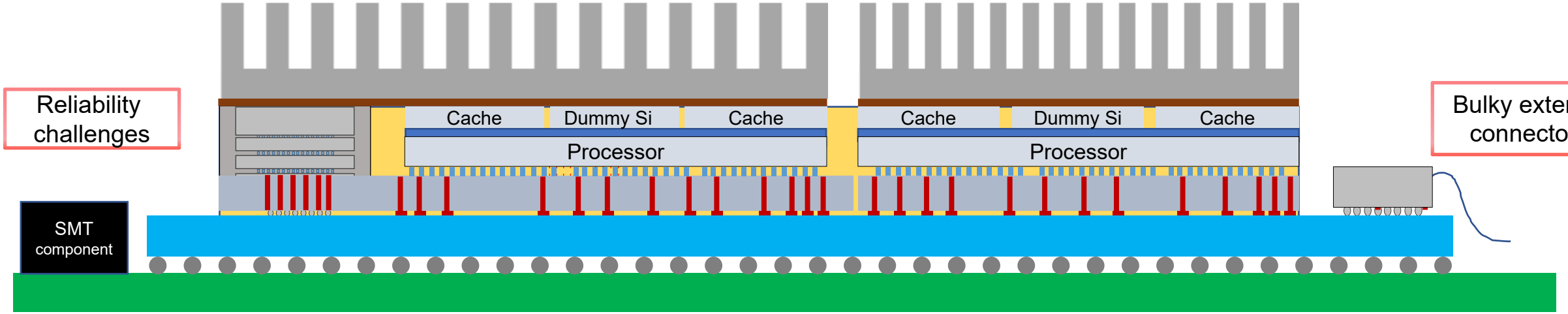
But today, packages are incredibly complex and costly

Materials with large CTE mismatches and high stresses

Known good die, testing, and rework challenges

Thermal and hot spot challenges
Power delivery challenges

Reliability challenges



Bulky external connectors

Increasingly complex hierarchies (e.g.: interposers) and assembly techniques

Organic substrates and laminates with large warpage and coarse pitches with embedded and SMT passives and expensive interposers

Simplify packaging and make it cost effective to manufacture in the U.S.

CTE: coefficient of thermal expansion; SMT: surface mount technology

NAPMP Vision, Mission, and Expected Outcomes

George Orji

CHIPS R&D | Engagement and Outreach

NAPMP implementation planning is informed by

- Input from the public in response to the CHIPS RFI
- PCAST and CHIPS IAC recommendations
- More than 100 meetings with stakeholders, including:
  - Industry: IDMs, foundries, and OSATs; equipment, materials, and EDA vendors; PCB manufacturers, and electronics manufacturing services
  - Academia, professional societies, standards development organizations, industry road-mapping groups
  - Other U.S. government agencies
  - …and more

CHIPS R&D | Engagement and Outreach

NAPMP | Summary of Responses to January 2022 RFI

- The NAPMP should serve as a critical resource to develop advanced packaging and related R&D
- In view of the U.S.'s current dependence on foreign resources, advanced packaging is a matter of national security
- NAPMP must be competent in heterogeneous integration, chiplets, photonics, and codesign
- The NAPMP should have easily accessible and flexible user facilities or hubs that focus on low-volume, cost-effective prototyping, including material characterization, metrology, modeling and simulation, and standards
- It is important to build a skilled workforce to support this industry

Additional Recommendations from CHIPS IAC

- Create programs that establish and extend enabling processes and capabilities across multiple technologies and materials (i.e., not just silicon)
- Create a community of stakeholders to build a digital twin capability from R&D to manufacturing with tight integration to EDA/simulation as well as for workforce development support and training

NAPMP Vision, Mission, and Outcomes

Vision

The National Advanced Packaging Manufacturing Program will drive **U.S. leadership** in advanced packaging and provide the technology needed for packaging manufacturing in the United States.

Mission

The NAPMP will develop **critical and relevant innovations** for advanced packaging technologies and **accelerate their scaled transition** to U.S. manufacturing entities.

Outcomes

- Within a decade, NAPMP-funded activities, **coupled with CHIPS manufacturing incentives,** will establish a vibrant, self-sustaining, profitable, high-volume, domestic, advanced packaging industry where advanced-node chips manufactured in the U.S. are packaged in the U.S.
- We expect the technology developed to be leveraged in new applications and market sectors and at scale.

Congressional Interest in U.S. Manufacturing

Our Authorization - 15 U.S.C. 4656(d)

[The] Secretary of Commerce shall establish a National Advanced Packaging Manufacturing Program in coordination with the national semiconductor technology center established under subsection (c**), to strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem**, and which shall coordinate with a Manufacturing USA institute established under subsection (f), if applicable.

The Director may make financial assistance awards, including construction awards, in support of the National Advanced Packaging Manufacturing Program.

NAPMP Investment Areas

Subu Iyer

Establishing Advanced Packaging in the U.S.

Packaging Roadmaps

- NIST-sponsored roadmaps: MRHIEP, MAESTRO and MAPT
- Other roadmaps: HIR and IRDS

Technology Investment Areas

- All aspects of technologies required to develop a leading-edge on-shore advanced packaging manufacturing capability

The Advanced Packaging Piloting Facility (APPF)

- Key to facilitating high-volume manufacturing
- Piloting and prototyping functions

The Chiplet and Design Ecosystem

- Chiplet discovery, disaggregation and reaggregation methodologies, protocols, standards, fabrication and warehousing design for test, repair and reliability, and holistic design tools and methodologies

Design in the U.S., build in the U.S., and sell worldwide

- Successful development efforts will be transitioned and validated for scaled transition to U.S. manufacturing

NAPMP Priority Research Investment Areas

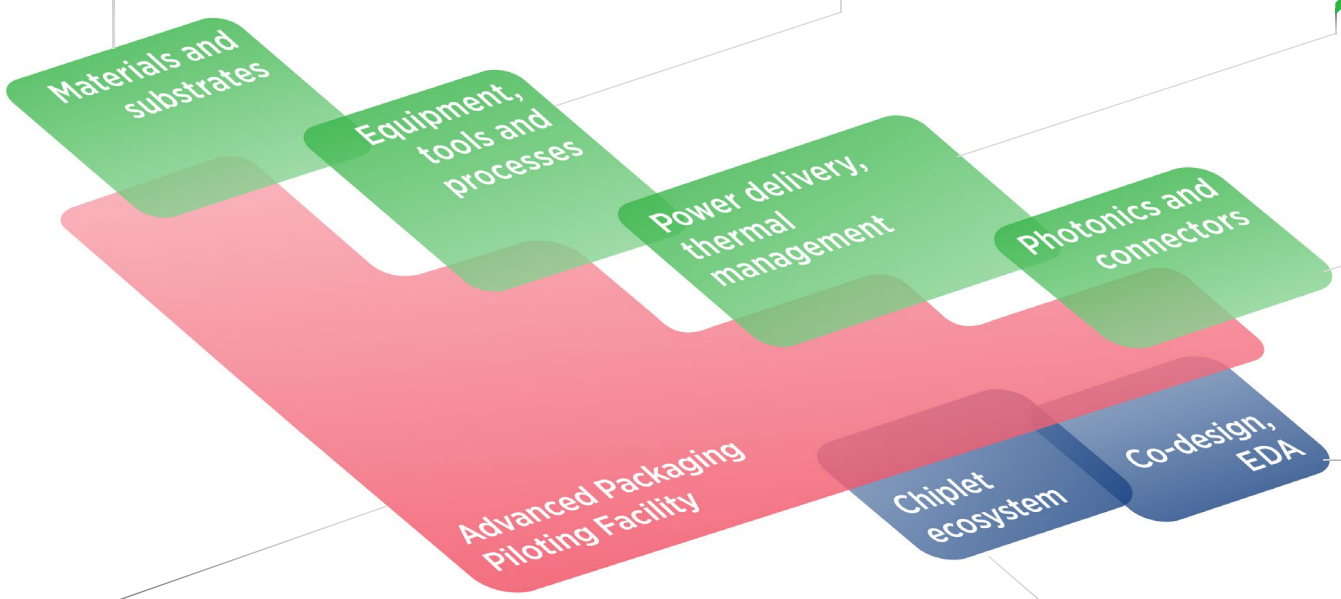
Materials and substrates are the platform for heterogeneous integration of dielets

Equipment, tools, and processes are needed to pattern substrates and assemble dielets and passivate assemblies

Thermal management and efficient power delivery are critical needs

Photonics and connectors allow the assembly to interact with the outside world

Automated design for test, repair, security, and reliability; substrate and process dependent



The APPF provides a test bed for integration of the different investment areas and also functions as a piloting and prototyping facility

The chiplet ecosystem is crucial for any implementation of advanced packaging

APPF: Advanced Packaging Piloting Facility

Materials and Substrates

"The key requirements of new substrates include multiple levels of fine wiring and via pitches, low warpage, large area, and the ability to integrate active and passive components."

- Materials and substrates are the platform on which advanced packaging is built
- These substrates or interconnect fabrics (IF) may be based on silicon, glass, or organic materials and can include fan-out wafer-level processes
- The IF needs to
  - be compatible with advanced and legacy nodes and different semiconductor material systems
  - have integrable active and passive components
  - be compatible with either mass reflow, thermal compression bonding, or hybrid bonding
- Meet environmental and sustainability goals

Equipment, Tools, and Processes

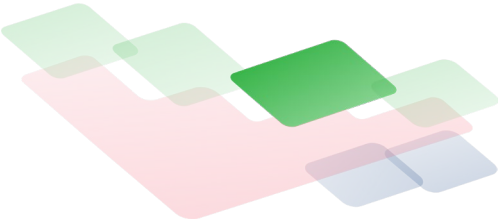
"Advances in equipment, tools, and processes are required, where substrates are patterned and chiplets are reliably assembled on these substrates."

- To achieve goals in reducing patterned feature sizes on large areas, including through substrate vias as well as strategies to reliably assemble chiplets onto these finer substrates and passivate them
- We expect that CMOS equipment and processes will be adapted to handle dies, wafers, and panels as appropriate
- We expect the APPF to benefit from developments in equipment, tools, and processes

Power Delivery and Thermal Management

"These activities will require new thermal materials as well as novel circuit topologies that employ advanced substrates and heterogeneous integration."

- Advanced packaging makes severe demands on power density and can restrict heat spreading
- Heterogenous integration will require multiple voltage domains and high granularity. Power delivery will likely require wide bandgap materials integrated into the substrate
- This investment area will focus on the development and evaluation of innovative materials and solutions that are compatible with the materials, substrates, and assembly processes used in manufacturing
- Modeling and optimization to achieve high efficiency is a must



Photonics and Connectors

"The focus will be on reliable and manufacturable integrated connectors that include computational capability, data pre-processing, security, and ease of installation to the packaged assembly."

- Packaged assemblies to interact with other assemblies and the outside world (a few centimeters to kilometers)
- Connectors can be wired, RF, and optical

Chiplet Ecosystem

"Chiplet discovery methodologies will be developed to ensure a high level of reusability, design, and warehousing of these chiplets."

- The vision of advanced packaging relies on the availability of high-reuse chiplets
  - This has not yet happened
- Chiplets need to be small and work better when connection pitches and distances are small
- Chiplet dicing and ESD-free transport
- Chiplet ecosystem requires standards and a warehousing infrastructure where bare dies are stocked
- NAPMP will focus on chiplet discovery methodologies, high-value chiplet design, and integration methodologies
- Common protocols and protocol translator chiplets

Co-design

Holistic package co-design “will be adapted for advanced packaging with consideration for built-in test and repair, security, interoperability, and reliability, with a detailed understanding of the substrate and processes used for assembly.”

- The intimate connection between chiplets and advanced packaging constructs requires a co-design platform that comprehends:
  - Chiplet architectures and communication options
  - Design for test, repair, security, and reliability especially “graceful failure”
  - Thermal and thermomechanical constraints
  - Substrate and assembly technology (no rework)
- The extension of chip design methodologies to advance packaging
- The NAPMP will support co-design efforts

Packaging Workforce Development

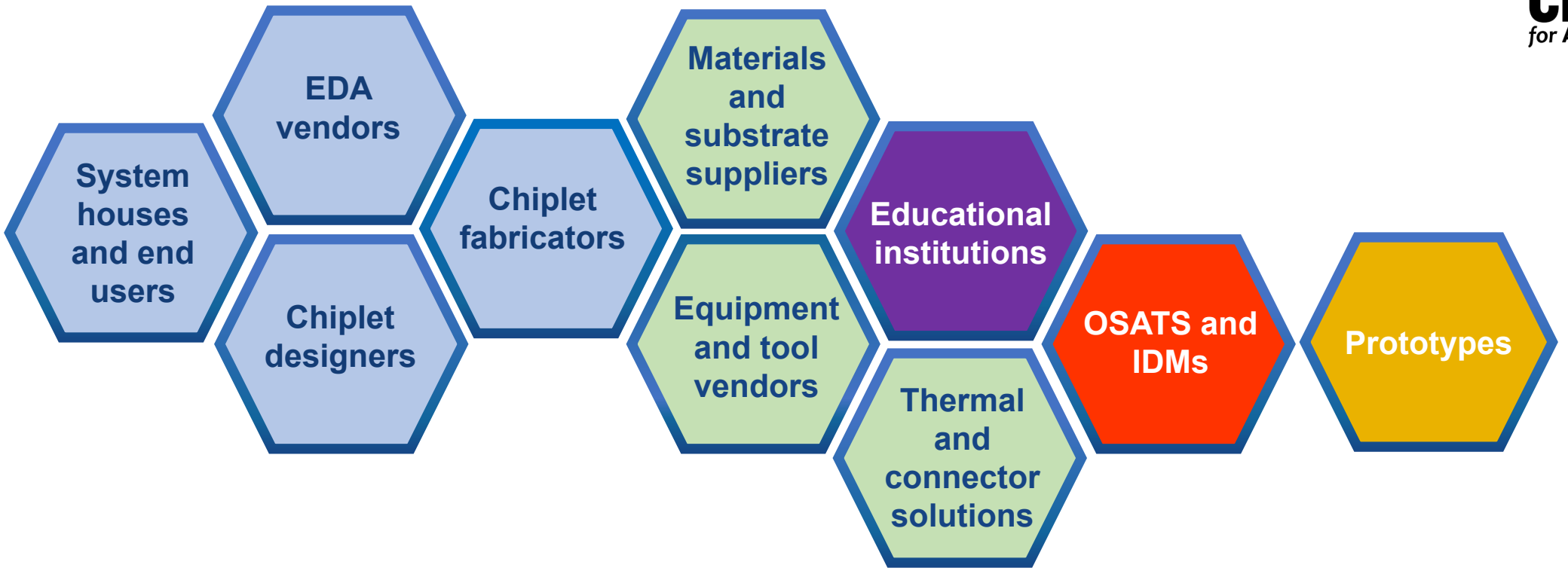
"The NAPMP intends to integrate workforce education and training into all NAPMP efforts leveraging internships, co-ops, work-study programs, seminars, hands-on experiential learning, and other educational advancement activities within each investment area and in the APPF."

- Packaging is very interdisciplinary and requires multi-disciplinary teams
- The NAPMP intends to fund projects that incorporate strong workforce development plans that emphasize educational advancement and professional development

The Advanced Packaging Piloting Facility (APPF) - Where it all comes together

- Investment areas are expected to connect with activities at the APPF
- The APPF is:
  - Where successful development efforts will be transitioned and validated for scaled transition to U.S. manufacturing
  - A key facility for technology transfer to high-volume manufacturing
- The APPF could include
  - Integrated process flows that can reach commercial scale
  - Validating new technology specifications, compatibility with other processes, yield, and reliability
  - Assessing technologies for scaled transition to U.S. manufacturing
- The APPF may consider prototyping innovative design ideas from the community

Collaboration is Critical for Success



We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the NAPMP.

Next steps

- The NAPMP expects to release its first funding opportunity in early 2024
  - Materials and substrates will be the topic of the first funding opportunity
- We expect to host
  - Webinars to update the community as we develop programs
  - “Industry Days” to promote teaming and community building
- Learn about webinars, events, and funding opportunities by subscribing to updates at CHIPS.gov

Summary and discussion

- Advanced packaging is all about scale down and scale out
  - Minimal hierarchy and reusable chiplets
  - Innovative architectures and products
  - Small NREs and short times to market
- It offers a different way of building complex chips and systems which leverages our strengths in design and system architecture
- Our focus is on R&D that leads to
  - Products designed and manufactured in the U.S. with U.S. software and equipment
  - U.S. manufacturing and R&D workforce
  - A self-sustaining innovation pipeline that fuels U.S. packaging leadership

NAPMP Frequently Asked Questions

George Orji

What is the relationship between the NAPMP and the NSTC?

The National Advanced Packaging Manufacturing Program (NAPMP) and the National Semiconductor Technology Center (NSTC) are both part of the CHIPS Research and Development Office. The NSTC is a public-private consortium that will serve as the focal point for semiconductor research for the nation. The NAPMP will help establish U.S. leadership in advanced packaging and provide the technology needed for packaging manufacturing in the U.S.

The NAPMP and the NSTC program are working closely together.

Will the NAPMP be a public-private consortium?

No. The NAPMP is operated by NIST's CHIPS Research and Development Office.

Are standards part of NAPMP's strategy?

Standards development is an important part of the CHIPS R&D and NAPMP strategies. Advancements in the CHIPS Metrology Program, including standards research, benefit all of the CHIPS programs.

The feedback we received from industry is that standards are needed for advanced packaging. We will work with standards development organizations to provide guidance on standards.

The CHIPS R&D office has already held a **CHIPS R&D Standards Summit,** and will soon hold a **CHIPS R&D Chiplets Interfaces Technical Standards Workshop** and a **CHIPS R&D Digital Twin Technical Standards Workshop**. Please go to CHIPS.gov to register.

Thank You For Attending

- Questions? Askchips@chips.gov
- Visit CHIPS.gov for future updates and additional information