CHIPS for AMERICA
METROLOGY

Inside CHIPS Metrology: Research that Accelerates Innovation

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

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CHIPS for America Programs

CHIPS for AMERICA

$39 billion
for manufacturing

Two component programs:

1. Attract large-scale investments in advanced technologies such as leading-edge logic and memory
2. Incentivize expansion of manufacturing capacity for mature and other types of semiconductors

$11 billion
for R&D

Four integrated programs to:

1. Conduct research and prototyping of advanced semiconductor technology
2. Strengthen semiconductor advanced test, assembly, and packaging
3. Enable advances in measurement science, standards, material characterization, instrumentation, testing, and manufacturing

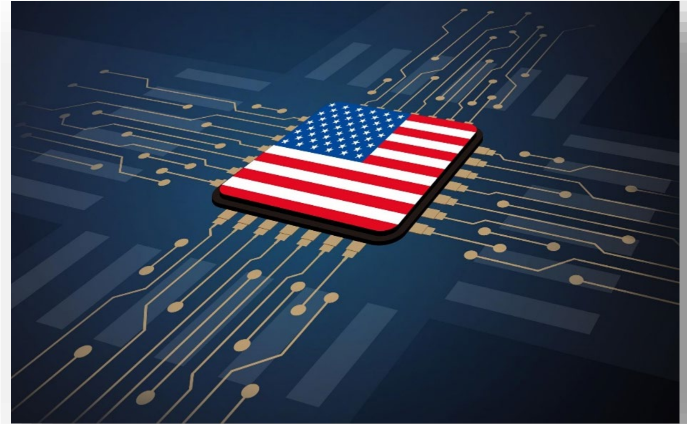
Together with CHIPS initiatives from other agencies, including DOD, State, NSF, and Treasury

The CHIPS and Science Act

CHIPS for AMERICA

How did we get here?

- Congress created a set of programs aimed at restoring U.S. leadership in semiconductor manufacturing and fostering growth in the microelectronics and semiconductor R&D ecosystem
- The CHIPS and Science Act strategy is informed by extensive engagement with semiconductor industry leaders and stakeholders across all fields
- NIST was selected as the bureau within DOC to house these new units



CHIPS R&D

CHIPS for AMERICA

Vision

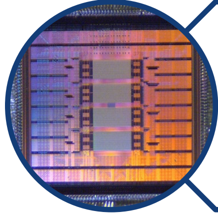
A vibrant and self-sustaining U.S. domestic semiconductor ecosystem that revitalizes American manufacturing, grows a skilled and diverse workforce, and leads the world in semiconductor research and innovation.

Mission

Accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic tools, resources, workforce, and facilities.

2030 Goals

CHIPS for AMERICA



U.S. technology leadership

Accelerate ideas to market

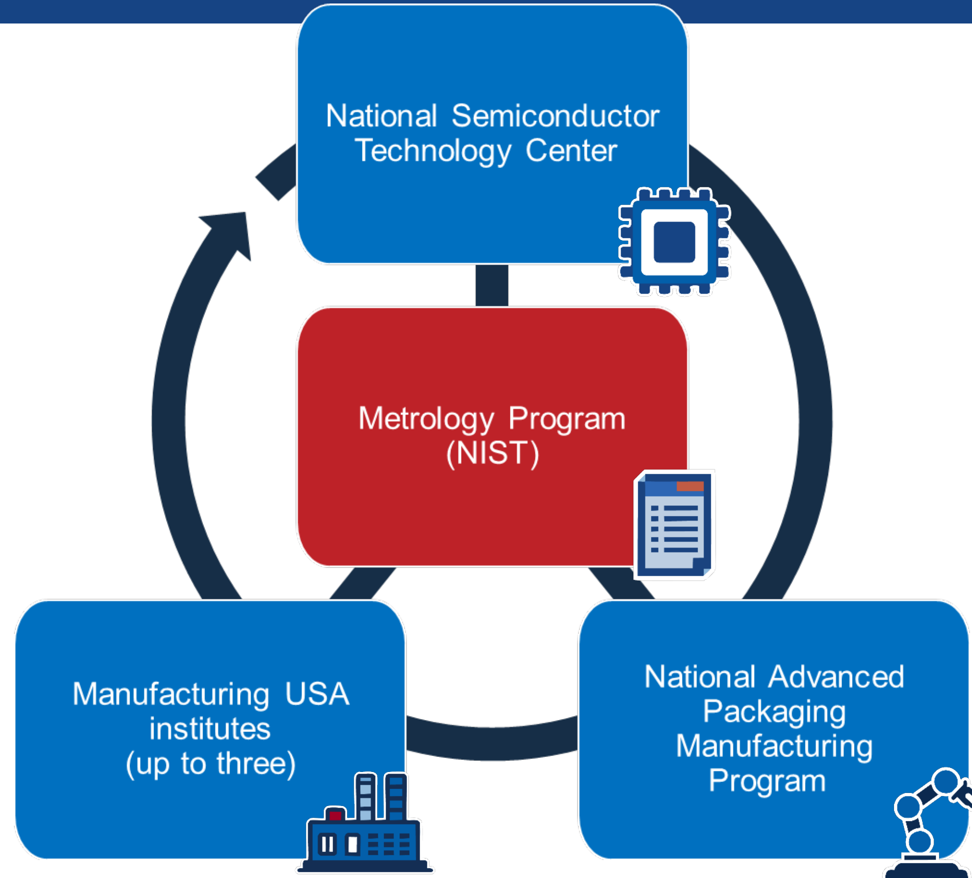
A robust semiconductor workforce

CHIPS for America

To address gaps in the semiconductor ecosystem, CHIPS for America is investing in four overlapping entities, all of which include some aspect of workforce training.

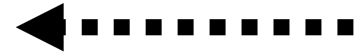
These programs will share infrastructure, participants, and projects.

They will operate in coordination with each other, with the CHIPS for America manufacturing incentives program, and with microelectronics R&D programs supported by other U.S. federal agencies.

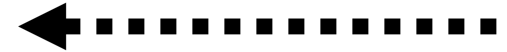


Success Requires CHIPS-Industry Partnerships

Metrology is **foundational** and fundamental for all CHIPS R&D.



Metrology **solutions are delivered** to industry stakeholders.



High-impact research areas **sourced from industry.**

Metrology technologies should reach **commercial scale.**

Engage with the CHIPS Metrology Program

Opportunities are being created for industry, government partners, and academia to participate in CHIPS for America and the CHIPS Metrology Program.

Collaborate with the Metrology Community

- CHIPS Metrology will help to foster collaboration among the semiconductor community with focused groups based around each Grand Challenge
    - Members of the semiconductor space will have the chance to join webinars, in-person poster sessions, networking sessions, community chat
    - This is an opportunity to share knowledge with other stakeholders and learn about what other projects are working on
    - Visit chips.gov to join our email list and stay involved.

Join our email list!

METIS RFI

CHIPS for AMERICA

What is METIS?

- The Metrology Exchange to Innovate in Semiconductors, or METIS, is a data exchange ecosystem developed by NIST that will give stakeholders access to CHIPS Metrology research results and serve to catalyze innovative breakthroughs in U.S. semiconductor manufacturing.
- METIS will make research and data available in a manner that guards intellectual property, protects U.S. security interests, is aligned with the approach used by NIST for access to research results, and is self-sustaining to meet future needs.

How to Provide Feedback

- Visit nist.gov/programs-projects/metis and follow the directions on how to provide feedback.
- The public comment period runs until January 31st, 2024.

Metrology Program Grand Challenges

GC4 – Modeling and Simulating Semiconductor Materials, Devices, and Components

GC1 - Materials Purity, Properties, and Provenance

GC5 – Modeling and Simulating Semiconductor Manufacturing Processes

GC2 – Advanced Metrology for Future Manufacturing

GC3 –Metrology for Advanced Packaging

Cross Cutting

GC6 – Standardizing New Materials, Processes, and Equipment

GC7 – Security and Provenance of Microelectronic Components and Products

DESIGN METROLOGY
Material and device models; physical metrology

DESIGN

Mask Design *Template for the IC*

Circuit Design *Integrated circuits (IC), systems integration*

MATERIALS SUPPLY
Over 800 diverse materials

MATERIALS QUALITY METROLOGY
Acceptance inspection and testing for defects, purity, and other properties

WAFER FABRICATION
Deposit a film, pattern a photoresist (litho), use as a stencil to etch the film

Repeat 40 to 100 times

Deposition *Metal, dielectric*

Lithography *Photoresist spin coat, expose, and develop*

Etching *Heat/bake, etch, and remove resist*

40-70 different masks, up to 2000 steps

FAB METROLOGY
In-line metrology; inspection for defects; wafer and thin film quality inspection; mechanical testing, density and surface charge analysis; dimensional analysis of fine patterns and contact hole diameters

TESTING — **Wafer Test** *Each die individually tested on wafer*

PACKAGING — **Assembly / Integration** *Wafer dice, sorting, die attach, bonding*

TESTING — **Test Packages** *Final product testing*

END PRODUCTS — **Integration** *Chips integrated in end products (OEMs)*

WAFER/PACKAGE METROLOGY
In-line metology; inspection and testing for accuracy and precision of performance; patterned wafer inspection for defects; quality inspection of packaging performance

Adapted from CHIPS.1000

CHIPS Metrology: How far we've come

CHIPS for AMERICA

Grand Challenge Funded Research Projects

- Over **$109 million** in funding has been provided to **29 approved research projects** over three Grand Challenges
  - GC2 - Advanced Metrology for Future Microelectronics Manufacturing: **10 projects funded**
  - GC3 - Enabling Metrology for Integrating Components in Advanced Packaging: **6 projects funded**
  - GC4 - Modeling and Simulating Semiconductor Materials, Designs, and Components: **13 projects funded**
- Current projects are helping to develop new measurement instruments, measurement methods, and measurement-informed models and simulations for advanced microelectronics design and manufacturing.
- Additional projects will be selected by the end of the year

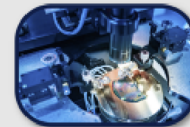
Industry & Academia Collaboration

- Research teams have proposed several distinct industry collaborators to provide materials and software and/or conduct joint research with researchers
- Several collaborations with U.S. universities, nonprofit consortiums, research institutes, and associations related to the microelectronics industries have also been proposed

Grand Challenge 2:

Advanced Metrology for Future Microelectronics Manufacturing

The challenge: Ensure that critical metrology advances are made to keep pace with cutting-edge and future microelectronics and semiconductor manufacturing, while maintaining a competitive U.S. advantage.



The strategy: Develop advanced physical and computational metrology adaptable to next-generation manufacturing of advanced complex, integrated technologies and systems.

The path forward: Conduct activities in critical areas to develop innovative, cost-effective metrology applicable to 3D device and next-generation manufacturing, including tools and methods in the following critical areas:

- Properties of new materials and devices, such as GAA, complementary FET, and novel interconnects and dielectrics.
- Physical properties characterization (e.g., size, roughness, thermal, mechanical, electrical, magnetic, optical) for surfaces, buried features, interfaces, and devices with increased resolution, sensitivity, accuracy, and throughput.
- Rapid, high-resolution, non-destructive techniques for characterizing defects and impurities and correlating them with performance and reliability.
- Evaluation and correlation of relevant data across the semiconductor manufacturing process.
- Standards for process design, development, and control, such as reference materials and documentary standards.
- Statistical analysis for rare but catastrophic defects such as stochastic events in extreme ultraviolet (EUV) lithography.

https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

GC2 Funded Research Projects

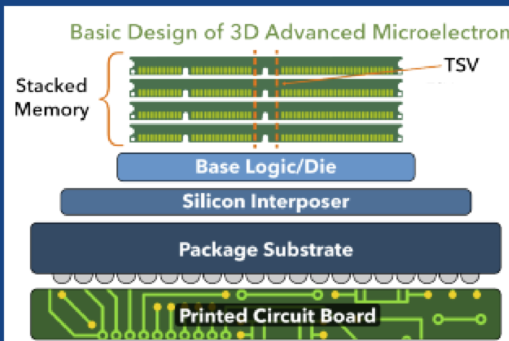
Project Title	Summary
Accurate Measurements of Thermal Properties at the Nanoscale	Developing accurate tools to map how heat moves through materials on a tiny scale with high precision (with less than 5% error for thermal conductivity and less than 10% for interfacial thermal conductance) and on shorter time scales (approximately 10^7 improvement).
Advanced Analytical Electron Tomography for Materials Development and Failure Analysis in Semiconductor Devices	Developing robust atomic-resolution methods for three-dimensional characterization of complex semiconductor devices through electron tomography, addressing industry challenges with advanced specimen preparation, cutting-edge microscopy, and AI-driven data collection.
Advanced Metrology to Enable Next Generation EUV Photoresists	Innovating measurements of nanoscale chemical distributions and in situ patterning processes. Through tailored metrology techniques, the project seeks to understand the impact of extreme ultraviolet (EUV) exposure on resist chemistry, critical dimensions, and edge roughness, providing the industry with a roadmap for rapid characterization and fostering competitiveness in high-yield manufacturing for the U.S.
Atom Probe Topography: Nanostructured Semiconductor Materials, Interfaces, and Devices	Revolutionizing semiconductor metrology with advanced atom probe tomography: Elevating yield, enhancing device performance, and accelerating time to market.
Critical Dimension Small Angle X-Ray Scattering (CDSAXS) for Next Generation in-line Metrology	NIST's Critical Dimension Small Angle X-Ray Scattering (CDSAXS) transforms semiconductor dimensional metrology, surpassing optical scatterometry limits, and is crucial for advanced applications in 3D-NAND memory arrays, gate-all-around (GAA) nanosheet transistors, and through-silicon vias.
Electron-Solid Interactions	Reducing uncertainties in electron-solid interactions, crucial for accurate measurements in critical dimension, contour, roughness metrology, and defect analysis using scanning electron microscopy (SEM) through innovative modeling and validated data.

GC2 Funded Research Projects (cont.)

Project Title	Summary
EUV Scatterometry Metrology	Revolutionizing integrated circuits (IC) manufacturing with advanced extreme ultraviolet (EUV) optics, promising a 1000-fold increase in information through optical techniques and proactive technology transfer to U.S. industry.
Non-Destructive Semiconductor Structure Function and Process Optimization for future Microelectronics Manufacturing at the NIST NSLS-II Beamline for XAFS and Diffraction	Enhancing non-destructive semiconductor structure optimization for microelectronics manufacturing, increasing sample throughput and sensitivity, and providing advanced capabilities for probing device interfaces and nanoscale structures.
Overcoming Barriers: Nanoscale Interface Metrology and Electrical Characterization for Advanced Electronics	Developing standardized protocols for nanoscale electric field determination from artifact-free 4D-STEM data aims to advance device development and optimize fabrication processes.
Strain Measurement for Semiconductor Devices and Packages	Advancing correlative measurement technology to measure strain at nanoscale for semiconductor devices and packages, improving accuracy and supplying reference materials for future-generation semiconductor manufacturing.

Grand Challenge 3:

Enabling metrology for integrating components in advanced packaging



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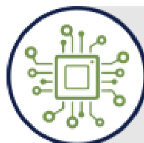


The challenge: Provide enabling metrology that spans multiple length scales and physical properties and supports acceleration of advanced packaging concepts for future-generation microelectronics.

The strategy: Develop metrology to enable complex integration of sophisticated components and novel materials for advanced microelectronics, strengthening the domestic semiconductor packaging industry and U.S. leadership in this critical sector.

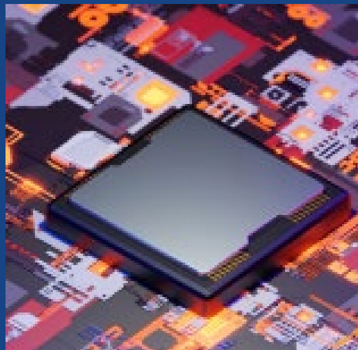
The path forward: Conduct R&D to develop metrology to address the unique challenges presented by advanced packaging, including subsurface features and aspects related to heterogeneous integration and other innovative concepts. Critical areas include:

- Measurements for in situ, rapid measurements and verification methods for interfaces and subsurface interconnects, and internal 3D structures including warpage, voids, substrate yield, stresses, adhesion, and reliability with improved throughput and resolution.
- Physical properties (e.g., size, thermal, mechanical, electrical, magnetic, optical) for films, surfaces, buried features, and interfaces.
- Methods for integrating chiplets, dielets, SoCs, and memories into packages.
- Mechanical measurements for component integration (e.g., hybrid bonding and interfacial adhesion and bond integrity).
- Evaluation and correlation of data across the packaging process.
- Standards for packaging, such as reference materials and documentary standards for areas including chiplets and SoCs.

GC3 Funded Research Projects

Project Title	Summary
Accurate Cure Kinetics, Stress, Mechanical Properties and Warpage Measurements for Next-Generation Microelectronics Packaging under Device Relevant Conditions	Providing accurate measurements and tools for designing systems that focus on handling tight connections, smaller patterns, and increased layers, all while minimizing warping and maximizing thermal performance for long-lasting reliability, within a microchip.
Characterization of nano-to-microscale process-induced thermo-mechanical changes in heterogeneously integrated microelectronics	Develop and provide advanced measurement methodologies and data for addressing the thermal and mechanical challenges in the heterogeneous integration of modular chips in system-in-package manufacturing.
Metrology of Materials, Surfaces, and Processes for Hybrid Advanced Packaging	Applying NIST's analytical and metrological expertise to develop a scientific understanding of bonding processes in chiplet manufacturing, aiming to establish a predictive framework for efficient development of known good processes.
Metrology for Integration of New Magnetic Materials	Developing the necessary metrology, materials, and methods for integrating magnetic components with semiconductor materials, aiming to miniaturize and enhance the functionality of electromagnetic systems in fields like communications, radar, and advanced computation.
Nanoscale, Element-Specific X-ray Imaging for Integrated Circuit Metrology	Developing an advanced x-ray computed tomography instrument for 3D, element-sensitive imaging at micro to nano scales, enhancing subsurface feature characterization in integrated circuit (IC) chips for manufacturing and security, standardizing this technology for industry-wide 3D IC diagnostics.
Standardizing New Materials, Processes, and Equipment for Microelectronics - CalNet	Facilitating the measurement of S-parameters in integrated circuits by distributing research-grade on-wafer calibration kits and integrating NIST models into commercial software, culminating in a round robin evaluation.

Grand Challenge 4:
Modeling and Simulating Semiconductor Materials, Designs, and Components



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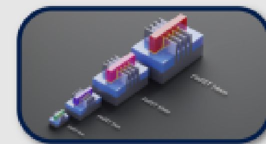
The challenge: Seamlessly model and simulate the entire semiconductor value chain, from materials inputs to chip fabrication, system assembly, and end products.



The strategy: Create a suite of advanced computational models, methods, data, standards, and tools that will enable domestic semiconductor manufacturers and the value chain to improve overall yields, accelerate time to market of devices, and enhance competitiveness in global markets.

The path forward: Conduct R&D to develop a variety of effective manufacturing simulation tools and related standards that can be applied to in-line processes and model key parameters. Critical R&D areas include:

- Modeling, data analysis, and validation tools to enable efficient process development and optimization.
- Standards, protocols, and standard data for automation and virtualization.
- Measurements and standards supporting digital twins, from individual processing steps up to the complete chip fabrication and system assembly.
- Application and validation of advanced analytics such as ML and AI for modeling and optimization of complex manufacturing process design, development, automation, and integration.

GC4 Funded Research Projects

Project Title	Summary
Advancing Power Electronics with Defect Metrology	Defect measurements at both materials and device levels, enabling correlation between atomic- and microscopic-scale defects and spatial variation in electronic structure directly linked to power device performance.
Causal Green's function simulations of phonons for multiscale/multiphysics modeling of thermal transport in gate-all-around transistors	Utilizing a Causal Green's Function (CGF) method, advances thermal transport modeling in nanoscale semiconductors, seamlessly linking femtosecond to nanosecond time scales, improving numerical convergence significantly and proving effective for complex boundary value problems, particularly in modeling gate-all-around (GAA) transistors with multiple interfaces.
Electro-acoustic metrology of piezoelectric materials for wireless communications	Improving materials measurements and models to predict performance of microwave acoustic resonators, widely used to filter signals on multiple frequency bands for microelectronics and mobile communications.
High Speed Metrology for Magnetoelectronic Devices and Models	Providing precise measurement of magnetic material and device parameters in ferromagnet-based microelectronic devices, particularly for Magnetic RAM (MRAM), by expanding NIST-developed measurement methods, facilitating improved models to accelerate the development of magnetic devices.
Metrology of Nanoscopic Thermal Transport	Developing new tools for measuring thermal properties of materials, interfaces, and devices at the nanoscale, with high precision and throughput.
Molecular Dynamics Simulation of Heat Transport in Gate-All-Around Transistors	Leveraging NIST's computational resources and theoretical expertise, assess nanoscale heat transport near CMOS conductive channels through molecular dynamics simulations and measurements, with the goal of refining finite-element models and paving the way for knowledge-based engineering in the heat management of next-generation semiconductor devices.
Multiscale Modeling and Validation of Semiconductor Materials and Devices	Developing qualitative and quantitative models for advanced semiconductor heterostructures, focusing on material properties and interface quality impacts, using multi-scale, multi-fidelity computational approaches from atomistic to mesoscale levels, targeting materials like silicon, Gallium nitride (GaN), various metals, and insulator interfaces.

GC4 Funded Research Projects (cont.)

Project Title	Summary
Nanocalorimetry for Semiconductors and Semiconductor Process Metrology	Enhance direct measurement of thermal properties in nanoscale materials and devices through advancements in nanocalorimetry for application to in-process monitoring of Atomic Layer Deposition and Plasma Processing.
Quantitative Assessment of Defects and Related Modeling Parameters in GaN Semiconductor Devices	Validated data on defects in Gallium nitride (GaN), Aluminum gallium nitride (AlGaN), and Silicon carbide (SiC) semiconductors, identifying their physical and chemical structures to aid foundries in defect elimination, thereby enhancing performance in power electronics and RF communications for the electrification of the U.S. economy and advancement of 5G/6G technologies.
RF Channel Propagation Measurements and Models for Communications Circuits	Developing novel measurements and instruments for characterizing RF propagation and developing models and datasets for use in modeling and simulation of RF communications circuits.
RF Metrology for Models of High-Frequency Transistors	Developing and verifying high-frequency transistor models through new on-wafer standards, precision noise measurements, enhanced characterizations, technology-tailored models, and cross-frequency verification with key performance indicators, addressing the challenges in yield and reproducibility in advanced semiconductor technology.
Thermoreflectance Thermal Property Measurements for Heterogeneously Integrated Materials and Power Electronics	Advancing the characterization of thermal properties in microelectronics and power electronics using Transient Thermoreflectance (TR) metrology, the initiative collaborates with industry and instrument vendors to validate and enhance TR methods, providing accurate data, protocols, and reference standards.
Time-resolved emission microscopy for circuit evaluation and failure analysis	Enhancing Time-resolved-emission microscopy (TREM) for advanced semiconductor circuit analysis by improving sensor sensitivity and pixel count, utilizing NIST's single-photon detectors scaled to the megapixel level.

Atom Probe Tomography: Nanostructured Semiconductor Materials, Interfaces, and Devices

Ann Chiaramonti Debay

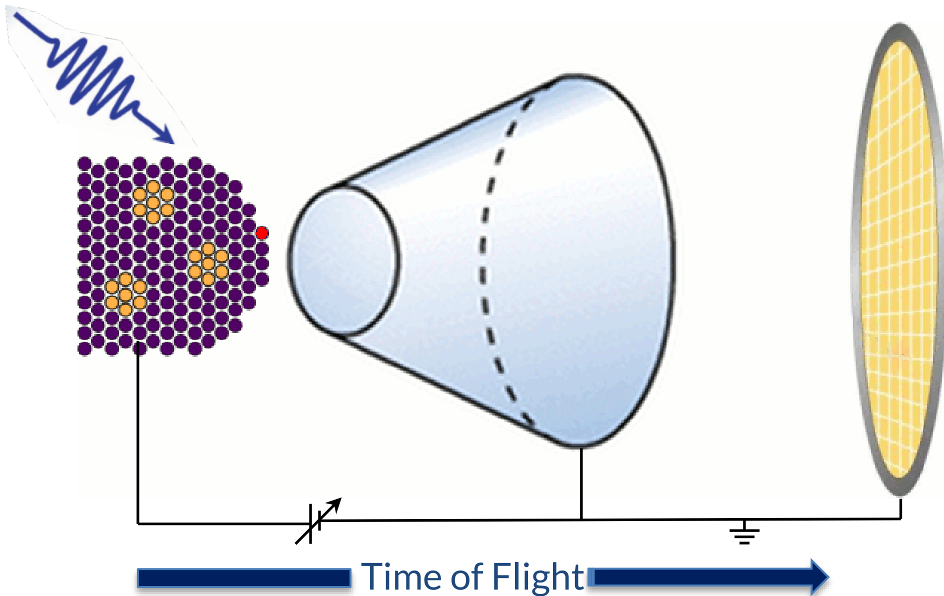
Material Measurement Laboratory

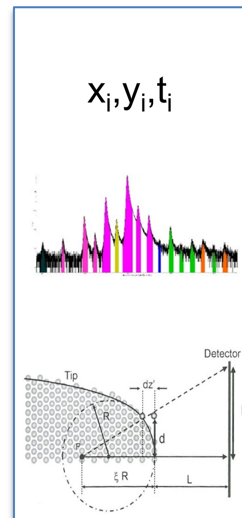
CHIPS Metrology Webinar | January 16, 2024

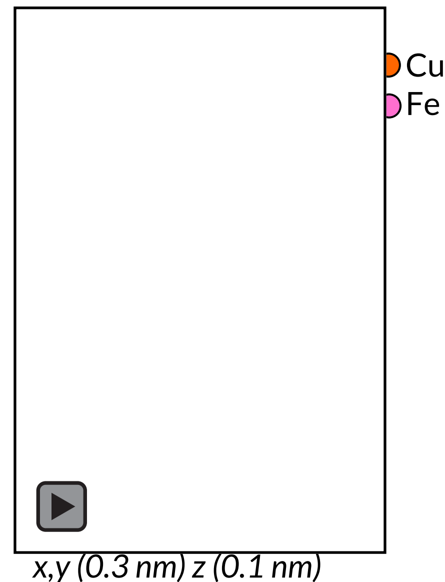
NIST National Institute of Standards and Technology
U.S. Department of Commerce

CHIPS for America

What is Atom Probe Tomography?







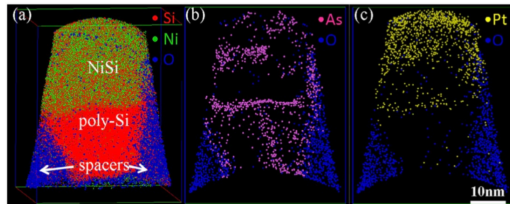
APT unique among 3D chemical mapping techniques: atom maps of any isotope with sub-nm spatial resolution, ppm sensitivity, and equal detection efficiency

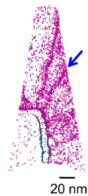
What problem are you trying to solve?

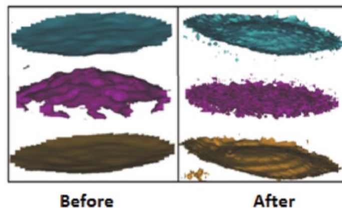
CHIPS for AMERICA

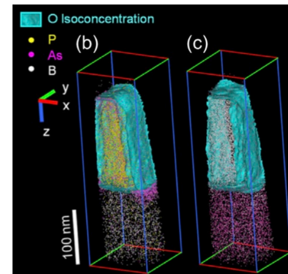
APT employed by a majority of the 10 largest semiconductor manufacturers worldwide – near in-line metrology
- Process development, failure analysis, and competitive engineering

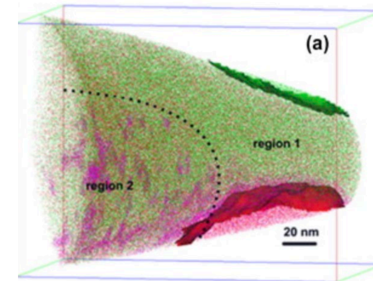
Dopant concentrations and spatial distributions, composition, interfacial chemistry, interfacial roughness, evidence of nucleation and clustering, diffusion, etc.
in nm-sized regions and structures

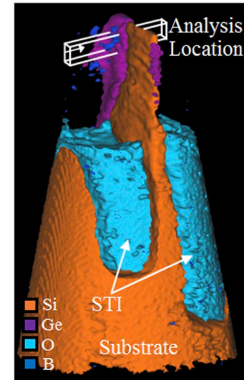












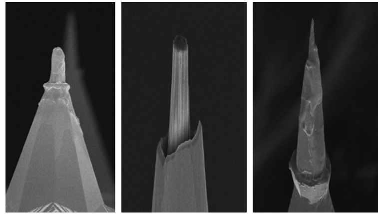
doi.org/10.1016/j.scriptamat.2017.09.004, doi.org/10.1016/j.mee.2013.12.018, doi.org/10.1002/admi.201500713, doi.org/10.1016/j.ultramic.2017.12.013.

What problem are you trying to solve?

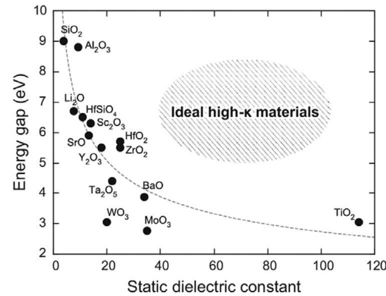
CHIPS for AMERICA

Hardware, experimental techniques, and analysis methods often come up short

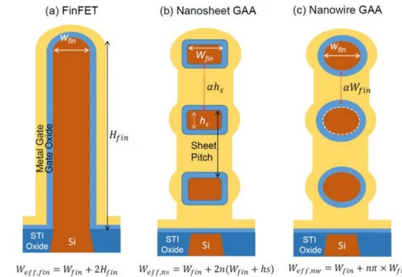
Industry roadmaps highlight importance, but recognize need for improvement



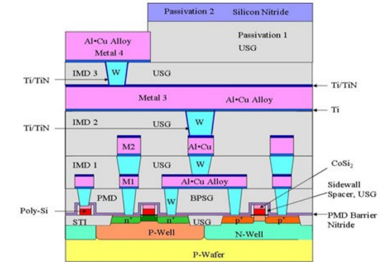
Specimen fracture



Oxide composition

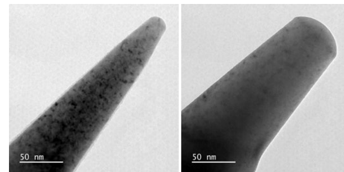


Metal/oxide interfaces



Tungsten

Results depend on specimen geometry and run conditions.



Specimen geometry

Run conditions

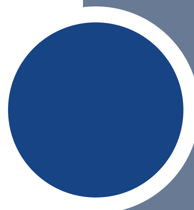
doi:10.1557/jmr.2019.335, doi:10.3390/nano12101739

Why does it matter?

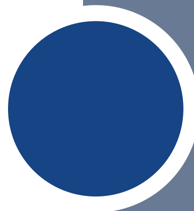
Improvements in APT would revolutionize its use in industry.

For some problems, it is the *only technique* capable of providing the information needed.

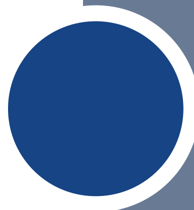
It can measure things in ways that TEM and SIMS cannot.



Improve device performance
Correlate atomic-scale changes in process to device performance



Increase yield
Diagnose root-cause failures at the atomic scale

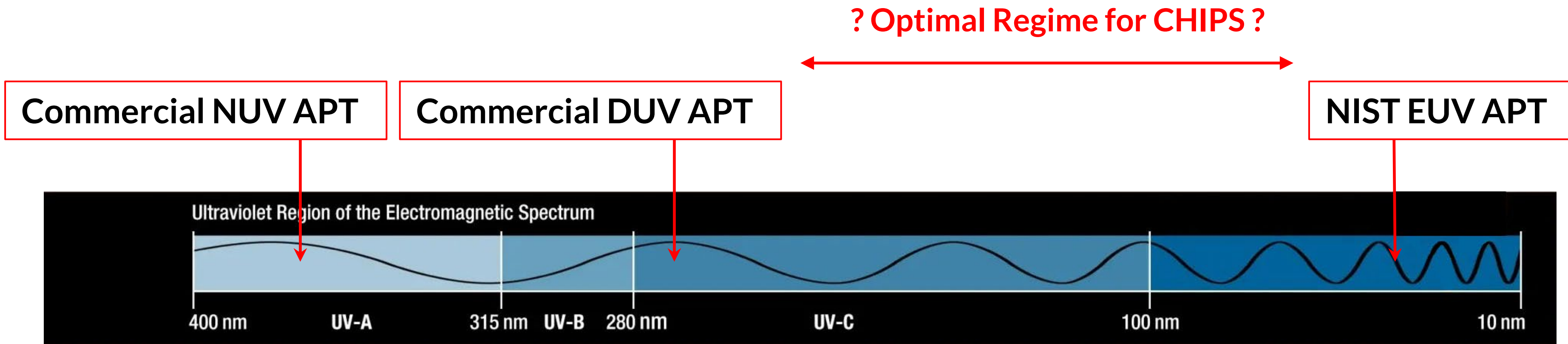


Accelerate time to market
Decrease R&D cycle time

What is your approach?

<u>Thrust 1:</u> Determine the optimal laser pulsing strategy for CHIPS materials.

Tailor APT pulsing to optimize absorption and thermophysical response for complex semiconductor materials, heterostructures, and devices.



What is your approach?

Thrust 2: Optimize measurements on commercial APT systems using specimens and materials provided by CHIPS stakeholders.

NIST-B getting early DUV commercial APT

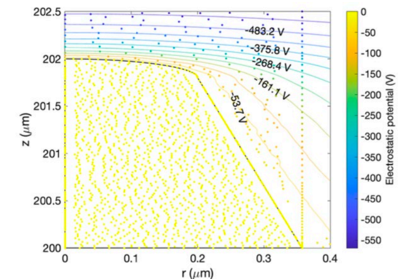
Best Known Methods for measurements on commercial systems – same as industry uses

Thrust 3: Develop advanced electrostatic modeling approaches to simulate field ion evaporation using structures/geometries provided by CHIPS stakeholders.

Understand fundamental physics

Improve reconstruction fidelity

Decrease uncertainty in measurements



Who is on your team?

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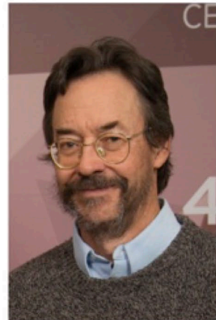
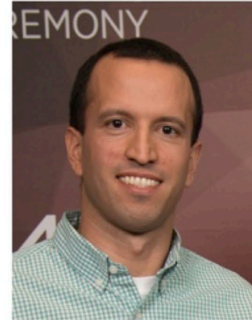
Material Measurement Lab		Physical Measurement Lab		NRC Postdoc
				
Ann Chiaramonti	Benjamin Caplins	Norman Sanford	Luis Miaja-Avila	Jacob Garcia

Materials science, physics, chemistry, ultrafast lasers, spectroscopy, laser-matter interactions, materials characterization, high-field nanoscience, semiconductor processing

---

- ✓ Proven record of building advanced experimental atom probe instruments (IMS FY16)
- ✓ 2 APT patents awarded, 2 more disclosures filed with NIST (1 related to this work)
- ✓ Patent license
- ✓ 3 semiconductor industry-related CRADAs (4th, 5th in the works)
- ✓ Collectively 35+ years experience in APT

How will you engage with industry?

Partner with Metrology Tool Manufacturer	Partner with US Foundries	International Standards
CRADA, License, CRDO	**CRADA, CRDO**	**IFES/ISO**
Co-develop optimal atom probe microscope for semiconductor applications Specimens provided by US foundries Time to market decreased	Foundries provide specimens/geometries/ materials of interest NIST optimizes measurements on commercial tools	Definition of terms through IFES and ISO/TC 201 *Surface Chemical Analysis* Round Robin testing of standard samples, standard run conditions through VAMAS?
Commercial atom probe microscope optimized for semiconductor manufacturing	**NIST Best Practice Guide, scientific publication, data products from simulation efforts**	**New terms in ISO/TC 201**

Accurate Cure Kinetics, Stress and Warpage Measurements for Next-Generation Microelectronics Packaging Under Device Relevant Conditions

Ran Tao

Material Measurement Laboratory

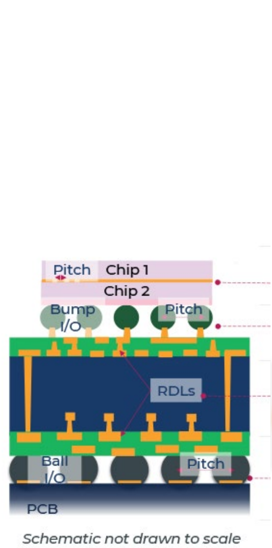
CHIPS Metrology Webinar | January 16, 2024

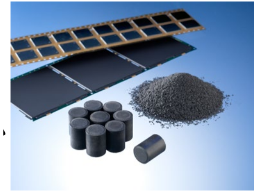
CHIPS TEAM
Amanda Forster
Chris Soles
Ran Tao
Alex Landauer
Young Jong Lee
Steve Stranick

NIST National Institute of Standards and Technology
U.S. Department of Commerce

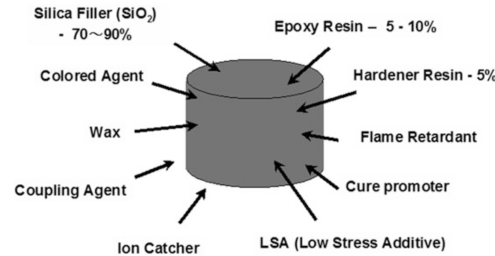
CHIPS for America

Polymer Materials for Advanced Packaging

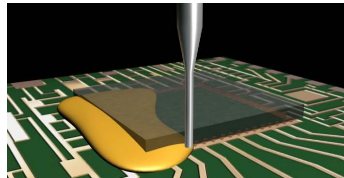




Materials are produced in different forms (liquid, film, paste, granulated)



Multi-component, highly filled materials with proprietary additives and ingredients

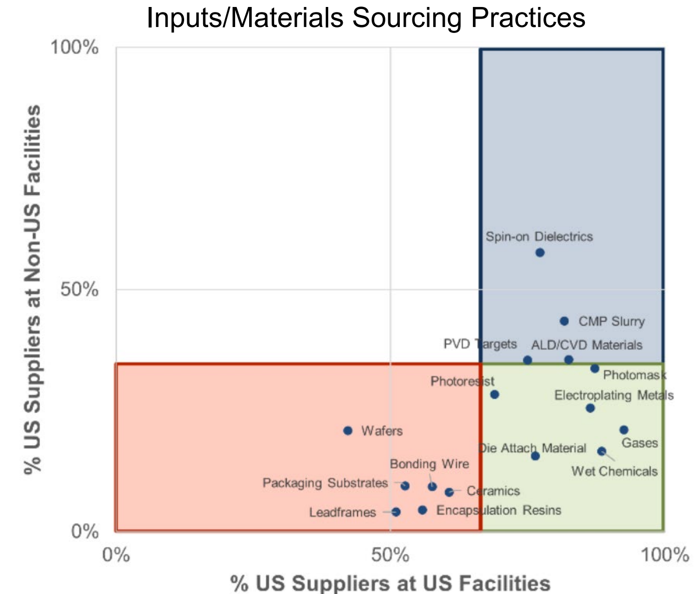


Materials are transformed from liquids or melts to cross-linked solids to protect the sensitive electronics they surround

(Source: Status of the Advanced Packaging 2023, Yole Intelligence)

What is the problem we are trying to solve?

- Polymeric materials for electronic packaging are purchased from overseas suppliers.
- Challenges for domestic manufacturers:
  - ➢ ***Lack of accessible materials data***
  - ➢ ***Inability to verify thermomechanical properties of incoming feed materials***
- Complications in Current Techniques:
  - ➢ *Present metrologies limited for complex cure kinetics*
  - ➢ *Complicated environments with temperature and humidity fluctuations*
  - ➢ *Compromises the validity of measurements and predictions*



The industry is shifting to complex chemistries and multifunctional fillers, necessitating improved metrological and analytical approaches for engineering design.

(Source: Status of the Advanced Packaging 2023, Yole Intelligence)

Working example

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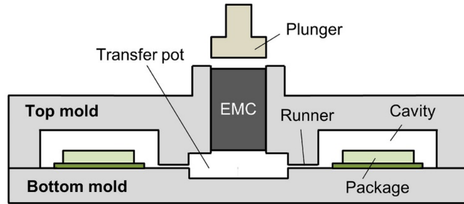
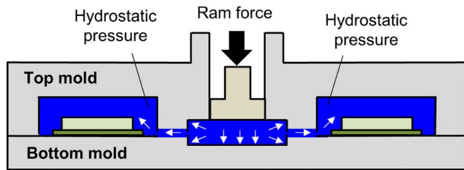
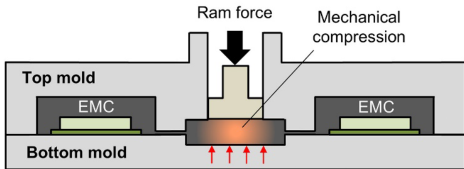
Transfer Molding Process



(a)



(b)



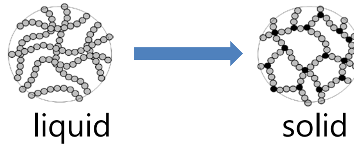
(c)

DOI: 10.1016/j.microrel.2022.114480

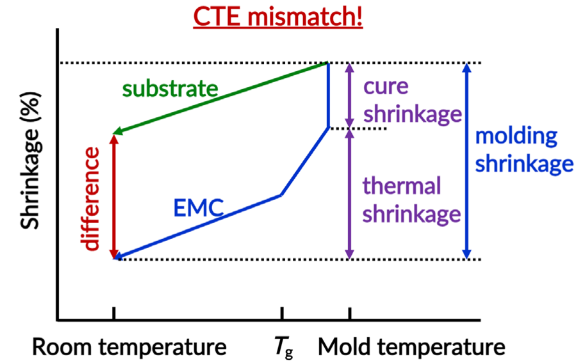
Material is heated to lower its viscosity

Material starts as a viscous liquid and flows into the mold increasing pressure

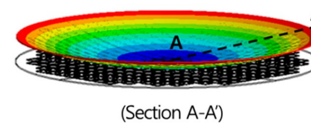
Material cures at high T and P



liquid solid



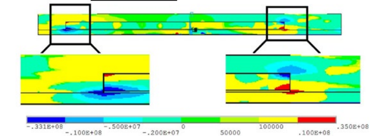
Warpage



(Section A-A′)

DOI: 10.3390/mi7060095

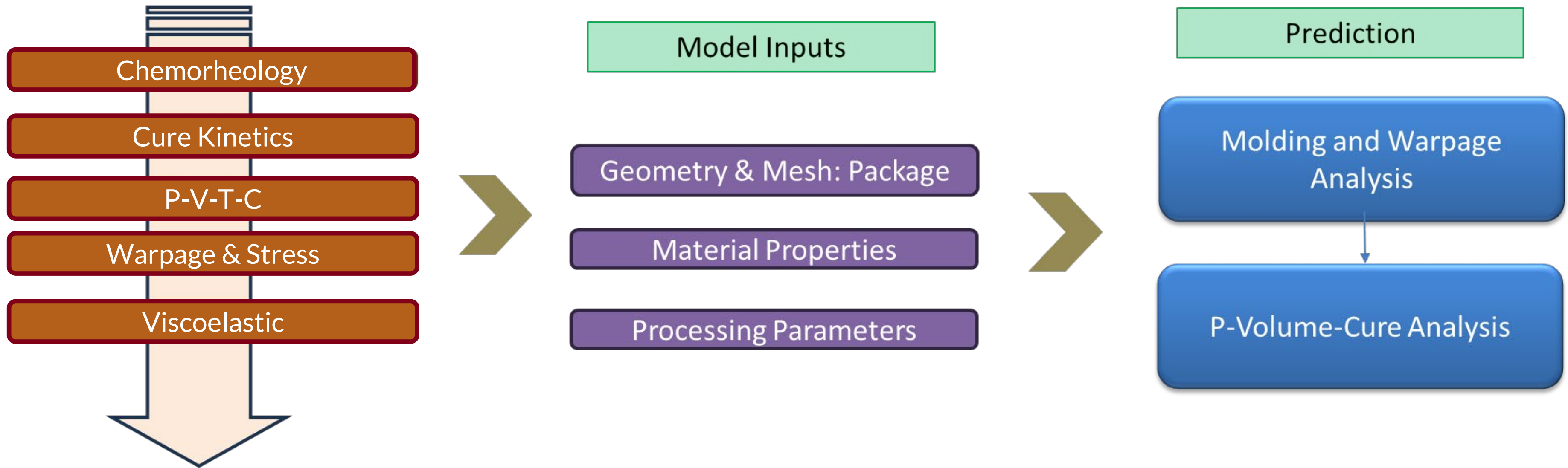
Residual Stress



DOI: 10.1109/TCPMT.2021.3070893

Mech. Properties, CTE, shrinkage, warpage are affected by (degree of cure, formulation, temperature, pressure, time, humidity)

How are we going to solve the problem?



Measurement Challenges:

- Small polymer fraction
- Heterogeneous formulations
- Overlapping and competing reactions
- Viscoelasticity & RH effects

Adapted from Fang et al., *Int. J. of Adv. Man. Tech. (2023)* ***124***, 1017-1039

Cure Kinetics and Chemorheology

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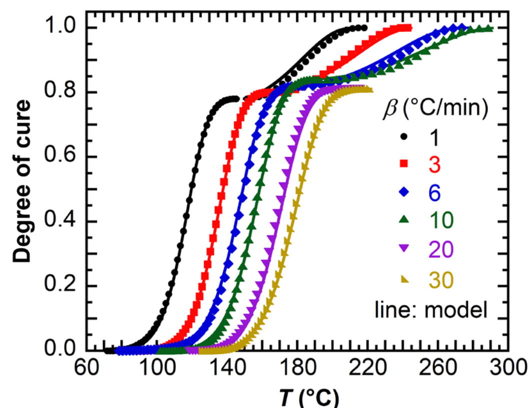
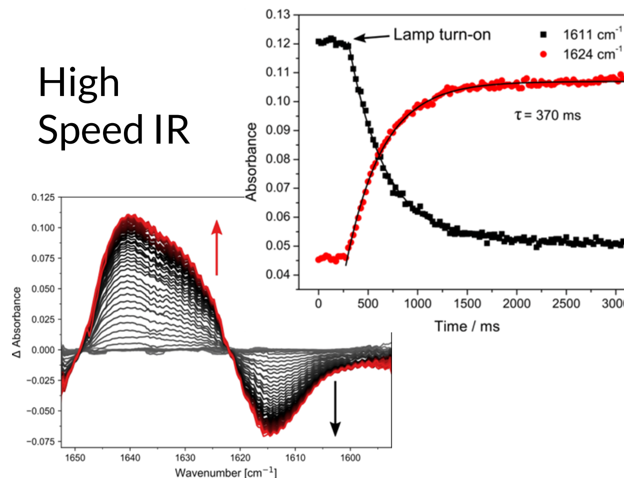
Accurate cure kinetic models require measurement of degree of cure, crosslink density, and modulus as a function of pressure, time, and temperature

High Pressure Differential Scanning Calorimetry



DOI: 10.1109/ECTC51909.2023.00225

High Speed IR

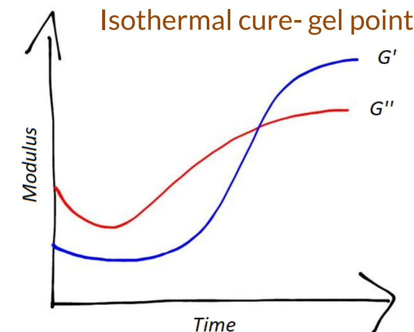


https://irsweep.com/application-notes/rapid-reaction-monitoring-of-curing-processes-with-the-iris-f1/

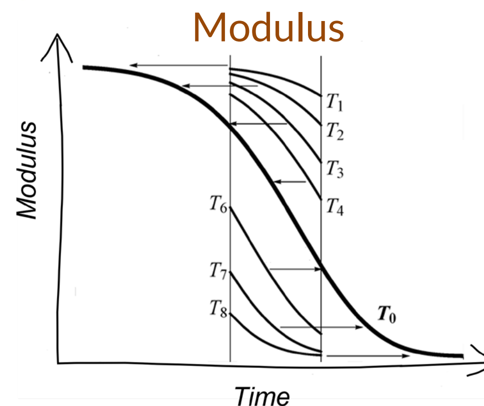
+

solid-state NMR

Viscoelasticity



Modulus



Heterogenous Chemical & Mechanical Properties

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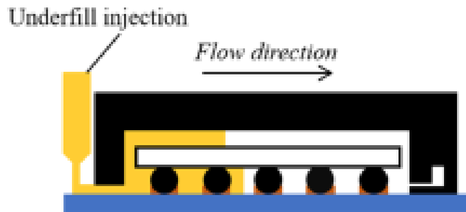
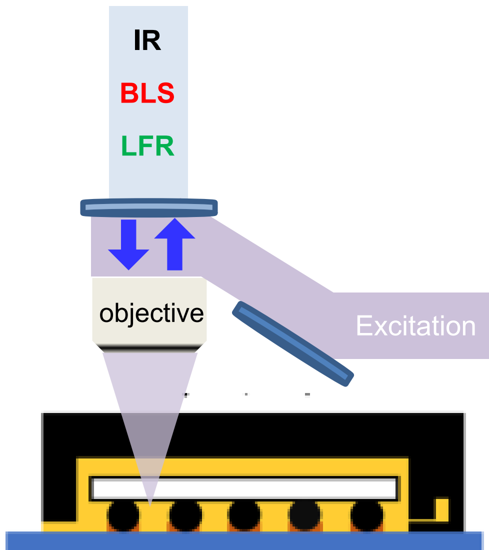


https://doi.org/10.1115/1.4050697



Heterogeneous integration brings together disparate materials w/ different heat capacities, thermal conductivities, and surface energies.

This in turn leads to:

- Local variations in the resin degree of cure
- Local variations of key mechanical properties
- Resin properties that are not uniform!

Measurements that quantify these heterogeneities and validated across length scales are critically needed

Development of microscopy tools for imaging these critical properties:

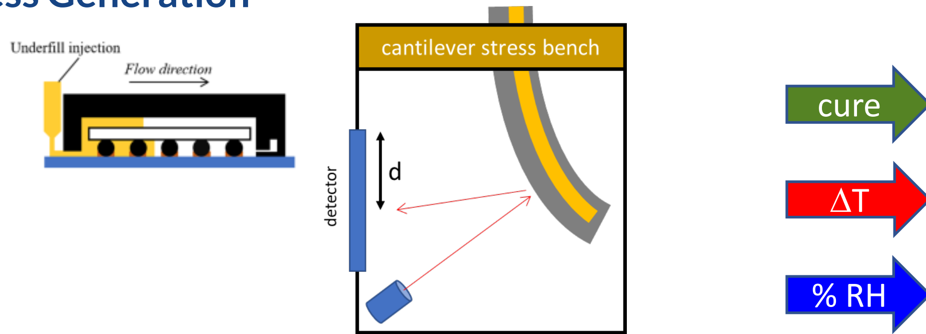
Infrared spectroscopy (QCL-IR) for local variations in the degree of cure

Brillion Light Scattering (BLS) for local variations in the stiffness / modulus

Low Frequency Raman (LFR) for local variations in the GHz mechanical dissipation

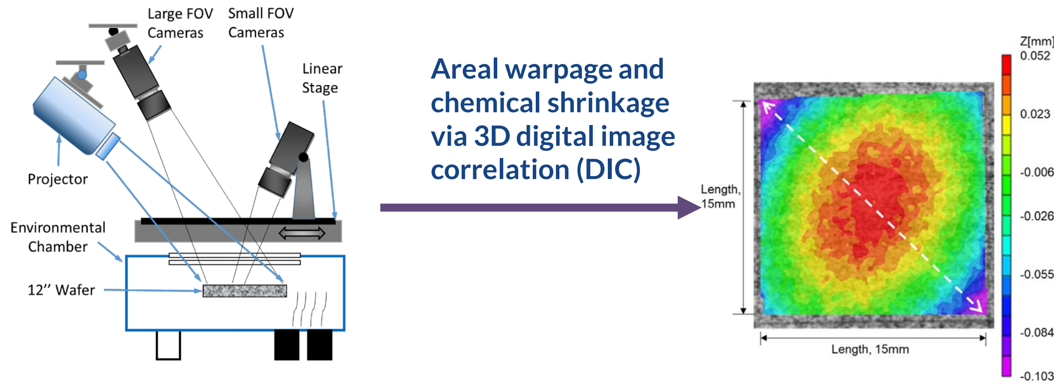
Stress Generation & Dynamic Warpage in Packaging

Stress Generation



- Quantify resin stress thru cantilever deflection (stress ∝ d)
  - Cure shrinkage
  - CTE mismatch
  - Hygrothermal

Shrinkage and Warpage



- In-situ full field strain measurement during cure and post-gelation
- Multiple fields of view dynamic warpage measurement under thermal loading
- Semiconductor specific calibration and optimization protocols

DOI: 10.1109/ECTC.2015.7159627

DOI: 10.1007/s00170-018-2834-8

Outcomes & Impacts

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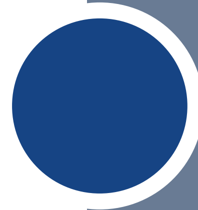
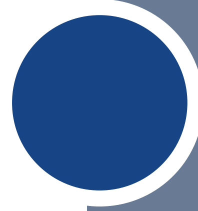
Quantitative structure-property-processing relationships



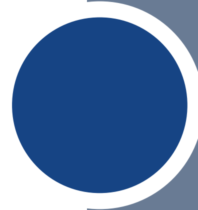
Accelerating introduction of new and improved packaging materials into process workflows

Research Grade Test Materials and Analysis Toolkits



Quantitative measures of environment-materials-system interactions

Materials and processing data needed to build accurate predictive models (*chemorheology, cure kinetics, CTE, stress, shrinkage, warpage*)



Accelerate time to market
Decrease R&D cycle time

Thermoreflectance Thermal Property Measurements

Joshua Martin, Dylan Kirsch, and Mark McLean

Material Measurement Laboratory | National Institute of Standards and Technology | Gaithersburg, MD

CHIPS Metrology Webinar | January 16, 2024

CHIPS TEAM

Joshua Martin
Dylan Kirsch
Mark McLean
Ron Warzoha (USNA)
CHIPS Postdoc (TBD)

NIST MATERIAL MEASUREMENT LABORATORY

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The Thermal Problem and a Path Forward

Thermal conductivity, heat capacity, and interface conductance are fundamental properties that govern semiconductor devices

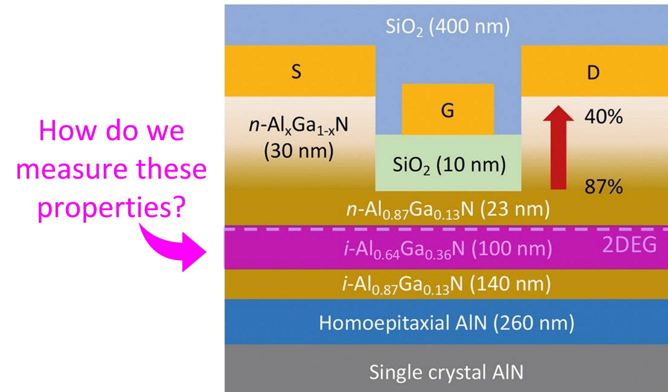
- These properties are not characterized at device length scales and growth conditions
- How do we measure materials in semiconductor devices?

Thermoreflectance (TR) is poised as the emergent industry standard measurement technique

- Can uniquely resolve the in-situ thermal properties of thin film, embedded, and multilayer materials
- Only recently commercialized

Accurate and reliable thermal data would improve:

- Device design and modeling
- Thermal management and device performance
- Device reliability and operational lifespan



Schematic cross-section of a metal-oxide-semiconductor-heterojunction-field-effect-transistor (MOSHFET) on bulk AlN substrate

A. Mamun *et. al.*, Applied Physics Express 16, 061001 (2023)

Thermoreflectance (TR)

Transient TR uses modulated laser heating and thermal models to probe thermal properties

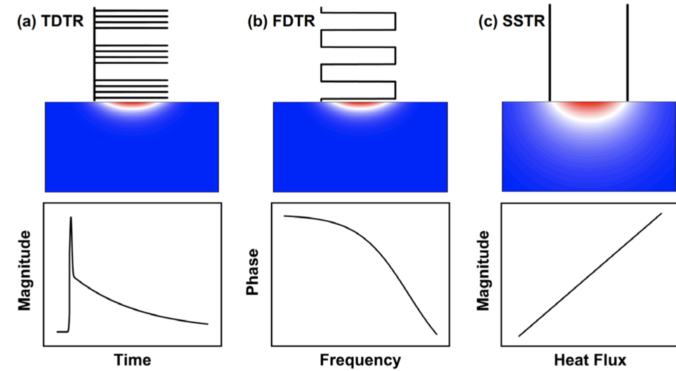
- The Coefficient of TR relates a material's change in temperature to the resulting change in optical reflectance
- Measures thin film, embedded, and multilayer materials
- Large property range: ≈ 0.1 W/mK to ≈ 2000 W/mK
- Simultaneously probe at variable depths

Techniques leverage sensitivity to different properties:

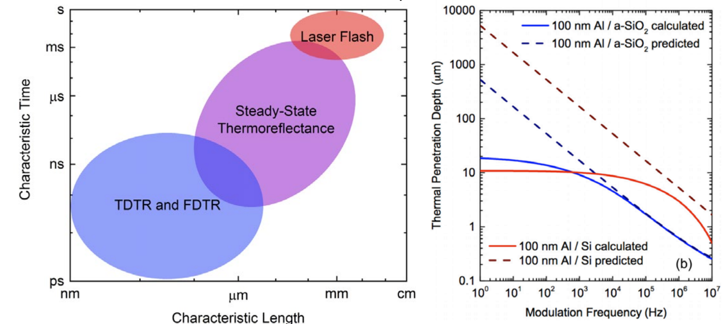
- Time Domain TR (TDTR)
- Frequency Domain TR (FDTR)
- Steady State TR (SSTR)

Challenges to wider adoption:

- Custom built, requiring experienced staff to operate
- Data fitting and uncertainty analysis can be complex
- Need for standards and improved protocols



Characteristic excitations and corresponding responses for (a) TDTR, (b) FDTR, and (c) SSTR techniques

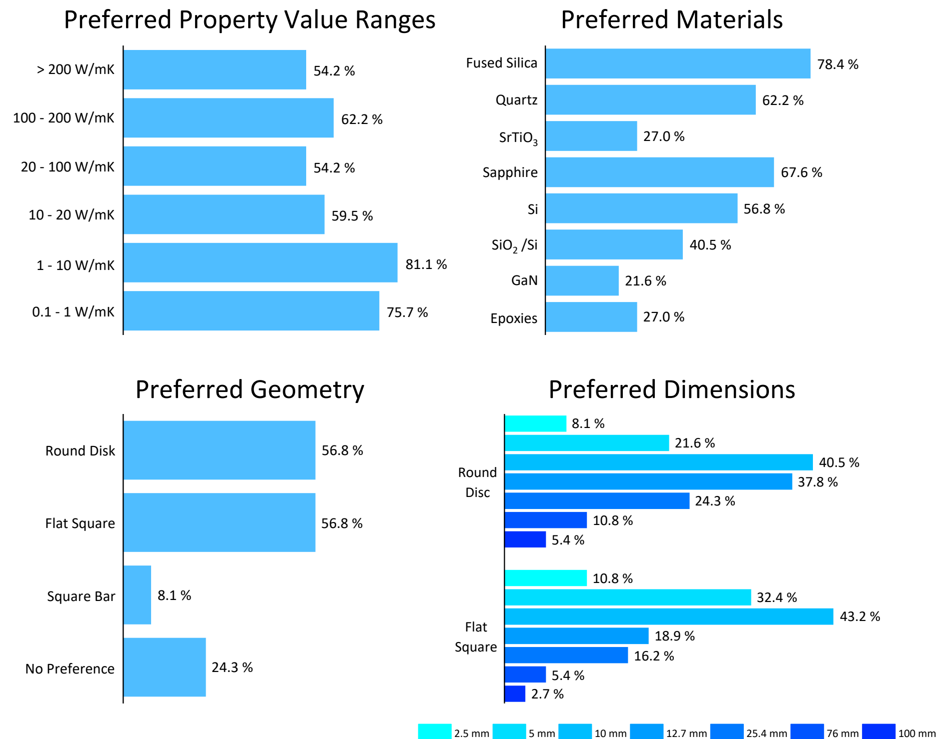


Characteristic length and time scales (left), and frequency dependent penetration depth (right)
D. Olson, J. Braun, P. Hopkins, *Journal of Applied Physics* 126, 150901 (2019)

Thermal Conductivity RGTM Suite

Objective 1: Develop thermal conductivity standards that span the materials and property value ranges relevant for semiconductor devices.

- Developing a suite of Research-Grade Test Materials (RGTMs)
    - A new *pre-standards* development tool
    - Faster development time (≈ 1 year)
    - RGTMs *do not* provide traceability
- Based on 25 question thermal reference survey
- Materials: fused silica, quartz, sapphire, silicon, and silicon/SiO2 (for interface conductance)
- Geometry: 10 mm x 10 mm; thickness: ≈ 1 mm
- An Interlaboratory Study will compare different measurement techniques and evaluate fitness of materials for further RM or SRM development
- RGTMs will be available for free by Fall 2024



https://nvlpubs.nist.gov/nistpubs/SpecialPublications/NIST.SP.260-136-2020.pdf

Frequency Domain TR (FDTR) Instrument

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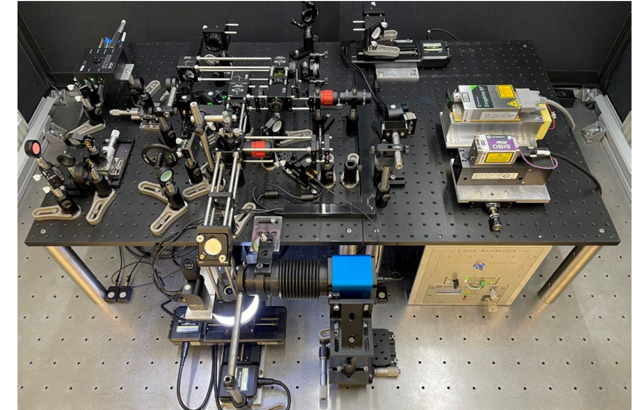
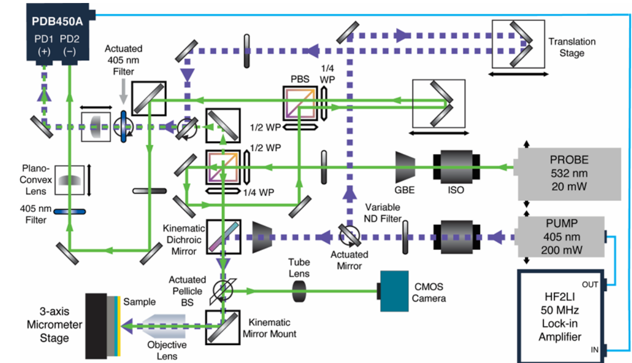
Objective 2: Leverage our existing custom-built instrumentation, expertise, and collaborations to improve and refine TR thermal measurement methods, protocols, and instrumentation that are likely to be adopted by industry.

- A thin Au transducer film is sputter-deposited on the sample
- A modulated *pump* laser (405 nm) heats the transducer, inducing a corresponding periodic change in reflectivity
- A second *probe* laser (532 nm) is coaxially focused and reflected from the surface; the reflected probe beam acquires the same modulation as the pump but with a phase lag
- The phase of the reflected probe beam is measured as a function of the modulation frequency of the pump beam (100 Hz to 20 MHz)
- Properties are obtained by modeling a fit of the phase curve
- Publishing a comprehensive instrumentation guide
- Implementing instrument improvements



Photograph of the NIST custom FDTR Instrument



Beam Path Diagram & Instrument Schematic

Thermal Model and Property Extraction

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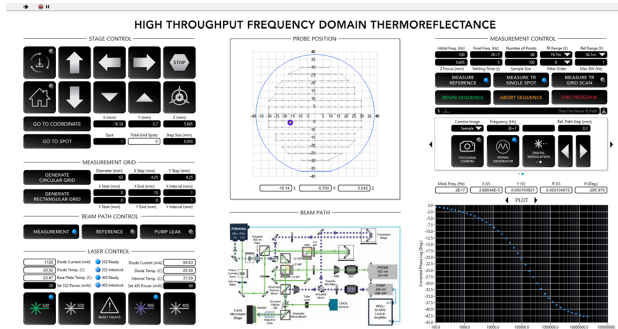
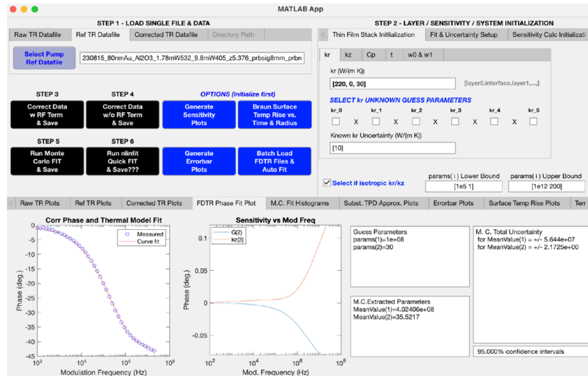
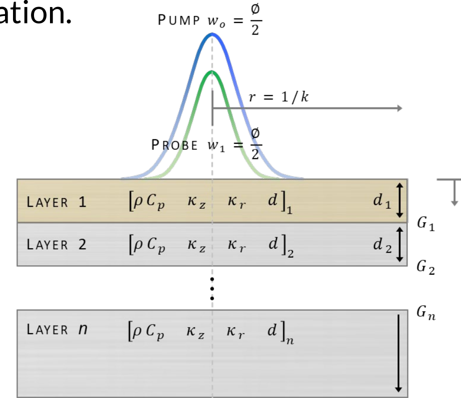


Custom LabVIEW code fully automates safety, laser operation, measurement sweeps, optical component flippers, beam paths, focal plane alignment, and motorized stages



Custom MATLAB Interface simplifies complex fitting

Each layer is modeled with a volumetric heat capacity, cross-plane and in-plane thermal conductivities, layer thickness, and thermal boundary conductance at each interface. The surface temperature is numerically solved using the heat diffusion equation.



$$I(r,t) = \frac{2P(t)}{\pi w_o^2} e^{\frac{-2r^2}{w_o^2}}$$

ρC_p : Volumetric specific heat capacity

κ_z : Cross-plane thermal conductivity

κ_r : In-plane thermal conductivity

d_n : Layer thickness

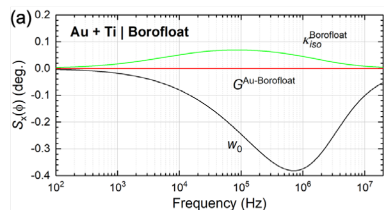
G_n : Thermal boundary conductance

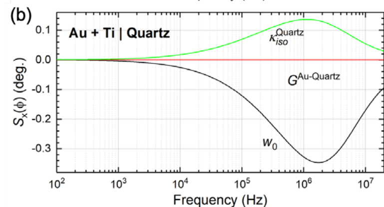
$$\mathbf{H}(r,\omega) = \frac{\kappa_r}{r}\frac{\partial}{\partial r}\left(\frac{\partial \theta}{\partial r}\right) + \kappa_z \frac{\partial^2 \theta}{\partial r^2} = \rho C_p \frac{\partial \theta}{\partial t}$$

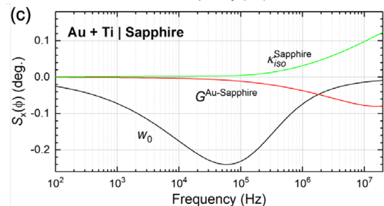
$$\phi = \tan^{-1}\frac{\Im(\mathbf{H}(r,\omega))}{\Re(\mathbf{H}(r,\omega))} + \phi_{ext}$$

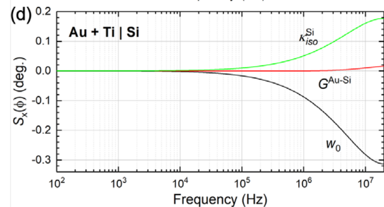
A.J. Schmidt et. al., Rev. Sci. Instrum. 80, 094901 (2009)

Sensitivity Calculations and Reference Measurements

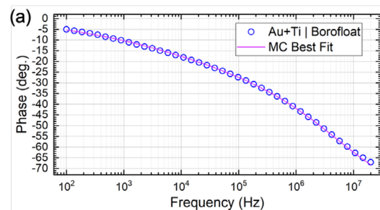


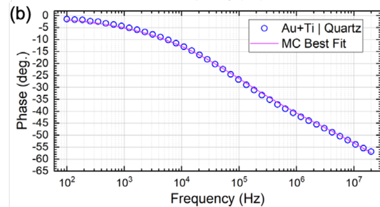


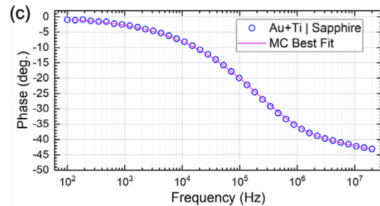


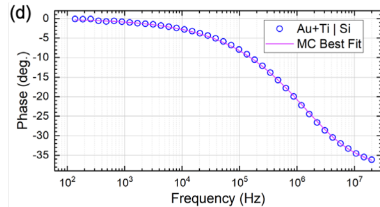


Sensitivity Plots









Measured and Fitted Phase Data

Sensitivity is calculated to determine which parameters can be extracted with the highest confidence

- Can modify setup (pump and probe radii, frequency scan region, thermal properties of the layers and substrate) to increase sensitivity to a parameter of interest
- Calculated as the phase response to a small (1 %) perturbation of a selected thermal parameter

$$S_x(\omega) = \frac{\partial \phi(\omega)}{\partial \ln x}.$$

			MATLAB nlinfit & nlparci Fit Uncertainty		Monte Carlo Fit & Total Uncertainty	
	Reference Values		Unknown Fit Parameter 1	Unknown Fit Parameter 2	Unknown Fit Parameter 1	Unknown Fit Parameter 2
Substrate	ρC_p (MJ m^{-3} K^{-1})	κ_{iso} (W m^{-1} K^{-1})	κ_{iso} (W m^{-1} K^{-1})	G (MW m^{-2} K^{-1})	κ_{iso} (W m^{-1} K^{-1})	G (MW m^{-2} K^{-1})
Borofloat Silica Glass	1.83 ± 0.1 [a]	1.41 ± 0.07 [a]	1.28 ± 0.06	> 200	1.23 ± 0.15	> 200
Quartz	2.0 ± 0.2 [b]	8.15 ± 1.0 [b]	8.15 ± 0.5	> 200	8.27 ± 0.62	> 200
Sapphire	3.06 ± 0.1 [c]	35.0 ± 5 [d,e]	35.5 ± 1.6	> 200	35.4 ± 2.6	> 200
Silicon	1.66 ± 0.1 [f]	145 ± 10 [g,h]	152.9 ± 3.2	> 200	153.0 ± 10.3	> 200

Support for DARPA THREADS Program

Objective 3: Provide Independent Verification & Validation measurements for the DARPA THREADS Program to improve thermal management in wide bandgap Field Effect Transistors (FETs).

Technologies for Heat Removal in Electronics At the Device Scale (THREADS)

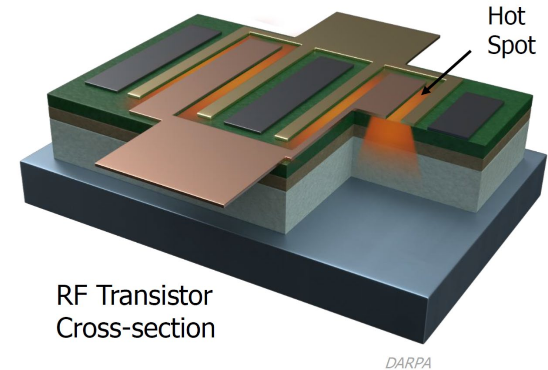
- Program goal: improve thermal management in wide bandgap Field Effect Transistors (FETs)
- Kickoff December 18-19, 2023

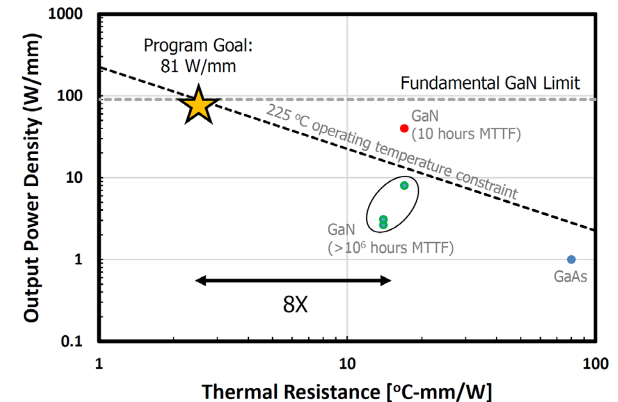
NIST's Role

- Provide Independent Verification and Validation (IV&V) thermal measurements to ensure consistency and reliability across performers
- 4-year funded participation

Impact

- New industry collaborations and interactions
- Access to cutting-edge materials, devices, and measurement challenges
- Additional resources to improve instrumentation
- Increased stakeholder buy-in for thermal conductivity standards and ILS





Develop New Time Domain TR (TDTR) Instrument

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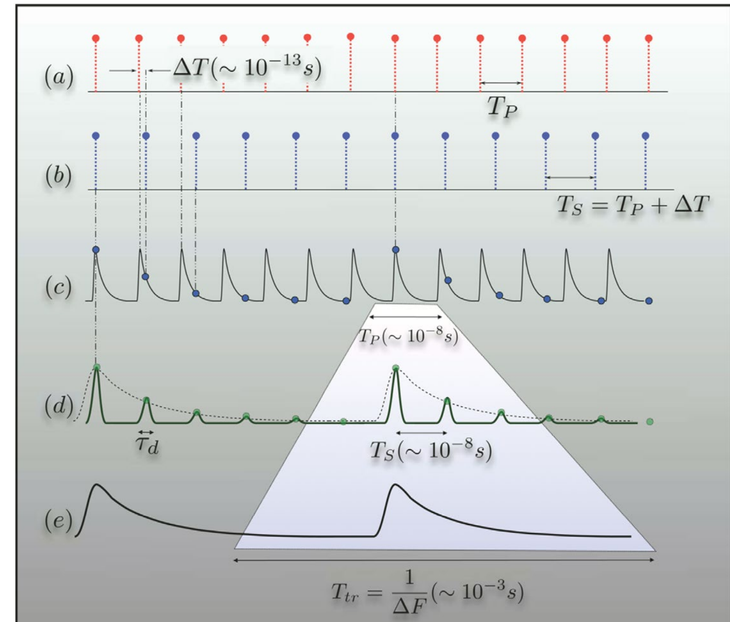
Objective 4: Design and construct a new TDTR thermal metrology instrument to more accurately measure thermal interface conductance.

- TDTR has increased sensitivity to boundary conductance
- TDTR uses much more complex and expensive lasers
- We will incorporate ASynchronous OPtical Sampling (ASOPS) using two *custom* modelocked lasers with slightly different (& variable) pulse repetition rates
- Much faster data acquisition << 1 s
- Improved uncertainty ≈ 5 %
- Compatible with Au & Al transducers for comparison
- Risk mitigation: hiring 3-term summer technical expert
- Design Summer FY24; construction Fall FY25+
- Suite of FDTR, SSTR, and TDTR instruments



Time diagram of H-TDTR signals, (a) pump beam $I_P(t)$, (b) probe beam $I_S(t)$, (c) temperature, (d) reflected probe beam signal received by the photodiode, $S(t)$, and (e) envelope of $S(t)$ delivered by the detector. Both pump and probe pulses (a) and (b) are represented by Dirac combs for clarity (duration is 100 fs). For $S(t)$, each pulse duration is the detector response time s_d.

S. Dilhaire, *et. al.*, *J. Appl. Phys.* 110, 114314 (2011)

Summary and Impact

- Develop thermal conductivity reference materials
- Develop custom TDTR instrument to more accurately measure thermal interface conductance
- Support companies that are commercializing TR thermal measurement techniques
- Provide Independent Verification & Validation measurements for the DARPA THREADS Program
- Using the TR suite, improve and refine thermal measurement methods, protocols, and instrumentation
- Provide thermal property measurements and data that directly support other CHIPS projects

Time-resolved emission microscopy for circuit evaluation and failure analysis

Jeff Shainline, Saeed Khan, Marty Stevens, Bryce Primavera, Ravin Chowdhury, Varun Verma, Rich Mirin

NIST Physical Measurement Laboratory, Applied Physics Division, Quantum Nanophotonics Group

CHIPS Metrology Webinar | January 16, 2024

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY U.S. DEPARTMENT OF COMMERCE

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The Measurement Need

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Hot electrons in a transistor channel emit mid-IR photons

Imaging these photons has been a powerful tool for circuit evaluation

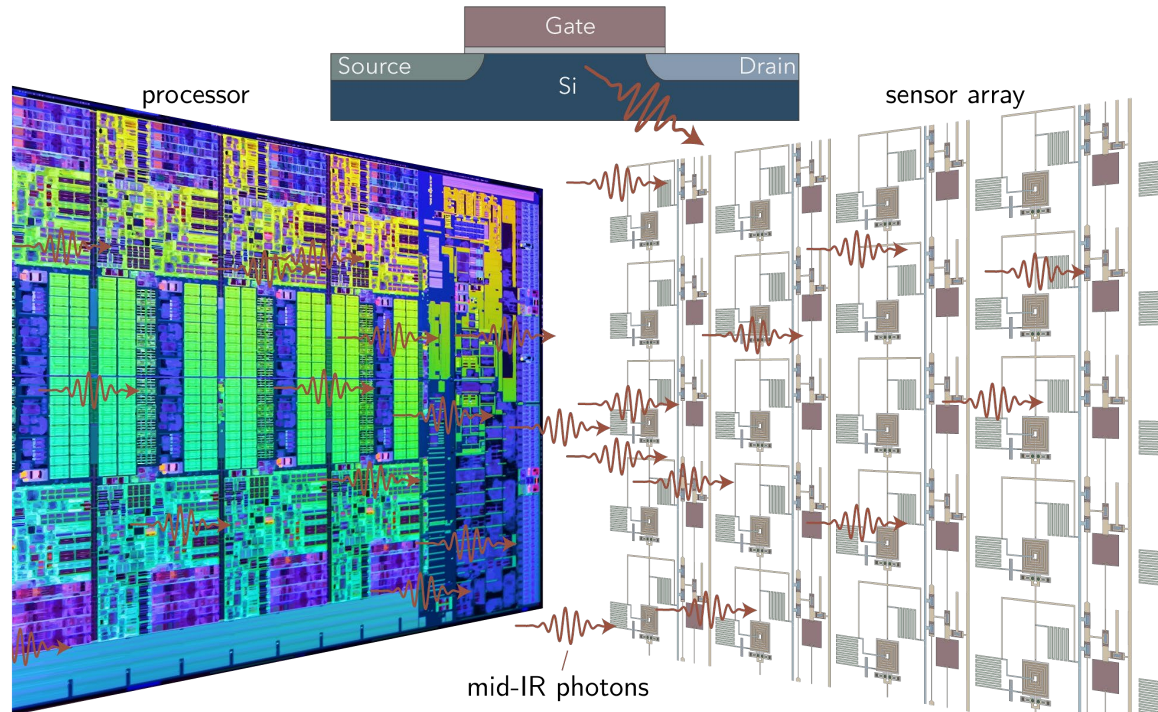
But, smaller transistors lead to:

Fainter emission signals

Below diffraction limit

And, lower V_{dd} leads to:

Longer wavelengths (2μm)



https://news.softpedia.com/news/Intel-Officially-Launches-the-Core-i7-5000X-Extreme-Edition-CPUs-457010.shtml#sgal_0

The Measurement Need

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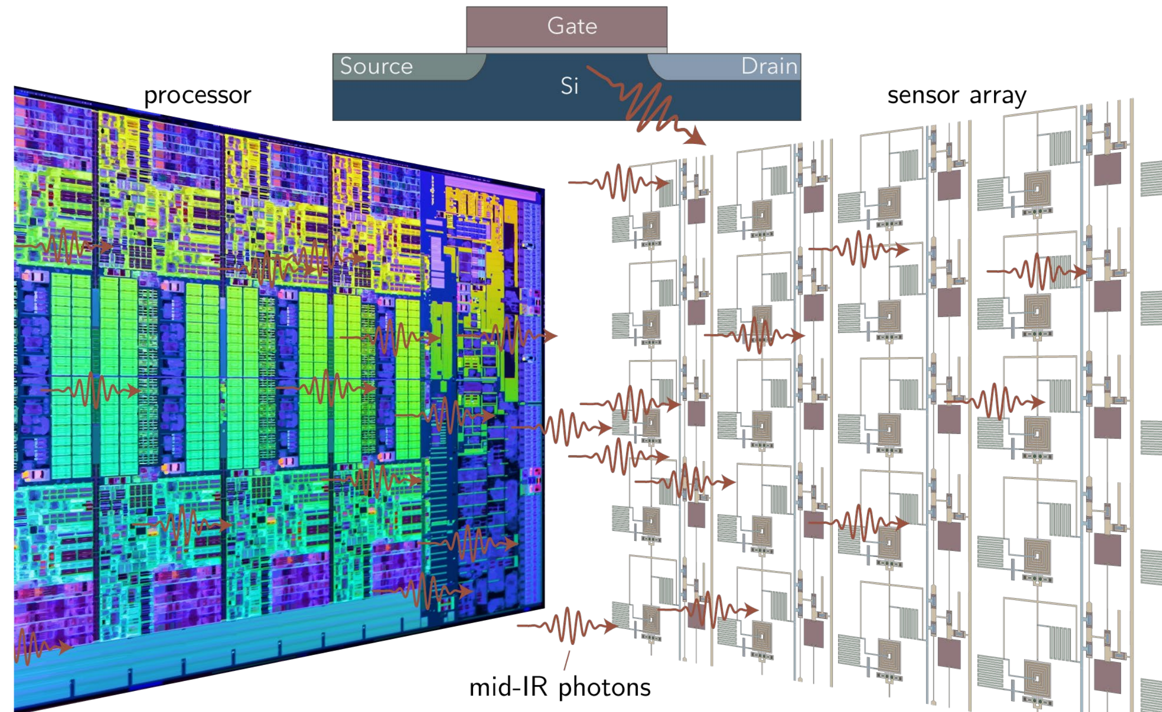
It is currently impossible to:

Characterize entire integrated circuits with billions of transistors

Extract photoemission data from individual transistors during operation



https://news.softpedia.com/news/Intel-Officially-Launches-the-Core-i7-5000X-Extreme-Edition-CPUs-457010.shtml#sgal_0

Industry Relevance

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Electronic Device Failure Analysis Technology Roadmap
Electronic Device Failure Analysis Society

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Laser-Based, Photon, and Thermal Emission

Venkat Krishnan Ravikumar, AMD
Christian Boit, TU Berlin
Kristofor Dickson, NXP

“We may be able to achieve sub-diffraction-limited emissions by separating emissions in time, which can be achieved through careful pattern execution or emerging low-energy photon-detection schemes. Superconducting nanowire single photon detectors could provide a means to effectively collect sufficient photons...”

Our Approach

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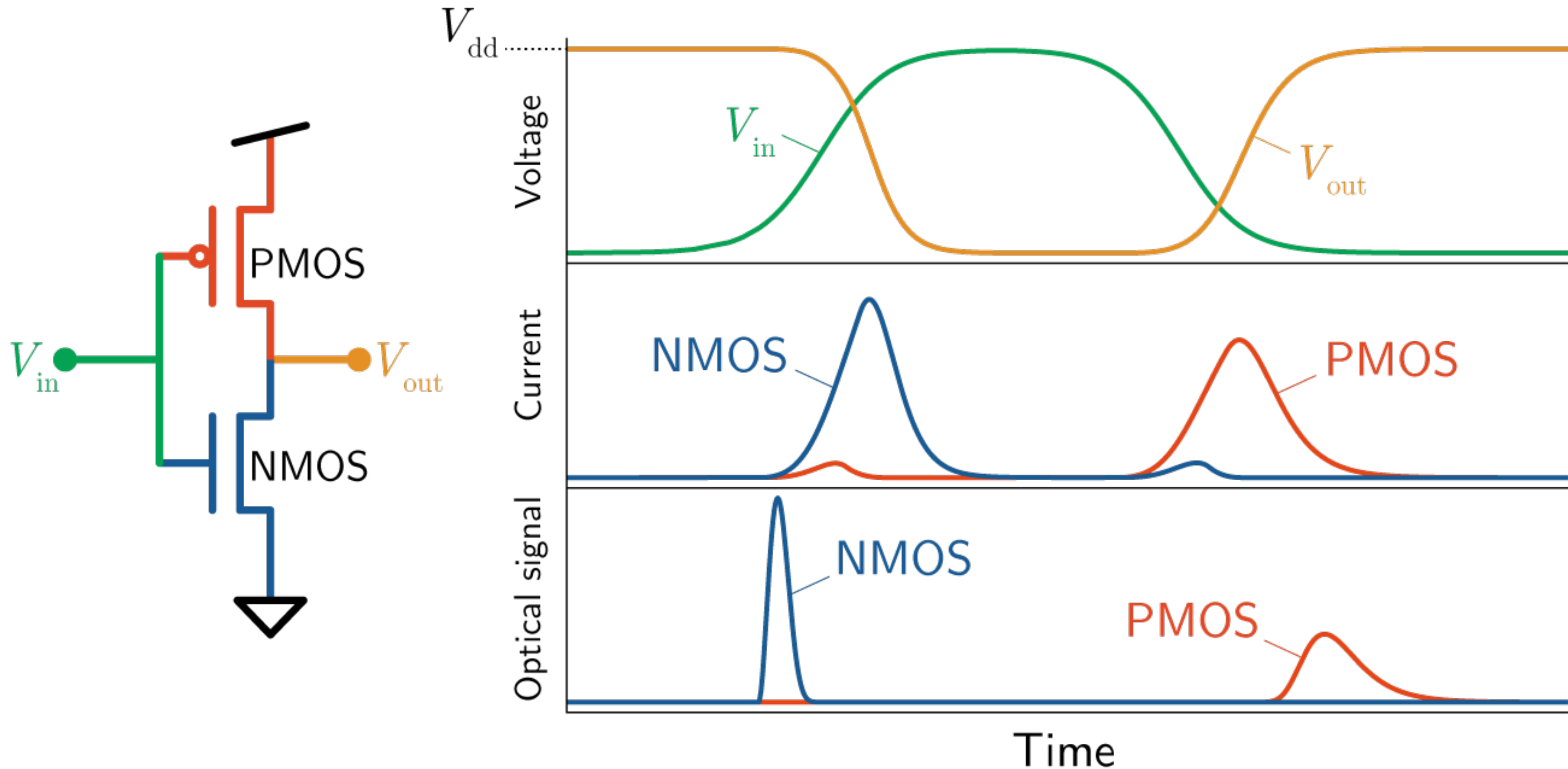
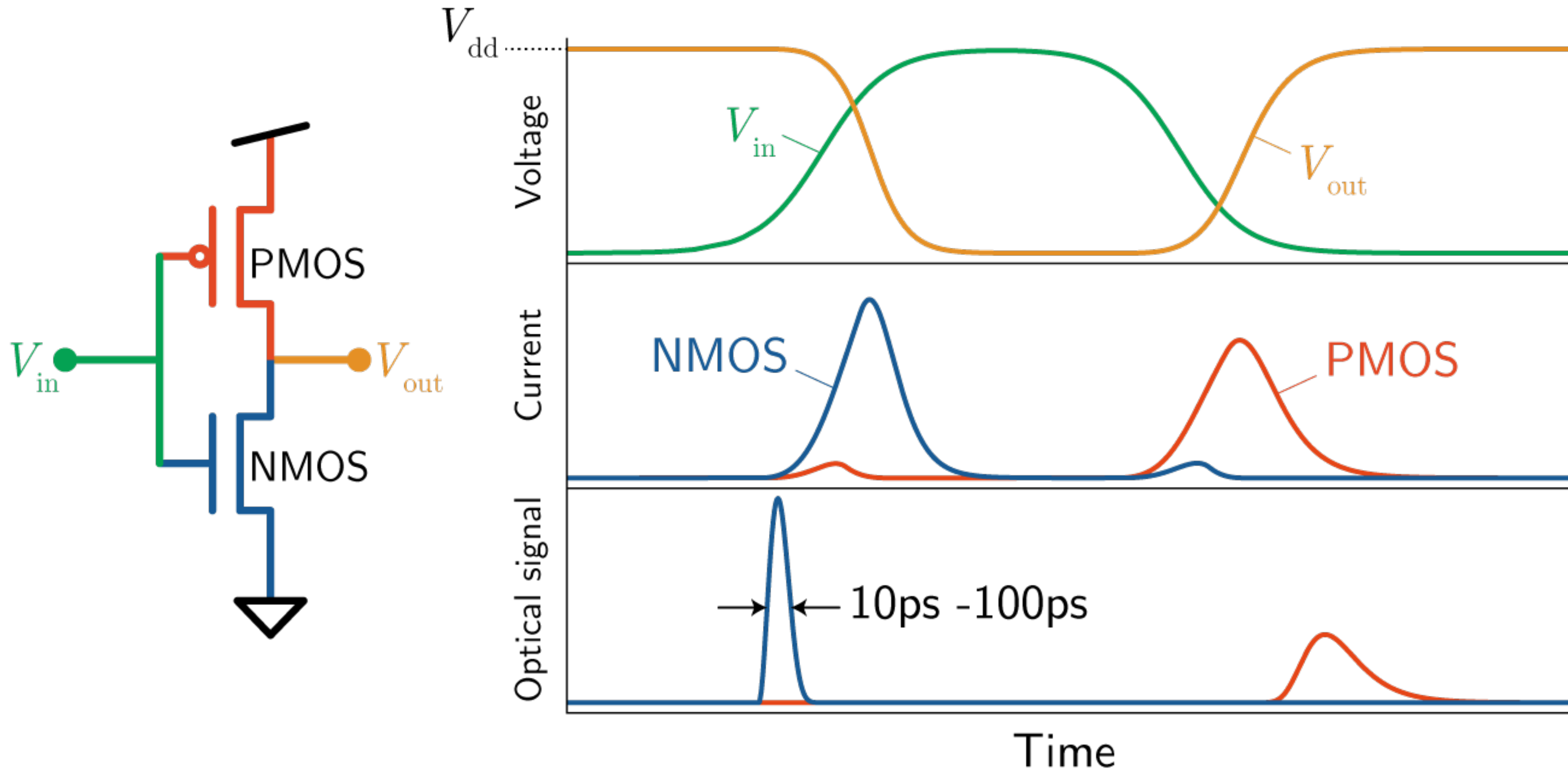


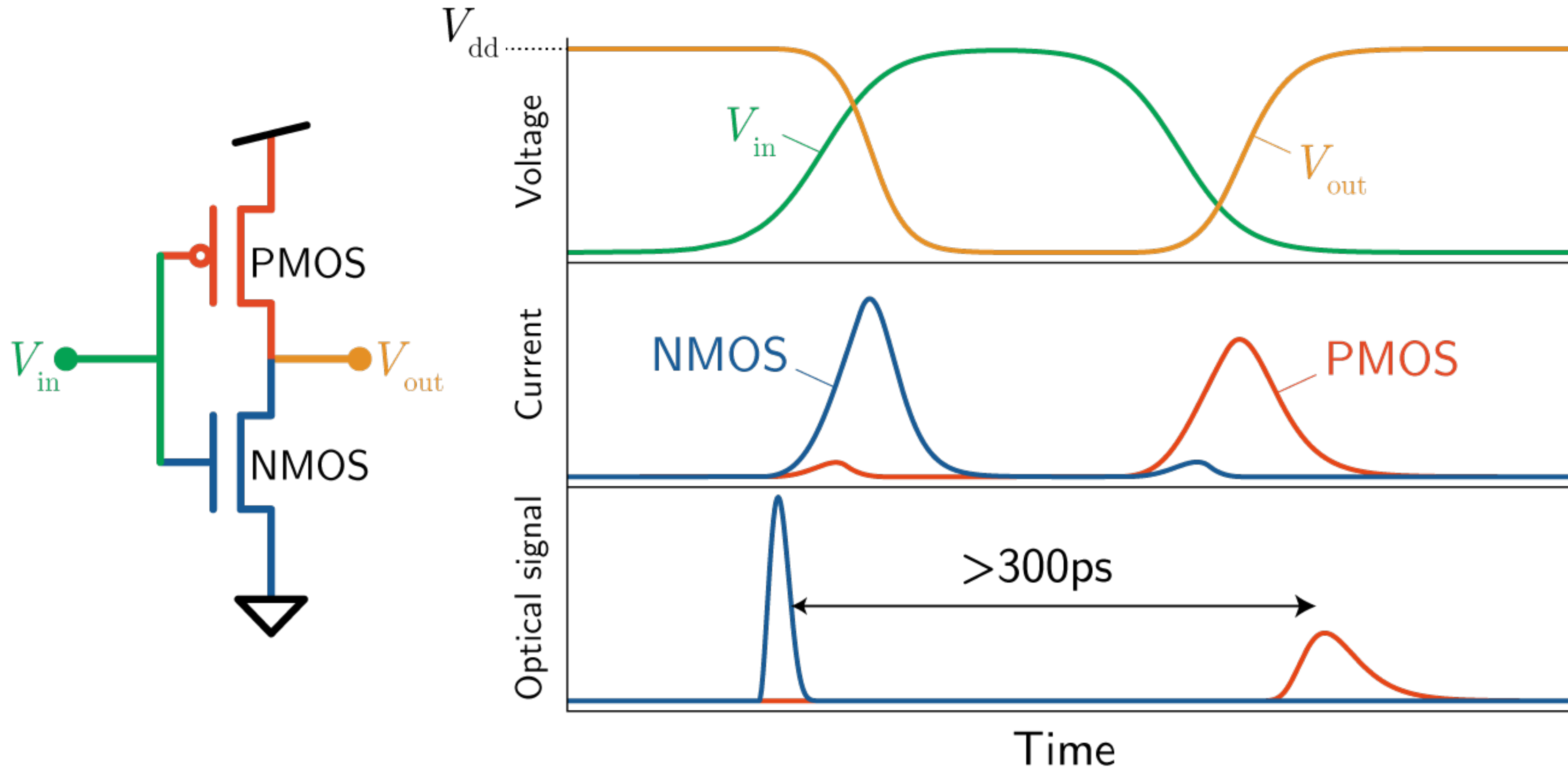
Source: NIST

Our Approach



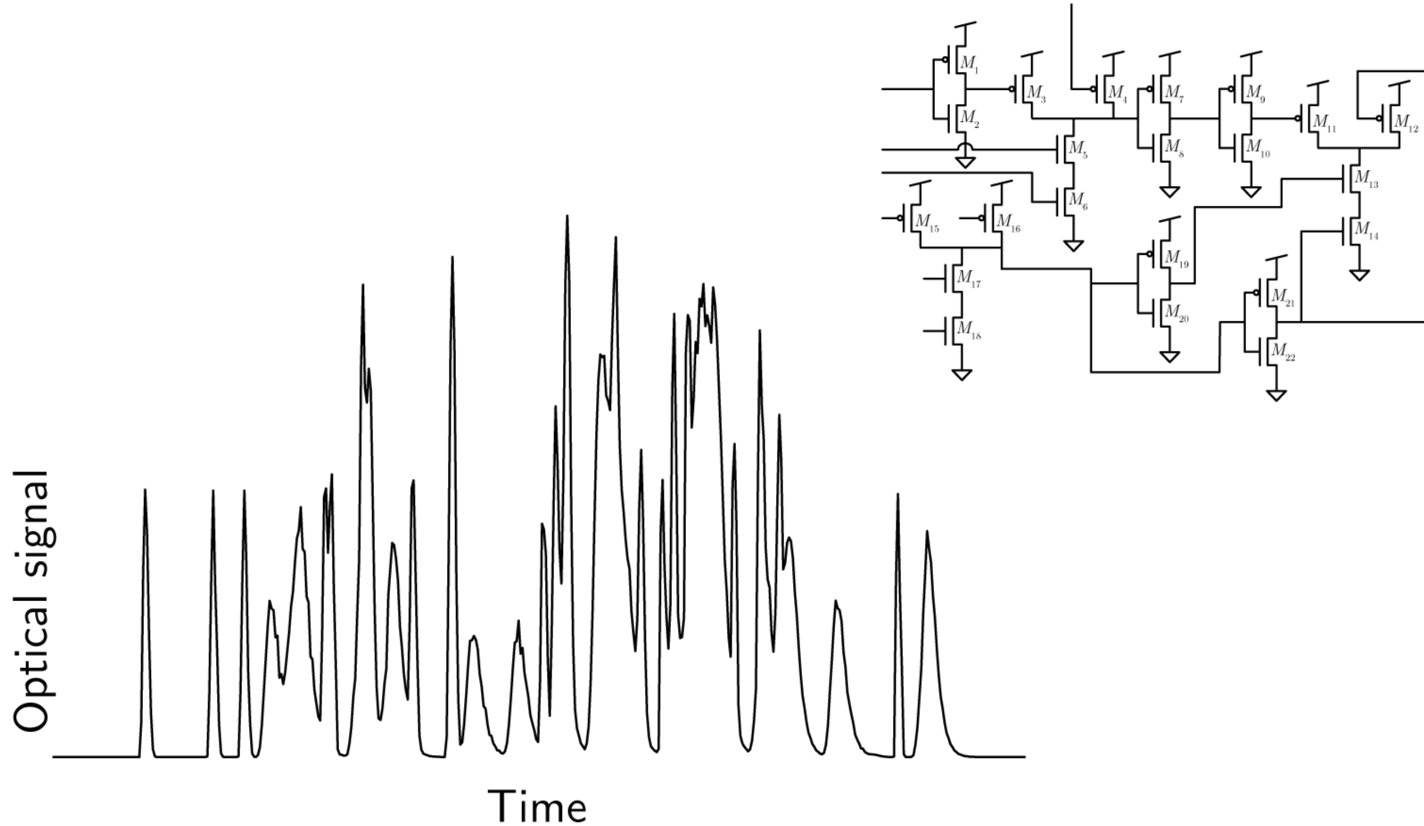
Source: NIST

Our Approach



Source: NIST

Our Approach



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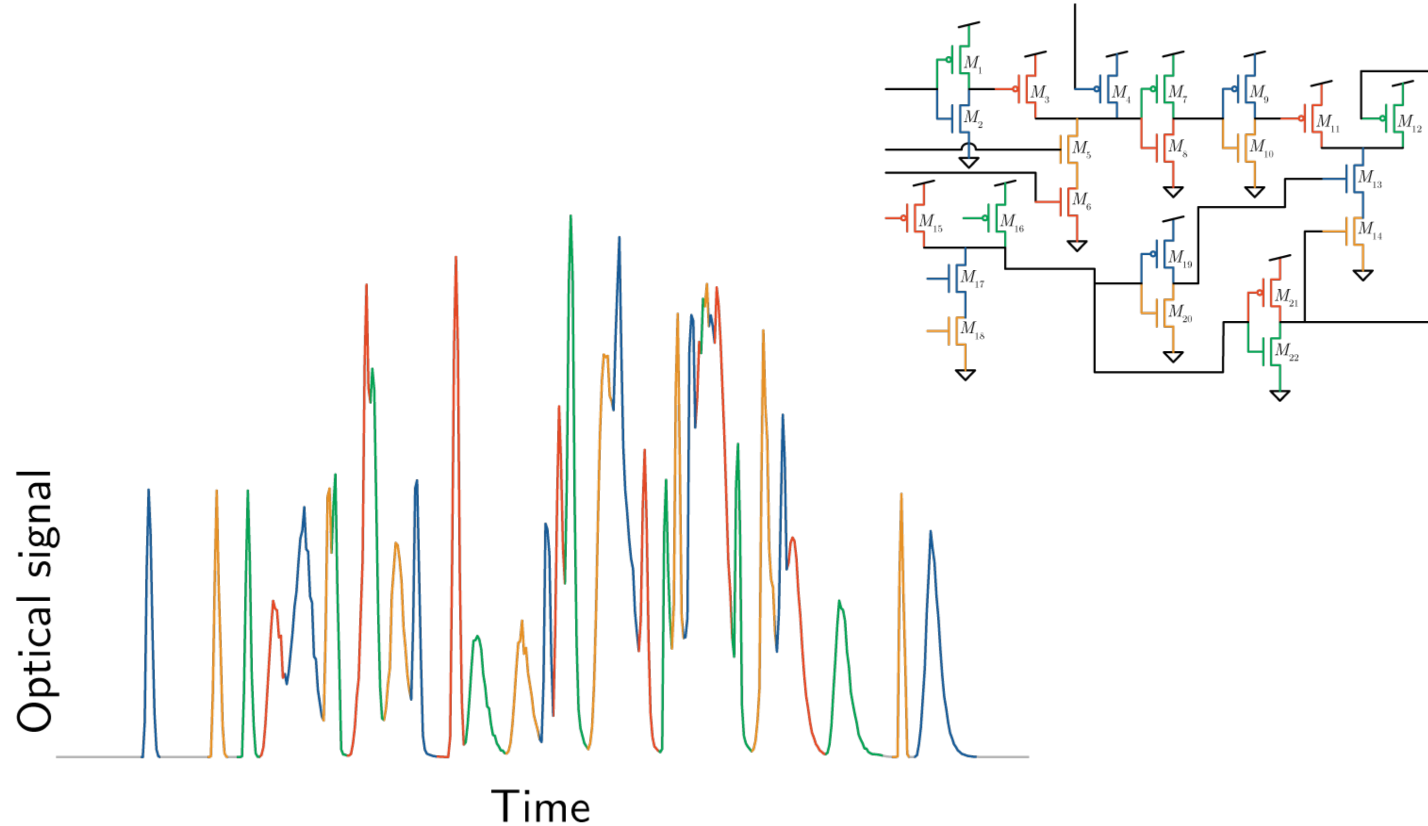
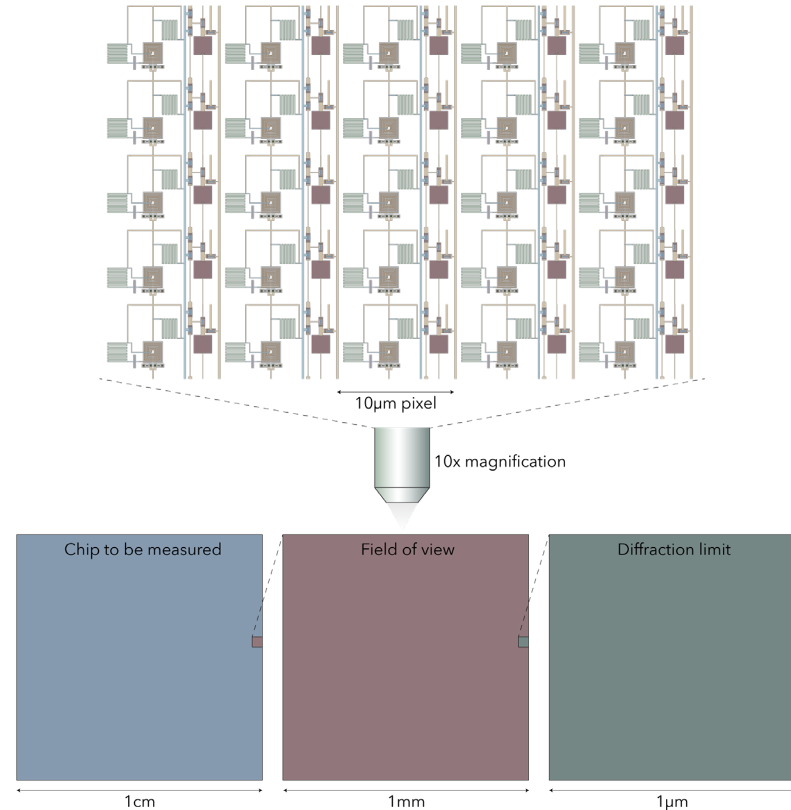
Our Approach



Source: NIST

Our Approach: Large Arrays

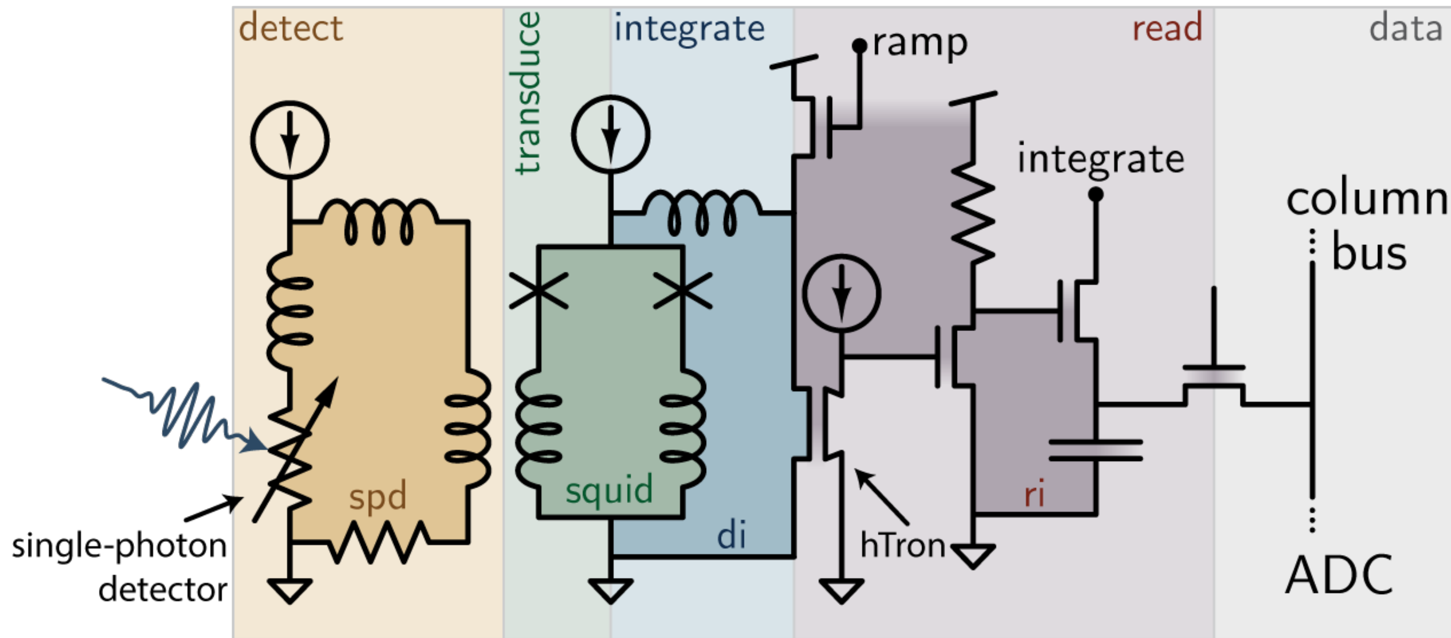
Measurement throughput scales linearly with number of pixels



Source: NIST

Our Approach: Circuit Readout

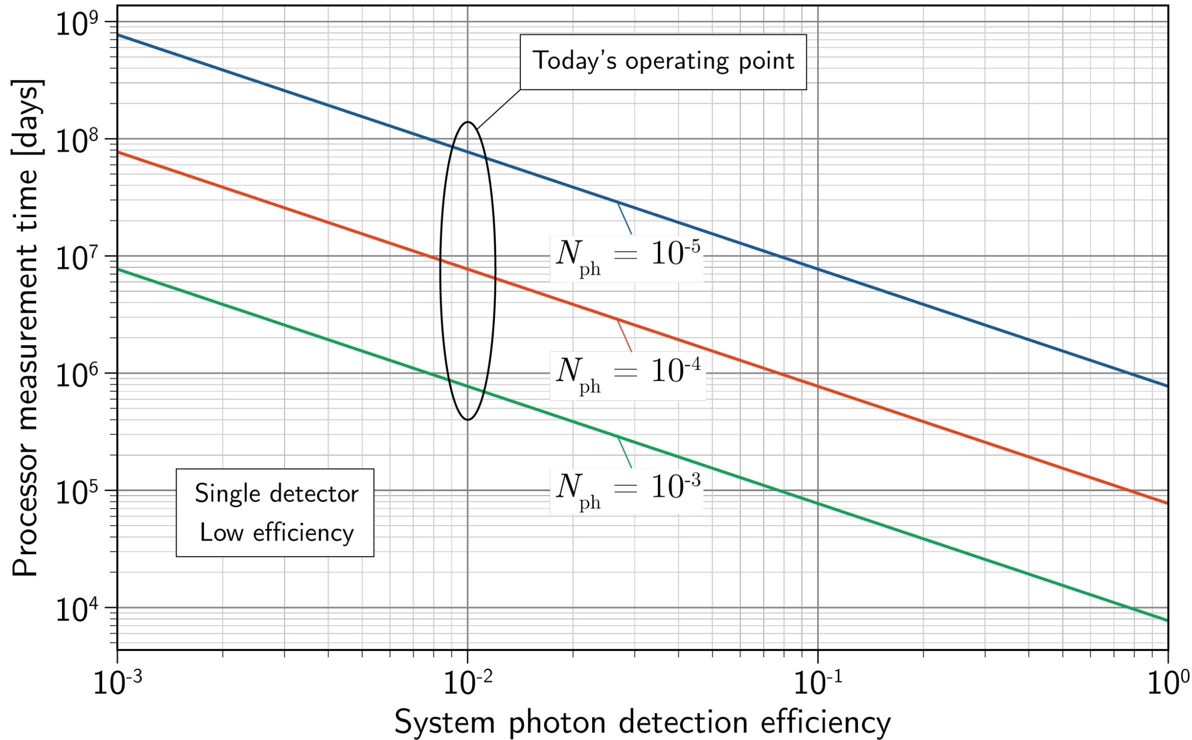
Integrated counts or timing information converted to charge on a capacitor to be read out just like a CMOS sensor array



Source: NIST

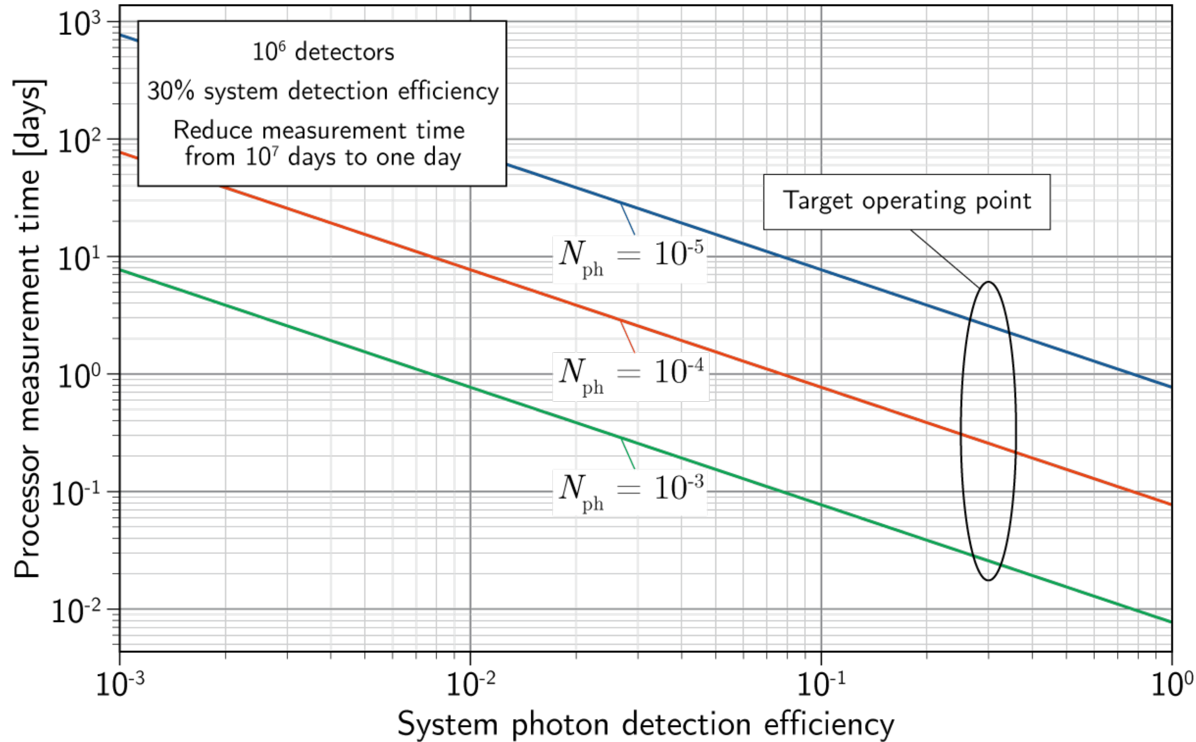
The Current State of the Art

N_{ph} is the number of photons per transistor switching event



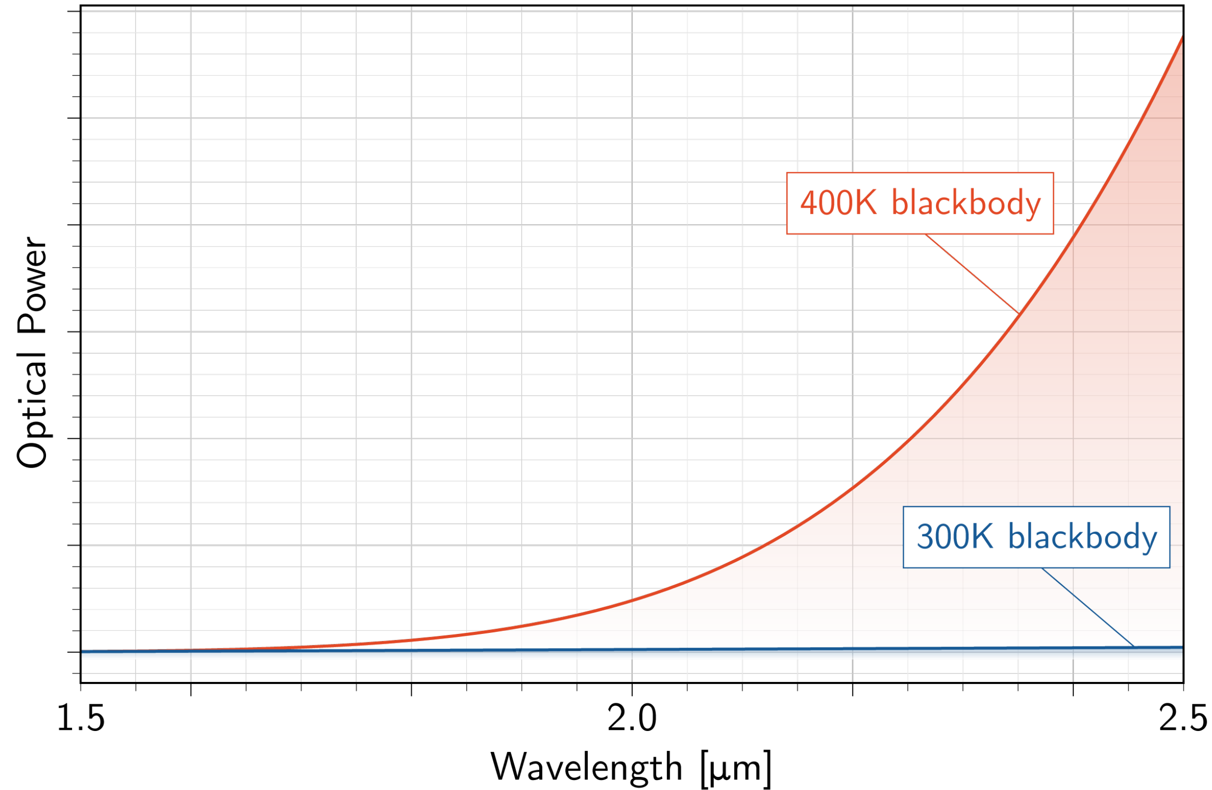
Source: NIST

The Delta



Source: NIST

First Order of Business



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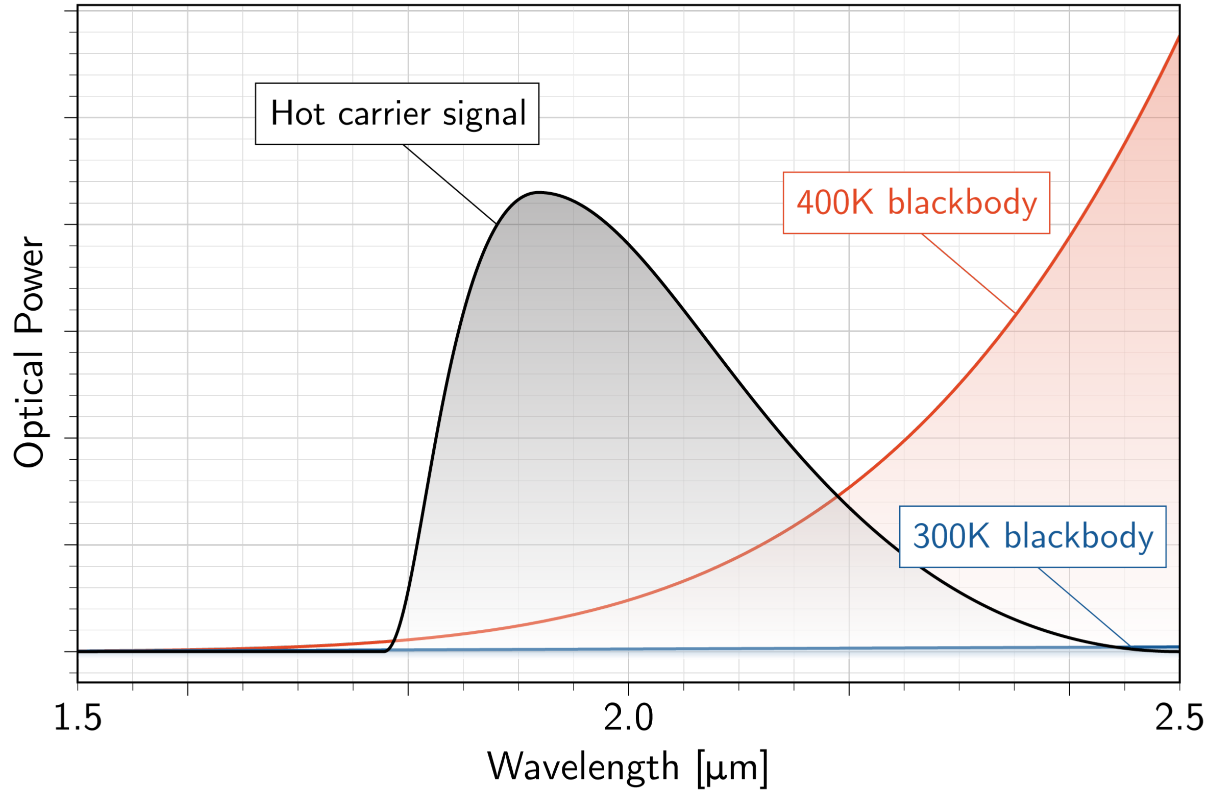

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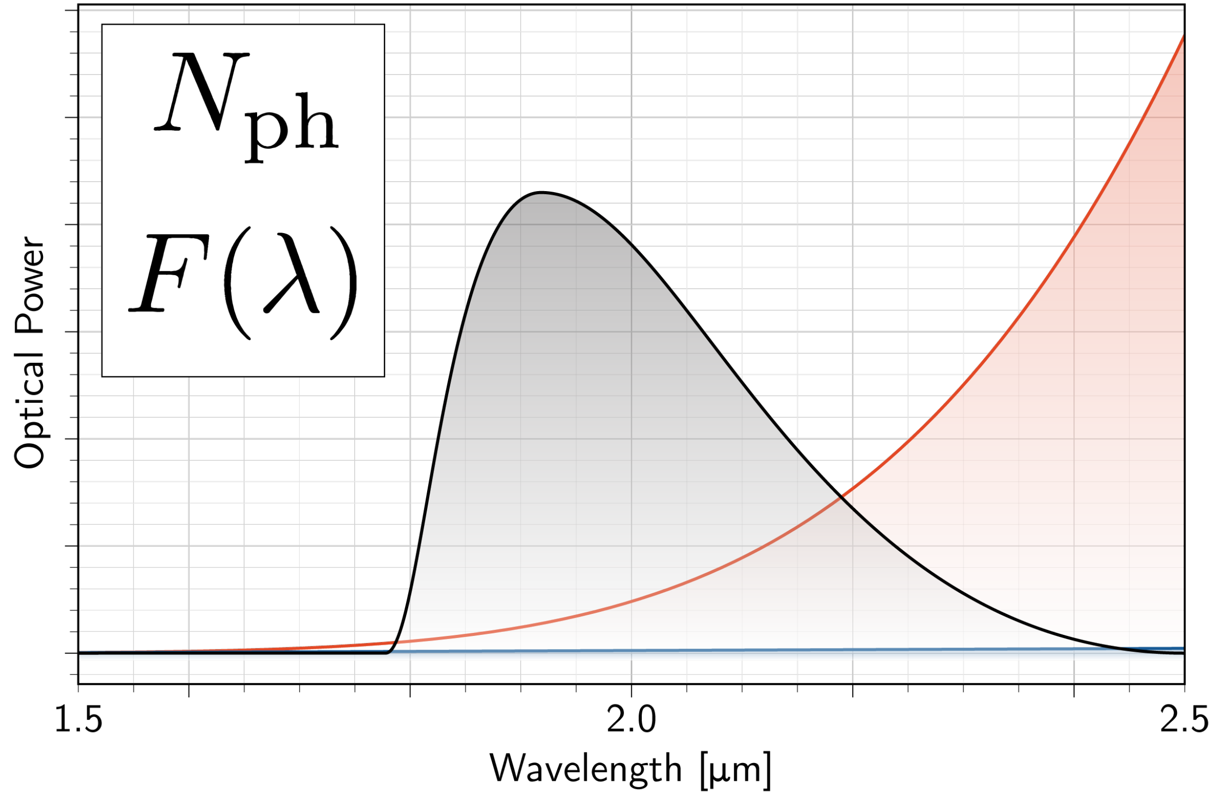

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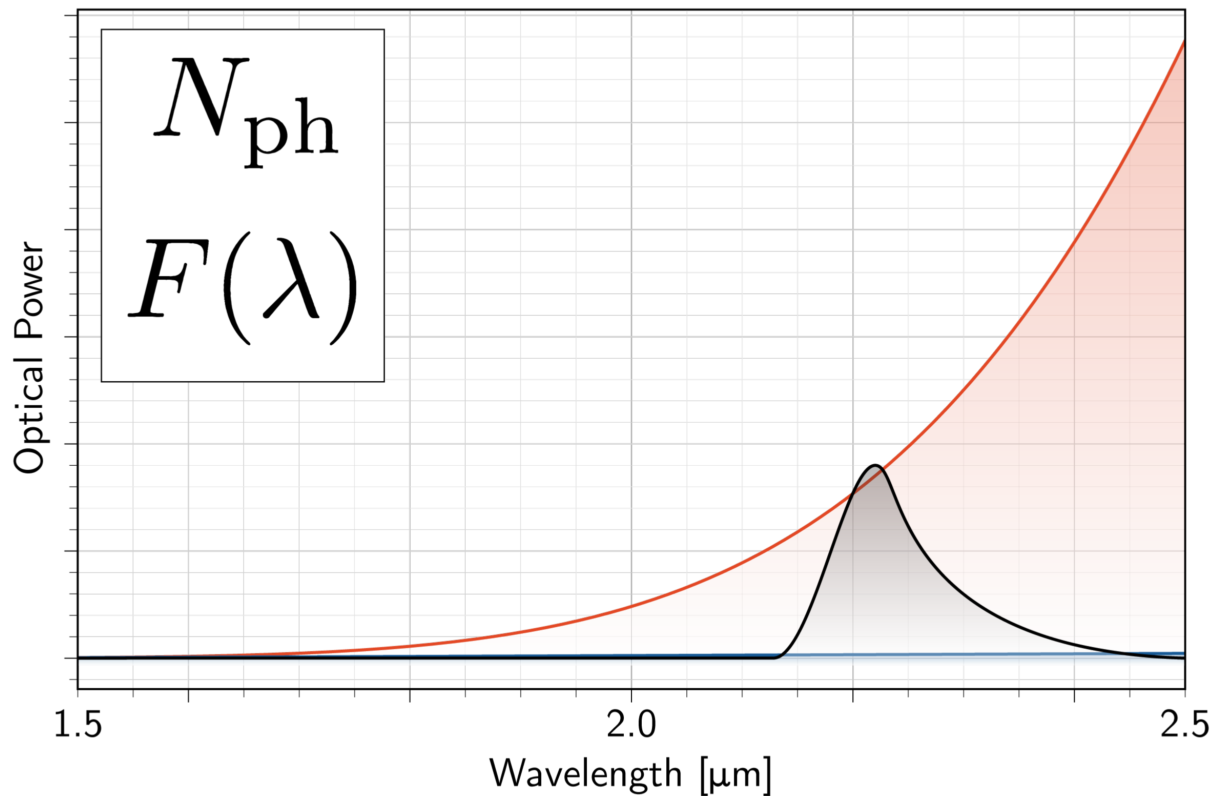
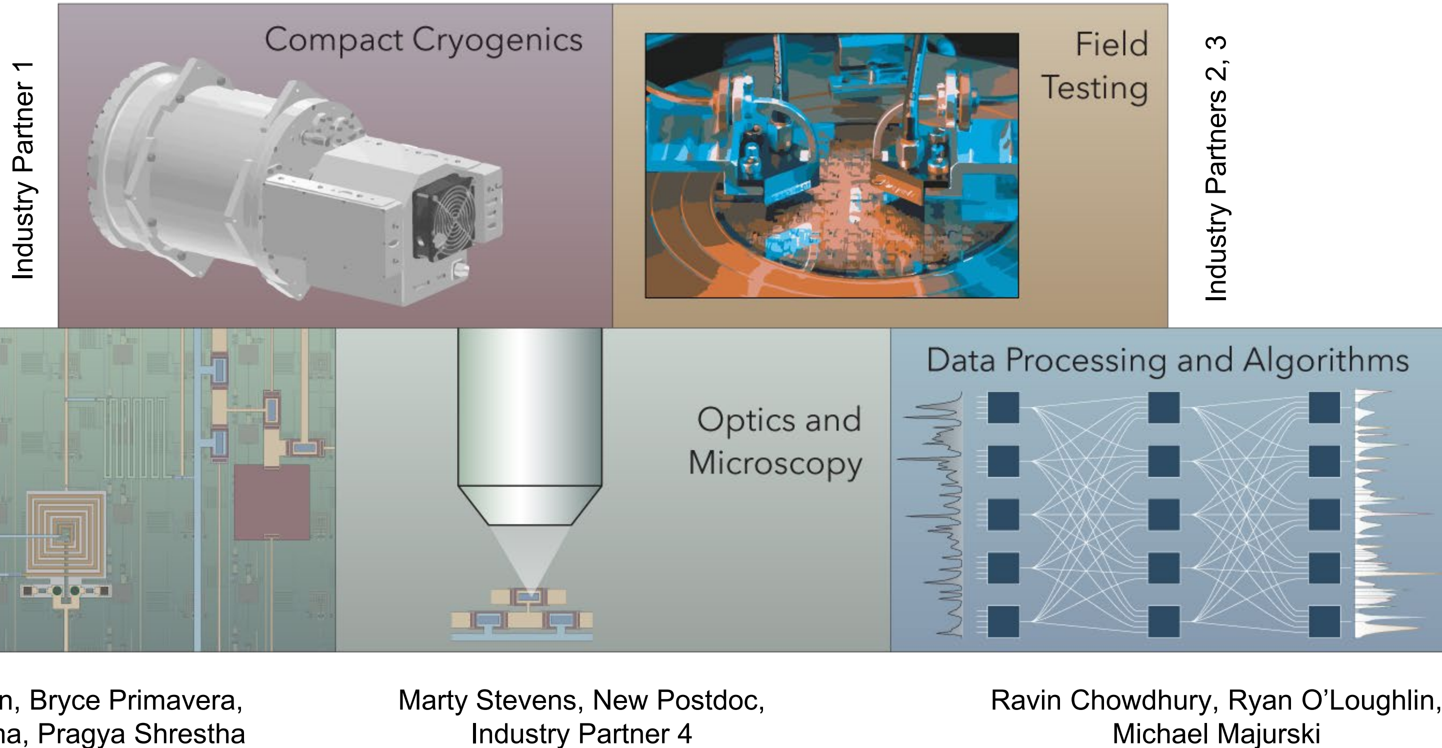


Source: NIST

Structure of the Team



Saeed Khan, Bryce Primavera, Varun Verma, Pragya Shrestha

Marty Stevens, New Postdoc, Industry Partner 4

Ravin Chowdhury, Ryan O'Loughlin, Michael Majurski

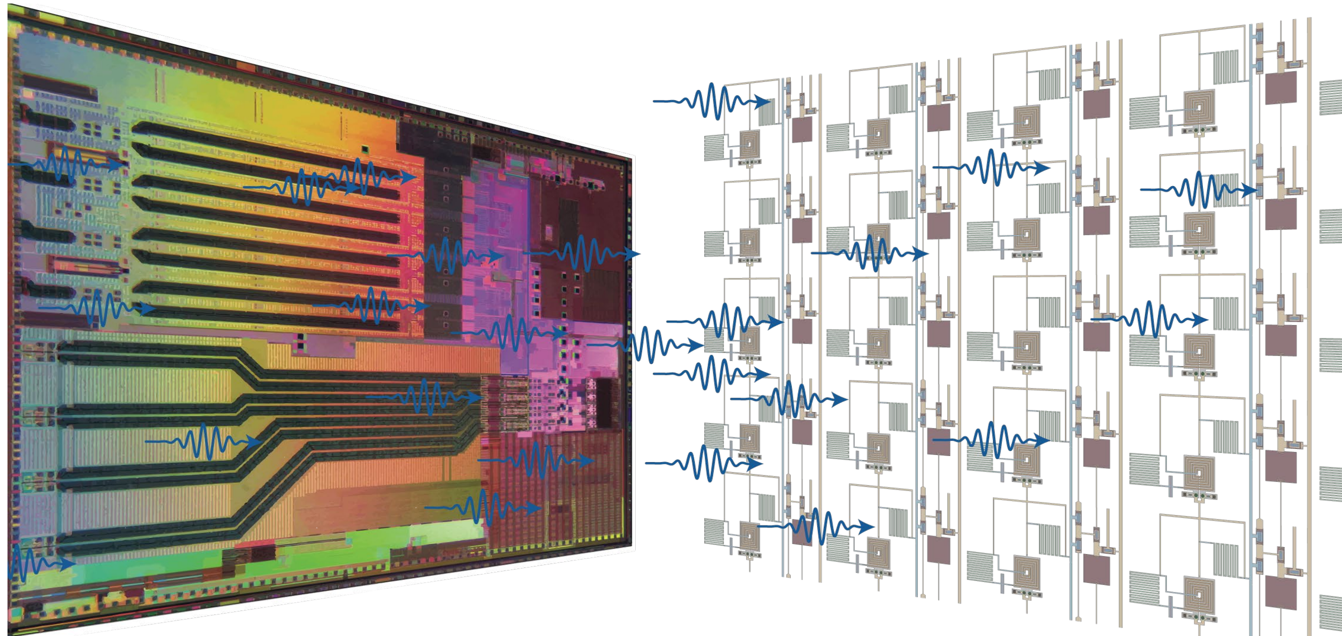
Collaborators at JPL, Rich Mirin, Sae Woo Nam, Jeff Shainline

Source: NIST

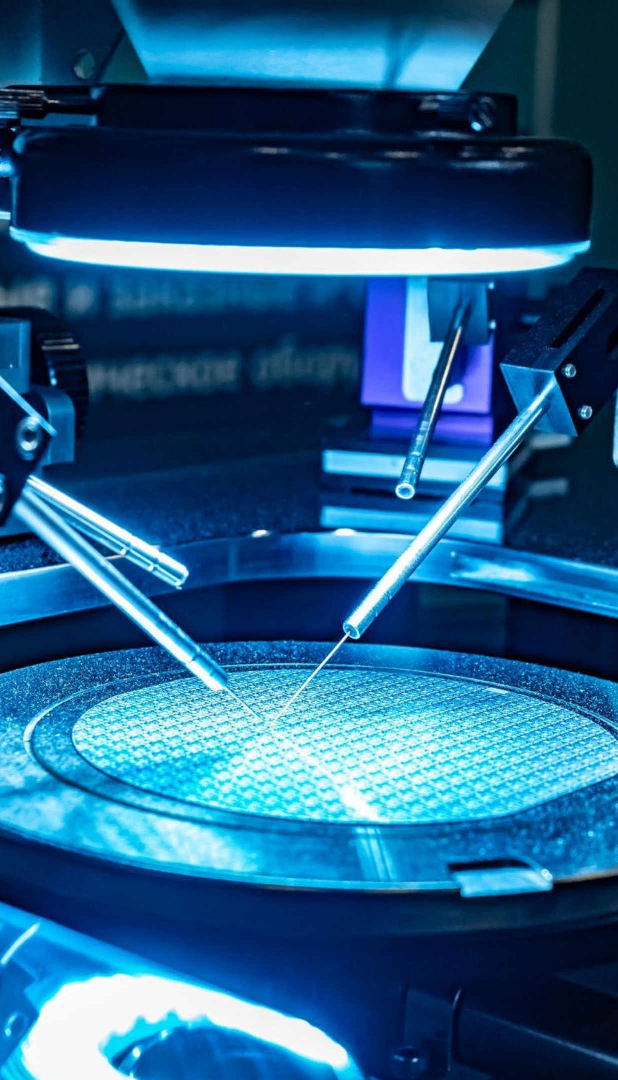
Impact: Silicon Photonics

Modulator eye diagrams across entire wafers

Identify known good die prior to dicing



https://www.techbriefs.com/component/content/article/7978-28053-200



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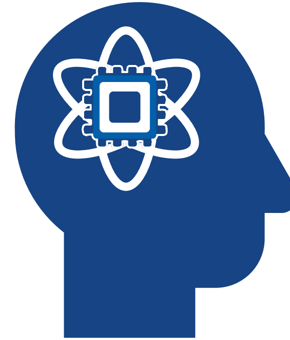
Questions?

Join the CHIPS R&D Metrology Program Team

Researcher Associates - Accepting Applications on a Rolling Basis



- NIST is seeking several full-time Researcher Associates for the CHIPS R&D Metrology Program.
- Researcher Associates will be a full-time physical scientists ZP-III position with a salary range of $76,860 - $119,760 per year
- Boulder, CO and Gaithersburg, MD duty stations

How to Apply

- Visit nist.gov/chips/current-chips-job-openings, to see the rolling announcement.
- Qualified candidates should send their cover letter and resume to researchjobs@chips.gov with the subject line "CHIPS R&D Metrology Researcher Associate - [Full Name]."

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METROLOGY

Thank You