CHIPS NAPMP & NASA AMES

Advanced Packaging Summit

April 18–19, 2024

NASA Ames Conference Center
(Moffett Field, CA)

CHIPS for AMERICA

NASA

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

NAPMP Overview and Update

Daniel Berger, Associate Director of the NAPMP

Disclaimer

- Statements and responses to questions about advanced microelectronics research and development programs in this summit:
  - Are informational, pre-decisional, and preliminary in nature,
  - Do not constitute a commitment and are not binding on NIST or the Department of Commerce,
  - Are subject in their entirety to any final action by NIST or the Department of Commerce.
- Nothing in this presentation is intended to contradict or supersede the requirements published in current or future policy documents or Notices of Funding Opportunity, which are the controlling documents.

NAPMP Proposer's Day – March 12th

Materials and Substrates NOFO: Key dates

February 28, 2024

Materials and Substrates Funding Opportunity (Released)

For R&D activities that will **establish and accelerate domestic capacity for advanced packaging substrates and substrate materials**

March 12, 2024

Materials and Substrates Proposer's Day

Share detailed information on Materials and Substrates NOFO, in a collaborative atmosphere

Due: April 12, 2024 11:59 pm EST

Concept Papers Review

Mandatory concept papers submitted by teams

On or About May 21st

Teams invited to submit full applications

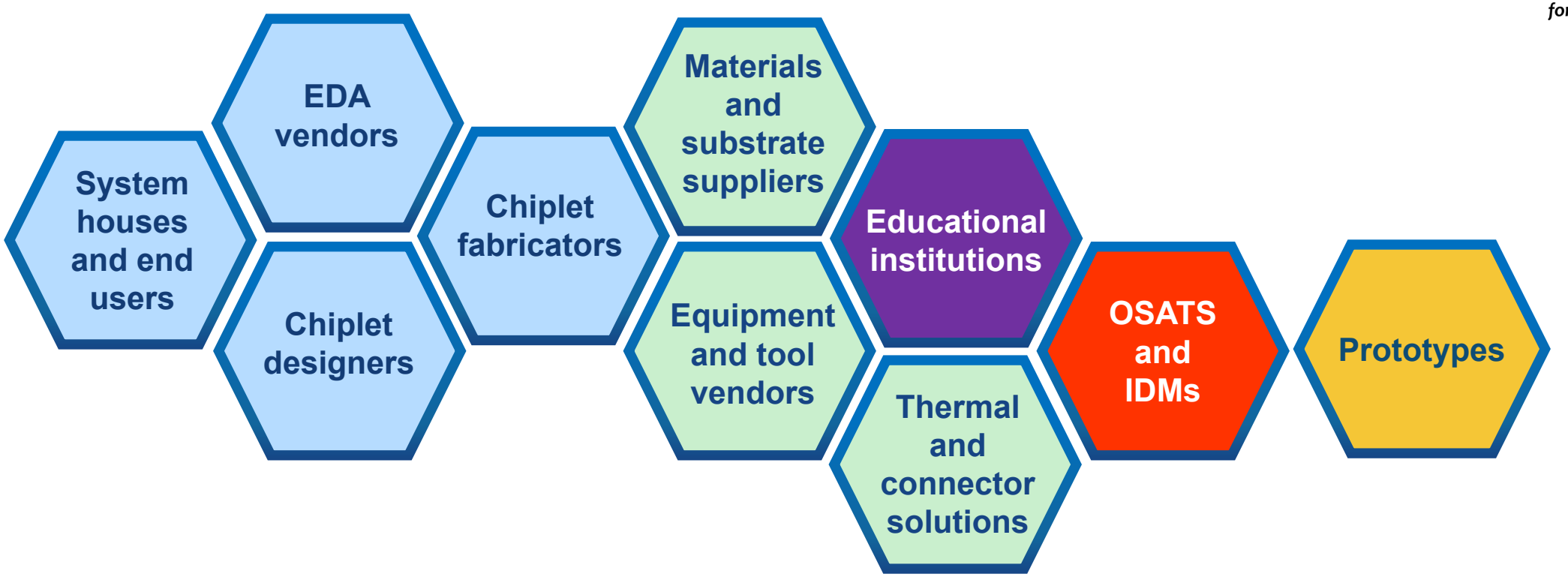
July 3, 2024

Full Application Due

The full application from applicants due

CHIPS for America QR Code: **CHIPS NAPMP Materials and Substrates NOFO** (full text)

Collaboration is Critical for Success



We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the NAPMP.

CHIPS for America

$39 billion
for incentives

Two component programs to:

1. Attract large-scale investments in advanced technologies such as leading-edge logic and memory, and advanced packaging
2. Incentivize expansion of manufacturing capacity for mature and other types of semiconductors

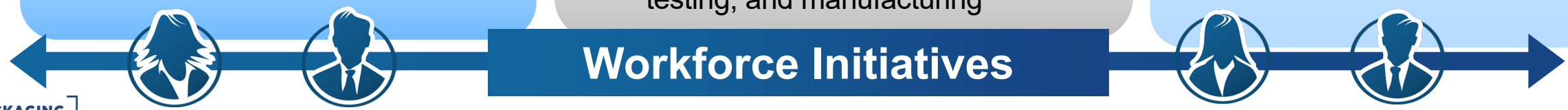
$11 billion
for R&D

Four integrated programs to:

1. Conduct research and prototyping of advanced semiconductor technology
2. Strengthen semiconductor advanced packaging, assembly, and test
3. Enable advances in measurement science, standards, material characterization, instrumentation, testing, and manufacturing

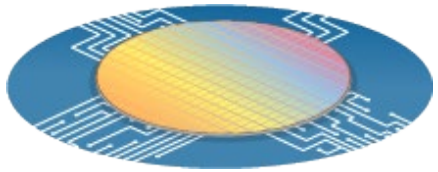
$2 billion
for DoD Microelectronics Commons

A national network that will create direct pathways to commercialization for US microelectronics researchers and designers from “lab to fab.”



PACKAGING CHIPS for AMERICA

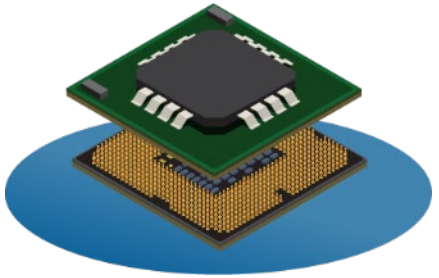
CHIPS R&D Programs



CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

Manufacturing USA

CHIPS Manufacturing USA Program



CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast

Natcast is an independent nonprofit organization and operator of the NSTC consortium

CHIPS Metrology Program

Workforce Initiatives

PACKAGING CHIPS for AMERICA

Establishing Advanced Packaging in the U.S.

Packaging Roadmaps

- NIST-sponsored roadmaps: MRHIEP, MAESTRO and MAPT
- Other roadmaps: HIR and IRDS

Technology Investment Areas

- All aspects of technologies required to develop a leading-edge on-shore advanced packaging manufacturing capability

The National Advanced Packaging Piloting Facility (NAPPF)

- Key to facilitating high-volume manufacturing
- Piloting and prototyping functions

The Chiplet and Design Ecosystem

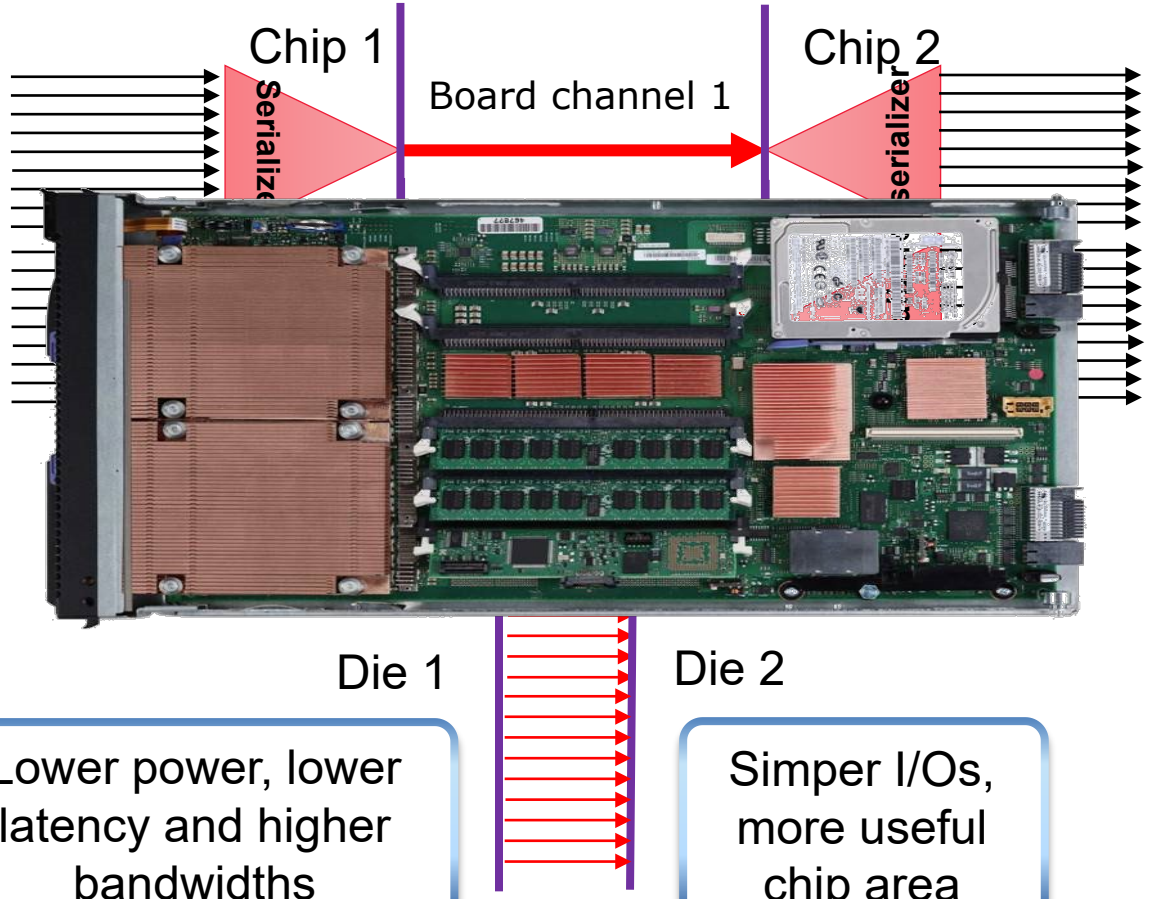
- Chiplet discovery, disaggregation and reaggregation methodologies, protocols, standards, fabrication and warehousing design for test, repair and reliability, and holistic design tools and methodologies

Design in the U.S., build in the U.S., and sell worldwide

- Successful development efforts will be transitioned and validated for scaled transition to U.S. manufacturing

Advanced packaging is all about scale

The difference now is scale:



Lower power, lower latency and higher bandwidths

Simper I/Os, more useful chip area

- More Channels on the package
  - Finer ”bump/pillar” pitch
  - Approach on-chip via pitches (<1 μm)
- Finer Trace Pitch
  - Approach on-chip wiring pitches
- Shorter inter die distance
  - ~ μm

Scale Down

- Significantly more intimately connected Silicon

Scale Out

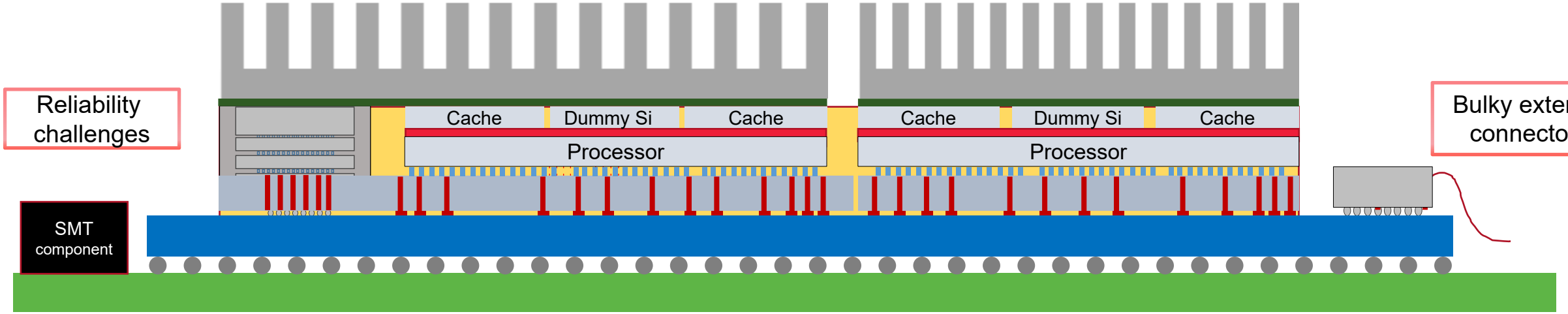
We do it today — but with complexity and added hierarchy

Materials with large CTE mismatches and high stresses

Known good die, testing and rework challenges

Thermal and hot spot challenges
Power delivery challenges

Reliability challenges



Bulky external connectors

Increasingly complex hierarchies (e.g.: interposers) and assembly techniques

Organic substrates and laminates with large warpage and coarse pitches with embedded and SMT passives and expensive interposers

Simplify packaging and make it cost effective to manufacture in the US

CTE: coefficient of thermal expansion; SMT: surface mount technology

The Role of the package

Mechanical protection
- Handling
- Stability

Environmental protection
- Moisture
- Hermeticity
- Corrosion

Thermal protection
- Heat spreading
- Heat sinking
- Hotspot reduction

To protect and to serve

Connect electrically to other chips

Deliver power

Stable test and integration platform

NAPMP Structure: six hardware and eco-system thrusts + piloting facility + prototyping challenges

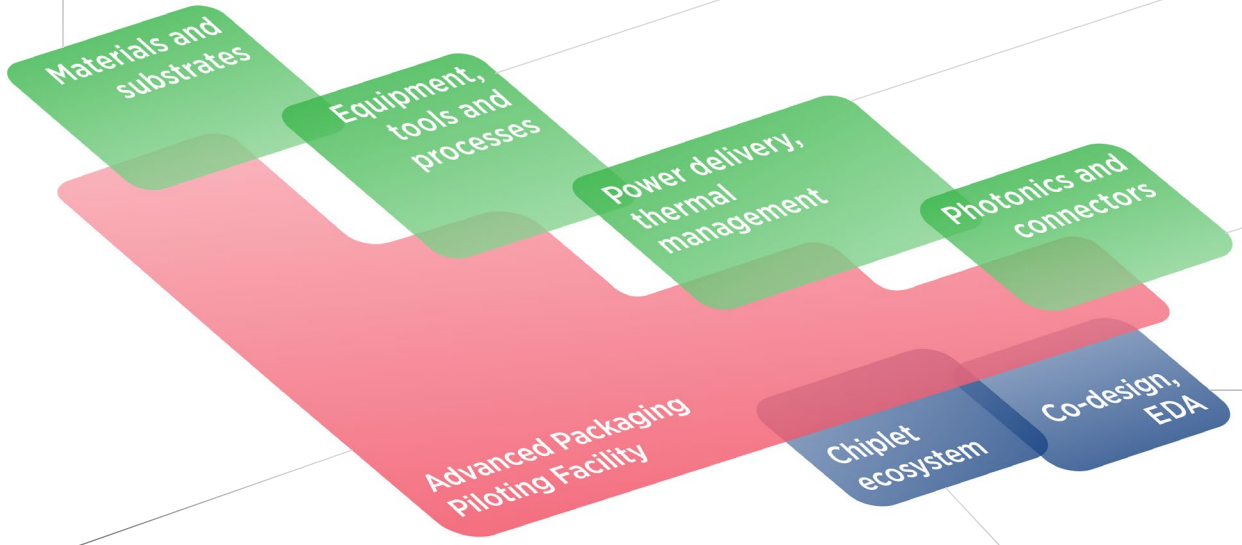
Substrates & materials are the platform for heterogeneous integration of dielets

Equipment, tools & processes are needed to pattern substrates and assemble dielets and passivate assemblies

Thermal management and efficient power delivery are critical needs

Photonics and connectors allow the assembly to interact with the outside world

Automated design for test, repair, security, and reliability; substrate and process dependent



The NAPPF provides a test bed for integration of the different investment areas and also functions as a piloting and prototyping facility

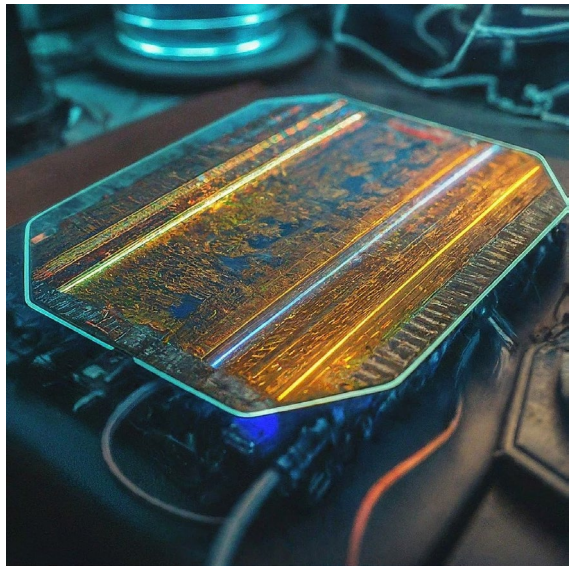
The chiplet eco system is crucial for any implementation of advanced packaging

NAPPF: National Advanced Packaging Piloting Facility

The National Advanced Packaging Piloting Facility (NAPPF) - Where it all comes together

- Investment Area Thrusts should connect activities with the APPF
- NAPPF will be focused on integrated process flows that can reach commercial scale
- NAPPF will be focused on validating new technology specifications, compatibility with other processes, yield, and reliability
- The NAPPF will be focused on assessing technologies for scaled transition to U.S. manufacturing including yield and reliability
- We will do this with baseline processes and prototyping and piloting exemplars

Choosing exemplars and corresponding baseline processes



AI and HPC

Low power edge communication devices

Medical Electronics

Others: auto, extreme ……

We could probably run two or three baseline processes in the NAPPF based on our three substrate types

**No decisions have been made on the number and types of processes*

Advanced Packaging Summit

Plenary sessions:

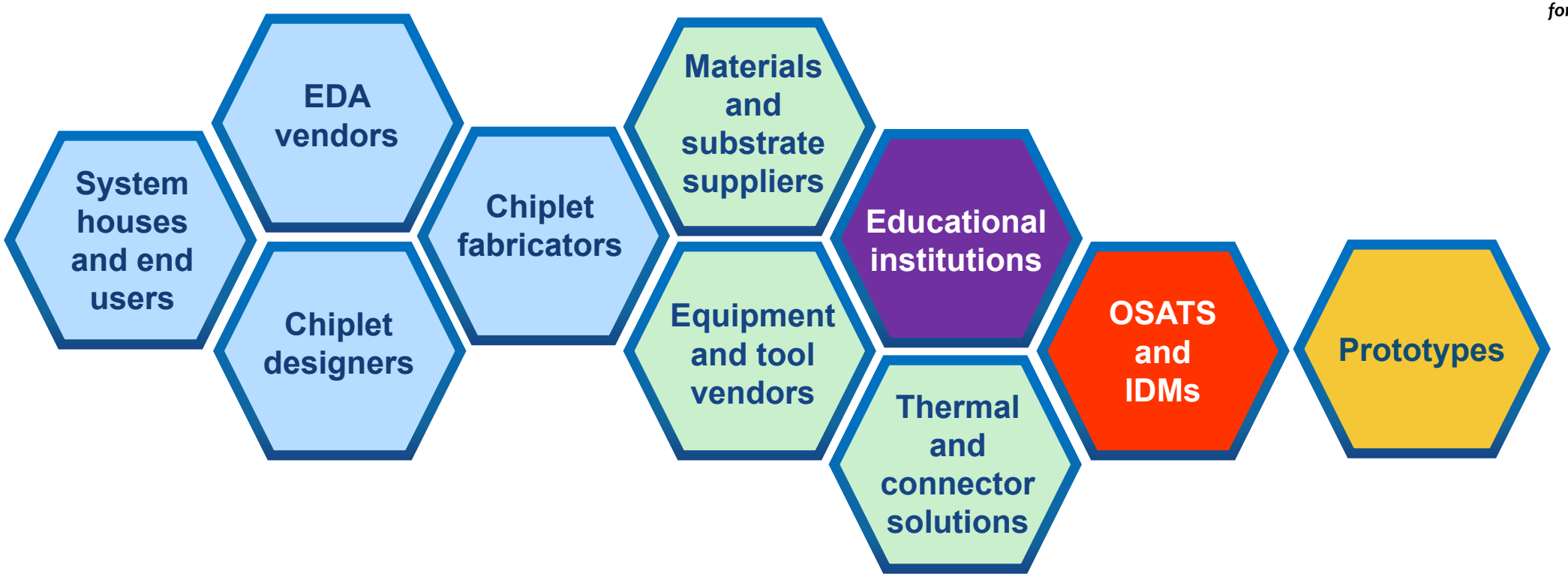
- The goals of the NAPMP program in the context of CHIPS for America, CHIPS Incentives, and CHIPS R&D
- Strategic challenges in advanced packaging
- Overview of advanced packaging efforts in the government and private sector
- Vision for a National Advanced Packaging Facility (NAPPF)
- Opportunities for international cooperation in advanced packaging

Tracks will include panel and discussions in the following areas:

1. Applications – HPC & AI
2. Applications – 5G / Edge / Mobile
3. Applications – Biomedical
4. Applications – Aerospace & Automotive
5. Other Advanced Packaging Topics
6. Packaging Pilot Needs & The Path to High-Volume Manufacturing
7. Barriers to Adoption of Advanced Packaging
8. Challenges for Startups

Exchange Ideas on Advanced Packaging in the U.S.

Before we begin ….. Questions?



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CHIPS National Advanced Packaging Manufacturing Program (NAPMP) Chiplet Ecosystem

Bapiraju Vinnakota, NAPMP Program Manager

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Establishing Advanced Packaging in the U.S.

(continued)

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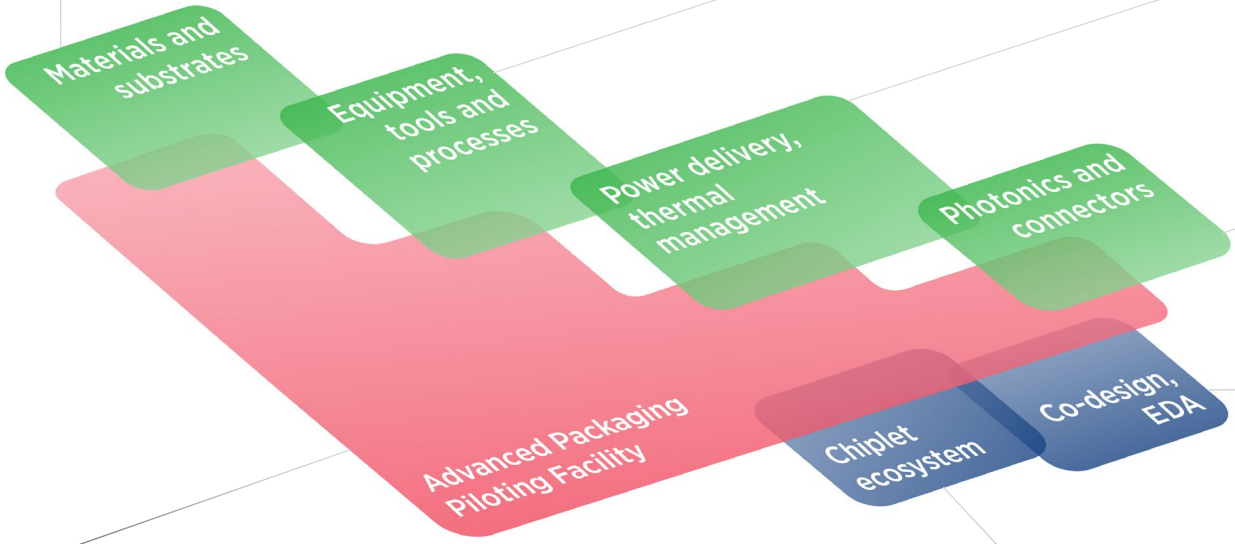

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The chiplet eco system is crucial for any implementation of advanced packaging

NAPPF: National Advanced Packaging Piloting Facility

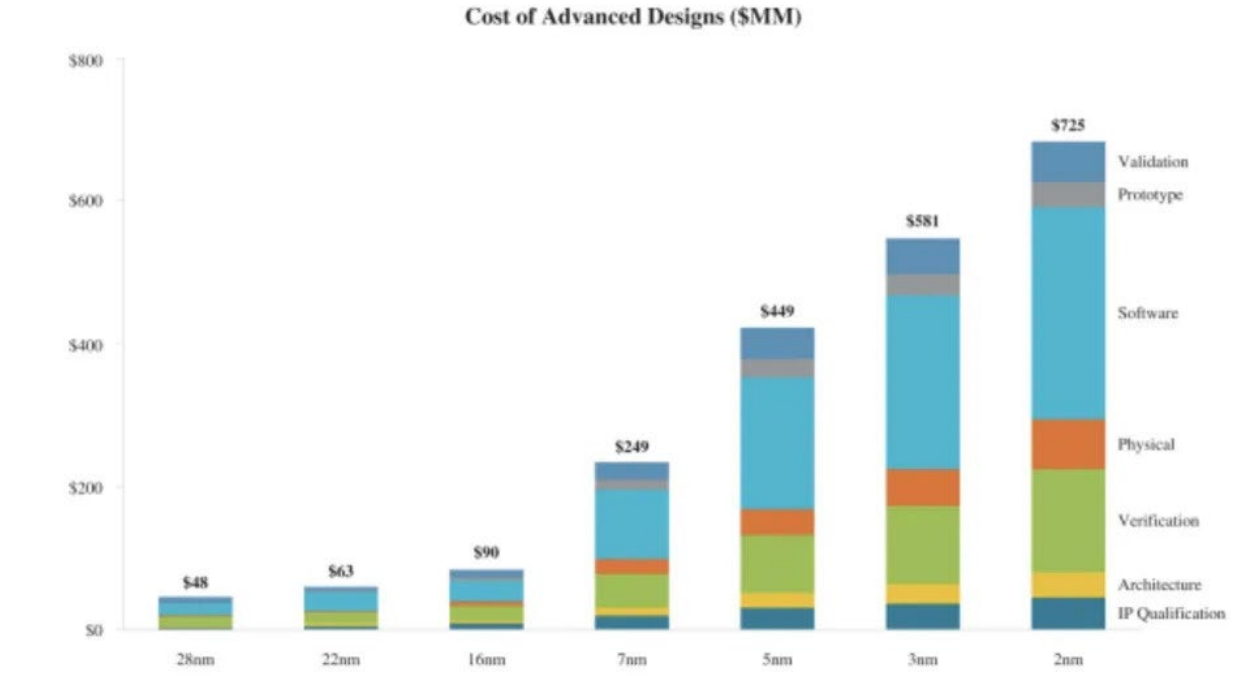
Industry Move to Chiplets: Motivation

- Build Big (Reticle busters)
- Build Fast (Modularity, Reuse)
- Build Cheap (Optimize function to process node)

https://www.nextplatform.com/2021/06/09/amd-on-why-chiplets-and-why-now/
https://www.pcmag.com/news/to-meteor-lake-and-beyond-how-intel-plans-a-new-era-of-chiplet-based-cpus

Important Trends

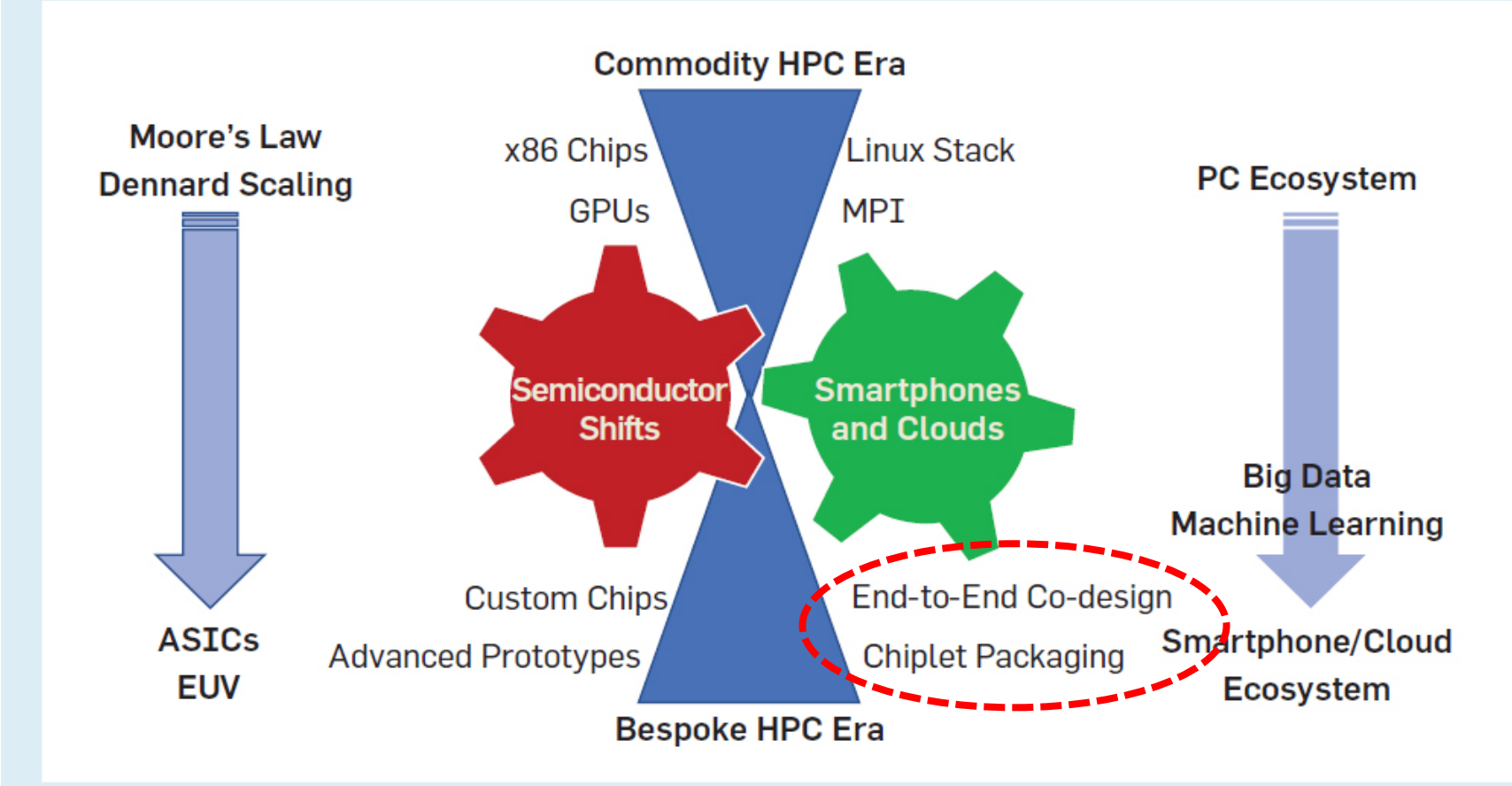
- Soaring Product Costs
- Heterogeneous Architectures
- US Chiplet Leadership
- AI = More Memory + More Compute



Source: IBS July 2022.

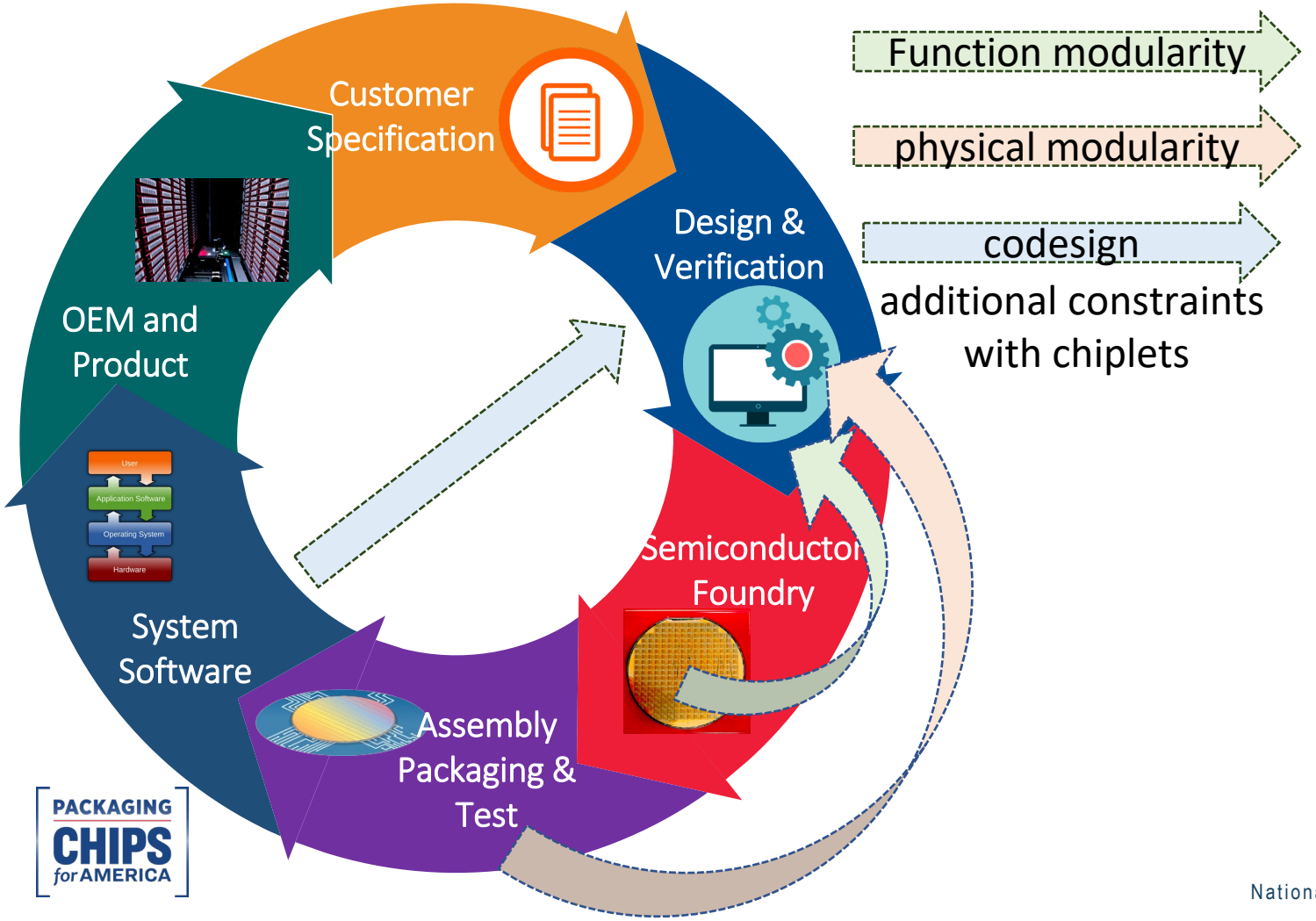
https://community.arm.com/arm-research/b/articles/posts/three-dimensions-in-3dic-part-1
https://www.intc.com/news-events/press-releases/detail/186/intel-unveils-industrys-first-fpga-integrated-with-high
https://www.intel.com/content/www/us/en/newsroom/news/intel-accelerates-process-packaging-innovations.html
https://www.techpowerup.com/258069/2nd-gen-amd-epyc-processors-set-new-standard-for-the-modern-datacenter
https://www.nvidia.com/en-us/data-center/a100/
https://www.amd.com/en/technologies/3d-v-cache
https://finance.yahoo.com/news/firm-estimates-2nm-chip-now-160152130.html

HPC: Back to the Future



D. Reed, D. Gannon, J. Dongarra, "HPC Forecast: Cloudy and Uncertain", https://cacm.acm.org/research/hpc-forecast/

Addressing Challenges in Developing with Chiplets

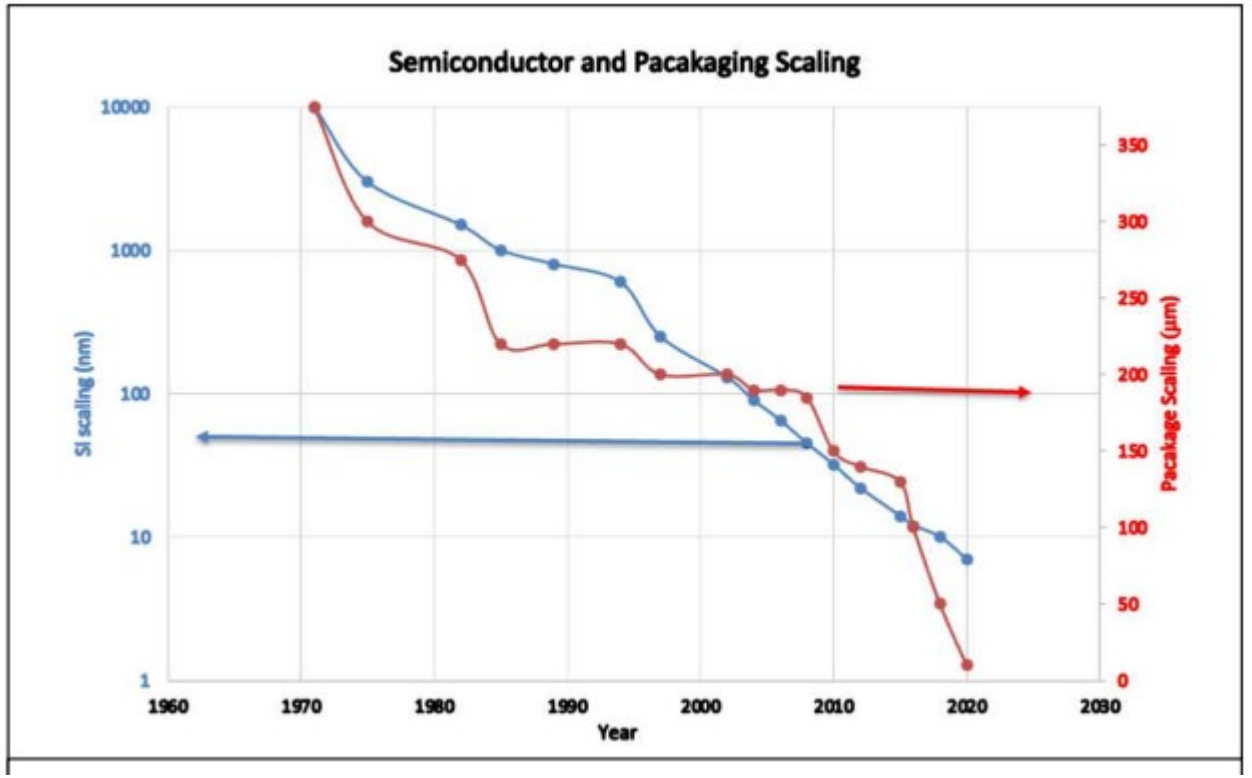


Factors brought forward or made more complex

- Functional modularity
- Physical modularity
- Interconnect
- (Advanced) Packaging
- Test and operations
- Inventory

Trends: Packaging is Changing

- Packaging scaling accelerated in the recent past.
- Architectures have not evolved to exploit this scaling
- Cheaper/lighter D2D interconnect at finer pitches



S.S. Iyer, 2022 IEEE Electron Devices Technology and Manufacturing Conference Proceedings of Technical Papers

Advanced packaging blurs the line between a monolithic chip and a packaged assembly of heterogeneous chips

Scaling down features on the package:

- Making the features on the package approach those at the top level on a monolithic CMOS chip
- Connecting the dies to the package at pitches approaching the final via pitches on a chip
- Reducing the distance between dies that are assembled on a multi-chip package to approach the distance between IP blocks on a monolithic chip

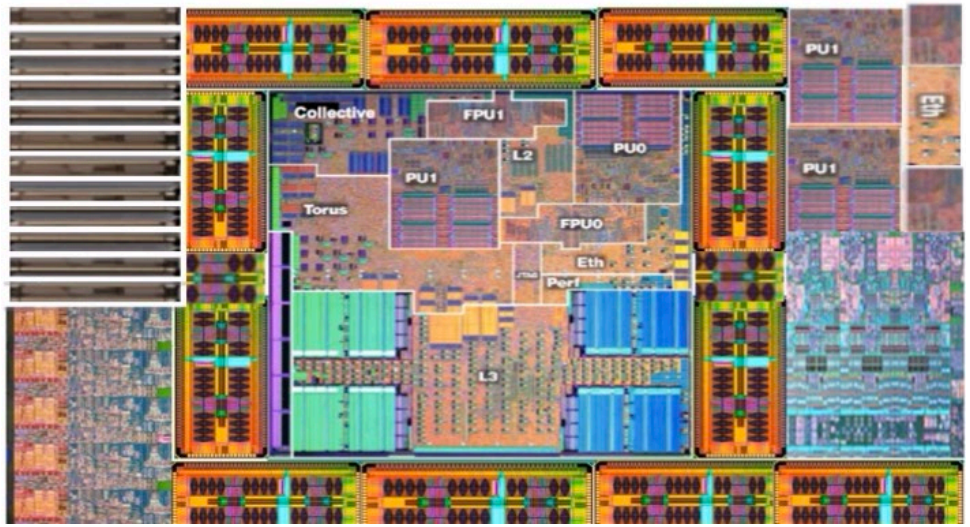
Scaling out the package

- Accommodate a larger number of closely packed heterogeneous dies
- Address the power delivery, thermal dissipation, and external connection challenges
- Develop standards and protocols to accommodate this large and diverse set of chips (chiplets)

Advanced packaging allows us to change the way we put complex systems together[1]

Adapting SoC methods to packaged systems

- IP blocks transformed into hardware verified dielets (chiplets)
  - Chiplets are IP designs
  - Chiplets are not small chips but need to be connected to complementary chiplets to function
  - Dielets are hardware instantiated chiplets
- Bare dielets are stacked (3D) or integrated side by side at fine pitch on an interconnect fabric (substrate)
- Dielets are heterogeneous
- A simpler and flatter hierarchy is possible



Chiplet discovery, disaggregation, and dielet reintegration

[1]S.S. Iyer T-CPMT (2016)

Faster/Cheaper Chiplet Integration Needs…

Component	Status
D2D Interconnect (Huge growth/awareness here)	**UCIe**, BoW, AIB, SuperChips, XSR
Test	IEEE 1838, IEEE P3405
Chiplet description	JEDEC-OCP JEP 30 CDXML
Size guardrails	

A Chiplet Integration Layer to Fully Leverage Advanced Packaging

Today's standards: Protocol integration

Tomorrow: A simpler chiplet integration layer

- Physical Integration: Specs for size, power, mechanicals, thermals…
- Logic integration: Chiplets intimately integrated with wires, like IP.

Bond Pitch	Physical Integration	Logic Integration	Protocol Integration
50μ	✓		

Integrate chiplets with EDA
(not protocols)

Available Options to Create a Chiplet Ecosystem

Parameter Selection

Bond Pitch

- ○ 50μ
- ○ 10μ
- ○ 2μ*
- ○ 1μ*

Bonding Type

- ○ Single
- ○ Mixed*

Chiplet Logic

- ○ Traditional
- ○ Package-optimized*

Chiplet Ecosystem

- ○ Single design
- ○ Closed ecosystem
- ○ Open ecosystem*
- ○ Integration layer*

Dimensions

- ○ Flat
- ○ Stacked*
- ○ Flat + Stacked*

* indicates inflection points

Example: Enable Reuse of Today's Chiplets*

Type	Purpose
Physical Utility Chiplets	No functional value in ASIP prototype and/or product, help test package design and process. e.g., thermal dielet
Logical Utility Chiplets	No visible impact to the product datapath, help connect two existing chiplets, operate a package, validate a design etc. e.g., translators
Functional Utility Chiplets	Non-differentiated functions, but essential to ASIP product development.

*"The vision of advanced packaging relies on the availability of high-reuse chiplets…This has not yet happened" CHIPS National Advanced Packaging Manufacturing Program (NAPMP) Briefing. https://www.nist.gov/news-events/events/chips-national-advanced-packaging-manufacturing-program-napmp-briefing

NAPMP Chiplet Approach

- **Enable reuse of today's chiplets***
  - Use utility chiplets (e.g. translators) to glue today's chiplets together into prototypes and products
  - Create platforms that leverage trends in memory and I/O for faster/cheaper prototyping
  - Accelerate the development of an open chiplet economy/ecosystem
- **Create better integrated highly reusable smaller chiplets at fine pitches***
  - Standards for physical/functional integration and manufacturing - for cheaper/faster development and manufacturing e.g. chiplet warehousing
  - Extreme proof points – rack'n'pack – 100s-1000s of heterogenous chiplets in one package
  - 10/10/10 ecosystem that fully leverages advanced packaging - 10μ substrate pitch/10-person/$10m to product
- **Research focused on Chiplets Useability, Portability and Reuse***
  - Architecting for the future – lowering derivative cost, and changing interfaces,
  - Resilient reliability – systems not reliant on perfect die manufacturing and packaging assembly…
  - Algorithms to scale down design team size, chiplet discovery

*CHIPS National Advanced Packaging Manufacturing Program (NAPMP) Briefing
https://www.nist.gov/news-events/events/chips-national-advanced-packaging-manufacturing-program-napmp-briefing

Summary: Chiplet ecosystem crucial for advanced packaging

- **Today** — potential to accelerate the development of an ecosystem by enabling more reuse of today's chiplets.
- **But** — advanced packaging has been scaling more quickly in the recent past.
- **Ultimately** — a chiplet ecosystem that fully leverages advanced packaging, enables high degree of reuse to dramatically reduce product development cost.