CHIPS for America R&D Facilities Model

Introduction

The CHIPS Act requires the Department of Commerce "to establish the national semiconductor technology center [NSTC]" "to strengthen the economic competitiveness and security of the domestic supply chain." 15 U.S.C. 4656(c). The NSTC must "conduct advanced semiconductor manufacturing, design and packaging research, and prototyping that strengthens the entire domestic ecosystem." 15 U.S.C. 4656(c)(2)(A). In coordination with the NSTC, the Department of Commerce must also establish the National Advanced Packaging Manufacturing Program (NAPMP) "to strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem." 15 U.S.C. 4656(d).

Last year, the NSTC Vision and Strategy Paper (NSTC Vision) and the CHIPS National Advanced Packaging Manufacturing Program (NAPMP) Vision for Success (NAPMP Vision) highlighted the importance of increasing domestic access to advanced prototyping capabilities to support U.S. semiconductor research and development (R&D). The NSTC Vision also introduced the concept of a network of technical centers capable of end-to-end fabrication to enable R&D prototyping needs and highlighted as an imperative the need for close coordination between the NSTC and NAPMP programs.

Since then, the Department in partnership with Natcast, has been planning and assessing the needs of the community to prioritize initial CHIPS for America R&D facilities that can maximally benefit the semiconductor ecosystem.

CHIPS for America has developed a set of five principles to guide the approach to align those capabilities into an integrated CHIPS R&D facility strategy:

- **Accelerate innovation** by enabling world class R&D across the full range of microelectronics technical areas—including access to extreme ultraviolet (EUV) lithography, which is needed for research using the most advanced patterning technology;
- **Create differentiation** to ensure there is a clear value to the semiconductor ecosystem beyond existing comparable facilities;
- **Be financially sustainable** by creating enduring value for decades and attracting investment from all types and sizes of companies;
- **Be independent and neutral** by enabling Natcast, on behalf of the NSTC, and the NAPMP to make strategic decisions about the operation of the facilities, and by ensuring that the facilities are places where all member entities and their employees have the opportunity to successfully innovate;
- **Exist in thriving and vibrant ecosystems** that can provide, foster, and grow a talented workforce and a robust ecosystem of semiconductor companies, educational and research institutions, and local support to advance the mission.

These principles have guided the development of the first three CHIPS for America Research and Development facilities:

- NSTC Administrative and Design Facility
- NSTC Extreme Ultraviolet (EUV) Center
- NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility

These three state-of-the art facilities will establish world-class destinations for advanced semiconductor R&D in the United States. These facilities will address critical gaps in the current ecosystem, offering unparalleled value to a diverse array of stakeholders across the semiconductor value chain, including universities, businesses of all sizes, and government agencies. Together, these facilities will allow innovators to collaborate and solve the most challenging problems in microelectronics.

Key Drivers of CHIPS R&D Facilities Model

The CHIPS R&D facilities model is informed by over a year of discussions with stakeholders building on the release of the NSTC and NAPMP vision papers with stakeholders, and robust analysis on the current and planned future state of the U.S. semiconductor manufacturing, packaging, and R&D ecosystems. A request for information published by Natcast, in March 2024, collected feedback on the demand for prototyping facilities capabilities and also informed the facility model. The capabilities defined in this model are also aligned with strategy documents and thought pieces published by several independent entities that identified gaps and opportunities, and discussed how CHIPS for America should meet current industry demands.

The facilities defined in this model will complement many of the fabrication facilities enabled by the CHIPS Act. This facilities model is intended to support the ability for new innovations to better transition to those domestic fabs as a result of increased access to more robust prototyping and piloting capabilities.

As one example of a strategic imperative that will be met with this model, emerging artificial intelligence (AI)-driven applications are pushing the boundaries of current technologies like high performance computing and low power electronics, requiring significant advances in microelectronics capabilities. To meet the technical challenges posed by these technologies, the U.S. is investing in integrated R&D activities to improve all aspects of system performance. To help accelerate the time from lab to commercialization, the NSTC and NAPMP facilities will be equipped with the capabilities needed to validate and transition at scale the technologies necessary for continued U.S. leadership in critical and emerging technology like AI.

CHIPS R&D Facilities Model

Model Attributes

The CHIPS R&D facilities model initially focuses on core capabilities arranged into three dedicated facilities aligned for programmatic outcomes and efficiency. Given the scale and ambition of the CHIPS R&D facilities model and its importance to realizing critical economic and national security imperatives, the Department and Natcast will prioritize operationalizing these facilities. The Department and Natcast intend for the NSTC Administrative and Design Facility to be operational in 2025, the NSTC EUV Center by 2026, and the NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility in 2028.

Model Facilities

The NSTC Administrative and Design Facility

The NSTC Vision outlines a clear vision of a place-based institution for research and ecosystem convenings. The NSTC Administrative and Design Facility will be a multi-functional facility, serving as the location for key operations of the NSTC, including: hosting Natcast administrative functions; convening consortium members; and conducting NSTC programmatic activity such as the Workforce Center of Excellence and the NSTC Design Enablement Gateway.

This facility will serve as the center for advanced semiconductor research in chip design, electronic design automation (EDA), chip and system architecture, and hardware security.

Initial capabilities for design research will focus on rapid progress in using artificial intelligence and the move towards broad co-optimization between chip, package, and system-level requirements. The design, EDA, and architecture-related R&D conducted in this facility could then connect to prototyping at the NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility.

Natcast intends to have the NSTC Administrative and Design Facility operational in 2025.

The NSTC Administrative and Design Facility will require access to semiconductor design and manufacturing, EDA, packaging, workforce, and administrative expertise, and proximity to universities with advanced microelectronics research. The facility will have office space that can host Natcast employees, stakeholders, researchers, vendors, industry, and member assignees; as well as access to large convening spaces to hold consortium events, Advisory Boards and other meetings. Additionally, the facility is expected to have the ability to add test and characterization labs for chips and packages. Since there is not significant overlap with the activities taking place at the prototyping facilities, the NSTC Administrative and Design Facility need not be co-located with the packaging and prototyping facilities.

NSTC EUV Center

The NSTC EUV Center will provide NSTC members with access to EUV technology to facilitate a wider range of research and a path to commercialization, including technologies with the most challenging feature sizes. Next-generation technology development requires access to EUV lithography. Promising technologies that will be used in the most advanced logic or memory technology nodes must be evaluated and developed at length scales at or beyond the state of the art, and these can only be achieved today using EUV lithography tools.

EUV lithography systems require significant capital and operational expense. Since there are existing entities with EUV lithography capabilities, the facilities model envisions partnering with one of those entities to provide access to this capability for NSTC programs in a prompt and sustainable manner. As a result, the EUV Center does not require co-location with the two other facilities.

The Department and Natcast envision this center to include a full-flow EUV or High Numerical Aperture EUV technology and to be operational in an existing facility by no later than 2026. In addition to access to EUV technology, this center will also provide appropriate space for Natcast researchers and staff as well as member researchers and assignees to conduct research and collaborate in the facility.

NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility

The CHIPS R&D facilities model envisions co-located research and development prototyping and advanced packaging capabilities to further both the NSTC and NAPMP programs. The Department and Natcast believe a dedicated facility will allow the NSTC and NAPMP to fully optimize the design of the facility to meet its mission.

This prototyping capability will allow for research on new materials, tools, device structures, and integration methods of semiconductors. The Department and Natcast envision the prototyping capabilities to initially include at least one full-flow, complementary metal-oxide-semiconductor (CMOS) technology as a stable baseline for experiments. This technology will also help evaluate new ideas compared to standard devices and yield baselines before being judged suitable for introduction into production. The facility will include equipment that can process 300mm wafers, which enables the CMOS baseline flow described above. Most importantly, this equipment is the most compatible with state of the art logic and memory manufacturing

and will allow R&D developed in the facility to more easily transition to manufacturing. The same tooling will be used to provide recipe-level and module-level capability for a wide variety of experiments.

Silicon CMOS technology provides a foundation for research and a broad range of technologies that will be critical to future industry needs. Initially, the prototyping capability will focus on advanced computing that addresses AI and other workloads for which the core differentiated chips are based on silicon CMOS technology. Beyond the chips that are used for training and inferencing of AI models today, the model will support the research required for future technological advancements such as interconnect, embedded memory, and other materials and device innovations.

The Department envisions an advanced packaging capability that includes a stable advanced packaging baseline flow that will focus on heterogeneous integration of multi-component assemblies with a large number of interconnects to achieve a degree of integration that blurs the line between the chip and package. The capability would include an initial baseline flow oriented to high performance compute on silicon substrates, which represents the current majority of industry demand-driven needs of advanced packaging applications and will exercise heterogeneous integration by decreasing the pitch of the attached chiplets. To run the baseline flow, the facility will utilize 300mm semiconductor manufacturing tools supplemented with equipment to provide capability for package processing such as die singulation, chip and wafer bonding and pick and placement of chips and components. Finally, the facility will have the ability to integrate innovations realized through the NAPMP investments in the areas of: materials and substrates; chiplets; thermal and power management; equipment, tools, and processes; photonics and connectors; and EDA, so that successful development efforts can be transitioned, validated, and scaled for adoption in U.S. manufacturing as outlined in the NAPMP Vision.

Co-locating the NSTC R&D prototyping and NAPMP packaging capabilities in a single facility site will provide the domestic semiconductor ecosystem with unique value to conduct collaborative semiconductor and advanced packaging research. A facility with co-located capabilities will provide differentiated value enabling worldclass research across the full technology stack for semiconductors —from materials to design, to manufacturing, to silicon, to packaging.

Co-location of capabilities has several other operational efficiencies and financial savings. First, the Department and Natcast expect economies of scale in capital expenditures in the construction or retrofitting of a physical facility with two capabilities, as well as the ability to share some 300mm equipment. Additional operational efficiency and financial savings are envisioned to be realized through equipment maintenance, operational costs, and other resources that would otherwise be duplicated, such as failure-analysis and reliability labs.

Natcast, as the operator of the NSTC consortium, has the primary responsibility for standing up and operating the NSTC. While the NAPMP is a separate program, it is closely aligning with the NSTC as this model has been developed to maximize the synergy between the programs and impact of the facilities. This includes Natcast leading the operational process for site selection of these facilities.

This facility is intended to be operational by the end of 2028. Therefore, the Department and Natcast anticipate prioritizing options that can meet or expedite this projected timing (as well as achieve the other factors discussed, including costs, capabilities, and specifications). These options could include pre-existing facilities or greenfield sites that can meet or expedite the timeline.

Future Capabilities

Affiliated Technical Centers

The NSTC and NAPMP expect to prioritize the development of the initial foundational capabilities as described above. However, as discussed in the NSTC Vision, additional facilities capabilities are likely needed in the long term. As the NSTC Technical Advisory Board provides input on the NSTC Research Strategy, it may recommend acquiring additional capabilities such as access to labs to conduct earlier stage research and testing with new materials and equipment, compound semiconductors, sensors, micro-electromechanical systems, glass panel advanced packaging, advanced lithography or other specialized technologies. Natcast, on behalf of the NSTC, and the NAPMP will assess how members might access those capabilities including through future technical centers.

Multi-Project Wafers

NSTC members will need additional resources to support chip design, which is sometimes also referred to as prototyping. The Department and Natcast plan to facilitate that support through multi-project wafer (MPW) run programs. As outlined in the NSTC Vision, Natcast, on behalf of the NSTC, plan to aggregate and manage demand for access to MPW services at select commercial fabs. Details on the MPW program will be forthcoming.

Conclusion

CHIPS for America is beginning an unprecedented investment to establish and sustain a U.S. collaborative semiconductor R&D ecosystem. The Department and Natcast believe this model will enable CHIPS for America and Natcast to fulfill the ambitious visions that the NSTC and NAPMP have laid out. Once operational, these facilities aim to enable U.S. researchers, technologists, and businesses of all sizes to develop the innovations that will bend the trajectory of the future of semiconductor technology in a way that solidifies U.S. leadership and sustains our economic and national security.