U.S. Department of Commerce, NIST, National Advanced Packaging Manufacturing Program (NAPMP) Advanced Packaging Research and Development (R&D) 2025-NIST-CHIPS-NAPMP-01	
Funding Opportunity Description:	Applications such as high performance computing and low-power electronics, both needed for artificial intelligence (AI), require leap-ahead advances in semiconductor advanced packaging. This Notice of Funding Opportunity (NOFO) seeks proposals for R&D activities that will establish and accelerate domestic semiconductor advanced packaging through investments in five (5) R&D Areas: (1) Equipment, Tools, Processes, and Process Integration; (2) Power Delivery and Thermal Management; (3) Connector Technology, including Photonics and Radio Frequency (RF); (4) Chiplets Ecosystem; and (5) Co-design/Electronic Design Automation (EDA).
Announcement Type:	Initial
Funding Instrument:	Other transaction agreements (OTs), as authorized by 15 U.S.C. § 4659(a)(1).
Assistance Listing (CFDA Number):	11.042 – CHIPS R&D
Award Project Period:	Five (5) years
Goals & Objectives:	The NAPMP seeks to drive U.S. leadership in advanced packaging and provide the technology and skilled workforce needed for packaging manufacturing in the United States. Within a decade, NAPMP-funded activities, coupled with CHIPS manufacturing incentives, will establish a vibrant, self-sustaining, profitable, domestic advanced packaging industry where advanced-node chips manufactured in the United States and abroad can be packaged in appropriate volumes within the United States and innovative designs and architectures are enabled through leading-edge packaging capabilities. In combination with other CHIPS for America education and workforce efforts, NAPMP-funded activities will produce the diverse and capable workforce needed for the success of the domestic packaging sector. The objective of this NOFO is to enable, through R&D, innovative new advanced packaging flows suitable for adoption by U.S. industry.
Eligible Projects:	This NOFO envisions projects in five (5) R&D Areas: (1) Equipment, Tools, Processes, and Process Integration; (2) Power Delivery and Thermal Management; (3) Connector Technology, including Photonics and RF; (4) Chiplets Ecosystem; and (5) Co-design/EDA.

<table>
<tr><td>Eligible Applicants:</td><td>Eligible applicants are domestic non-profit organizations; domestic accredited institutions of higher education; State, local, and Tribal governments; and domestic for-profit organizations. A domestic entity is one that is incorporated within the United States (including a U.S. territory) with its principal place of business in the United States (including a U.S. territory).</td></tr>
<tr><td>Funding Amount:</td><td>CHIPS R&D anticipates making available up to approximately $1,550,000,000 for funding multiple awards of varying size and scope, with anticipated amounts ranging from approximately $10,000,000 to approximately $150,000,000 in Federal funds per award over a five (5) year period of performance. Anticipated total funding and approximate maximum award sizes per R&D Area are as follows:
<table>
<tr><th>R&D Area</th><th>Total Funding</th><th>Anticipated Maximum Award</th></tr>
<tr><td>Equipment, Tools, Processes, and Process Integration</td><td>$450M</td><td>$150M</td></tr>
<tr><td>Power Delivery and Thermal Management</td><td>$250M</td><td>$50M</td></tr>
<tr><td>Connector Technology, Including Photonics and Radio Frequency (RF)</td><td>$250M</td><td>$100M</td></tr>
<tr><td>Chiplets Ecosystem</td><td>$300M</td><td>$75M</td></tr>
<tr><td>Co-design/Electronic Design Automation (EDA)</td><td>$250M</td><td>$100M</td></tr>
</table>

CHIPS R&D anticipates reserving up to $50,000,000 to support recipients under this NOFO pursuing prototyping activities, to be awarded once the NAPMP National Advanced Packaging Piloting Facility (NAPPF) has established a baseline capability. Prototypes will focus on application areas such as high-performance computing and low-power systems needed for AI. Funding for prototyping activities will be executed as add-on projects to existing awards based on information that will be requested by CHIPS R&D at a later date.</td></tr>
<tr><td>Cost Share/Matching Requirements:</td><td>A non-Federal cost share over the lifetime of an award is strongly encouraged but not required. CHIPS R&D will give preference to proposals that demonstrate committed cost share in their Concept Paper and Full Application Project Narrative, Budget Narrative and Justification. The non-Federal cost share is that portion of the project costs not borne by the Federal government. Cost share may include cash, services, and third-party in-kind contributions, as described at 2 C.F.R. § 200.306.</td></tr>
</table>

<table>
<tr><td></td><td>Applicants may propose other types of cost share, provided that the proposed cost share is necessary and reasonable for accomplishment of the project objectives and approved by NIST.</td></tr>
<tr><td>Estimated Number and Type of Award(s):</td><td>Multiple awards for projects varying in scope and funding amount are expected under this NOFO.</td></tr>
<tr><td>How to Apply:</td><td>The submission of a concept paper is required. Eligible applicants may submit only one concept paper per R&D Area. Each concept paper may only include one R&D Area. Applicants may submit separate concept papers on different R&D Areas. Following concept paper evaluation, CHIPS R&D will invite and accept full applications from selected applicants only.

Applicants must submit concept papers and full applications through Grants.gov. Paper or emailed submissions will not be accepted. Applicants should be aware and factor into their submission planning that the Grants.gov system closes periodically for routine maintenance. Applicants should visit Grants.gov for information on any scheduled closures. Please note that an active registration in the System for Award Management (SAM) is required to submit concept paper and full application materials through Grants.gov. CHIPS R&D encourages prospective applicants and subrecipients to begin the process of registering in SAM.gov as early as possible.</td></tr>
<tr><td>Relevant Events and Dates</td><td>
<table>
<tr><th colspan="2">Advanced Packaging R&D NOFO Key Dates</th></tr>
<tr><td>Proposers Day(s)</td><td>October 22, 2024</td></tr>
<tr><td>Concept Papers Due</td><td>December 20, 2024, 60 days after publication</td></tr>
<tr><td>Invited Full Applications Due</td><td>Full applications will be due 60 days from the date of the invitation to submit.</td></tr>
</table>

Concept papers must be received no later than 11:59 p.m. Eastern Time, December 20, 2024, 60 days after publication. Full applications will be due 60 days from the date of invitation. Concept papers and full applications received after the specified deadlines will not be reviewed or considered.

Prior to the relevant concept paper and full application deadlines and within two weeks from the date of this announcement, CHIPS R&D plans to host a Proposers Day to promote awareness of the funding opportunity and provide a</td></tr>
</table>

	forum for organizations to identify prospective partners. After Proposers Day, CHIPS R&D will post a series of recorded webinars with more detail on the R&D Areas in this announcement. Questions about the funding opportunity, eligibility requirements, evaluation and award criteria, selection process, and the general characteristics of a competitive application will be addressed at Proposers Day and by e-mail for inquiries sent to research@chips.gov with "2025-NIST-CHIPS-NAPMP-01 Questions" in the subject line. Proposers Day participants must register in advance at National Advanced Packaging Manufacturing Program (NAPMP) Proposers Day (nist.gov). There is no cost to attend the informational webinars, but participants must register in advance at National Advanced Packaging Manufacturing Program (NAPMP) Proposers Day (nist.gov). Participation in Proposers Day and/or the informational webinars is not required and will not be considered in the review and selection process. Information about these events can be found on the CHIPS for America Webinars website.
Review and Selection Process:	The CHIPS R&D merit review process will assess both concept papers and full applications against the following five criteria: (1) relevance to economic and national security; (2) overall scientific and technical merit; (3) project management, resources, and budget; (4) transition and impact strategy; and (5) education and workforce development. The evaluation will be qualitative, not numerical. Following the merit review, an evaluation panel consisting of CHIPS R&D staff and/or other Federal employees with the appropriate expertise will conduct a panel review of the rated applications. The Selecting Official, the NIST Director or designee, will make final award recommendations to the NIST Agreements Officer.
Agency Contacts:	**Programmatic and Technical Questions:** E-mail: research@chips.gov with "2025-NIST-CHIPS-NAPMP-01 Questions" in the subject line **Award Rules and Regulations:** Lisa Ko E-mail: NOFO@nist.gov with "2025-NIST-CHIPS-NAPMP-01 Questions" in the subject line CHIPS R&D also maintains a public website that includes a Frequently Asked Questions page and other information pertaining to this funding opportunity.
Additional Information:	The U.S. Department of Commerce may amend this NOFO at any time. It may also close the funding opportunity with at least

	60 days' notice. Any changes will be communicated via https://www.grants.gov and https://www.chips.gov.

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Full Announcement Text

1 PROGRAM DESCRIPTION

The statutory authorities for the National Advanced Packaging Manufacturing Program (NAPMP) Advanced Packaging R&D Notice of Funding Opportunity (NOFO) are 15 U.S.C. § 4656(d) and 15 U.S.C. § 4659, as amended,[1] and 15 U.S.C. § 272(b)(4).

1.1 NAPMP PROGRAM OVERVIEW

The 2022 CHIPS and Science Act appropriated $50 billion to the U.S. Department of Commerce (the Department's) CHIPS for America program, to support semiconductor research and development (R&D) and to expand semiconductor manufacturing capacity in the United States. This includes $39 billion for the Department to expand domestic semiconductor manufacturing capacity through an incentives program and $11 billion to advance U.S. leadership in semiconductor R&D. These R&D advances are being realized through four programs: (1) the National Semiconductor Technology Center (NSTC), (2) the NAPMP, (3) the CHIPS Metrology Program, and (4) a CHIPS Manufacturing USA Institute. These investments, across both the R&D and incentives programs, seek to strengthen U.S. competitiveness, support domestic production and innovation, create, across the country, good jobs with working conditions consistent with the Good Jobs Principles published by the Departments of Commerce and Labor, and advance U.S. economic and national security.

1.1.1 CHIPS R&D Mission and Goals

Within the CHIPS for America program, the mission of the National Institute of Standards and Technology's (NIST) CHIPS Research and Development Office (CHIPS R&D) is to accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic research efforts, tools, resources, workers, and facilities. CHIPS R&D aims to achieve the following goals by 2030:

- ***U.S. Technology Leadership***: The United States improves its capacity to invent, develop, prototype, manufacture, and deploy the foundational semiconductor technologies of the future.
- ***Accelerated Ideas to Market***: The best ideas achieve commercial scale as quickly and cost effectively as possible.
- ***Robust Semiconductor Workforce***: Inventors, designers, researchers, developers, engineers, technicians, and staff sustainably meet evolving domestic government and commercial sector needs.

1.1.2 NAPMP Objectives

The NAPMP seeks to drive U.S. leadership in advanced packaging and provide the technology and skilled workforce needed for packaging manufacturing in the United States. Coupled with

[1] DOC CHIPS activities are authorized by Title XCIX—Creating Helpful Incentives to Produce Semiconductors for America of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Pub. L. 116-283, referred to as the CHIPS Act).

CHIPS manufacturing incentives, NAPMP-funded objectives will establish a vibrant, self-sustaining, profitable, domestic advanced packaging industry where advanced-node chips manufactured in the United States and abroad can be packaged in appropriate volumes within the United States and innovative designs and architectures are enabled through leading-edge packaging capabilities. In combination with other CHIPS for America education and workforce efforts, NAPMP-funded activities will produce the diverse and capable workforce needed for the success of the domestic packaging sector.

1.1.3 NAPMP Advanced Packaging R&D NOFO Objectives

The objective of this NOFO is to enable, through R&D, innovative new advanced packaging flows suitable for adoption by U.S. industry. To pursue this objective, CHIPS R&D designed the NOFO with the following elements.

- First, the NOFO sets out, across multiple R&D areas, key challenges and technology gaps in advanced packaging which must be addressed.
- Second, it provides for coordinated R&D efforts aligned through common technical targets so that results collectively contribute to composable and implementable advanced packaging flows.
- Finally, it provides for demonstrating the benefits of R&D results through a combination of prototypes and baseline packaging flows.

1.2 DEFINITIONS

For purposes of this NOFO, the terms listed below have the following meanings.

(1) **3DHI** – Three-dimensional heterogeneous integration (3DHI) refers to the ability to stack separately manufactured components – chips or wafers originating in different facilities, containing different semiconductors and materials – within a single package to improve functionality and performance.

(2) **Applied Research** – "Original investigation undertaken in order to acquire new knowledge."[2]

(3) **ASIC** – An application-specific integrated circuit (ASIC) is a chip that is designed for a particular application or use.

(4) **Associate Recipient** – A Recipient that agrees to cooperate with other Recipients by sharing information, data, technical knowledge, expertise, and/or resources essential to meet the objectives of the program under a mutual agreement that protects the proprietary information and intellectual property of both parties.

(5) **Basic Research** – "Experimental or theoretical work undertaken primarily to acquire new knowledge of the underlying foundations of phenomena and observable facts. Basic research may include activities with broad or general applications in mind, such as the study of how plant genomes change, but should exclude research directed towards a specific application or requirement, such as the optimization of the genome of a specific crop species."[3]

[2] OMB Circular A-11 84.2.(c).1
[3] OMB Circular A-11 84.2.(c).2

(6) **Bring up** – An iterative, phased process including initial testing, debugging, adjusting, and validating a device or system to achieve readiness for production or manufacturing.

(7) **Chip** – An assembly of electronic components, including miniaturized active and passive devices and their interconnections, that are built up on a semiconductor material, forming an integrated circuit.[4]

(8) **Chiplet** – A small, functionally targeted semiconductor chip that, when assembled at tight pitch and placement, results in a highly functional subsystem. Examples of chiplets in an ecosystem include common functions such as CPU, input/output devices, memory, domain-specific accelerators, etc.

(9) **Cluster** – A sequence of packaging steps, including relevant equipment and processes, that enables a key part of the packaging flow.

(10) **CMP** – Chemical Mechanical Planarization, a process to remove excess materials and smooth surfaces through a combination of chemical and mechanical methods.

(11) **Design Targets** – Information provided to applicants for this NOFO to inform their technology design and implementation choices; design targets in this NOFO are not mandatory but are provided to facilitate adoption by industry and make design efforts more manageable by focusing design options.

(12) **Die** – A small block of semiconducting material on which a given functional circuit is fabricated.

(13) **Exemplar Application** – An application area that serves as a model or archetype representing a broad range of computing system needs and challenges. For purposes of this NOFO, Exemplar Applications are limited to high-performance computing (e.g. for artificial intelligence) or low-power systems (e.g. hand-held mobile devices).

(14) **Heterogeneous Integration** – The integration of separately manufactured components into a higher-level assembly that, in the aggregate, provides enhanced functionality and improved operating characteristics.[5]

(15) **High-performance computing (HPC)**[6] – The use of supercomputers or computer clusters to solve advanced, intensive computational problems such as artificial intelligence applications or extreme-scale models and simulations.

(16) **Low-Power Systems** – Computational systems in which power is a primary limiting factor such as battery-powered, hand-held mobile devices.

(17) **Milestones** – Actions or events marking a significant change or stage in developments in a project.

(18) **Non-Technical Target** – Specific non-technical objectives in either education and workforce development, environmental sustainability, or commercial viability and domestic production to be achieved by the end of a project phase or at the end of the project as specified in the NOFO.

(19) **PDK/ADK** – A process design kit (PDK) is a set of files created by a semiconductor foundry to model and simulate the design and performance of the foundry fabrication

[4] https://www.britannica.com/technology/integrated-circuit
[5] https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html
[6] https://ieeexplore.ieee.org/abstract/document/6345493

processes. An assembly design kit (ADK) extends many of the benefits of PDKs to semiconductor packaging or assembly.

(20) **Phase-specific Target** – Includes both technical and non-technical targets, derived from applicant-specified milestones, to inform go/revise/no-go points for the transition from one project phase to the next. Phase-specific technical targets focus on measurable progress toward Project-Level Technical Targets. Phase-specific non-technical targets focus on measurable progress towards the Project-Level Non-Technical Targets defined by the applicant's Education and Workforce Development plan and Commercial Viability and Domestic Production plan. CHIPS R&D may identify additional phase-specific targets, including to address other applicant-defined plans.

(21) **Power Delivery Network or Power Distribution Network (PDN)** – A network of devices, traces, and planes that supply power to a chiplet(s). The purpose of the PDN is to ensure that the correct voltages and currents are delivered to each device without being over- or under-designed for the application.

(22) **Process integration** – Sequences and combinations of Unit Processes in which the end result is influenced by the unit process parameters and interactions between the processes.

(23) **Project** – All activities funded under a single award made under this NOFO, including but not limited to all planning and management; basic and applied research; systems, equipment, tools, and software systems development and production as appropriate to the R&D area; commercial viability analyses and domestic production preparation, integrated education and workforce development, and prototype production.

(24) **Project-level Technical Target** – Specific technical advances to be achieved by the end of the project (See Section 1.6).

(25) **Project-level Non-Technical Target** – Specific non-technical targets in either education and workforce development, environmental sustainability, or commercial viability and domestic production to be achieved by the end of the project (See Section 1.7).

(26) **Prototype** – A functional system and the end-to-end process flow for producing that system, both of which are designed for the purpose of measuring the characteristics of the flow and the resulting system. These characteristics include packaging process characteristics such as process stability, yield, reliability, and defectivity; and system characteristics such as functionality, performance, power/energy consumption, and thermal dissipation.

(27) **Recipient** – The entity that receives an award directly from a Federal awarding agency to carry out an activity under a financial assistance program.

(28) **Semiconductor** – An integrated electronic device or system, most commonly manufactured using materials such as, but not limited to, silicon, silicon carbide, or III-V compounds, and processes such as, but not limited to, lithography, deposition, and etching. Such devices and systems include but are not limited to analog and digital electronics, power electronics, and photonics, for memory, processing, sensing, actuation, and communications applications.

(29) **SMART**– A framework for writing objectives that are Specific, Measurable, Achievable, Relevant, and Time-Bound and provide the details for how an organization will achieve an objective.
(30) **Subassembly** – An assembled unit designed to be incorporated with other units in a finished product.[7]
(31) **Subrecipient** – An entity that receives a subaward from a pass-through entity (Recipient) to perform part of a program or project in accord with terms of a subaward. A subrecipient may also be a recipient of another award made by a Federal awarding agency.
(32) **Substrate** – The foundation or supporting platform on which or within which the elements of a semiconductor device are fabricated or attached.[8]
(33) **Substrate material** – The class of materials from which a substrate is made. Substrates relevant to this NOFO are organic, glass, and semiconductor-based (e.g., silicon-based) classes of materials.
(34) **Tape out** – The final stage of the design process for integrated circuits or printed circuit boards before they are sent for manufacturing.[9]
(35) **Technical Targets** – Technical specifications, such as line spacing, set by CHIPS R&D as objectives for project outputs to promote innovation.
(36) **Technology Demonstrator** – A functional device or system specifically designed to assess technologies and capabilities created by funded projects through scale-down, scale-out, and chiplets ecosystem approaches in comparison to conventional technologies.
(37) **Technology Node, Process Node, or Node** – While historically used to refer to chip feature sizes, such as gate length or line pitch, these terms are now widely used, including in this NOFO, to refer to a particular generation of chip technologies.[10]
(38) **TSV** – Through silicon via, a vertical electrical connection that passes through a silicon wafer or die.[11]
(39) **Unit process** – A discrete operation in a semiconductor manufacturing flow, such as lithography, deposition, or etching.

1.3 BACKGROUND

The technical focus and R&D area goals of this NOFO are informed by a series of industry roadmaps, including the 2024 IEEE Heterogeneous Integration Roadmap and International Roadmap for Devices and Systems, the Semiconductor Research Corporation (SRC) Microelectronics Advanced Packaging Technologies Roadmap; the UCLA and SEMI Manufacturing Roadmap for Heterogeneous Integration and Electronics Packaging (MRHIEP); and the iNEMI 5G/6G mmWave Materials and Electrical Test Technology Roadmap.

[7] https://www.merriam-webster.com/dictionary/subassembly
[8] Derived from the JEDEC general dictionary at https://www.jedec.org/standards-documents/dictionary/terms/substrate-semiconductor-device-1-general#
[9] https://en.wikipedia.org/wiki/Tape-out
[10] https://semiengineering.com/knowledge_centers/manufacturing/process/nodes/
[11] https://en.wikipedia.org/wiki/Through-silicon_via

Collectively, these roadmaps emphasize that emerging technologies like high performance computing and artificial intelligence, advanced telecommunications, biomedical devices, and autonomous vehicles require leap-ahead advances in microelectronics capabilities.[12]

In the past, the semiconductor industry has largely addressed performance needs by increasing the number and density of transistors on a chip, a process known as transistor scaling. However, the previous pace of transistor scaling, as expressed by Moore's Law, is slowing and cannot alone provide the performance improvements needed for emerging microelectronics technologies. Improving all aspects of system performance to support the breadth of new semiconductor applications will require innovations in advanced packaging.

Semiconductor packaging serves two general purposes. One is to protect the chip mechanically, thermally, and environmentally. The other is to enable reliable inter-chip communication and data processing, power delivery, and a stable test and system integration platform. Advanced packaging and related capabilities, such as heterogeneous integration, are designed to increase all aspects of system performance by linking multi-component assemblies with large numbers of interconnects to achieve a degree of integration that blurs the line between chip and package.

1.3.1 Program Drivers

Aligned with the industry roadmaps referenced above and the objectives outlined in Section 1.1.2, NAPMP has identified multiple program drivers required for domestic improvements in advanced packaging, as detailed in the subsections set out below.

1.3.1.1 Scale Down and Scale Out

The first program driver is the ability in advanced packaging to **scale down and scale out.** Scaling down refers to shrinking the size of the features on the package and increasing interconnect densities. Scaling out refers to increasing the number of chips assembled on the substrate and overall functional density in both two-dimensional (2D) and three-dimensional (3D) architectures. Examples of scaling down goals and targets can be found in the MRHIEP roadmap.

> *The primary driver for advanced 2D and 3D packaging technologies is the need for increased interconnect densities to support* [heterogeneous integration] *and deliver increasing bandwidth in a power efficient manner while enabling efficient power delivery.* 2024 IEEE Heterogeneous Integration Roadmap (Chapter 22, p. 14)

Accordingly, in their planning activities, applicants should consider interdisciplinary, team-based approaches that contribute to scaling down and scaling out in advanced packaging.

[12] These roadmaps are cited in this NOFO for informational purposes. The fact that the roadmaps are cited does not necessarily mean that the entire content of these publications reflects the views of the Department of Commerce, CRDO and/or NIST.

1.3.1.2 Heterogeneous Integration Including Chiplets

The second program driver is advancing capabilities for **three-dimensional heterogeneous integration (3DHI), including chiplets**. This driver focuses on the NAPMP vision for creating "an advanced packaging ecosystem based on heterogeneous chiplet technology to promote widespread and easy use of the technologies developed." NAPMP Vision Paper (p. 3)

> *Heterogeneous Integration is essential to maintain the pace of progress with higher performance, lower latency, smaller size, lighter weight, lower power requirement per function, and lower cost.* IEEE Heterogeneous Integration Roadmap 2021 (Chapter 1, p. 12)

> [T]*he exponential growth in package pin counts and I/O power consumption, domain-specific architectures, technical and business models of* [intellectual property] *reuse, and mixed technology node chiplets will drive advances in HI and advanced packaging*. SRC Microelectronics Advanced Packaging Technologies Roadmap (p. 154)

In developing proposals, applicants should incorporate considerations for heterogeneous integration and chiplets-based architectures.

1.3.1.3 End-to-End Advanced Packaging Flows

The third program driver is enabling **end-to-end advanced packaging flows** suitable for adoption by industry. This driver, per the NAPMP Vision Paper, addresses the NAPMP objective to "develop packaging platforms capable of both high-volume and customized manufacturing."

> *The CHIPS Research and Development Office has designed the NAPMP to include an Advanced Packaging Piloting Facility ([N]APPF) where successful development efforts will be transitioned and validated for scaled transition to U.S. manufacturing*. NAPMP Vision Paper (p. 3)

To address this driver, applicants should plan for implementing their research outputs in a full packaging flow.

1.3.1.4 Prototypes for Demonstrating Functionality

The fourth driver is **demonstrating functionality in prototypes** to provide evidence for new capabilities, increased efficiencies, lowered production costs, reduced environmental impact, or other benefits resulting from research advances. This driver addresses the NAPMP vision, per the NAPMP Vision Paper, for enabling "successful advanced packaging development efforts to be validated and transitioned at scale to U.S. manufacturing." This NOFO includes support for designing prototypes in two exemplar application areas: high performance computing (HPC), including artificial intelligence (AI), and low-power systems, such as handheld mobile devices.

1.3.1.5 Aligning R&D Efforts for Implementable Packaging Flows.

The final program driver is **aligning R&D** efforts so that R&D results are not isolated or incompatible but instead collectively contribute to implementable advanced packaging flows. Successful applicants should expect to participate in coordination and information-sharing across projects in all R&D areas, consistent with Section 1.5.

1.4 FUNDING OPPORTUNITY DETAILED DESCRIPTION

1.4.1 Project Activities

Project activities are expected to include, but not necessarily be limited to, all of the following: basic and applied research; systems, equipment, tools, and software systems development and production as appropriate to the R&D area; commercial viability analyses and domestic production preparation; integrated education and workforce development; and prototype production.

CHIPS R&D expects that applicants assembling teams (i.e., an applicant from industry or academia working with one or more eligible subrecipients) may be best suited to collectively provide the full range of expertise and capabilities needed to achieve the program objectives and to successfully strengthen U.S. advanced packaging innovation. Equally important, effective partnerships can promote inventiveness, clarify future demand, improve transparency and security, solidify business and domestic manufacturing plans (including plans for technology adoption by defense and commercial partners), develop environmentally sustainable manufacturing solutions, help educate the future workforce, mitigate the risk of future chip shortages or oversupply, and support a more productive, efficient, and self-sustaining semiconductor ecosystem.

CHIPS R&D therefore strongly encourages proposals from teams that demonstrate collaboration across the innovation, manufacturing, supply chain, and customer landscape, as well as across the industry, non-profit, and academic sectors.

1.4.2 Project Structure

Consistent with the objectives described in Section 1.1.2 and Section 1.1.3, applications under this NOFO must describe projects that:

(1) Focus on one of the R&D areas described in Section 1.4.3
(2) Propose achieving specific R&D area Technical Targets and Project-Level Non-Technical Targets, as described in Sections 1.6 and 1.7
(3) Define milestones marking measurable progress toward those targets
(4) Provide for supplying any required demonstration devices to CHIPS R&D and to other entities for research purposes, as described under each R&D area in Sections 1.6.1 through 1.6.5
(5) Sub-divide project activities into four phases, with each phase ranging in length as described under each R&D area in Sections 1.6.1 through 1.6.5
(6) Are structured around a five (5) year period of performance

1.4.3 R&D Areas Overview

Consistent with the NAPMP Vision Paper, this NOFO calls for Concept Papers and invited Full Applications in the following five R&D areas:

(1) Equipment, Tools, Processes, and Process Integration

(2) Power Delivery and Thermal Management
(3) Connector Technology, Including Photonics and Radio Frequency (RF)
(4) Chiplets Ecosystem
(5) Co-design/Electronic Design Automation (EDA)

To ensure that funded R&D efforts meet the objectives described in Section 1.1technical targets for applicants to achieve are described in each of the five R&D areas described in Sections 1.6.1 through 1.6.5 below. Individual Concept Papers and invited Full Applications must address only one of the R&D areas.

1.4.4 Milestones and Phase-Specific Targets

Applicants should propose milestones that represent measurable steps toward achieving the applicant's Project-Level Technical Plans under the relevant, applicant-selected R&D areas (see relevant R&D area requirements in Section 1.6). Applicants should also propose milestones that represent measurable steps toward achieving their EWD plans and CVDP plans as described in Sections 1.7.1 and 1.7.2. Applicants may propose additional non-technical milestones.

Milestones for Project-Level Technical plans, EWD plans, and CVDP plans should be SMART and suitable for validation by the applicant, CHIPS R&D staff, independent expert technology evaluators, or a combination of these entities, as appropriate.

The CVDP milestones should complement the technical milestones. For example, technical milestones should, as appropriate, inform CVDP targets and milestones, such as manufacturing time, cost, performance, and projected customer demand. Additional CVDP milestones may include measurable progress in business plan development, customer identification, investor commitments, technology licensing agreements, and enabling manufacturing in the United States.

In coordination with the Financial Assistance Agreements Management Office (FAAMO), CHIPS R&D may conduct negotiations with applicants deemed meritorious by the evaluation panel and determined by CHIPS R&D to stand a reasonable chance of being funded, in order to (1) refine the proposed milestones (2) define phase-specific targets derived from the proposed milestones, and (3) address other matters as determined by CHIPS R&D. These phase-specific targets will inform go/revise/no-go points for the transition from one project phase to the next.

1.5 General Roles of Award Recipients and NIST

1.5.1 Substantial Involvement

CHIPS R&D will have ongoing and substantial programmatic involvement with award recipients throughout the award period of performance, although primary responsibility for project activities will reside with award recipients.

1.5.2 Recipient Responsibilities

This program is subject to Attachment A – Associate Recipient Agreements (see Section 8.3). The success of funded activities under this NOFO hinges upon continuous collaboration and coordination across funding recipients. Therefore, any resultant award will contain terms and conditions pursuant to the stipulations outlined in Attachment A.

CHIPS R&D may further require the recipients to:

(1) Attend a kick-off conference, held at the beginning of the performance period, to help ensure that recipients have a clear understanding of the program and its components; and
(2) If applicable, coordinate with NIST in the development of collaborations with other Federal agencies, including NIST laboratory programs, or other CHIPS-funded activities.

1.5.3 Involvement of NIST and CHIPS R&D

NIST / CHIPS R&D may provide, as appropriate:

(1) Programmatic and financial oversight of the Institute award;
(2) Input or direction relevant to the coordinated provision of information or deliverables across recipients, consistent with any requirements to protect intellectual property;
(3) Subject matter experts to support collaborative research;
(4) Coordination and engagement with other Federal agencies or with other CHIPS-funded activities; and
(5) Research security and other relevant support, as described in Section 2.7and Section 3.1.4.

In an award agreement issued under this NOFO, NIST and potentially other Federal agencies may require access to research material and data.

1.6 R&D AREA-SPECIFIC INFORMATION FOR PROJECT-LEVEL TECHNICAL PLANS

The following subsections provide information specific to each R&D area to assist applicants in preparing responsive Project-Level Technical Plans for both Concept Papers (see Section 4.5) and Full Applications (see Section 4.6).

1.6.1 R&D Area 1: Equipment, Tools, Processes, and Process Integration

1.6.1.1 Anticipated Amounts

For the Equipment, Tools, Processes, and Process Integration R&D area, CHIPS R&D anticipates making available up to approximately $450,000,000 for funding multiple awards in amounts ranging from approximately $10,000,000 to approximately $150,000,000 in Federal funds per award, with a five (5) year period of performance per award. While cost share is not required, CHIPS R&D will give preference to proposals that demonstrate credible cost share commitments, consistent with Section 3.2.

1.6.1.2 Background

Advances in packaging processes and equipment are required to achieve the scaled down dimensions set out in the previous NAPMP Materials and Substrates NOFO (see Table 2, page 14 in that document) and to enable innovative, manufacturable advanced packaging flows suitable for adoption by U.S. industry. The processes and equipment that are the focus for this R&D area are those that will enable end-to-end advanced packaging flows suitable for high-volume manufacturing, customized manufacturing, piloting, and prototyping. The new tools and processes that emerge from this R&D activity will create a need for education and training programs to supply a skilled equipment and process workforce to a vibrant and growing U.S. advanced packaging sector.

Proposals within this R&D area should focus on developing: (1) advanced, flexible, extensible process technologies and integration sequences required to produce a packaged subassembly; and (2) packaging equipment to run the advanced processes and to handle the required substrates, wafers and dies, all at scaled down dimensions and designed for use at commercial scale.

This investment in equipment, tools, processes, and process integration is intended to achieve the following outcomes.

- **3-5 years:** New tools, processes, and integrated flows from R&D projects are installed in the NAPPF to assess efficacy and extendibility and to gather insights into suitability for commercial adoption. Tools and processes are incorporated in NAPPF prototyping flows. Programs are established to improve tool and process performance and packaging flow manufacturability. The first new graduates emerge from new education and training programs for advanced packaging equipment and process technology. Enrollments are diverse and growing.
- **10 years:** Robust production equipment and environmentally sustainable, integrated advanced packaging processes for chiplet-based manufacturing at commercial scale are available for use by U.S. industry. End-to-end advanced packaging flows composed of the equipment, processes, and integration sequences developed in this R&D area are being used by U.S. industry in chiplet-based heterogenous integration and 3D architectures. Graduates from education and training programs are employed in good jobs in the advanced packaging sector.

1.6.1.3 Equipment, Tools, Processes, and Process Integration Objectives

The objective of this R&D area is to develop, demonstrate and deliver advanced tools, processes, process integration sequences and fine-pitch assembly methods required for chiplet-based packaging architectures and 3DHI. Development activities are organized around packaging process clusters, with a cluster defined as a sequence of steps that enable a key part of the packaging flow.

The five process clusters relevant to this R&D area are the following.

1. **Chiplet Singulation:** Producing singulated chiplets from incoming wafers that are fully patterned with dies for subsequent assembly

2. **Chiplet to Substrate Assembly and Bonding:** Positioning and attaching chiplets with ultra-fine-pitch bonding pads to substrates in dense arrays with close chiplet-to-chiplet spacing
3. **3DHI:** Forming heterogeneous chiplet stacks with ultra-fine bonding pad pitches
4. **Collective Chiplet Processing:** Methods to simultaneously process an array of singulated chiplets using a handler wafer or other suitable substrate
5. **Finishing:** Incorporating advanced power delivery, passivation, thermal management, and connectors, using technologies included but not limited to photonics, into the packaged device

Applications for this R&D area must address one or both of the following two categories:

1) Process Cluster Development: Applications in this category must address full tool and process solutions for one or more of the five packaging process clusters described above. Successful applications will present a comprehensive R&D approach that encompasses integrated tool and process development, interactions between process steps, and step sequencing within each cluster and between clusters as appropriate. Applicants are strongly encouraged to incorporate in their applications innovative and potentially transformative technologies to improve cluster performance and capabilities.

2) End-to-End Advanced Packaging Flows: Applications in this category must focus on sequencing multiple clusters into end-to-end packaging process flows to create a functional, testable packaged system (or subsystem) with all the required elements and with performance characteristics that leverage the advanced packaging constructs being funded. These complete systems can be targeted for specific applications such as high-performance computing, artificial intelligence, and low-power systems (including low power sensor nodes, IoT, and biomedical applications), among others. If the intended end-to-end flow requires additional tools or processes not covered in the clusters, they need to be developed or provided as part of the application and included in the proposed budget.

   For this category, applications are sought that will include plans for the following:
   1. Developing an integrated end-to-end packaging process flow based on the process technology and equipment developed in this R&D area
   2. A performer-developed Bring-up Assembly Vehicle (described in Section 1.6.1.9) to demonstrate the integrated process flow
   3. Plans to transition the integrated process flow to the NAPPF

The subsections below describe objectives for each of the five clusters and end-to-end packaging flows.

1.6.1.4 Cluster 1 - Chiplet Singulation

The R&D objective for this cluster is to develop advanced, extensible, manufacturable process flows and associated equipment to produce singulated chiplets from incoming wafers that are patterned with dies.

Advanced packaging architectures based on heterogeneous chiplet technology use advanced bonding methods to attach chiplets with ultra-fine-pitch bonding pads to substrates. The singulation cluster must therefore produce chiplets that are free from surface particles, defects, and contaminants that negatively impact bond quality, yield, and reliability. Close chiplet spacing is an important parameter for system-level performance scaling. The singulation cluster must therefore produce chiplets with repeatable dimensions and sidewalls free from defects such as cracks and chips that limit chiplet-to-chiplet spacing. Also, flexible tools and processes will be required to singulate a variety of incoming wafers, which may include, for example:

- Different wafer sizes (e.g., 300 mm, 200 mm, 150 mm, 100 mm)
- Full thickness wafers and thinned wafers, with and without thru silicon vias (TSVs)
- Different materials (e.g., Si, SiC, GaAs, GaN)
- Assembled 3DHI wafer stacks

Successful R&D proposals will center on advanced, high-precision, low-damage dicing methods that minimize and/or eliminate defects that impact assembly, bond quality, yield, and reliability. Examples include, but are not limited to, chemical methods that allow for rounded corners and chamfered edges. Extensions of saw blade dicing used in conventional packaging flows are not in scope. However, multi-step methods that require a saw blade step to achieve cluster targets are permitted.

Proposals must describe tool and process development for a full flow to produce singulated chiplets ready for the assembly process. In addition to the dicing/separation method, development should include all operations required for the proposed flow, such as patterning, thinning, and cleans. Proposals should include a description of the test vehicles and methods that will be used to characterize, optimize, and demonstrate process, tool, and cluster efficacy.

Proposals must describe the singulation method, wafer types to be singulated, key equipment and processes within the flow including metrology, and focus areas to improve cluster performance and capabilities. Activities to improve throughput, cost-of-ownership, and overall cluster efficiency and manufacturability are encouraged. Solutions that minimize use of per- and polyfluoroalkyl substances (PFAS)[13] and other harmful chemicals, reduce emissions and water usage, improve manufacturing energy efficiency, and/or incorporate circular manufacturing are also encouraged.

Singulated chiplets may be placed in carriers for subsequent operations, transport, or storage. Proposals for standardized chiplet carriers and tool interfaces suitable for a chiplet-based commercial packaging line are included in this cluster's scope. The carriers must have placement accuracy consistent with the assembly sub-micrometer (μm) overlay accuracies and sub-10 μm inter-chiplet spacings.

1.6.1.5 Cluster 2 - Chiplet to Substrate Assembly and Bonding

[13] For context and details on chemicals and production challenges, see for example the technical papers at https://www.semiconductors.org/pfas/

The objective for this cluster is to develop advanced processes and equipment to bond chiplets with ultra-fine-pitch bonding pads to substrates in dense arrays with close (sub-10 μm) chiplet-to-chiplet spacing. This is an essential process capability for developing advanced packaging flows suitable for adoption by U.S. industry. This R&D area has the opportunity to significantly advance and expand the performance and manufacturing capabilities of available bonding platforms.

R&D for this cluster must focus on bonding methods that will scale bond pad pitch to 1 μm and below. Examples include hybrid bonding (HB), thermal compression bonding (TCB), and alternative methods that meet the cluster Technical Targets (see Section 1.6.1.10). Extensions to conventional solder-based assembly are not in scope. However, enhancements to the bond interface metallurgy that yield measurable benefits are permitted. Chiplet shear force, pull strength, and thermal and humidity cycling standards must meet MIL-STD-883G standards.

Successful proposals will present an integrated tool and process approach to develop and optimize all factors related to alignment and bonding. Examples include, but are not limited to, bonding surface topography, bonding interface activation and treatments, alignment methodology, bonding sequence, anneal, tool configuration, and environmental control. Additional tools and processes required to produce a bonded chiplet array are included in the development scope, including but not limited to chemical mechanical polishing (CMP), etching, cleans, film deposition and gap fill. Inclusion of integrated and/or stand-alone inspection, appropriate metrology, and testing capability to verify process and tool performance is encouraged. A consolidated throughput of over 1,000 chiplets/hour is expected for chiplet assembly including surface preparation steps and alignment.

Alignment methodologies must be clearly described in the proposals, including drawings and/or tables detailing alignment fiducial type, dimensions, required area, formation, and locations on the pairs to be bonded. This will inform chiplet design and EDA and may require iteration to achieve standardization.

Wafer-to-wafer, chiplet-to-substrate, and chiplet-to-chiplet assembly and bonding all have applications for advanced packaging and 3DHI and are therefore in scope. Applications can address one or more of these assembly methods. Additional assembly methods may be included along with a detailed description of the tool and method, target applications, and potential benefits of the proposed method.

Applications must include a description of the test vehicles and metrology methods that will be used to characterize, optimize, and validate process, tool, and cluster efficacy. Note that test vehicle design and procurement are the responsibility of the applicant.

In addition to chiplet arrays, assembly and bonding are required for the 3DHI cluster and Collective Chiplet Processing cluster. CHIPS R&D will work with successful Assembly and Bonding applicants during the award period to coordinate with the 3DHI and Collective Chiplet Processing teams so that project results collectively contribute to flexible, extensible assembly and bond solutions for a range of advanced packaging architectures and process flows.

The tools and process technology elements developed in this cluster will be installed in the NAPPF as key enablers for development and prototyping activities. Respondents to this Assembly and Bonding cluster are encouraged to include in their application plans for an End-to-End Packaging Flow (or flows) and a Bring-Up Assembly Vehicle as described in Sections 1.6.1.3 and 1.6.1.9.

1.6.1.6 Cluster 3 - Three-Dimensional Heterogeneous Integration (3DHI)

The R&D objective for this cluster is to develop integrated process flows to: (1) produce functional stacks of heterogeneous chiplets with ultra-fine-pitch die-to-die connection points, and (2) integrate these stacks into a packaged device. This R&D area has the opportunity to significantly advance 3DHI manufacturing technology for adoption by U.S. industry.

Successful proposals will present an integrated tool and process R&D approach for 3DHI stacks composed of at least six (6) chiplets with a target maximum stack of 24 chiplets including thermal solutions as needed. Chiplet-to-chiplet connection density is an important parameter for high-bandwidth memory (HBM) and other 3DHI devices. Proposed development should therefore target <1 μm bond pad pitch between stack layers with stack-to-substrate connection pitch of 10 μm or less. At a minimum, development should target stacks of identically-sized chiplets with different functions. Applicants may optionally propose additional stacks containing different size chiplets and/or layers with more than one chiplet, and such options are encouraged.

3DHI stack assembly and integration into the package will require using and/or sequencing many of the tool and process technology elements developed in other process clusters. CHIPS R&D will work with successful 3DHI applicants to coordinate with the Assembly and Bonding, Collective Chiplet Assembly, and Singulation cluster teams so project results collectively contribute to advancing 3DHI packaging architectures.

Applicants must propose an integrated approach to developing and optimizing the 3DHI process flow from incoming chiplet preparation to stack assembly, stack testing, and integration into the package. 3DHI stacks assembled and integrated by wafer-to-wafer, chiplet-to-substrate and chiplet-to-chiplet bonding are in scope, and applications may address any or all assembly and bonding methods. Alternative 3DHI assembly and integration methods that meet cluster technical targets for fine-pitch assembly will be considered. In addition to assembly and bonding, development must encompass all tools and processes in the flow, such as TSV pattern and etch, liner formation, via fill, dielectric deposition, metallization, CMP, and associated metrology.

Applications must include a description of the test vehicles and metrology methods that will be used to characterize, optimize, and validate process, tool, and cluster efficacy. Note that test vehicle design and procurement are the responsibility of the applicant.

Successful applications for the 3DHI cluster should have a method to test and validate the tools and processes by proposed End-to-End Integrated flows and Bring-Up Assembly Vehicles, which are described below (Section 1.6.1.9).

Dense packaging architectures such as 3DHI create new challenges for three-dimensional power delivery and thermal management. The Power Delivery and Thermal Management (PDTM) R&D area of this NOFO (R&D area 2 - Section 1.6.2) targets developing innovative solutions to these types of challenges. The Finishing process cluster (Section 1.6.1.8) includes a technical activity to integrate these PDTM innovations into the 3DHI stack. Applicants to this 3DHI cluster are encouraged to include activities under Cluster 5 to integrate R&D Area 2 power delivery and thermal management solutions into the 3DHI stacks (See Figure 1 in Section 1.6.1.9). CHIPS R&D will work with successful 3DHI applicants during project execution to coordinate with the PDTM R&D team, so project results collectively contribute to advances in 3DHI performance and functionality.

The tools and process technology elements developed in this 3DHI cluster will be installed in the NAPPF as key enablers for development and prototyping activities. Applicants to this 3DHI cluster are encouraged to include in their applications plans for an End-to-End Packaging Flow (or flows) and a Bring-Up Assembly Vehicle as described in Sections 1.6.1.3 and 1.6.1.9.

1.6.1.7 Cluster 4 - Collective Chiplet Processing

Manufacturable advanced packaging flows will require methods to collectively process arrays of singulated chiplets through operations within the flow. The objective for this cluster is to develop collective chiplet assembly and processing methods suitable for advanced packaging at commercial volumes. Collective chiplet processing should be compatible with the scaled down dimensions set out in the previous NAPMP Materials and Substrates NOFO (see Table 2, page 14).

One example of collective chiplet assembly and processing is to temporarily bond or adhere a precisely positioned chiplet array to a handler such as a semiconductor or glass wafer. The chiplets are then processed on the carrier through the required operations. The chiplets may be de-bonded from the handler upon completion of the processing steps.

Examples of operations that may benefit from collective chiplet processing include:

- Backside thinning and polishing to produce chiplets with uniform thickness
- TSV formation and reveal
- Bonding surface CMP
- Wet cleaning and surface preparation
- Applying materials such as gap fill and passivation layers to the chiplet array
- Chiplet array reconstitution
- Using a handler wafer to simultaneously bond a chiplet array to a packaging substrate

Proposals must identify the target applications for collective chiplet processing, describe the potential benefit to advanced packaging architectures, and describe an integrated tool and process development approach for all steps required for collective chiplet assembly and subsequent processing. Proposals to expand collective processing to key chiplet processing operations are encouraged.

Proposals must describe the tools and methods for positioning, attaching, and releasing chiplets to/from the handler. Chiplet-to-handler attachment based on, for example, tape, spin-on applied adhesives, and multi-layer adhesive systems are in scope, as are attachment methods that do not require an adhesive. Also in scope are equipment for chiplet-to-handler placement, equipment for temporary bond and de-bond, required metrology, and other tools and processes required for the flow.

Proposals for using a handler wafer to simultaneously bond a chiplet array to a substrate are encouraged. CHIPS R&D will work with successful Collective Processing applicants during project execution to coordinate with the Assembly and Bonding R&D team (Cluster 2), so project results collectively contribute to flexible assembly and bond solutions for a range of advanced packaging architectures and process flows. Note that Cluster 2 technical targets for chiplet positioning and chiplet-to-chiplet spacing will apply to this collective bonding application.

1.6.1.8 Cluster 5 - Finishing

The objective for this cluster is to develop equipment, processes, and methods that enable advanced finishing operations for substrates that have completed the assembly and bonding cluster. These operations include:

- Incorporating power delivery and thermal management elements developed in R&D area 2 (Power Delivery and Thermal Management - Section 1.6.2)
- Integrating and attaching the advanced connectors (wired, RF or photonics) developed in R&D area 3 (Connector Technology - Section 1.6.3)
- Passivation – Protection and encasement of the bonded chiplets and other elements incorporated in the package as needed
- Testing the chiplet assembly for functionality at a level sufficient to proceed with finishing operations
- Substrate singulation

The R&D objectives, package integration challenges, technical targets, and expected outputs for R&D Area 2 (Power Delivery and Thermal Management) and R&D Area 3 (Connector Technology, Including Photonics and RF) are described in their respective sections. Application teams responding to R&D Area 2 and/or R&D Area 3 are encouraged to include in their applications development activities to integrate the resulting innovations into the packaged device under this Finishing cluster.

As part of the finishing process, advanced chiplet-based packaged assemblies will require a variety of passivation materials targeted at the characteristics of the architecture. Highly conformal deposition methods are required to uniformly deposit the films in the restrictive geometries that result from close chiplet-to-chiplet and chiplet-to-substrate spacing. Thicker films will be required to planarize dense chiplet arrays that include three-dimensional stacks, and other components in the assembly. Applications for materials and deposition methods are solicited, including applied research studies to characterize factors that impact reliability.

1.6.1.9 End-to-End Advanced Packaging Flows

Integrated Process Flows: The objective of this R&D category is to develop manufacturable end-to-end integrated process flows (IPF) for assembly methods such as (but not limited to) wafer and panel scale integration, 3D chiplet stacking, and Fan-out Wafer-Level Packaging, on substrates to be developed under the NAPMP Materials and Substrates NOFO and that incorporate the thermal, power delivery and connector solutions being developed in R&D Area 2 and R&D Area 3 of this NOFO. Successful IPF applications will be based on sequencing and integrating the process clusters developed in this R&D Area 1 and include additional processes and modules as required for the complete flow. The integrated process flows will be installed in the NAPPF and used to develop, fabricate, and pilot functional prototypes.

Bring-Up Assembly Vehicle: In order to demonstrate this flow, proposals should include plans to produce a bring-up assembly vehicle comprised of test chiplets designed to verify and characterize cluster and integrated-flow efficacy. The bring-up assembly vehicle should have full diagnostics that are required to debug and optimize the process technology needed for a functional prototype, including yield and reliability, while also having the ability to test all the elements that will be developed under this NOFO, including power, connectors, and thermal solutions. Furthermore, the bring-up vehicle should also be able to validate the PDKs and ADKs used in the NAPPF. Ideally, the vehicle is modular such that, while it could be run in its entirety, it could also be run in short-loop segments for specific experiments.

Figure 1 shows the relationship of the integrated process flow and the bring-up assembly vehicle in relationship to the individual R&D areas. Note that these IPFs will be used to fabricate and pilot functional prototypes in the NAPPF using the bring-up assembly vehicle.

Installation into NAPPF: The IPFs will need to be installed as baseline flows in the NAPPF, where they will be the primary vehicles for further process optimization, functional optimization, and packaging node development. It is expected that the bring-up assembly vehicle will be run on these baseline flows with continuous improvements and periodic feature scaling similar to the Silicon CMOS scaling model that drove “Moore’s Law.” While the NAPPF is being constructed, proposer teams are expected to exercise these flows in a reasonable fashion in their own facilities.

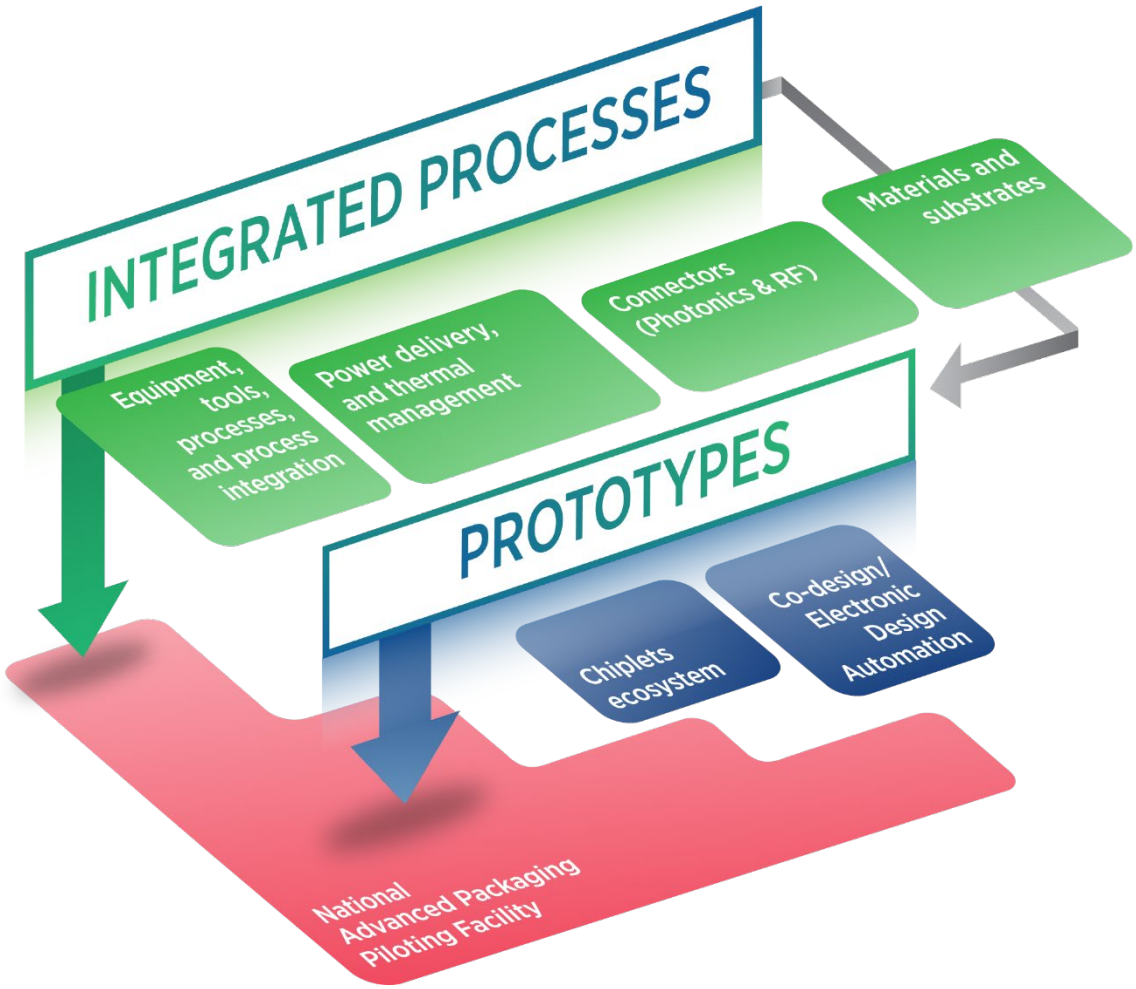

Figure 1. The relationship of the integrated process flow and the process bring-up chiplets in relationship to the individual R&D areas.

1.6.1.10 R&D Outputs, Design and Technical Targets

1.6.1.10.1 Outputs

Expected R&D outputs include: (1) advanced processes and assembly methods for chiplet-based advanced packaging architectures, (2) equipment to achieve targeted specs at piloting volumes, and (3) end-to-end packaging flows composed of the resulting tools and processes.

1.6.1.10.2 Design and Technical Targets

This section provides:

- Design Targets providing information for applicants to inform their technology design and implementation choices; and
- Technical Targets providing technical specifications set by CHIPS R&D as objectives for project outputs to promote innovation.

Applicants are asked to indicate for each Technical Target whether they will exceed, meet, or not meet the target or whether the target is not applicable to their approach.

The Technical Targets in the tables below are intended to drive significant advances in tools, processes, and fine-pitch assembly methods required for chiplet-based packaging architectures and 3DHI. For all technical areas, applicants are strongly encouraged to incorporate in their proposals innovative and potentially transformative technologies to improve cluster performance and capabilities.

Applicants may propose additional Technical Targets beyond the CHIPS R&D-specified Technical Targets described in each table. In cases where the applicant does not intend to meet or exceed a technical target and/or opts to include additional technical targets, the applicant should carefully explain how their proposed approach nonetheless represents a significant technical advance relative to the global state of the art, and will accomplish the CHIPS R&D mission and goals (see Section 1.1.1) and the specific objectives of this NOFO (see Section 1.1.3).

1.6.1.10.3 Chiplet Singulation Cluster Targets

Tables 2 and 3 below provide design and technical target information specific to proposals addressing the Chiplets Singulation Cluster.

Table 2: Chiplet Singulation Design Targets: Incoming Wafer and Chiplet Information	
Incoming Wafer Information	Full thickness wafers patterned with chiplets
	Thinned wafers patterned with chiplets
	Bonded stacks of full wafers (2 to 24 wafers high)
	One chiplet size per wafer
	Note: Methods to singulate wafers with multiple chiplet sizes will be considered but are not required.
	100 mm, 150 mm, 200 mm, 300 mm wafers
	Substrate materials: Si, SiC, GaAs, GaN
	Alignment fiducials on wafers
	Passivation film on bonding surface
	Note: Dicing streets will have no metal. Methods to address metal structures will be considered but are not required.
Chiplet Information	Chiplet sizes (mm): 2×2, 5×5, 10×10, 4×6, 8×10
	Chiplet sizes for 3DHI (mm): 5×5, 10×10, 8×10
	Note: Chiplet sizes are for cluster and process flow development. To ensure accurate and reliable handling of relevant chiplet sizes, equipment

	should be capable of handling both large and small chiplets, which might be as small as 1 mm × 1 mm (or smaller).
	Alignment fiducials on chiplets
	Bonding pads on device side
	Passivation film on bonding surface
	Non-yielding chiplets identified

Table 3: Technical Targets for Chiplets Singulation	
Chiplet Singulation Parameter	**Technical Target**
X and Y dicing precision	+/- 0.5 μm
Sidewall variation	+/- 0.1 μm 3 sigma
Post-singulation cracking / chipping	No cracks or chips beyond 0.5 μm from chiplet edge
Electrostatic discharge (ESD) failures	< 0.1 ppm (one out of 10^{-7})
Chiplet corners	Chamfer or rounding preferred but not required
Dicing cluster minimum throughput	Ten (10) 300 mm wafers per hour, higher preferred
Note: Technical Targets are for Si, SiC, GaAs, GaN wafers. Spec deltas for any material should be specified in the proposal.	

1.6.1.10.4 Chiplet to Substrate Assembly and Bonding Cluster Targets

Tables 4 and 5 below provide design and technical target information specific to s addressing the Chiplet to Substrate Assembly and Bond cluster.

Table 4: Incoming Chiplet and Substrate Information	
Substrates	1) 300 mm semiconductor-based substrates, including substrates developed under the NAPMP Materials and Substrates NOFO. 2) Glass or organic panels up to 510 mm x 515 mm, including substrates developed under the NAPMP Materials and Substrates NOFO. Proposals for alternative substrates will be considered.
	Alignment fiducials on substrate
Chiplets	Chiplets in carrier or on adhesive tape
	Bonding pads on device side
	Passivation film on bonding surface
	Alignment fiducials on chiplets
	Chiplet sizes (mm): 2×2, 5×5, 10×10, 4×6, 8×10
	Note: Chiplet sizes are for cluster and process flow development. To ensure accurate and reliable handling of relevant chiplet sizes, equipment should be

	capable of handling both large and small chiplets, which might be as small as 1 mm × 1 mm (or smaller).

Table 5: Technical Targets for Chiplet to Substrate Assembly and Bonding	
Assembly and Bonding Parameter	**Technical Target**
Chiplet-to-substrate assembly	Arrays containing five (5) chiplet sizes on substrate
Maximum bond pad pitch	10 μm
Ultimate bond pad pitch target	<1 μm
Pad to pad placement accuracy (x, y)	<10% of bonding pitch
Maximum chiplet to chiplet spacing	<12 μm, closer spacing preferred
Post-bond voids	No voids greater than 0.5 % of bonding pitch, collective void density not to exceed 2.5 % of bond pitch.
Metallurgical bond strength	Cohesive failure within metal pads seen during bond test (e.g., die shear or chevron testing) as per MIL-STD-883G.
Electrostatic discharge (ESD) failures	< 0.1 ppm (one out of 10^{-7})
Production throughput – Chiplet-to-substrate	> 3000 chiplet placements per hour; consolidated 1000 chiplets per hour (consolidated includes any ex-situ process such as surface preparation)

1.6.1.10.5 3DHI Cluster Targets

Tables 6 and 7 below provide design and technical target information specific to applications addressing the 3DHI Cluster.

3DHI	NOFO target
Chiplet sizes for 3DHI cluster development (mm)	5×5, 10×10, 8×10
Chiplet substrate material	Si. Stacks including alternative materials (e.g., SiC or GaN for power delivery) are encouraged.
Alignment fiducials	On chiplets and substrates
Assembly methods	Wafer-to-Wafer, Chiplet-to-Substrate, Chiplet-to-Chiplet. Alternative assembly methods will be considered.

Table 6: Technical Targets for 3DHI	
3DHI Parameter	**Technical Target**
Minimum chiplet stack	6

Maximum chiplet stack	24
Stacks of identically sized chiplets with different functions are required for all applications. Stacks containing different size chiplets and/or layers with more than one chiplet are encouraged.	
Chiplet-to-chiplet bond pad pitch target	1 μm. Below 1 μm will be considered
3DHI stack to substrate bond pad pitch target	10 μm initial, ≤ 1 μm final
Placement Accuracy (3 sigma)	10% of bond pitch
Wafer-to-wafer bond production throughput	≥ 12 bonded pairs per hour
Chiplet-to-chiplet bond production throughput	> 3000 chiplet bonds per hour.
Post-bond voids	No voids greater than 0.5 % of bonding pitch, collective void density not to exceed 2.5 % of bond pitch
Metallurgical bond strength	Cohesive failure within metal pads seen during bond test (e.g., die shear or chevron testing) must meet MILSPEC
Electrostatic discharge (ESD) failures	< 0.1 ppm (1e-7)

1.6.1.10.6 Collective Chiplet Assembly Cluster Targets

Table 7: Design Targets for Collective Chiplet Assembly	
Carrier	300 mm Si wafers, 300 mm glass wafers. Alternative carriers will be considered
Chiplet sizes (mm)	2×2, 5×5, 10×10, 4×6, 8×10
Alignment fiducials	On chiplets and carrier as needed
Collective Assembly Parameter	**Technical Target**
Chiplet assembly	Arrays containing five (5) chiplet sizes on carrier
Chiplet placement and spacing	As required for the collective processing operations
Note: For applications using a carrier wafer to simultaneously bond a chiplet array to a substrate, chiplet positioning targets for Cluster 2 - Assembly and Bond will apply. Targets below.	
Placement accuracy for simultaneous bond (x, y)	<10% of bond pitch (3 sigma)
Max. chiplet to chiplet spacing for simultaneous bond	Approximately <12 μm, closer spacing preferred

1.6.1.10.7 Finishing Cluster Targets

Design and technical targets for Power Delivery/Thermal Management and Connector integration are provided in the respective R&D area sections of this NOFO.

1.6.1.10.8 End-to-End Advanced Packaging Flow Assembly Cluster Targets

Table 8: Design Targets for End-to End Package Flow and Bring Up Assembly Vehicle	
End-to-End Advanced Package Flow	**NOFO target**
Target Application	Wafer or panel scale integration; Stacking Chiplets; Fan-out-Wafer Level Packaging or similar
Design of Bring up Assembly Vehicle	Created by performer to be representative of a future prototype. Minimum of 25 chiplets with over 1M daisy chain connections
Content of Bring up Assembly Vehicle	Created by performer with as many diagnostics structures as possible. Inclusive of ADK/PDK validation, yield/Reliability, and forward-looking ground rule structures.
Chiplet	Sourcing is performer choice, could be supplied by chiplet R&D Area
Thermal Solution	Sourcing is performer choice, could be supplied by Thermal R&D Area
Connector	Sourcing is performer choice, could be supplied by Connector Technology R&D Area
Connector, Photonic	Sourcing is performer choice, could be supplied by Connector Technology R&D Area
Commercial Availability	Chiplets and materials for End-to-End Advanced Package flow should be able to be purchased by NAPPF for use as an ongoing baseline

1.6.1.11 Project Structure

1.6.1.11.1 Required Team Capabilities

CHIPS R&D strongly encourages applications from multi-disciplinary, multi-organization project teams that collectively demonstrate the full range of expertise, experience, and development capabilities needed to achieve the technical objectives of this R&D area. For the purposes of this NOFO, a project team comprises all funded entities (the applicant and any proposed subrecipients) as well as unfunded collaborators planned for inclusion in a single application. Project team participation from academic and other research entities is strongly encouraged.

Collective team experience designing, developing, demonstrating, and delivering advanced packaging equipment and integrated processes for forward-looking technology nodes will be a key factor in the application evaluation.

Due to the compressed timeline of this program, team members responsible for key development activities must have commercially active capability to manufacture targeted equipment, as well as the ability to create and modify equipment to achieve the targeted technical results. For example, a team that proposes development for a bonder that achieves the targeted technical specs should include an organization that is currently producing a bonder.

Applicants should propose milestones that represent measurable steps toward achieving Project-Level Non-Technical Targets, as described in Sections 1.7.1 and 1.7.2. Applicants may also propose additional non-technical milestones.

1.6.1.12 Project Phases

1.6.1.12.1 Overview

Applicants must propose a detailed project plan for achieving Project-Level Technical Targets. Projects should be divided into four (4) phases over a five (5) year period of performance. Phases 1 and 2 should be 12 months each and Phases 3 and 4 should be 18 months each. Execution plans for each phase should describe key R&D activities and risk assessments, milestones within the phase and go/no-go checkpoints between the phases. Go/no-go checkpoints will be evaluated by CRDO and will encompass a comprehensive review of progress toward achieving technical targets, risk assessment, and mitigation plans. Progress towards achieving cluster technical targets will be benchmarked by data sets supporting tool capabilities and process performance.

1.6.1.12.2 Phase 1 (12 months)

CHIPS R&D expects activities in Phase 1 to include, as necessary:

- Define and document baseline toolset, unit processes, and process flows for development
- Align with other ETPI cluster teams, R&D Area teams and NAPPF on tool and process requirements
- Optimize unit processes, integration sequences and assembly methods towards cluster technical targets
- Test vehicle design and procurement

Phase 1 SMART technical milestones should define progress toward demonstrating equipment and process capabilities relative to the technical targets. Go/revise/no-go decision points for transition from Phase 1 to Phase 2 will be finalized at the time of award including, but not limited to, demonstration of fundamental tool and process capability to achieve cluster technical targets.

1.6.1.12.3 Phase 2 (12 months)

CHIPS R&D expects activities in Phase 2 to include, for example:

- Periodic project alignment checkpoints with NAPPF and other R&D Areas
- Initial integrated cluster development towards technical targets
- Co-optimize tools, processes, and integration sequences to improve repeatability, process windows, and throughput

- Demonstrate tool, process, and cluster performance relative to technical targets
- Finalize process flows and tool configurations as well as generate appropriate tool documentation (operation manuals, maintenance schedules, etc.)
- Finalize plan to build and install tools developed under this program in the NAPPF

Phase 2 SMART technical milestones should define progress toward achieving Project-Level Technical Targets and ETPI R&D area outputs.

Phase-specific go/revise/no-go decision points for transition from Phase 2 to Phase 3 will be finalized at the time of award including, but not limited to, achieving cluster technical targets or determining whether they can be achieved with further development and optimization.

1.6.1.12.4 Phase 3 (18 months)

CHIPS R&D expects Phase 3 to focus on activities to transfer technology elements developed under this program to the NAPPF, for example:

- Periodic alignment checkpoints with NAPPF, other R&D areas, and prototyping team
- Optimizing process flow and short-loop cycles of learning using Bring-Up Assembly Vehicle
- Install, start-up and verify performance of the tools developed under this R&D Area in NAPPF, including documentation and training for NAPPF support staff
- Demonstrate cluster flows and IPFs in the NAPPF using Bring-Up Assembly Vehicles

Phase 3 SMART technical milestones should focus on achieving the Project-Level Technical Targets. Milestones should leverage research and engineering progress to refine and extend tool and process capabilities, as well as demonstrating readiness for installing key tools and IPFs in NAPPF.

Phase-specific milestones marking go/revise/no-go decision points for transition from Phase 3 to Phase 4 will be defined at the time of award including, but not limited to, validating that the equipment and processes are ready to achieve the production level target required to execute cluster development plans.

1.6.1.12.5 Phase 4 (18 months)

CHIPS R&D expects Phase 4 activities to focus on NAPPF bring up, development and prototyping, for example:

- Complete cycles of learning to verify capability for functional prototypes
- Determine and document best known methods for producing packaged functional prototypes
- Continuous improvement activities for tools, processes, and integration sequences

Phase 4 SMART technical milestones should focus on steps toward prototyping and pilot-level production.

During Phase 4, CHIPS R&D aims to provide equipment, tools, processes, and process integration samples, along with relevant documentation such as process assumptions, design manuals, process design kits (PDK, compatible with NAPMP-specified format), and electrical specifications, to Federally funded research projects in other areas of packaging research that would benefit from access. Examples of these other research areas include new equipment, tools, and processes; innovation in power delivery and thermal management; novel chiplet technologies; and wired, radio frequency, and optical connectors. Examples of research projects include those associated with the NAPPF, the NSTC, the CHIPS Manufacturing USA Institute, or other Federally funded research programs. NIST will allow award recipients to recover costs for producing these tools for CHIPS R&D-designated research projects. Options for cost recovery are direct, reimbursable provisions by the applicant; licensing to other domestic entities with capacity for reimbursable production at pilot scale; or installing manufacturing capability in an NAPMP-funded facility, such as the planned NAPPF.

1.6.2 R&D Area 2: Power Delivery and Thermal Management

1.6.2.1 Anticipated Amounts

For the Power Delivery and Thermal Management R&D area, CHIPS R&D anticipates making available up to approximately $250,000,000 for funding multiple awards in amounts ranging from approximately $10,000,000 to approximately $50,000,000 in Federal funds per award, with a five (5) year period of performance. While cost share is not required, CHIPS R&D will give preference to applications that demonstrate credible cost share commitments consistent with Section 3.2.

1.6.2.2 Background

This R&D area focuses on power delivery, power efficiency, and thermal management challenges for advanced packaging. Overcoming these challenges is needed to enable continued improvements in the speed and efficiency of semiconductor-based systems. For example, high-performance computers are increasingly power-intensive but must avoid running at too high a temperature to avoid damaging internal components. Low-power and mobile electronics push the limits of performance and efficiency and must make trade-offs between maximum performance and long battery life. Advanced chiplet-based architectures, including 3DHI and dense architectures, create new, three-dimensional power and thermal design and management challenges.

Examples of needed advances in this R&D area include innovation in delivering power efficiently, locally, and dynamically; producing less waste heat through energy efficiency strategies; supporting integration with emerging technologies, such as connectors; designing systems that tolerate heat better; and improving heat removal and management.

Proposals should focus on (1) improving the performance, reliability, and overall efficiency of semiconductor devices through innovation in power delivery and thermal management and (2) transitioning the resulting innovations into commercial scale manufacturing.

This investment in innovation in power delivery and thermal management is intended to achieve the following outcomes.

- **3-5 years:** New materials, designs, processes, and tools are poised to transition to high-volume manufacturing. Innovative approaches emerge for active and passive cooling for low-power and active cooling for HPC, including 3DHI, that greatly enhance system performance and efficiency. New measurement methods, including utility chiplets, are developed and validated to improve materials, models, designs, processes and tools for power delivery and thermal management. Thermal and power modeling capabilities are expanded to handle complex chiplet stacks produced in advanced packaging flows. Validated power and thermal models are aligned with new design tools developed under the NAPMP Co-Design/Electronic Design Automation R&D area (see Section 1.6.5) and other CHIPS R&D design activities.
- **10 years:** Devices assembled with advanced packaging operate reliably at higher power density and with greater energy efficiency. Thermal dissipation and power delivery are no longer gating factors limiting advanced packaging. Chiplets that are thermally- and power-aware with powerful dynamic management capabilities are readily available in the chiplets ecosystem.

1.6.2.3 Power Delivery and Thermal Management Objectives

Proposals for this R&D area must address one or more of the four objectives described in the subsections below. Within each objective, proposals must address one or more of the challenges but are not required to address all challenges listed within that objective.

1.6.2.3.1 Objective 1: Power Delivery and Management

For applications focused on HPC systems, this objective includes innovative approaches to delivering power at high density with efficient voltage regulators and dynamic power management schemes for 3DHI devices, including modular designs and devices for integration with a variety of chiplets.

For applications focused on low-power systems, this objective includes design optimization, energy efficiency, and energy harvesting technologies.

Under this objective, all applicants must address one or more of the following six power challenges. Unless otherwise noted, each challenge is applicable to both HPC and low-power systems.

1. **Power Delivery Networks (PDN) optimization:** Optimize the design of power delivery networks, including the layout of power planes, passives including decoupling capacitors, and voltage regulation.
2. **Energy-Efficient and Integrated Voltage Regulators:** Develop advanced voltage regulators that dynamically adjust based on workload, optimizing energy efficiency

without compromising performance. Integrate voltage regulation directly onto chips, minimizing power distribution losses and enabling finer control.

3. **Wide Bandgap Semiconductors:** Incorporation of advanced materials, such as silicon carbide (SiC) and gallium nitride (GaN), to reduce power losses and enhance efficiency for integrated power management.
4. **Energy-Aware Application Specific Integrated Package (ASIP) and Low-Power Design:** Optimize the allocation of resources and minimize power consumption while maintaining performance using low-power design methodologies, such as power gating, clock gating, and other techniques to reduce static and dynamic power consumption.
5. **Energy Harvesting Technologies:** Develop energy harvesting with embedded local energy storage techniques to supplement or replace traditional power sources for appropriate applications (*only applicable to low-power systems*).
6. **Emerging Technologies:** Integrate emerging technologies, such as photonics, that will drive simultaneous improvements in performance and energy efficiency.

1.6.2.3.2 Objective 2: Thermal Management

For applications focused on HPC systems, this objective includes new thermal solutions that are compatible with advanced substrates, 3DHI, and other advanced packaging design aspects to reduce hotspots, maintain thermal targets, and enable reliability in 3DHI multilayer stacks without constraining connectivity.

For low-power systems, this objective includes compact and lightweight thermal solutions, often working in a narrower temperature range.

Under this objective, applicants must address one or more of the following four thermal management challenges, which are all applicable to both HPC and low-power systems.

1. **Materials and Devices for Thermal Management:** Develop advanced materials and processes with improved thermal conductivity, electrical insulation, and suitable thermo-mechanical properties.
2. **Microscale and Nanoscale Heat Transfer:** Study and exploit heat transfer at the micro- and nano- scale to address challenges unique to small-scale semiconductor components, including interfacial thermal resistance and microfluidic and microscale heat exchangers.
3. **Thermal Aware Circuit Design and Dynamic Thermal Management:** Integrate thermal considerations into the circuit design and power management strategies to optimize power distribution and minimize localized heating, thereby improving overall device thermal performance.

Reliability: Improve the long-term reliability of components and their susceptibility to aging and thermo-mechanical effects via improvements in thermal management.

1.6.2.3.3 Objective 3: Power and Thermal Models

This objective includes validated, higher fidelity thermal and power models and accelerated learning using artificial intelligence and machine learning (AI/ML) to accurately predict power and thermal distributions across chiplet stacks and enable and accelerate advanced system design and evaluation.

Under this objective, applicants must address one or more of the following modeling challenges, which are applicable to both HPC and low-power solutions.

1. **Thermal Modeling and Simulation:** Improve thermal modeling and simulation techniques to better understand heat dissipation mechanisms, including at interfaces, enabling more accurate predictions and optimizations in device design.
2. **Validation of models:** Validate models using data from utility chiplets, preferably in coordination with CHIPS Metrology and the forthcoming CHIPS Manufacturing USA Institute.
3. **Automation of models:** Use automation to take advantage of accelerated learning cycles with tools such as AI/ML and reduce time to develop and validate new thermal and power solutions.
4. **Design Kits:** Create PDTM process and assembly, thermal, and/or power design kits, in collaboration with EDA performers, to accelerate and automate the implementation of thermal and power solutions.

1.6.2.3.4 Objective 4: Integrated Power and Thermal Management

Under this objective, applicants must address the following integrated management challenge.

1. **Integrated Management:** Integrate power delivery and thermal management to achieve maximum performance, reduce hot spots, and improve overall reliability.

Proposals within this R&D area should consider related research challenges within other R&D areas, including Co-Design/Electronic Design Automation (Section 1.6.5) and Chiplets Ecosystem (Section 1.6.4). In scope are vertical heat extraction; local heat spreading; embedded cooling; advanced methods for active and passive cooling of 3DHI devices to reliably operate at higher power density; wide bandgap chiplets for 3DHI; and advanced models, materials, and architectures to achieve specific thermal goals such as low-resistance thermal interfaces. On chiplet embedded structures, 3D stacks and films are in scope.

Out of scope in this R&D area are discrete packaged wide bandgap devices, conventional air-cooling approaches, discrete passives, and development of batteries. Application-specific thermal and power solutions, such as solutions developed for a single device that cannot be used for other devices without substantial redesign, are out of scope for this R&D area to ensure thermal and power solutions are modular, reusable, and useful for multiple applications within the chiplet ecosystem.

1.6.2.4 R&D Outputs and Technical Targets

1.6.2.4.1 Outputs

Expected R&D outputs include. novel equipment, tools, materials, processes, devices, and models that demonstrate improved performance; utilization of test devices and chiplets to demonstrate performance in 3DHI stacks with a path to scale; standards and metrologies derived from test devices; test and evaluation at prototype- and pilot-scale manufacturing; and proven processes, materials, models and devices with improved performance available for the CHIPS ecosystem.

Implementing the CHIPS R&D Chiplet Ecosystem vision (Section1.6.4) requires the development of specific power delivery and thermal management chiplets. Chiplets should be modular and reusable for multiple applications and should not be application specific.

1.6.2.4.2 Provision of Thermal and Power Solutions for CHIPS R&D-Designated Research Projects

CHIPS R&D aims to provide thermal and power solutions developed under this NOFO to research projects in other areas of packaging research that would benefit from the new technology. Examples of these other research areas include new equipment, tools, and processes; advanced substrates; Co-Design/EDA; Chiplets Ecosystem; and Connector Technology, Including RF and Photonics. Examples of research projects include those associated with the NAPPF, the NSTC, the CHIPS Manufacturing USA Institute, or other Federally funded research programs.

CHIPS R&D will expect recipients to make available for use by other research projects CHIPS R&D-designated thermal and power solutions along with relevant tools and documentation including process assumptions, design manuals, process design kits (PDK, compatible with NAPMP-specified format), and physical, electrical, thermal, and mechanical specifications for use by other research projects. CHIPS R&D will work with award recipients to ensure appropriate protections for the recipient's IP rights (see Section 2.8). For Phase 4 budgeting purposes, applicants should plan to provide a minimum of 100 and a maximum of 1,000 each of thermal and power solutions samples. NIST will allow award recipients to recover costs for producing these thermal and power solutions samples for CHIPS R&D-designated research projects as part of the award costs.

Options for providing thermal and power solutions are direct, reimbursable provision of these solutions by the applicant; licensing to other NAPMP-approved U.S.-based entities with capacity for reimbursable production at pilot scale; or installing manufacturing capability in an NAPMP-funded facility such as the planned NAPPF.

1.6.2.4.3 Technical Targets

The following subsections provide Technical Targets for each of the four objectives above. Applicants must indicate, for each of either the HPC targets or the low-power system targets as

appropriate to their application, whether they will meet, exceed, or not meet the target or whether the target is not applicable for their approach. Proposals for Objectives 1 and/or 2 are encouraged to also include utility chiplets as described in Objective 3.

1.6.2.4.3.1 Objective 1: Power Delivery and Management

Technical Targets for HPC, including 3DHI

1. Demonstrate high efficiency voltage regulation with the ability to test and implement advanced power management strategies including segmented power delivery and dynamic power management for chiplet-based advanced packaging, including 3DHI.
    a. Power delivery and regulation chiplets should be modular and not application specific.
    b. Achieve better than 95% efficiency at both low power and full power operation with the same device and with a small footprint.
2. Demonstrate power delivery in excess of 2 kW per packaged device with a focus on sub-1 V power regulation (e.g., 2000 A, 0.8 V) and power density[14] exceeding 4 W/mm^2.
    a. Achieve stable power-delivery-network-impedance less than 0.025 mΩ at operating frequency.
    b. Demonstrate power delivery and power management on an assembly of densely packed chiplets, with an arrangement that is at least three chiplets wide, three chiplets deep and three chiplets tall and includes side-by-side and/or alternating stacks of logic and memory chiplets, with an area of at least 900 mm^2.
    c. Demonstrate integration using a combination of silicon and advanced materials (e.g., GaN or SiC).
    d. Idle power consumption shall not exceed 4% of full power.
    e. A standby or suspend state shall not exceed 1% of full power.
    f. Reliable power connections for the power solutions shall be included.
3. Develop chiplet-based passives for advanced packaging, including 3DHI, such as inductors and capacitors, for integration within the package. Applicants should note that NAPMP expects to coordinate R&D in this area with R&D undertaken under the previous NAPMP Materials and Substrates NOFO; work in this area would supplement and not replace work on passives embedded in the substrate and should conform to specifications in the Chiplets Ecosystem R&D Area (Section 1.6.4).
    a. Capacitors: Demonstrate a capacitance greater than 3 $\mu F/mm^2$ with a high quality factor.
    b. Inductors: Demonstrate a density greater than 70 nH/mm^2 with a high quality factor.

[14] https://eps.ieee.org/images/files/HIR_2023/ch20_thermalfinal.pdf

Technical Targets for low-power systems, including 3DHI

1. Demonstrate power delivery and power regulation chiplet designs for low power applications.
    a. Power delivery and power regulation chiplets should be modular and not application specific.
    b. Idle power consumption shall not exceed 2.5% of full power.
    c. A standby or suspend state shall not exceed 0.25% of full power.
2. Demonstrate power delivery and regulation for ultra-low-power applications such as sensors, wearables, etc., powered, at least in part, by energy harvesting where both space and power are constraints.
    a. Exceed 10 mW/cm^2 and 50 mWh/cm^2 of power and energy harvesting per 24 hours.
    b. Integrated energy harvesting and storage method should be able to run a demonstration sensor (specified by the applicant) for at least 1 week, and, preferably, for longer periods.
3. Develop high-efficiency voltage regulation and conversion with the ability to test and implement advanced power management strategies.
    a. Achieve better than 95% efficiency for low-power systems.
    b. May include advanced materials (e.g., SiC or GaN).
    c. Demonstrate extremely low standby / resting-state power consumption over a 24-hour cycle.
4. Develop chiplet-based passives for advanced packaging, including 3DHI, such as inductors and capacitors, for integration within the package. Applicants should note that NAPMP expects to coordinate R&D in Chiplet-based passives with R&D undertaken under the previous NAPMP Materials and Substrates NOFO; work in this area would supplement and not replace work on passives embedded in the substrate and should conform to specifications in the Chiplets Ecosystem R&D Area (Section 1.6.4).
    a. Capacitors: Demonstrate a capacitance greater than 3 $\mu F/mm^2$ with a high quality factor.
    b. Inductors: Demonstrate a density greater than 70 nH/mm^2 with a high quality factor.

1.6.2.4.3.2 Objective 2: Thermal Management

Technical Targets for HPC, including 3DHI

1. Develop advanced materials, devices, and strategies for thermal management to allow for reliable operation in excess of a power dissipation of 4 W/mm^2.
    a. Desirable to demonstrate improvements in compute efficiency of 100× over 2024 levels by the five-year mark and not simply implement thermal solutions for higher power without improvements in efficiency.
2. Develop advanced cooling strategies to include:
    a. Ambient pressure working fluids.

    b. One-phase and two-phase liquid cooling.
    c. Refrigerant-based cooling, including low global warming potential refrigerants[15].
    d. Submerged cooling with relevant working fluids in approaches that allow for cost effective repair or rework of submerged components.
    e. Reliable connectors for the thermal solutions (e.g. connections for the working fluid) where necessary.
3. Reduce hot spots—The peak local chiplet temperature should be no greater than 10 °C hotter than the mean temperature at full power (measured on those chiplets limiting the thermal load, such as logic).
4. Develop heat spreading and heat buffering materials and processes.
    a. Phase change materials for heat buffering.
    b. High thermal conductivity materials for heat spreading and heat removal.
        i. Emphasis on materials with thermal conductivity above 1500 W/m·K.
    c. Materials and methods to reduce or eliminate interfacial thermal resistance.
        i. Ideal thermal performance would match an interface-free design.
        ii. May include but must not be limited to basic research needed on thermal interfaces and reducing interfacial thermal resistance.
5. Demonstrate compatibility of power delivery and thermal solutions with existing (or new) in-line testing and failure analysis techniques.

Technical Targets for low-power systems, including 3DHI

1. Develop thermal strategies for wearables to control surface temperatures below 34 °C.
2. Develop advanced lightweight/compact cooling strategies to include:
    a. Heat pipes, vapor chambers and in-plane heat spreaders.
    b. Liquid cooling where appropriate for the intended application.
3. Reduce hot spots—The peak local chiplet temperature should be no greater than 7 °C above the mean temperature at full power (measured on those chiplets limiting the thermal load, such as logic).
4. Develop heat spreading and heat buffering materials and processes.
    a. Phase change materials for heat buffering.
    b. High thermal conductivity materials for heat spreading and heat removal.
        i. Emphasis on materials with thermal conductivity above 1000 W/m·K.
    c. Materials to reduce or eliminate interfacial thermal resistance.
        i. Ideal thermal performance would match an interface-free design.
        ii. May include but must not be limited to basic research needed on phonon transport at interfaces and reducing interfacial thermal resistance.
5. Develop advanced thermal insulation to protect exposed surfaces and/or heat sensitive internal components.

[15] https://www.epa.gov/system/files/documents/2023-10/technology-transitions-final-rule-fact-sheet-2023.pdf

6. Demonstrate compatibility of power delivery and thermal solutions with existing (or new) in-line testing and failure analysis techniques.

1.6.2.4.3.3 Objective 3: Power and Thermal Models, Designs and Validation

Technical Targets for this objective are as follows.

1. Develop high fidelity modeling approaches capable of handling large arrays of chiplets on a substrate to predict, automate, and accelerate the development of future thermal and power solutions.
    a. These models shall be developed and demonstrated in coordination (to ensure compatibility) with EDA performers.
2. Fabricate and validate highly instrumented and diagnosable chiplets that can be assembled and tested in bonded stacks as test devices, with appropriate supporting thermal and/or power models for an arrangement that is at least three chiplets wide, three chiplets deep, and three chiplets tall covering an area of at least 900 mm^2.
    a. These test devices must be compatible (preferably fully integrated) with existing design software and design resources from the EDA area (Section 1.6.5).
    b. Thermal utility chiplets shall report temperature for a grid spaced at 0.2 mm or less across the chiplet.
    c. Thermal utility chiplets shall have heaters capable of creating a dummy thermal load up to at least double the design power density to test limits of models and devices and can be utilized to create uniform and non-uniform heating patterns such as heating in a checkerboard arrangement, heating of only the center, heating of only the corners, etc., with a reasonable heater grid spacing that simulates intended device design, operation and edge cases.
    d. Detailed specifications for chiplet design and interfaces are provided in the Chiplets Ecosystem and EDA sections.
    e. Performers of this work must coordinate with Chiplet Ecosystem performers and EDA performers to provide utility chiplets that use a common size, bond pitch, interface, etc.
    f. Utility chiplets must be compatible with, and bondable to, substrates to be produced under the NAPMP Materials and Substrates NOFO.
    g. For example, a thermal utility chiplet could incorporate a heater array and array of thermal sensors for model validation and be compatible with very fine pitch bonding strategies.
    h. Active features for data reporting in initial utility chiplets are optional but not required.

1.6.2.4.3.4 Objective 4: Integration of Power and Thermal Management

Technical Targets for the integration of power and thermal management follow.

1. Demonstrate integrated power delivery, power management and thermal management to maximize system performance and efficiency.

2. Demonstrate integrated power delivery and thermal management that would allow chiplets on both sides of a substrate.
3. Demonstrate compatibility of power delivery and thermal solutions with existing (or new) in-line testing and failure analysis techniques.
4. Develop reliable power and thermal connectors where necessary.

1.6.2.5 Project Structure

1.6.2.5.1 Required Team Capabilities

CHIPS R&D strongly encourages applications from multi-disciplinary, multi-organization project teams that collectively demonstrate the full range of expertise, experience, and capabilities needed to achieve the technical objectives of this R&D area. For the purposes of this NOFO, a project team comprises all funded entities (the applicant and any proposed subrecipients) as well as unfunded collaborators planned for inclusion in a single application. Project team participation from academic and other research entities is strongly encouraged.

Applicants are encouraged to form teams to have suitable capabilities to address development challenges, basic research problems, and progression from prototyping to pilot scale production as well as having suitable partners for education and workforce development and environmental sustainability. For example, the proposed team should have the ability to develop new devices, materials, and processes and to model, design, and develop new thermal and power solutions and evaluate those using utility chiplets in bonded arrangements to validate performance and refine design models. Applicants must explain within their proposals that they or one or more subrecipients have a demonstrated capability to generate one or more initial test devices within three months of award.

Applicants should propose milestones that represent measurable steps toward achieving Project-Level Non-Technical Targets as described in Sections 1.7.1 and 1.7.2. Applicants may also propose additional non-technical milestones.

1.6.2.5.2 Project Phases

1.6.2.5.2.1 Overview

Applicants must propose a detailed project plan for achieving Project-Level Technical Targets. Projects should be divided into four (4) phases over a five (5) year period of performance. Phases 1 and 2 should be 12 months each and Phases 3 and 4 should be 18 months each. Execution plans for each phase should describe key R&D activities and risk assessments, milestones within the phase and go/no-go checkpoints between the phases. Go/no-go checkpoints will be evaluated by CHIPS R&D and encompass a comprehensive review of progress toward achieving technical targets, risk assessment, and mitigation plans.

1. Phase 1 - Design, fabrication, and evaluation of utility chiplets needed for thermal solutions and/or power solution evaluation; procurement of equipment, recruiting staff, and setup of facilities and programs as needed.

2. Phase 2 - Design, fabrication and evaluation of concepts and test devices of initial solutions using utility chiplets where applicable; development and improvement of models for thermal solutions and/or power solutions for advanced packaging, including 3DHI, devices.
3. Phase 3 - Refinement of designs, materials, processes, and models and begin transition to NAPPF or other prototyping facilities; Utilization of refined models for ML/AI approaches to accelerate design cycles.
4. Phase 4 - Transfer of the leading solutions to the NAPPF for prototyping use within the pilot line with best solutions made accessible to the CHIPs ecosystem.

The following subsections provide additional information for applicants regarding each of the four phases, including expected project outputs.

1.6.2.5.2.2 Phase 1

CHIPS R&D expects activities in Phase 1 to include, as necessary, acquiring any required equipment and staff, demonstrating the capability for demonstration-level evaluation of thermal and power solutions, gathering appropriate data to refine CVDP plans, conducting initial education/workforce outreach efforts, and similar activities. Phase 1 also should include the design and fabrication of utility chiplets needed to advance and evaluate future progress. Performers should expect that at the end of Phase 1, the capabilities of utility chiplets will be evaluated across multiple R&D areas, and certain designs may be chosen for use across R&D areas to allow comparisons among performers. Likewise, at the end of phase one, support for further development of certain utility chiplets may be withdrawn.

Phase 1 technical milestones should define progress toward achieving production of demonstration devices. Phase 1 commercial viability and domestic production milestones should include, for example, progress in refining the CVDP plan, including gathering any relevant data.

Award recipients will be expected to deliver to CHIPS R&D, Associate Recipients, or independent evaluators as applicable:

1. Utility chiplets
2. Thermal and power demonstration devic1es and data for evaluation, including relevant documentation such as process assumptions, design manuals, PDK, reliability criteria, and physical, electrical, mechanical, and thermal specifications, each compatible with formats specified by CHIPS R&D during negotiation and with appropriate licensing provisions to protect IP rights
3. A refined CVDP plan
4. Evidence of successful EWD outreach efforts

Phase-specific targets marking go/revise/no-go decision points for transition from Phase 1 to Phase 2 will be finalized at the time of award.

1.6.2.5.2.3 Phase 2

CHIPS R&D expects activities in Phase 2 to include, for example, basic and applied research, innovations in process engineering, development and application of advanced metrology and testing capabilities, refining the CVDP plan based on technical progress, and implementing the EWD plan.

Phase 2 technical milestones should define progress toward achieving Project-Level Technical Targets. Phase 2 CVDP milestones should leverage research and engineering progress to inform refinement and implementation of the CVDP plan and demonstrate progress towards the relevant Project-Level Non-Technical Targets. Phase 2 EWD milestones should include implementing relevant programs, collecting data for assessing success metrics, and demonstrating progress towards the relevant Project-Level Non-Technical Targets.

Award recipients will be expected to deliver to CHIPS R&D, Associate Recipients, or independent evaluators, as applicable:

1. Thermal solution and power solution samples and data for evaluation, including relevant documentation such as process assumptions, design manuals, PDK, reliability criteria, and physical, electrical, mechanical, and thermal specifications, each compatible with formats specified by CHIPS R&D during negotiation and with appropriate licensing provisions to protect IP rights
2. A refined CVDP plan and a detailed description of progress against the plan
3. A refined EWD plan and a detailed description of progress against the plan

Phase-specific targets marking go/revise/no-go decision points for transition from Phase 2 to Phase 3 will be finalized at the time of award.

1.6.2.5.2.4 Phase 3

CHIPS R&D expects activities in Phase 3 to include, for example, continued work on thermal and power solution development, additional basic and applied R&D on thermal and power solution integration and integration process engineering, development of device-level metrology and testing capabilities, refining and progressing against the CVDP plan, and continued progress against the EWD plan.

Phase 3 technical milestones should focus on achieving the Project-Level Technical Targets. Phase 3 CVDP milestones should leverage research and engineering progress to inform refinement and implementation of the CVDP plan and demonstrate progress towards the relevant Project-Level Non-Technical Targets. Phase 3 EWD should include implementing relevant programs, collecting data and success metrics, and demonstrating progress towards relevant Project-Level Non-Technical Targets.

Award recipients will be expected to deliver each of the following to CHIPS R&D, Associate Recipients, or independent evaluators, as applicable.

1. Thermal and power solution samples and data for evaluation, including relevant documentation such as process assumptions, design manuals, PDK (compatible with

NAPMP-specified formats and with appropriate licensing provisions to protect IP rights), reliability criteria, and electrical, mechanical and thermal specifications
2. Demonstration devices in lots sufficient for independent evaluation (approximately 25).
3. A refined CVDP plan and evidence of progress against the plan
4. Data-driven evidence of progress against the EWD plan

Phase-specific targets marking go/revise/no-go decision points for transition from Phase 3 to Phase 4 will be finalized at the time of award.

1.6.2.5.2.5 Phase 4

CHIPS R&D expects Phase 4 activities to include:
1. Scaling up from prototype-level production to larger lots to evaluate reliability. These would require moving from the production of prototype lots to pilot-level production of at least 10 lots of 100 samples each;
2. Reimbursable provision of advanced thermal and power solutions emerging from work in previous phases for use in other research projects and areas designated by CHIPS R&D;
3. Refining and implementing the CVDP plan based on initial pilot-level production experience; and
4. A data-enabled analysis of EWD program progress.

Phase 4 technical milestones should focus on steps toward pilot-level production. Phase 4 CVDP milestones should reflect lessons learned in scaling to pilot-level production. Phase 4 EWD should focus on data gathering and analysis of funded EWD programs.

1.6.3 R&D Area 3: Connector Technology, Including Photonics and Radio Frequency (RF)

1.6.3.1 Anticipated Amounts

For the Connector Technology, Including Photonics and RF R&D area, CHIPS R&D anticipates making available up to approximately $250,000,000 for funding multiple awards in amounts ranging from approximately $10,000,000 to approximately $100,000,000 in Federal funds per award, with a five (5) year period of performance. While cost share is not required, CHIPS R&D will give preference to applications that demonstrate credible cost share commitments, consistent with Section 3.2.

1.6.3.2 Background

Recent years have seen an explosion of progress in high performance computing, including machine learning and AI. The size of these systems is rapidly scaling, with trillions of parameters needing to be optimized in training large language models, as an example. Further, to properly train and use these systems, an enormous amount of data needs to be transmitted between devices. Data transmission in these systems is a limitation in terms of quantity, speed, and power consumption. The goal for this R&D area is innovation for high data-rate, low latency, small footprint, error-free, and energy efficient connections between packaged sub-

assemblies. High-density system integration requires innovations in connector technology to achieve high-bandwidth density while at the same time delivering the energy efficiency necessary for high performance computing and low power applications. The focus is on reliable and manufacturable integrated connectors that include computational capability, data pre-processing, security, and ease of installation to the packaged assembly. Ultimate goals are to achieve over 100 Tb/s aggregate data transmission at a power consumption of less than 0.1pJ/bit overall length scales.

It is expected that the intended sub-assemblies will be integrated chip packages composed of three-dimensional stacks of separated chiplets and/or chiplet populated substrates, possibly including integrated optical sources, where the substrates have the characteristics set out in Section 1.5 of the NAPMP Materials and Substrates NOFO and the chiplets have the characteristics set out in Section 1.6.4 of this NOFO. It is expected that connector assembly targets can be met with the investments set out in Section 1.6.1 of this NOFO.

This investment in innovation in connector technology is intended to achieve the following outcomes.

- **3-5 years:** New materials, designs, documentation, processes, and tools are poised to prototype and demonstrate manufacturability. Innovative approaches emerge for both flexible wired and wireless connections relying on RF (including microwave and millimeter-wave bands) and/or optical approaches that greatly enhance system connector performance and efficiency. New measurement methods are developed and validated, including connector chiplets and or substrate/sub-assembly features, to improve materials, models, designs, processes and tools for connector solutions and data transfer management. Connector modeling capabilities are expanded to handle complex advanced packaging flows. Validated connector models and connector assembly reliability are aligned with new design tools developed under the NAPMP Co-Design/Electronic Design Automation R&D area (see Section 1.6.5) and other semiconductor R&D initiatives (see Section 1.8.2).
- **10 Years:** Devices assembled with advanced packaging connectors operate reliably at higher power performance and higher energy efficiency. Scale down and scale out connectors are no longer gating factors limiting advanced packaging for all data rate transfer distances. Chiplets and connector substrate features combined into advanced prototypes that are thermally- and power-aware with powerful dynamic management capabilities are readily available in the chiplets ecosystem. Extreme interconnect density needs of next-generation packaging will drive fine pitches (< 10 µm pitch) and fine line/space (< 1 µm L/S) circuitry. The assembly technologies and processes will involve development of silicon stacking solutions and tooling for die-to-wafer or die-to-die thermal compression or hybrid bonding.[16]

[16] https://srcmapt.org/wp-content/uploads/2024/03/SRC-MAPT-Roadmap-2023-v4.pdf, Ch. 7, p. 143, Table 7.1.

1.6.3.3 Connector Technology Including Photonics and RF Application Objectives

The Connector Technology R&D area seeks innovations to deliver high bandwidth, energy efficient data communications across three length domains. Applications in this R&D area must address at least one of the following three Objectives to advance program drivers for 3DHI and scale-down and scale-out. For the purposes of this R&D area we have delineated three objectives at three length scales:

Objective 1: Develop short-range, wired connections to enable high speed connectivity between neighboring packages. Proposed solutions should achieve data rates of about 10Gb/s per channel with a shoreline bandwidth of over 10 Tb/s/mm across a length scale that could reasonably be achieved between nearest neighbor wafer-scale systems, approximately 5 – 25mm.

Objective 2: Development for intermediate range wired or wireless connectors between local wafer-scale systems (but not necessarily nearest neighbor). Proposed solutions under this Objective should be able to demonstrate aggregate data rates > 100Tb/s bidirectional over length scales up to approximately the 1 m scale.

Objective 3: Develop long-range connectors capable of connecting wafer-scale systems at a range up to and exceeding the length of a server site, or approximately 1 km. Solutions proposed under this Objective should be able to demonstrate aggregate data rates > 100 Tb/s bidirectional at this range using optical fibers.

Power consumption in all of these is a critical driver of the technology. Each Objective is constrained to require less than 0.1 pJ/bit.

All approaches are expected to use a modular chiplet approach for the transceiver, and the link shall be optimized for bandwidth, shoreline bandwidth density, energy/bit transmitted, link distance, latency, and active chiplet area. A bit error rate of less than 10^{-12} /s is expected with error correction when accounted for (in terms of energy per bit, additional silicon area, etc.). The chiplets and technology needed to meet the requirements of this R&D area will need to be designed and tested as part of this response but must meet the mechanical requirements specified in the Chiplets Ecosystem section (1.6.4) of this NOFO. Prospective applicants may propose solutions to one or more of these Objectives. The boundaries between these areas are intended to be soft in the sense that there can be some overlap in the length scales.

Applications may address these objectives by means of wired and/or wireless connectors relying on RF or optical connector technologies, or a combination of those technologies, if properly justified. For all applications, the modes of data transfer must be relevant to the distance and desired bandwidth between the packaged assemblies. Modes in scope for this NOFO are via flexible wire-arrays, including serializer/deserializer (SerDes) circuitry with or without repeaters if needed; wired and/or wireless RF signal connection; or low-loss photonics via optical fibers or fiber arrays. RF and photonic transceivers are expected to be provided using chiplet-based technology or embedded directly into the advanced substrates. Potential applicants are encouraged to focus on new scale-down technologies (e.g. finer pitch connections), and should discuss how the proposed solution enables scale-out technologies (e.g. enabling larger numbers

of sub-assemblies in a system). In each case, connections must enable secure communications and provide for mechanical, electrical, and thermal reliability. Proposed approaches will make clear how the signaling Figure of Merit (s-FoM)[17] is maximized by the proposed approach and any trade-offs that are or could be taken to optimize for different applications.

Applicants should anticipate chiplet transceiver sub-systems that can be flip-chip bonded onto a logic or memory chip in packaging processes where the substrates have the scale-down characteristics set out in Section 1.5 of the NAPMP Materials and Substrates NOFO. In addition, connector reliability must be compatible with flip chip assembly and all processing and packaging steps, chemicals, and temperatures that may impact the connector solutions during subsequent manufacturing steps. In scope for this R&D area are chiplet sub-assembly to substrate connectors and connection techniques, such as automated, low loss, reliable fiber attachment approaches such as high fiber count fiber array units (FAUs) that may contain polarization maintaining fibers. Flip-chip optical connections, including evanescent coupling, between substrate waveguides and transceiver chiplets are also in scope, as are integrated optical sources on the transceiver chiplet. Not in scope are traditional ball grid array (BGA) or land grid array (LGA) connectors, conventional wire bonding, and free space optics.

1.6.3.4 R&D Outputs and Technical Targets

1.6.3.4.1 Outputs

Expected R&D outputs include novel connectors, tools, materials, processes, and devices that demonstrate improved performance; standards and metrologies derived from test devices; test and evaluation at prototype- and pilot-scale manufacturing; and proven connectors, materials, and devices with improved performance available for the CHIPS ecosystem.

During Phase 4, CHIPS R&D aims to provide connector solutions developed under this NOFO to research projects in other areas of packaging research that would benefit from access. Examples of these other research areas include new equipment, tools, processes, and process integration; materials and substrates; power delivery and thermal management; co-design/EDA; chiplets ecosystem; and prototype development. Examples of research projects include those associated with the NAPPF, the NSTC, the CHIPS Manufacturing USA Institute, or other Federally funded research programs.

CHIPS R&D will expect recipients to make available for use by other research projects CHIPS R&D-designated connector solutions along with relevant documentation and physical, performance, and mechanical specifications for use by other research projects. CHIPS R&D will work with award recipients to ensure appropriate protections for the recipient's IP rights (see Section 2.8). For Phase 4 budgeting purposes, applicants should plan for a minimum of 100 each of connector samples and a maximum of 1,000. NIST will allow award recipients to recover costs for producing these connector samples for CHIPS R&D-designated research projects, for example through direct, reimbursable provision of these solutions by the applicant; licensing to

[17] S. Jangam and S.S. Iyer, "A Signaling Figure of Merit (s-FoM) for Advanced Packaging," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 10, no. 10, pp. 1758-1761, Oct. 2020, doi: 10.1109/TCPMT.2020.3022760.

other NAPMP-approved U.S.-based entities with capacity for reimbursable production at pilot scale; or installing manufacturing capability in an NAPMP-funded facility, such as the planned NAPPF.

1.6.3.4.2 Technical Targets

The technical targets below establish a set of target categories and associated technical targets, selected by CHIPS R&D based on industry roadmaps (see Section 1.3.1) and refined for their potential to improve the performance, manufacturability, and cost effectiveness of connector technologies.

Technical targets for each connection modality are expected to be aggressive and the resulting connector is expected to be compatible with direct attach at fine pitch of advanced node CMOS, legacy nodes, and non-silicon chiplets. In cases where the applicant does not intend to meet or exceed a technical target and/or opts to include additional technical targets, the applicant should carefully explain how their proposed approach nonetheless represents a significant technical advance relative to the global state of the art and will accomplish the CHIPS R&D mission and goals (Section 1.1.1) and the specific objective of this NOFO (Section 1.1.3).

For each technical area, the applicant must call out their targets for the following parameters in their proposals:

1. Bandwidth/shoreline (Gb/s/mm): The effective data rate assuming all signal escapes are from the edge of the sub-assembly
2. Bandwidth/area (Gb/s/mm^2): The effective data rate accounting for all the area used by the connector
    a. Includes all the physical connections and the area used to deliver signals from the chiplet to the point of signal exit from the sub-assembly
    b. For a wired connector it represents the area of the connection of all the wires to the sub-assembly, for wireless connectors it is the area of the antenna array and for optical connectors it is the area occupied by the fiber array and associated waveguides on the assembly. If appropriate it should include ESD area
3. Total Chiplet area: The total area of the chiplet that is used to drive the signals. It includes any pre- and post-processing of the data (e.g., SerDes circuitry) power management, error detection and correction circuitry, as well as any other elements needed on the chiplet to ensure the full functionality and performance of the connector
    a. This chiplet should include all links to the connector (such as transfer of energy from the chiplet to the connector)
    b. In the case of optical connectors, there may be more than one chiplet including the laser, and the area for all the chiplets should be accounted for
    c. If the connector is active, the area of any embedded chiplets, including the transmitter and receiver areas, must be included here
4. Link length (mm): The length in mm between the transmitter and receiver
5. Clock rate, carrier frequency, or wavelength of operation
6. Energy per bit (pJ/b): The amortized energy per bit transmitted

a. Must include all the energy needed for the full functionality and performance of the connector, e.g., lasers, modulators, power delivery, error correction, clock forwarding, pre- and post-processing of data, etc.

7. Latency (ns): Total time for the electrical data being transmitted to be prepared, transmitted and received, in usable error-free electrical form, including time of flight (TOF) which can be stated separately)
8. Composite bit error rate: The effective error rate after error correction

Once these parameters are selected the applicant should compute the s-FoM given by

$$\mathrm{s-FoM} = \left(\frac{\text{bandwidth} \times \text{link length}}{\text{shoreline}}\right) / (\text{energy per bit} \times \text{transceiver area} \times \text{latency})$$

Applicants must describe targets for each parameter and how the proposed solution can deliver on the goals of over 100 Tb/s aggregate data transmission bidirectional, and at less than 0.1 pJ/bit. Applicants should discuss whether they expect to exceed the target, meet the target, partially meet the target, or not need to meet the target.

If applicants do not use the s-FoM supplied above, they may use an alternative figure of merit but must describe and justify their FoM for their selected Objective(s). Applicants may propose additional Project-Level Technical Targets in addition to the CHIPS R&D-specified Technical Targets above.

1.6.3.5 Project Structure

1.6.3.5.1 Required Team Capabilities

CHIPS R&D strongly encourages applications from multi-disciplinary, multi-organization project teams that collectively demonstrate the full range of expertise, experience, and capabilities needed to achieve the technical objectives of this R&D area. For the purposes of this NOFO, a project team comprises all funded entities (the applicant and any proposed subrecipients) as well as unfunded collaborators planned for inclusion in a single application. Project team participation from academic and other research entities is strongly encouraged.

The proposed team should have the ability to develop new devices, materials, and processes; to model, design and develop new connector solutions; and then to evaluate those using connector chiplets and substrates or sub-assemblies in bonded arrangements to validate connector performance, refine design models and validate connector assembly reliability. Applicants must explain within their proposals that they or one or more subrecipients have a demonstrated capability to generate one or more initial prototypes within three months of award.

Applicants should propose milestones that represent measurable steps toward achieving Project-Level Non-Technical Targets, as described in Sections 1.7.1 and 1.7.2. Applicants may also propose additional non-technical milestones.

1.6.3.5.2 Project Phases

1.6.3.5.2.1 Overview

Applicants must propose a detailed project plan for achieving Project-Level Technical Targets. Projects should be divided into four (4) phases over a five (5) year period of performance. Phases 1 and 2 should be 12 months each and Phases 3 and 4 should be 18 months each. Execution plans for each phase should describe key R&D activities and risk assessments, milestones within the phase and go/no-go checkpoints between the phases. Go/no-go checkpoints will be evaluated by CRDO and will encompass a comprehensive review of progress toward achieving technical targets, risk assessment and mitigation plans. The focus for each of the four phases can be summarized as follows.

Phase 1 (12 months): Design, fabrication, PDK documentation, and evaluation of preliminary connector solutions in at least one of the three application Objective areas; provision of prototype within three months of award; procurement of equipment, recruiting staff, and setup of facilities and programs as needed.

Phase 2 (12 months): Design, fabrication, PDK documentation, and evaluation of concepts and prototypes of initial solutions using connector-enabled chiplets and/or substrates where applicable; development and improvement of models for connector transceiver solutions and/or connector assembly solutions for Advanced Packaging, including 3DHI, devices. Provide initial assembly design kit documentation and model-to-hardware analysis.

Phase 3 (18 months): Refinement of designs, materials, tools, processes, PDK documentation, and models and begin transition of process to NAPPF or other prototyping facilities; Utilization of refined models for ML/AI or low power approaches to accelerate design cycles. Complete preliminary reliability validation.

Phase 4 (18 months): Transfer of the leading solutions to the NAPPF for prototyping use within the pilot line, with best connector technology solutions made accessible to the CHIPS ecosystem. Final assembly design kit and final reliability, stressing validation using appropriate standards.

The following subsections provide additional information for applicants regarding each of the four phases, including expected project outputs.

1.6.3.5.2.2 Phase 1 (12 months)

CHIPS R&D expects activities in Phase 1 to include, as necessary, acquiring any necessary equipment and staff, demonstrating the capability for evaluation of one or more of the connector Objective solutions and gathering appropriate data to refine CVDP plans, conducting initial education/workforce outreach efforts, and similar activities. Phase 1 should also include the design and fabrication of connector substrates and/or chiplets needed to advance and evaluate future progress. Performers should expect that at the end of Phase 1, the capabilities of connector solutions will be evaluated across multiple R&D areas and certain designs may be chosen for use

across the R&D areas to allow comparisons among performers; likewise, at that time, support for further development of certain connectors may be withdrawn.

Phase 1 technical milestones should define progress toward achieving production of demonstration devices. Phase 1 CVDP milestones should include, for example, progress in refining the CVDP plan, including gathering any relevant data.

Award recipients will be expected to deliver to CHIPS R&D, Associate Recipients, or independent evaluators, as applicable:

1. Connector chiplets
2. Connector substrates or sub-assemblies
3. Connector devices for evaluation, including relevant documentation such as process assumptions, design manuals, PDK, assembly design kits (ADK), reliability criteria, and physical, electrical, mechanical, and connector specifications, each compatible with formats specified by CHIPS R&D during negotiation and with appropriate licensing provisions to protect IP rights
4. A refined CVDP plan
5. Evidence of successful EWD outreach efforts

Phase-specific targets marking go/revise/no-go decision points for transition from Phase 1 to Phase 2 will be finalized at the time of award.

1.6.3.5.2.3 Phase 2 (12 months)

CHIPS R&D expects activities in Phase 2 to include, for example, basic and applied research, innovations in process engineering, development and application of advanced metrology and testing capabilities, refining the CVDP plan based on technical progress, and implementing the EWD plan.

Phase 2 technical milestones should define progress toward achieving Project-Level Technical Targets. Phase 2 CVDP milestones should leverage research and engineering progress and product cost projections to inform refinement and implementation of the CVDP plan and demonstrate progress towards the relevant Project-Level Non-Technical Targets. Phase 2 EWD milestones should include implementing relevant programs, collecting data for assessing success metrics, and demonstrating progress towards the relevant Project-Level Non-Technical Targets.

Award recipients will be expected to deliver to CHIPS R&D, Associate Recipients, or independent evaluators, as applicable:

1. Connector Solution samples for evaluation, including relevant documentation such as process assumptions, design manuals, PDKs, reliability criteria, and physical, electrical, mechanical, and thermal specifications, each compatible with formats specified by CHIPS R&D during negotiation and with appropriate licensing provisions to protect IP rights

2. A refined CVDP plan and a detailed description of progress against the plan
3. A refined EWD plan and a detailed description of progress against the plan

Phase-specific targets marking go/revise/no-go decision points for transition from Phase 2 to Phase 3 will be finalized at the time of award.

1.6.3.5.2.4 Phase 3 (18 months)

CHIPS R&D expects activities in Phase 3 to include, for example, continued work on connector solution development, additional basic and applied R&D on connector solution integration and integration process engineering, development of device-level metrology and testing capabilities, refining and progressing against the CVDP plan, and continued progress against the EWD plan.

Phase 3 technical milestones should focus on achieving the Project-Level Technical Targets. Phase 3 CVDP milestones should leverage research and engineering progress and product cost projections to inform refinement and implementation of the CVDP plan and demonstrate progress towards the relevant Project-Level Non-Technical Targets. Phase 3 EWD should include implementing relevant programs, collecting data and success metrics, and demonstrating progress towards relevant Project-Level Non-Technical Targets.

Award recipients will be expected to deliver each of the following to CHIPS R&D, Associate Recipients, or independent evaluators, as applicable:

1. Connector Solution samples for evaluation, including relevant documentation such as process assumptions, design manuals, process design kits (PDK, compatible with NAPMP-specified formats and with appropriate licensing provisions to protect IP rights), reliability criteria, and electrical, mechanical and connector specifications
2. Demonstration devices in lots sufficient for independent evaluation (approximately 25 per lot)
3. A refined CVDP plan and evidence of progress against the plan
4. Data-driven evidence of progress against the EWD plan

Phase-specific targets marking go/revise/no-go decision points for transition from Phase 3 to Phase 4 will be defined at the time of award.

1.6.3.5.2.5 Phase 4 (18 months)

CHIPS R&D expects Phase 4 activities to include:

1. Scaling up from prototype-level production to larger lots to evaluate reliability. These would require moving from the production of prototype lots to pilot-level production of at least 10 lots of 100 samples each
2. Reimbursable provision of advanced connector solutions emerging from work in previous phases for use in other research projects and areas designated by CHIPS R&D Refining and implementing the CVDP plan based on initial pilot-level production experience

3. A data-enabled analysis of EWD program progress

Phase 4 technical milestones should focus on steps toward pilot-level production. Phase 4 CVDP milestones should reflect lessons learned in scaling to pilot-level production. Phase 4 EWD should focus on data gathering and analysis of funded EWD programs.

1.6.4 R&D Area 4: Chiplets Ecosystem

1.6.4.1 Anticipated Amounts

For the Chiplets Ecosystem R&D area, CHIPS R&D anticipates making available up to approximately $300,000,000 for funding multiple awards in amounts ranging from approximately $10,000,000 to approximately $75,000,000 in Federal funds per award for the high-performance domain and approximately $25,000,000 in Federal funds per award for the low-power domain, with a five (5) year period of performance. While cost share is not required, CHIPS R&D will give preference to applications that demonstrate credible cost share commitments, consistent with Section 3.2.

1.6.4.2 Background

The Chiplets Ecosystem R&D area focuses on new chiplet ecosystems that leverage key attributes of advanced packaging such as wire abundance, ultra-large packages and heterogeneous integration for increasing performance, enabling modular composition, and for faster, cost-efficient, flexible design and development. For this NOFO, the term "chiplet ecosystem" refers to: (1) sets of chiplets that can be used to compose application-specific integrated packages; and (2) requirements that new chiplets can follow to be added to the ecosystem. The R&D outputs and technical targets aim to achieve the intent "to achieve a degree of integration that blurs the line between chip and package" as outlined in the Vision for the National Advanced Packaging Manufacturing Program.

The need for chiplet ecosystems has been widely cited. For example, the Report to the President: Revitalizing the U.S. Semiconductor Ecosystem by the President's Council of Advisors on Science and Technology in September 2022 recommends that "a platform system-on-a-chip must be made available, with a supporting software stack, that provides an interface to which small 'chiplets,' containing the innovative part of the system, can be attached using advanced packaging." The 2024 National Strategy on Microelectronics Research report by the Subcommittee on Microelectronics Leadership of the National Science and Technology Council's Committee on Homeland and National Security recommends "a library and supply of standard plug-and-play chiplets with standard interfaces, and opensource reference implementations of those interfaces."

Chiplet ecosystems today are largely based on the premise of wire scarcity, i.e., that wiring in a package is a limited resource. To use package wiring efficiently, data is typically moved between chiplets using die-to-die interfaces at a much higher rate than it is moved within a chiplet. Fast data movement requires complex circuitry to transmit/receive data, gear data up/down to the substrate, and manage data transmission. The overhead of this circuitry causes chiplets to be

larger and more complex to justify their development, almost as complex as large monolithic ASICs, potentially defeating their very purpose. System design with complex chiplets is similar in concept to printed circuit board design and very different from current ASIC design practices. These and other challenges have together inhibited the broad adoption of chiplet technologies.

Advanced packaging technology will allow for chiplets to be directly connected through hundreds or even thousands of package substrate wires. Data would then be transmitted between chiplets at rates comparable to on-chiplet rates. We believe this is an inflection point that should influence system design and propose the term "wire abundance" to label the contrast to today's wire-scarcity perspective. The ability to create package sizes 100x larger than commonly in use today extends wire abundance even further. Chiplet designs and system integration need to evolve non-linearly to fully leverage wire abundance. This R&D area aims to accelerate broad industry adoption of chiplets that leverage advanced packaging technology in high-volume manufacturing through innovations in chiplet design and organization into system architecture that directly leverage wire abundance, large package sizes, and heterogeneous integration, and deliver these innovations through Technology Demonstrators.

This investment in chiplets ecosystems is intended to achieve the following outcomes.

3-5 years: New silicon-proven, scaled-down, die-to-die (D2D) interfaces emerge that use wire abundance to improve power-efficiency by an order of magnitude, reduce latency and enable simpler chiplets. Progress includes implementations of powerful scale-out approaches such as a wafer-scale demonstrator that integrates several hundred chiplets, wafers of ecosystem-based chiplets for use at the NAPPF and other advanced packaging facilities, cost-effective low-power systems that leverage 3D-integration; tools to train a workforce in these new technologies that are available for wide adoption.

10 years: Industry converges around a consensus set of chiplets ecosystems that leverage scale-down, scale-out and heterogeneous integration to reduce the cost and time to develop new products while offering greater power-performance. An example might be future '10-10-10 chiplets ecosystems', made possible by the outcomes of the research in this NOFO, with 10 μm D2D (or less) substrate attach pitch enabling creation of a prototype by a 10-person team with $10 million in funding in 10-months timeline.

1.6.4.3 Chiplets Ecosystem Objectives

The Chiplets Ecosystem R&D area seeks innovation to leverage key attributes of advanced packaging such as wire abundance, ultra-large packages and heterogeneous integration to achieve the targeted 3-5 and 10-year outcomes.

The foundation is *scale-down* technology - wire abundance makes for simpler, cheaper D2D interfaces that in turn should make smaller, cheaper chiplets economically viable. Since these chiplets will be closer in complexity to ASIC IP[18] cores than to monolithic ASICs, system design will need novel algorithms like those used to synthesize ASICs from IP cores. These smaller

[18] https://en.wikipedia.org/wiki/Semiconductor_intellectual_property_core

chiplets will require novel *scale-out* technology to assemble systems from tens, hundreds or even thousands of chiplets in packages that are an order of magnitude (or more) larger than those in common use today. These chiplets will need to be available in novel domain-specific *chiplets ecosystems* that maximize reuse through rules that define physical and logical structure for chiplets to reduce product development time and manufacturing cost.

Applicants are expected to submit proposals that advance the state of the art in scale-down/scale-out/ecosystems. A proposal must be focused on one of two exemplar application domains, high-performance (i.e. high-performance computing, data-center AI or similar) or low-power (i.e. biomedical, AR/VR or similar). A single proposal may not address both domains.

This NOFO supports the NAPMP goal for establishing a vibrant, self-sustaining, profitable, domestic advanced packaging industry. Successful applicants will be expected to implement these innovations and aggregate the implementations in Technology Demonstrators that showcase the potential of advanced packaging and chiplets to cost-effectively deliver extreme power-performance. Successful applicants will also be expected to disseminate information about intermediate outputs and deliverables for broad industry use.

Proposals must take advantage of advanced packaging technologies. Out of scope for this R&D area are chiplet designs that are extensions of conventional approaches, based on commodity packaging that do not directly leverage advanced packaging in their architecture, chiplet designs with D2D interfaces tightly coupled to the choice of a SoC-bus (system-on-chip bus) or other high-level protocols, or standalone chiplet designs for any function not coupled to a chiplet ecosystem. Also out of scope are proposals that focus on unmodified reuse of existing chiplets, target the development of new chiplets to integrate with existing chiplets, or use wire-bonding for D2D interconnect.

The following sections provide background to assist applicants in addressing proposal objectives.

1.6.4.3.1 Scale-Down Chiplets

A D2D interface links two or more chiplets electrically through package wiring and enables them to exchange data. Packaging wire density has increased rapidly as package features scaled down, approaching that of on-chip wiring. For example, a 10 µm bond pitch between chiplets in current advanced systems is within an order of magnitude of the pitch of on-chip wiring in mid-2010 semiconductor process nodes. 3D interconnect densities already approach 1 µm pitch wire density. This trend will continue per the SRC MAPT Roadmap which concludes that "[t]he extreme interconnect density needs of next-generation packaging will drive ultra-fine pitches (< 10 µm assembly pitch) and very-fine-line/space (sub 1 µm L/S) circuitry*."* (MAPT p. 155.)

Applicants should exploit the coming trend of wire abundance to advance the state of the art and create a simple, highly parallel, power-efficient D2D interface for data transactions. For purposes of this NOFO, a data transaction is the transport of information between functional logic elements on chiplets connected by a D2D interface. The components of a data transaction include a link layer, logic to adjust for clock frequencies, coding for error correction, and circuitry for electrical transmission and reception over the substrate. We define the term "wire-

like" for the new interface, since data transaction latency and energy are expected to be close to that of physical wires directly connecting IP blocks within an integrated circuit. The interface proposed should show an ability to further exploit continual improvements in bond pitches to 1 μm or lower and be optimized for use at scale in high-performance systems or for 3D interconnect in low-power systems. Relative to designs with interfaces defined for wire scarcity, the lower overhead of scaled-down interfaces will make much smaller system functions viable as individual chiplets. An intended outcome is that the integration of chiplets in a package becomes like that of integrating IP cores in an ASIC, blurring the distinction between chiplet-based and chip IP core-based product design.

1.6.4.3.2 Scaling-Out for Performance Scaling

Many problems of interest such as large-language model (LLM) training[19] still have execution times that run into several months. Constantly growing problem sizes mean that data center energy consumption is now a pressing concern.[20] Advanced packaging can create packages that are greater than an order of magnitude larger than those in high-volume production today. Components today on different boards can be integrated with scaled-down interfaces in one energy-efficient large package. Commercial products and research have recently demonstrated how monolithic wafer-scale processing can improve performance by more than two orders of magnitude across problems in molecular dynamics, LLMs, etc. [21] However, memory size, memory bandwidth and compute requirements vary widely across high-performance applications. Scale-out systems offer the potential for wafer-scale designs that can cost-efficiently adapt to workloads by changing their chiplet composition. (Combining chiplets into a new design will be far less expensive than taping out a new monolithic wafer scale system.) For example, chiplets in a base design can be changed to increase memory bandwidth, change memory size to improve energy-efficiency with domain-specific compute chiplets, or change the types of CPU chiplets.

Proposed work under this objective should advance the state of the art to enable chiplet-based wafer-scale systems that aggregate internal and input/output (I/O) compute bandwidth at a scale two orders of magnitude greater than current practice. Applicants are expected to develop designs for packages as large as 50,000 mm^2 with a thousand or more chiplets; deliver adequate power (tens of kilowatts) to the package and individual chiplets; develop algorithms, protocols, and hardware to integrate and operate thousands of functional chiplets as one logical system; and develop algorithms and methods for clocking, reliability, telemetry, test, closed loop control, power management and other issues expected in operating a large system. In particular, we seek innovations in functional logic, 3D-memory, compute-in-memory, and memory management that directly leverage wire abundance in system architecture and design.

1.6.4.3.3 Chiplets Ecosystems

Developing architectures that simplify chiplet interchangeability requires an ecosystem approach. For this NOFO, a socket-based modular functional reference architecture ecosystem is

[19] https://www.nvidia.com/en-us/glossary/large-language-models/
[20] https://www.epri.com/research/products/3002028905
[21] https://arxiv.org/pdf/2405.07898

expected to capture all the physical and logical components and their interactions and dependencies, simplify heterogeneous integration to enable their composition in forming diverse, complex systems, and support their high-volume manufacture. Applicants must develop novel concepts for such an ecosystem to guide the design of a Technology Demonstrator and other functional systems, optimized for the selected exemplar application domain. Proposed work should leverage scale-down and scale-out innovation for a continuing increase in design capability and power-performance while decreasing design time and costs. Relevant components of a reference architecture include chiplets for logic, memory, input/output, scale-out/integration, and other functional blocks as necessary to create systems that meet application requirements. System performance must be scaled only through increasing the number of chiplets, not through bigger chiplets.

Specifications for "chiplet sockets", similar to the sockets for a CPU[22], can enable physical modularity for designs. Sockets must enable tailored integration of relevant technology innovations, such as the thermal or substrate advances supported in other NAPMP-funded work. While each applicant should propose their own ecosystem approach, CHIPS R&D will work with successful applicants in coordinating efforts, sharing information, and promoting opportunities for alignment and convergence around best practices, standardization, and shared solutions for consensus ecosystem approaches.

1.6.4.3.4 Technology Demonstrators for Exemplar Applications

The Technology Demonstrator (TD) objective aims to stimulate the development of advanced packaging technology and demonstrate its value in significant applications. It provides a context for scale-down, scale-out, and ecosystem innovation and demonstrates the suitability and utility of R&D project outputs for use by U.S. industry. Applicants should design and implement a TD for the selected exemplar application domain that integrates implementations of their innovations in scale-down, scale-out, and ecosystem technologies. The TD is expected to highlight the direct benefits of advanced packaging by demonstrating the improved performance possible on two applications of the applicant's choice.

1.6.4.4 R&D Outputs and Technical Targets

Applicants must focus a submission on one of two exemplar application domains, high-performance or low power. Sections 1.6.4.4.1 and 1.6.4.4.2 below provide background information, innovation tasks, and technical and design targets for each domain. For each technical target in the selected domain, applicants must indicate, in one consolidated table in the concept-paper submission, whether the project will meet, exceed, or not meet it. Proposals must address the following four required R&D output areas.

1. Scale-down - Advances the state of the art to enable a simpler, cheaper highly-parallel D2D interface and smaller chiplets made possible by wire abundance
2. Scale-out (high-performance only) - Advances the state of the art to leverage scale-down and ultra-large packages to create systems of hundreds to thousands of chiplets

[22] https://en.wikipedia.org/wiki/CPU_socket

Ecosystem - Advances the state of the art in modular design to cost-efficiently build and operate adaptable systems that leverage scale-down and scale-out
Technology demonstrators - Integrate outputs from scale-down, scale-out, and ecosystem into a system demonstrating suitability and utility of outputs for use by U.S. industry and research. Applicants are encouraged to use the Technology Demonstrators as context to guide their innovations in scale-down, scale-out and ecosystems.

1.6.4.4.1 High-Performance Domain Outputs and Targets

1.6.4.4.1.1 High-Performance Domain Scale-Down Technical Targets

The tasks for the scale-down objective are focused on developing an innovative wire-like D2D interface that can scale to leverage growing wire abundance across coming generations of packaging technology. The new interface must support and leverage up to thousands of wires between chiplets, enable very low-latency data transactions, make smaller chiplets viable, and support reliable manufacture and operation in systems with thousands of chiplets. The interface may also offer additional flexibility in other attributes (for example data path width and/or clocking) to meet energy goals. Applicants are expected to demonstrate interface performance in one or more meaningful test chips. The technical targets for these tasks are as follows.

Table 9: Technical targets for high-performance domain

Key	Parameter	Target
HPSD1	**Bond pitch**	Scales 10 μm -1 μm
HPSD2	**Substrates to be supported**	organic, glass, semiconductor
HPSD3	**Support for multiple process nodes**	Yes
HPSD4	**Energy per bit (per data transaction)**	< 0.1 pJ/bit
HPSD5	**Edge density with 4 routing layers**	>= 1.6 Tbps
HPSD6	**Low power state support**	Yes
HPSD7	**Target bit error rate**	1E-24
HPSD8	**Latency (per data transaction)**	Unidirectional < 4 ns at 1 GHz chiplet clock frequencies and data transmission rates
HPSD9	**Initialization/reset latency**	100 ms/10 ms
HPSD10	**Lane repair**	Yes for single-lane failure, clustered failures
HPSD11	**ESD protection Charged Device Model**	50 V
HPSD12	**ESD protection Human Body Model**	250 V

1.6.4.4.1.2 High-Performance Domain Scale-Out Technical Targets

The task for this objective is an analytical study to develop innovative technology that exploits wire abundance for the design, implementation, and reliable operation of high-performance

systems built from hundreds to thousands of chiplets in ultra-large packages. The Technology Demonstrator section lists tasks and targets for a physical implementation of these innovations.

This objective will require innovation in the physical design of a unit-packaged device of about 50,000 mm^2 in size that offers at least 1 peta operations per second of throughput realized through designs with 1000 or more chiplets. The design will need to deliver adequate power to and remove heat from the system and individual chiplets. In meeting the performance goals, applicants must scale other attributes such as memory bandwidth, memory size, package I/O bandwidth, and package power to meet performance requirements. Parameter values must be validated by the applicant based on a publicly documented ASIC specifications in 7nm or newer technology used for high-performance computing or data center AI.

The objective will require innovation in algorithms, logic, and protocols for scale-out networking in multiple areas. Achieving this objective will result in a network realized with scale-down and other interfaces that offers at least a petabyte per second of aggregate internal bandwidth for high-performance applications, support for connections to other wafer-scale systems, equal access at low latency to all the chiplets in the system, and high bandwidth between arbitrary chiplets. The network will need to support small control messages delivered at low latency to initialize, reset, monitor, operate, and manage the system. Networking logic may be realized through distinct scale-out chiplets or embedded in functional chiplets. The network will need methods for operation at scale that allow up to a thousand chiplets to operate together efficiently as a single entity and enable multiple wafer-scale packages to operate together. Conversely, the network must also support partitioning chiplets into physically dispersed logical subsets, each connected by their own low-latency logical subnetwork. The network will need innovation for reliable production and operation including but not limited to clocking, self-test, fault-tolerance (i.e. at least no single point of failure), sensing, telemetry, and closed-loop control. The network will need innovation in power management to match energy use to workload, support design innovation for redundancy and the use of workload-specific accelerators.

Wafer-scale systems can be enhanced with applications to create architectures and designs for functional chiplets that directly exploit advanced packaging. Examples of function innovation that leverage advanced packaging include, but are not limited to: 3D-stacked memory with a scalable wide interface (thousands of wires) that offers more bandwidth and capacity than projected in the future HBM4 standards; designs that enable multiple types of on-package memory, e.g. SRAM or multiple types of DRAM within a common system architecture; and memory management algorithms that leverage wire abundance to improve performance in packages 50,000 mm^2 and larger.

The targets for these tasks are as follows.

Table 10: Scale-out design and technical targets for high-performance domain		
Key	Parameter	Target
HPSO1	**Scale-out package performance and chiplet count**	> 1 Peta OP FP32, > 100 Peta OPs GEMM INT8 modeled design. Support up to 1024 chiplets, each no larger than 1010 mm x 1010 mm

HPSO2	**Scale-out network requirements**	On-package bandwidth > 1 Petabyte per second for up to a 1024-chiplet system, > 2 Tbps per logic-die edge with scale-down interface. Max latency grows at rate proportion to the logarithm of the number of chiplets or less. Support bandwidth > 1 Tbps between arbitrary chiplets. Deadlock-free routing.
HPSO3	**Grouped operation**	Support for physically dispersed subnetworks connected in a logical near-neighbor topology. Groups of up to 128. Up to 16 subnetworks.
HPSO4	**Control and Management**	Low latency reset and initialization. Reset/initialization time < 1 sec/10 msec for up to 1024 chiplets. Match active power to load. No-load power < 10% of max power.
HPSO5	**Reliable Manufacturing and Operation**	Functionality and performance can be validated after manufacture and preserved for three years with no component replacement within the package assuming a 5% failure rate.
HPSO6	**Memory type support innovation**	All memory is on-package memory. Chiplet to adapt to application - SRAM/DRAM/HBM
HPSO7	**Memory innovation bandwidth target**	Greater than (expected parameters for) HBM4
HPSO8	**Other Function Innovation**	Function innovation that directly leverages advanced packaging (e.g. wire abundance, package size)

1.6.4.4.1.3 High-Performance Domain Ecosystem Technical Targets

The task for this objective is an analytical study to develop a socket-based modular chiplet-based reference architecture composed of a discrete set of sockets and modules. The Technology Demonstrator section lists tasks and targets for a physical implementation of these innovations.

The architecture must be composed of modular functions, each implemented as a chiplet. A modular function is a sub-function designed to be added, removed, or altered as a unit from the reference architecture. Examples of modular functions include common logic functions such as CPU, domain-specific accelerators, Field-Programmable Gate Arrays (FPGAs), memory and memory management functions such as SRAM, DRAM, HBM control, cache control, system input/output, communications functions such as Ethernet/PCIe/Optical/RF, new functions necessary for scale-out and integration, or smaller modular functions made possible by scale-down. The datapath I/O for each modular function must be based on a scale-down D2D interface. The size of the D2D interface must match the performance requirements on the architecture. The architecture must also specify the control and management interface for each modular function.

The architecture must define physical sockets. A socket is a specification that lists a set of constraints on the implementation of a logical component chiplet in the reference architecture. A socket specification is expected to capture all the physical parameters necessary to guide the design of a new chiplet so it can be readily integrated with other conforming chiplets in the

ecosystem. Socket specifications for functions must be modeled to show they balance the application performance required by those functions, the need to support scale out, and the cost of design and manufacture. A package design for an implementation of the architecture must consist of a whole number of sockets. A reference architecture definition may require multiple types of sockets. Multiple logical components may map to the same socket definition.

The reference architecture must scale logically and physically in function and performance. System components must be changeable to adapt to power-performance and functionality needs for target applications including compute-intensity, latency, memory size and bandwidth, energy constraints, etc. For example, an appropriate approach could be replacing some of or all the general-purpose CPUs with domain-specific accelerators. Performance must be scaled by matching the number of instances of chiplets and physical sockets to meet application requirements, not with bigger chiplets.

The targets for this area are as follows:

Table 11: Ecosystem technical targets for high-performance domain		
Key	Parameter	Target
HPECO1	**Performance goals**	Scalable from a 32 chiplet system to scale-out goals in Table 10. Applicants propose reduced function and performance goals for 32 chiplet system.
HPECO2	**Functional scaling**	System components changeable to adapt to power-performance and functionality requirements for target applications. Incorporates any innovations in scale-down, scale-out and functional logic that leverage advanced packaging.
HPECO3	**Performance Scaling**	System throughput > 0.8*n*single_chiplet_performance for weak scaling - problem size per chiplet is a constant as the number of chiplets n in the system increases. e.g. assume 10 TOPS for a 10 mm x10 mm chiplet With 100 chiplets, achieve more than 800 TOPS of realized performance.
HPECO4	**Socket definition process**	Methods and/or algorithms to validate socket definitions for reference architecture.
HPECO5	**Implementation Constraints**	Socket-based architecture with limited number of chiplet types. Target < 10 sockets, < 20 chiplet types. With the following socket sizes recommended - 2x2, 5x5 and 10x10 for squares (mm), and 4x6 and 8x10 (mm) for rectangles. Other sizes with justification e.g. performance needed to match a memory interface

1.6.4.4.1.4 High-Performance Technology Demonstrator Technical Targets

The task for this objective is to exhibit the suitability and utility of R&D project outputs for use by U.S. industry in keeping with the NAPMP goal for establishing a vibrant, self-sustaining, profitable, domestic advanced packaging industry. Specifically:

1. Create TDs in a modular form factor popular in user data centers.
    a. Each TD must contain one or more TD unit packaged devices.
    b. The application demonstration must network 8 TD unit-packaged devices.
2. A TD unit-packaged device must implement a chiplet-based system that aggregates all the innovations in scale-down, scale-out, and ecosystem developed by the applicant.
    a. Enough modular functions sufficient to support at least two versions, a baseline and a derivative, must be implemented as chiplets. All chiplets cost-efficiently sized to meet target applications requirements.
    b. Applicants are encouraged to leverage off-the shelf IP for non-innovative functional components e.g. CPU, FPGA, Network IO, memory that do not uniquely leverage wire abundance other than at the D2D interface.
    c. Chiplets must include the scale-down datapath D2D interface and control I/O and protocols (for power on reset, initialization, self-test and other management functions) and other attributes as needed from the reference ecosystem.
3. Applications must demonstrate the adaptability of socket-based chiplet architectures by implementing at least two TD unit-package variants, a baseline system and derivative that replaces one or more chiplets in the baseline. This may include integrating independently designed chiplets to prove ecosystem definition quality. Proposals must demonstrate the performance improvement of the TD over conventional systems on two high-performance applications selected by the applicant. Any two from transformers (multiple activation functions), inferencing, low-resolution machine learning, weather simulation, neuromorphic simulation, molecular dynamics or other suitable application. Applicants are encouraged to choose applications, development stacks and environments likely to attract 3rd party developers and investment for future platform growth.

In developing high-performance TD designs, applicants are encouraged to consider the suggested design parameters in Table 12 below.

Table 12: Technology Demonstrator targets for high-performance domain

Key	Parameter	Value
HPTD1	**D2D interface**	Implement interface based on scale-down innovations at 10 μm pitch on the process nodes required for the Technology Demonstrator.
HPTD2	**Baseline system and performance target**	Implement modular demonstrator. Minimum 32 chiplets per unit package, target 3200 mm^2 logic area. Aggregate eight unit packages in demo.
HPTD3	**Chiplet Implementation**	Implements scale-down, scale-out, ecosystem innovations in chiplets needed for the demonstrator. Chiplets must meet NAPPF use requirements.
HPTD4	**Ecosystem demonstration**	System includes multiple instances of at least one chiplet designed by an entity by following functional interface and physical socket specifications.

HPTD5	**Demonstration applications**	Show two applications
HPTD6	**Software**	Support for an open-source stack relevant to the application (e.g. PyTorch for Machine Learning is encouraged.
HPTD7	**Baseline variants**	Change chiplets to change platform performance or function. Improve energy efficiency by 3x while preserving throughput or 50x memory capacity.
HPTD8	**System management**	Demonstrator system to be operated and managed from a system running a commonly accepted Linux distribution.

1.6.4.4.2 Low-Power Domain Outputs and Targets

1.6.4.4.2.1 Low-Power Domain Scale-Down Technical Targets

The tasks for the scale-down objective are to develop an innovative wire-like D2D interface that can scale to leverage growing wire abundance across coming generations of packaging technology. The new interface must support and leverage up to thousands of wires between chiplets, vertical logic die stacks, enable very low-latency data transactions, make smaller chiplets viable, and support reliable manufacture and operation. The interface may also offer additional flexibility in other attributes (for example data path width and/or clocking) to meet energy goals. Applicants are expected to demonstrate interface performance in one or more meaningful test chips. The technical targets for these tasks are as follows.

Table 13: Low power scale down technical targets		
Key	Parameter	Target
LPSD1	**Bond pitch**	Scales 10 μm -1 μm
LPSD2	**Substrates to be supported**	organic, glass, semiconductor
LPSD3	**Support for multiple process nodes**	Yes
LPSD4	**Energy per bit (per data transaction)**	< 0.01 pJ/bit
LPSD5	**Initialization/reset latency**	100ms/10ms
LPSD6	**Low power state support**	Yes
LPSD7	**Target bit error rate**	1E-22
LPSD8	**Latency (per data transaction)**	Unidirectional < 4 ns at 1 GHz chiplet clock frequencies and data transmission rates
LPSD9	**Lane repair**	Yes for single-lane failure, clustered failures
LPSD10	**ESD protection Charged Device Model**	50 V
LPSD11	**ESD protection Human Body Model**	250 V
LPSD12	**Number of dies stacked**	>= 3 (>= 2 logic)

1.6.4.4.2.2 Low-Power Domain Ecosystem Technical Targets

The task for this objective is an analytical study to develop a socket-based modular chiplet-based reference architecture composed of a discrete set of sockets and modules. The Technology Demonstrator section lists tasks and targets for a physical implementation of these innovations. The architecture must be composed of modular functions, each implemented as a chiplet. A modular function is a sub-function designed to be added, removed or altered as a unit from the reference architecture. Examples of modular functions include common logic functions such as CPU, domain-specific accelerators, FPGAs, memory functions such as SRAM, DRAM, system input/output including wireless, and memory management or smaller modular functions made possible by scale-down. The datapath I/O for each modular function must be based on a scale-down (3D where appropriate) D2D interface. The size of the D2D interface must match the performance and energy requirements on the architecture. The architecture must also specify the control and management interface for each modular function.

The architecture must define physical sockets. A socket is a specification that lists a set of constraints on the implementation of a logical component chiplet in the reference architecture. A socket specification is expected to capture all the physical parameters necessary to guide the design of a new chiplet so it can be readily integrated with other conforming chiplets in the ecosystem. Socket specifications for functions must be modeled to show they balance the application performance required by those functions and the cost of design and manufacture. A package design for an implementation of the architecture must consist of a whole number of sockets. Sockets may be stacked vertically. A reference architecture definition may require multiple types of sockets. Multiple logical components may map to the same socket definition.

The reference architecture must scale in function and performance both logically and physically. System components must be changeable to adapt to power-performance and functionality requirements for target applications including compute-intensity, latency, memory size and bandwidth, energy constraints, etc. For example, an appropriate approach could be replacing sensors or domain-specific accelerators to adapt to a new application. Performance must be scaled by matching the number of chiplet components and physical sockets to meet application requirements. An intended outcome is that the integration of chiplets in the ecosystem becomes like that of integrating IP cores in an ASIC, blurring the distinction between chiplet-based and chip IP core-based product design.

Innovations that directly exploit advanced packaging for energy efficiency, such as processing in memory, domain-specific accelerators coupled to sensors, and others are encouraged and methods for package-integrated logic for run-time telemetry and closed-loop control are of interest.

The targets for the low-power ecosystem objective are in Table 14 below.

Table 14: Low power ecosystem technical targets

Key	Parameter	Value
LPECO1	**Functional scaling**	System components changeable to adapt to power-performance and functionality requirements for target applications.
LPECO2	**Socket definition process**	Methods and/or algorithms to validate socket definitions for reference architecture.
LPECO3	**Logic Components**	Incorporates scale-down interface and innovations in functional logic that leverage advanced packaging.
LPECO4	**Architecture implementation**	Socket-based architecture with limited number of chiplet types. Target < 10 sockets, < 20 chiplet types
LPECO5	**Recommended socket sizes**	2x2, 5x5 and 10x10 (mm) for squares, and 4x6 and 8x10 (mm) for rectangles. Larger sockets with justification e.g. performance needed to match a memory interface

1.6.4.4.2.3 Low-Power Domain Technology Demonstrator Technical Targets

The task for this topic is to exhibit the suitability and utility of R&D project outputs for use by U.S. industry in keeping with NAPMP's goal for establishing a vibrant, self-sustaining, profitable, domestic advanced packaging industry.

1. Specifically, create a TD in a modular form factor with the ability to network multiple demonstrators.
2. A TD unit packaged device must implement a chiplet-based system that aggregates all the innovations in scale-down, scale-out, and ecosystem developed by the applicant.
    a. Enough modular functions for the TD must be implemented as chiplets. Implementations cost-efficiently sized to meet the target application requirements.

b. Applicants are encouraged to leverage off-the shelf IP for non-innovative functional components e.g. CPU, Network IO, memory.
c. Chiplets must include control I/O and support protocols (for power on reset, initialization, self-test and other management functions) and other attributes as necessary from the reference ecosystem.

3. Proposals may demonstrate the adaptability of socket-based chiplet architectures by implementing two TD unit-package variants, a baseline system and a variant that replaces one or more chiplets in the baseline.
4. Proposals must demonstrate the performance improvement of a TD over conventional systems on two applications selected by the applicant. Examples of relevant applications include biomedical, AR, AR/VR, wearables, internet-of-things devices or other suitable applications. Development stacks and environments likely to attract 3rd party developers and investment for future platform growth are encouraged.

In developing low-power TD designs, applicants are encouraged to consider the suggested design parameters in Table 15 below.

Table 15: Low power Technology Demonstrator (TD) technical targets

Key	Parameter	Value
LPTD1	**D2D interface**	Implement interface based on scale-down innovations at 10 μm pitch on the process nodes required for the TD.
LPTD2	**Baseline system**	Implement modular demonstrator.
LPTTD4	**Chiplet Implementation**	Implements scale-down, ecosystem innovations in chiplets needed for the demonstrator. Chiplets must meet NAPPF use requirements.
LPTD4	**Demonstration applications**	Developer's choice
LPTD5	**Package size**	10 mm x 10 mm Must use substrate-integrated passives (e.g. capacitors, resistors, inductors,, etc.)
LPTD6	**Power**	Active < 5 W, Standby < 50 mW
LPTD7	**Total platform I/O bandwidth**	< 1 Gbps
LPTD8	**Power-performance target**	10x energy efficiency with advanced packaging
LPTD9	**Scaling**	Three (3) dies stacked, at least two (2) logic. Network multiple instances
LPTD10	**Software**	Support for an open-source stack relevant to the application. Demonstrator supports an open-source operating system
LPTD11	**Baseline variants (optional)**	Change chiplets to change platform function e.g. change accelerators, actuators or sensors.

1.6.4.5 Project Structure

1.6.4.5.1 Required Team Capabilities

CHIPS R&D strongly encourages applications from multi-disciplinary, multi-organization project teams that collectively demonstrate the full range of expertise, experience, and capabilities needed to achieve the technical objectives of this R&D area. For the purposes of this NOFO, a project team comprises all funded entities (the applicant and any proposed subrecipients) as well as unfunded collaborators planned for inclusion in a single application. Project team participation from academic and other research entities is strongly encouraged.

The applicant and one or more subrecipients in either the low-power or high-performance domain must explain within their proposals that they have demonstrated experience with full end-to-end lifecycle design flow from architecture and design exploration through implementation, including verification, to sign-off and release to manufacturing and assembly. Applicants in the HPC domain must explain within their proposals that they have demonstrated experience in commercial semiconductor products or as an integrator in delivering products that integrate ASICs, COTS products, firmware, and custom software.

Proposals are expected to describe milestones for technical targets within a full end-to-end lifecycle design flow from architecture and design exploration, through implementation including the verification necessary for a demonstrator, to application demonstration. Award recipients will be expected to deliver outputs CHIPS R&D, Associate Recipients, or independent evaluators, as applicable. Phase-specific targets marking go/revise/no-go decision points for transition from one phase to the next will be finalized at the time of award including, but not limited to, technical targets that have been achieved or can be achieved with further development and optimization.

Applicants should propose milestones that represent measurable steps toward achieving Project-Level Non-Technical Targets, as described in Sections 1.7.1and 1.7.2. Applicants may also propose additional non-technical milestones.

1.6.4.5.2 Project Phases

1.6.4.5.2.1 Overview

Applicants must propose a detailed project plan for achieving Project-Level Technical Targets. Projects should be divided into four (4) phases over a five (5) year period of performance. Phase 1 should be 12 months, Phase 2 should be 21 months, Phase 3 should be 12 months and Phase 4 should be 15 months. Execution plans for each phase should describe key R&D activities and risk assessments, milestones within the phase, and go/no-go checkpoints between the phases. Go/no-go checkpoints will be evaluated in collaboration with the CHIPS team and will encompass a comprehensive review of progress toward achieving technical targets, risk assessment and mitigation plans. The focus for each of the four phases across both performance domains can be summarized as follows.

Phase 1 (12 months): Scale-down design, scale-out and ecosystem development
Phase 2 (21 months): Scale-out (high-performance only), ecosystem and Technology Demonstrator design, scale-down and chiplet implementation,
Phase 3 (12 months): Package design and assembly, system integration
Phase 4 (15 months): Technology Demonstrator

1.6.4.5.2.2 Phase 1 – High-Performance Domain

Suggested targets include:

1. Scale-down
    a. Specification for D2D interface that meets targets.
2. Scale-out
    a. Scale-out mechanisms (e.g. network architecture, protocols, logic, firmware) from chiplets to system specified in detail, meets function, reliability, and performance targets.
    b. Design proposals for functional chiplets that uniquely leverage advanced packaging (if applicable).
    c. Performance analysis on target applications.
    d. Operational control protocols defined. Firmware design document for scale-out operation.
3. Ecosystem
    a. Reference architecture definition that meets functional and scale-out performance targets. Specification (preferably open) listing modular functions, functional and performance scaling, chiplet control and management.
    b. Physical sockets definitions clearly correlated to reference architecture and performance targets and are consistent with NAPPF requirements Specification (preferably open) for dimensions, power, power-delivery grid, thermal intensity, scale-down D2D Data connector size and locations, control connectors and locations etc.
    c. Detailed Technology Demonstrator chiplets specifications (with power, performance targets) sufficient for reliable implementation schedule.
4. Technology Demonstrator
    a. Identification and analysis of baseline and variant designs and performance.
    b. Execution plan for chiplets in the TD.
    c. Application software requirements and execution plan.
5. Other
    a. Dissemination of Phase 1 outcomes.
    b. All dependencies and risks clearly identified.
    c. A refined CVDP plan.
    d. Evidence of successful EWD outreach efforts.

1.6.4.5.2.3 Phase 2 – High-Performance Domain

Suggested targets include:

1. Scale-down
    a. D2D interface performance verified and characterized on one or more meaningful test chips and substrate.
2. Scale-out
    a. Development of primitives for compute and communication.
3. Ecosystem
    a. Socket specifications published for 3rd party use.
    b. Socket-based wafer-scale package design for baseline with SI/PI analysis.
4. Technology Demonstrator (TD)
    a. TD baseline package design with SI/PI analysis.
    b. All chiplets for TD baseline taped out and brought up (derisked with intermediate proof-points as appropriate such as analysis, simulation, emulation etc.).
    c. Completion of exemplar application system design including identification of all components (beyond the package). System performance simulation. Completion of application software design. Completion of a development environment.
5. Other
    a. Dissemination of phase 2 outcomes
    b. A refined CVDP plan and a detailed description of progress against the plan.
    c. A refined EWD plan and a detailed description of progress against the plan.

1.6.4.5.2.4 Phase 3 – High-Performance Domain

Suggested targets include:

1. Scale-down
    a. The specifications and outputs developed under Phases 1 and 2 should be updated to reflect learnings identified during implementation.
2. Scale-out
    a. The specifications and outputs developed under Phases 1 and 2 should be updated to reflect learnings identified during implementation.
3. Ecosystem
    a. TD package design for variant with SI/PI analysis.
    b. Firmware implementation.
4. Technology demonstrator (TD)
    a. TD baseline packaging and assembly, integration and bring up.
    b. Application development.
    c. TD variant chiplet development.
    d. TD Chiplets available at cost for delivery to the NAPPF or other CHIPS R&D-designated research projects.
5. Other
    a. Dissemination of phase 3 outcomes.
    b. A refined CVDP plan and evidence of progress against the plan.
    c. Data-driven evidence of progress against the EWD plan.

1.6.4.5.2.5 Phase 4 – High-Performance Domain

Suggested targets include:

1. Scale-down
    a. The specifications and outputs developed under Phases 1 and 2 should be updated to reflect learnings identified during implementation.
2. Scale-out
    a. The specifications and outputs developed under Phases 1 and 2 should be updated to reflect learnings identified during implementation.
3. Ecosystem
    a. Chiplets available at cost for delivery to the NAPPF or other CHIPS R&D-designated research projects.
    b. Energy-efficient firmware revision.
4. Technology Demonstrator (TD)
    a. TD variant packaging, assembly, and bring up.
    b. Application demonstration on TD with 8 networked TD unit packages (both baseline and variant).
5. Other
    a. Dissemination of project outcomes.
    b. Completion of the CVDP against stated objectives.
    c. Completion of the EWD plan against stated objectives.

1.6.4.5.2.6 Phase 1 – Low-Power Domain

Suggested targets include:

1. Scale-down
    a. Specification for D2D interface that meets targets.
2. Ecosystem
    a. Reference architecture definition that meets functional and performance targets. Clear demonstration of potential for function scaling. Specification (preferably open) listing modular functions, functional and performance scaling, meets performance goals, chiplet control and management.
    b. Physical sockets (including 3d sockets as needed) specifications that are clearly correlated to reference architecture and performance targets and are consistent with NAPPF requirements. Specification (preferably open) for dimensions, power, power-delivery grid, thermal intensity, scale-down D2D Data connector size and locations, control connectors and locations etc.
    c. Detailed chiplets specifications (with power, performance targets) sufficient for reliable implementation schedule.
3. Technology Demonstrator (TD)
    a. Execution plan for chiplets (that support scaled-down interconnect) for TD.
    b. Identification and power-performance analysis of baseline and variant TDs.
    c. Application software requirements and execution plan.
4. Other
    a. Dissemination of phase 1 outcomes.
    b. All dependencies and risks clearly identified.
    c. A refined CVDP plan.
    d. Evidence of successful EWD outreach efforts.

1.6.4.5.2.7 Phase 2 – Low-Power Domain

Suggested targets include:

1. Scale-down
    a. D2D interface performance verified and characterized on one or more meaningful test chips and substrate.
2. Ecosystem
    a. Socket specifications published for third party use
3. Technology Demonstrator (TD)
    a. All chiplets for TD baseline platform taped out and brought up (derisked with intermediate proof-points as appropriate such as analysis, simulation, emulation etc.).
    b. Baseline TD package design with SI/PI analysis.
    c. Completion of exemplar Application system design. Identification of all components (beyond the unit package). System performance simulation. Completion of application software design. Completion of a development environment.
4. Other
    a. Dissemination of phase 2 outcomes
    b. A refined CVDP plan and a detailed description of progress against the plan
    c. A refined EWD plan and a detailed description of progress against the plan

1.6.4.5.2.8 Phase 3 – Low-Power Domain

Suggested targets include:

1. Scale-down
    a. The specifications and outputs developed under Phases 1 and 2 should be updated to reflect learnings identified during implementation.
2. Ecosystem
    a. TD package design for optional variant with SI/PI analysis.
    b. Firmware implementation.
3. Technology demonstrator (TD)
    a. TD baseline packaging and assembly, integration and bring up.
    b. TD Application development.
    c. Variant component and package development.
    d. Chiplets available at cost for delivery to the NAPPF or other CHIPS R&D-designated research projects.
4. Other
    a. Dissemination of phase 3 outcomes.
    b. A refined CVDP plan and evidence of progress against the plan.
    c. Data-driven evidence of progress against the EWD plan.

1.6.4.5.2.9 Phase 4 – Low-Power Domain

Suggested targets include:

1. Scale-down

    a. The specifications and outputs developed under Phases 1 and 2 should be updated to reflect learnings identified during implementation.
2. Ecosystem
    a. Chiplets available at cost for delivery to the NAPPF or other CHIPS R&D-designated research projects.
    b. Energy-efficient firmware revision.
3. Technology Demonstrator (TD)
    a. Optional TD variant packaging, assembly, and bring up.
    b. Application demonstration on TD (both baseline and optional variant), including networked demonstration.
4. Other
    a. Dissemination of project outcomes.
    b. Completion of the CVDP against stated objectives.
    c. Completion of the EWD plan against stated objectives.

1.6.5 R&D Area 5: Co-design/Electronic Design Automation (EDA)

1.6.5.1 Anticipated Amounts

For the Co-design/EDA R&D area, CHIPS R&D anticipates making available up to approximately $250,000,000 for funding multiple awards in amounts ranging from approximately $10,000,000 to approximately $100,000,000 in Federal funds per award, with a five (5) year period of performance. While cost share is not required, CHIPS R&D will give preference to applications that demonstrate credible cost share commitments, consistent with Section 3.2.

1.6.5.2 Background

Since its inception, EDA has been built around a series of layers of abstraction. However, abstraction limits in current EDA technology make it impossible to design at the full chip level for a chip or chiplet comprising more than approximately 100 million instances. Instead, in current practice, chips are partitioned into smaller blocks for implementation and reassembled before tapeout. Transporting this methodology to a system of a few chiplets is complex but feasible using existing tools. However, this approach does not scale to systems of hundreds or thousands of chiplets. A new layer of abstraction is needed for scale-out advanced package designs comprising systems of chiplets. Definition of this layer of abstraction, together with tools that use it to create a full end-to-end co-design and EDA solution for advanced packaging as an integral part of the overall semiconductor design stack, are the primary intended outputs for this R&D area.

The advanced end-to-end EDA solution(s) intended to emerge from this R&D investment comprise four elements. The first is a Design Platform providing a full suite of design implementation and verification capabilities and serving as the primary working interface for design teams. The Design Platform will integrate the three additional elements – distinct Security and Resilience Platforms and a full Process and Assembly Design Kit (PADK) – to ensure full design functionality.

To be effective, security must be designed in and not bolted on. The Security Platform is intended to enable verifiable secure-by-design capabilities for trustworthy products. Reliable and resilient system designs require a full lifecycle approach for security. The Resilience Platform is intended to provide all-life-stages test, repair, resilience, reliability, and fault tolerance design capabilities for reliably resilient products.

EDA platforms require standardized and accessible descriptions of their target manufacturing process. The PADK is intended to encapsulate all relevant data for advanced package co-design and EDA solutions.

This investment in innovation in co-design and EDA is intended to achieve the following outcomes.

3-5 years: New silicon-proven tools, flows, and methodologies from R&D projects are available commercially for designers of systems using advanced packaging. The new, standardized, chiplet layer of abstraction, along with tools featuring a scalable, cloud-based, software architecture, allows these system designs to take advantage of architectural and implementation optimizations that were previously unattainable. These innovations in turn spur additional EDA innovation and development, including from start-ups and academia. Tools, flows and on-chiplet infrastructure are available to NAPPF users and are incorporated in NAPPF prototyping flows and chiplet designs. The first new graduates emerge from new education and training programs for advanced packaging design technology. Enrollments are diverse and growing.

10 years: The new layer of abstraction and its associated scale-out cloud-based tool deployment approach are established as the foundation of a robust advanced packaging design ecosystem, which in turn supports a U.S. advanced packaging industry. This ecosystem is supported by all chiplet and EDA vendors and both enables and readily incorporates emerging innovations and new providers in all aspects of design and manufacturing, including advances in substrates, integration and inter-chiplet communication techniques, as well as system architecture, testability, security, resiliency, power delivery, and thermal management. Graduates from education and training programs are employed in good jobs in the advanced packaging sector.

1.6.5.3 Co-Design/Electronic Design Automation Objectives

Proposals for this R&D area must address at least one of Objectives 1-3, or Objective 4.

1. Design Implementation and Verification (Design)
2. Embedded Security (Security)
3. Test, Repair, Resilience, Reliability, and Fault Tolerance (Resilience)
4. Integrated, Independent Verification, and Validation (IV&V)

For each Objective selected by the applicant, the proposal must cover all R&D aspects listed in the corresponding Objective subsection below.

For Objectives 1 through 3, applicants must propose innovations in EDA tools, on-chiplet infrastructure, and co-design flows for scale-down and scale-out advanced package designs composed of chiplet-based systems. The intended R&D innovations include a full end-to-end lifecycle design flow from architecture and design exploration through implementation, including verification, to sign-off and release and on to manufacturing, test, and assembly, deployment, and end-of-life. Objectives 1-3 also include requirements for embedded, on-chiplet infrastructure that must be delivered as a synthesizable Register Transfer Level (RTL) description with full documentation and any needed scripts etc. and suitable for use throughout the product lifecycle.

Projects funded under this R&D area are intended to support other projects, and applicants should plan for collaboration with other project teams including, in NAPMP-specified cases, by providing tools and support for those tools for use within the NAPPF and other NAPMP-funded projects for the duration of the program. Applicants should also plan for alignment and collaboration discussions with participants in other programs funded by the CHIPS for America R&D Office, such as the Manufacturing USA Institute focused on digital twins, as well as other relevant government programs.[23]

The following subsections provide a detailed description for each of the four Objectives.

1.6.5.3.1 Objective 1: Design Implementation and Verification (Design)

This R&D area focuses on a comprehensive commercial-quality Design Platform capable of designing and co-optimizing a scale-down and scale-out system of hundreds or more chiplets, potentially of different sizes, in an advanced packaging design that could be up to wafer or panel scale, with substrates and ultrafine pitch wiring as specified in the NAPMP Materials and Substrates NOFO, and subsystems thereof, including logical, electrical, photonic, thermal, and mechanical models and any other information required for a complete end-to-end design environment.

The Design Platform should be cloud-based and structured around a chiplet-level layer of abstraction that encapsulates relevant properties and models of each chiplet's behavior while remaining agnostic to any EDA flow that was used to develop the chiplet. The Platform should also be designed to accommodate the Security and Resilience Platforms in Objectives 2 and 3 below and to make use of the Process and Assembly Design Kit in Objective 4 below.

The Design Platform may be derived from existing solutions, commercial or otherwise.

Covered Designs: The proposed platform must be able to handle, as a single entity, a package built on any substrate and containing a system with up to 1,000 chiplets including stacks up to 24 chiplets high with mixed, arbitrary chiplet sizes, composition, and function. The platform must also manage connectors, embedded passives, interposers, and/or bridges up to wafer/panel scale at the exploration, implementation and co-optimization, and sign-off design stages. The chiplet

[23] Related programs include DARPA Next Generation Microelectronics Manufacturing (NGMM), DoD Strategic Transition of Microelectronics to Accelerate Modernization by Prototyping and Innovating in the Packaging Ecosystem (STEAM PIPE), and NSF Future of Semiconductors (FuSe2), among others.

abstraction layer and tools/flows using it must support all of the following: any exemplar design or design-related deliverable from other NAPMP research areas, including thermal solutions being developed by the Power Delivery and Thermal Management R&D area ((potentially including microfluidics), multiple chiplets on a single stack layer, chiplets of different X, Y, and Z dimensions, including within a single stack, composite designs featuring multiple logical chiplets on a single physical chiplet, subsystems of multiple chiplets as a single entity (e.g. memory or processing stacks), and multiple interacting or independent heterogenous subsystems including analog, digital, photonic, and/or RF.

Out of scope for this Objective are design capabilities for purely monolithic systems, silicon tapeout or core circuit IP block development, or development of any chiplet-level application, operating system (OS), or driver software. While an automated place and route solution for chiplet-based systems is required, automated synthesis of these systems from a higher level description is not required. System architecture, neuromorphic solutions, and solutions primarily focused on chiplet-level EDA are out of scope. While the Design Platform is expected to be able to generate data that can be used by chiplet and system level digital twins, development of the twins themselves is not required.

1.6.5.3.2 Objective 2: Embedded Security (Security)

This Objective focuses on R&D for a Security Platform for full lifecycle security – design exploration through product end-of-life – suitable for advanced package designs. This includes threat model identification as well as selecting, implementing, verifying, and maintaining security, via online monitoring, detection, and response capabilities.

Applicants should describe an approach to Security Platforms that enables users to achieve their desired level of security in scale-down and scale-out systems consistent with the technical targets in this NOFO and those in the NAPMP Materials and Substrates NOFO. The proposed Security Platform may be derived from existing solutions, commercial or otherwise, but must work with an explicit chiplet-level layer of abstraction, such as that being developed under Objective 1 above and make use of access infrastructure being developed under Objective 3 below and the Process and Assembly Design Kit being developed under Objective 4 below. The approach must provide for in-system active security monitoring, detection, and threat response. It must also include appropriate, comprehensive, and extensible threat model(s) and associated security metrics that at minimum include malicious chiplets and side-channel attacks on inter-chiplet wiring.

The proposed platform must be cloud-based and able to handle, as a single entity, any advanced package as specified in “Covered Designs” in Objective 1 above at the exploration, implementation and co-optimization, and sign-off design stages with turnaround times measured in hours.

Proposals should specify the intended lifecycle definition for advanced packaging design automation – covering chiplets and systems of chiplets, and design, manufacturing/assembly, test, deployment, operation, and retirement stages – and how the proposed Security Design Platform addresses all aspects of that lifecycle.

Proposals should indicate whether Common Attack Pattern Enumeration and Classification (CAPEC) threats are intended to be covered, not covered, or out of scope for the planned approach.

Out of scope for this Objective are proposals focused on:

- Software security (e.g. software-based pointer checks),
- System security service functionality (e.g., encryption services),
- Secure communications protocols,
- Encryption techniques including fully homomorphic,
- Explainable AI,
- Anything subject to national security classification,
- Developing or managing external asset management capability, or
- Intra-chiplet hardware security techniques (e.g. physically unclonable functions, logic locking).

1.6.5.3.3 Objective 3: Test, Repair, Resilience, Reliability, and Fault Tolerance (Resilience)

This Objective focuses on R&D for an integrated Resilience Platform suitable for advanced package design. Applicants should describe approaches for a platform capable of designing and co-optimizing test, repair, resilience, reliability, and fault tolerance functionality in a scale-down and scale-out system of hundreds or more chiplets, potentially of different sizes, in an advanced packaging design that could be up to wafer or panel scale. The proposed design of the Resilience Platform should be compatible with the requirements for the Design and Security Platforms described above in Objectives 1 and 2, respectively, and make use of the Process and Assembly Design Kit being developed under Objective 4 below. Successful applicants will propose and develop a Resilience Platform based around a standardizable approach to chiplet-level test access, instrumentation, data collection and data analysis. Proposals will describe approaches that make use of existing standard access methods applicable to chiplet-based systems, including IEEE 1149.1-2013, 1687-2014 and 1838-2019.

Proposals should explicitly describe assumptions and requirements around chiplet-level design for test (DFT) and/or built-in self-test (BIST) capability, sign-off test coverage requirements (e.g., stuck-at fault coverage, pattern types etc.), required models and data, deliverable definition and formats (stimulus, built-in test, monitoring, repair, software/debug interfaces, keys, etc.). These must be aligned with the standards conformance defined above and must be independent of the EDA flow used to implement the chiplet and its DFT. Requirements for the Process and Assembly Design Kit being developed under Objective 4 below should also be noted.

The proposed Resilience Platform may be derived from existing solutions, commercial or otherwise, but must work with an explicit chiplet-level layer of abstraction, such as that being developed under Objective 1 above, and support the access infrastructure needs of the Design Platform and Security Platform being developed under Objectives 1 and 2 respectively. The proposed platform must be able to handle all Covered Designs as specified in Objective 1 above at the exploration, implementation and co-optimization, and sign-off design stages with

turnaround time measured in hours. Initial tool and support deliverables, as detailed below, for other NAPMP participants begins in Phase 1. Applicants should clearly demonstrate how they will be able to meet this timeline.

Out of scope for this Objective are proposals primarily focused on new test equipment or intra-chiplet DFT techniques; communication standards conformance demonstrations, including bit error rate (BER) demonstrations; fault tolerant system architectures; or new information coding techniques. Demonstrated compliance with ISO 26262 or other domain-specific functional safety standards is not required.

1.6.5.3.4 Objective 4: Integrated Independent Verification, and Validation (IV&V)

This Objective focuses on R&D for validating, integrating, and hosting Co-Design and EDA R&D deliverables for use across NAPMP. This includes R&D for defining, assembling, and developing a PADK that covers every manufacturing and assembly process to be supported by the NAPPF, as well as R&D for an integrated IV&V Platform covering all deliverables in the Co-design and EDA R&D area, and includes developing and supporting a cloud-based hosting platform for verified deliverables, including the Design Platform, Security Platform, and Resilience Platform being developed under Objectives 1-3 above. Applicants should describe approaches for a platform with these capabilities for a scale-down and scale-out system of hundreds or more chiplets, potentially of different sizes, in an advanced packaging design that could be up to wafer or panel scale. The proposed design of the IV&V platform should be compatible with the requirements for the Design, Security, and Resilience Platforms described above in Objectives 1, 2 and 3, respectively.

Applicants should describe the required and desirable elements for a PADK; its relationship to chiplet and substrate design, manufacturing, test, and assembly their application builds on, complements, and differs from related existing approaches (e.g. Open Compute Project, foundry-specific programs) and others under development (e.g. DARPA NGMM); and how they would coordinate their PADK development activities with those external organizations as well as internally within NAPMP. Applicants should also discuss the potential for standardization of their proposed PADK.

Applicants should also describe a platform to independently integrate and validate design, security, and resilience tools for HPC and low-power systems. The proposal should describe a cloud-based infrastructure for demonstrations, including system access, accounting, file transfer, version, permission, and IP control for users. This platform will include a portal to host advanced packaging design across NAPMP using validated and released versions of the Design Platform, Security Platform, and Resilience Platform described above, along with released versions of the PADK, for the duration of the program. Applicants should include a detailed costing proposal for this portal, along with a proposed cost allocation across users.

A key deliverable for successful applicants in this Objective will be working with successful applicants working on Objectives 1-3 on their program milestones to develop, in a timely fashion, a method to verify and validate that they have met each milestone and to use that

method to perform that verification and validation. Applicants should include evidence of prior experience working with multiple independent groups, including integrating and evaluating complex sets of interacting deliverables, while managing IP Rights and real or potential conflicts of interest. The proposed IV&V Platform may be derived from existing solutions, commercial or otherwise, but must work with an explicit chiplet-level layer of abstraction, such as that being developed under Objective 1 above. The proposed platform must be able to handle all Covered Designs as specified in Objective 1 above at the exploration, implementation and co-optimization, and sign-off design stages with acceptable throughput and latency.

Out of scope for this Objective are proposals that feature hardware or manufacturing demonstrations, proposals that are based around non-cloud computing platforms, and proposals that seek to alter or replicate rather than integrate and evaluate deliverables from other Objectives.

1.6.5.4 R&D Outputs and Technical Targets

1.6.5.4.1 Outputs

1.6.5.4.1.1 Outputs for Objective 1: Design

Required R&D outputs under this Objective include: (1) a documented Design Platform architecture; (2) a set of tools developed in accordance with that architecture; (3) system-based demonstrations of functionality; and (4) a built Design Platform system based on the architecture and integrating the tool sets produced in the project. Requirements for these outputs can be summarized as follows.

1. **Architecture:** Applicants should provide a description of the following.
    a. The proposed chiplet-level abstraction model and how it will be used by the Design Platform. The abstraction layer definition of chiplet will be broad in order to "future proof" it, and will be able to support HPC and low power systems design along with designs that include:
        i. Multiple chiplets on a single stack layer
        ii. Chiplets of different X, Y, and Z dimensions, including within a single stack
        iii. Multiple logical chiplets on a single physical chiplet
        iv. Subsystems of multiple chiplets as a single entity
        v. Chiplets with digital, analog, RF, and/or photonic interfaces
    b. The proposed sign-off process and release to manufacturing, including data required and reports and other output files generated to enable post-manufacture operation management and monitoring; evidence that each design constraint including mechanical, power, thermal, timing, and signal/power/thermal integrity has been met
    c. Any legacy tools (chip, package, PCB, or other level) that will be used as part of the proposed Design Platform, describing any linkages to them in the form of API or file accesses, format translators, etc.

d. How the proposed Design Platform will enable design with each of the substrates specified in the NAPMP Materials and Substrates NOFO
e. How the proposed Design Platform will link to processes and data described the other R&D areas in this NOFO: Equipment, Tools, Processes, and Process Integration (Section 1.6.1); Power Delivery and Thermal Management (Section 1.6.2); Connector Technology, Including Photonics and RF (Section 1.6.3); and Chiplets Ecosystem (Section 1.6.4)
f. Database(s) that will be used or are expected to be developed as part of the proposed Design Platform
g. If AI/ML is proposed as a portion of a solution, describe the expected models and training data along with an overview of any expected gains/limitations compared to an approach not using AI/ML

2. **Tools:** Applicants should address the following aspects in proposing design tool R&D.
   a. Tool(s) that read and write the chiplets-level abstraction model, including at least one open interchange format.
   b. A description of any characterization tools or other mechanisms, and input needed for them, that will be used or need to be developed or modified to incorporate any process, assembly or other design kit information needed by the proposed system.
   c. A description of any characterization tools or other mechanisms, and input needed for them, that will be used or need to be developed or modified to create a chiplet level of abstraction model for chiplets with analog, digital, mixed signal, RF, memory and/or photonic functionality.
   d. Constraint-aware automated design exploration and co-optimization capabilities. These capabilities include the following.
      i. System of chiplets: System partitioning, chiplet and socket selection/spec/connection, system interface and communication definition, power/thermal planning, Power, Thermal, Performance and Area/Cost (PTPAC) estimation, including wiring density and hotspot identification. These will enable a user to choose which portions of a system will be allocated to which chiplet, based on availability, cost, power, thermal, and/or other constraints, as well as to specify the interconnection requirements of the system.
      ii. Advanced package design and substrate specification; initial cost/BOM; initial architecture and analysis of mechanical, wiring, thermal, and power infrastructure; constraint generation, including user-specified density, electrical, matching, shielding, and redundancy requirements; and PCB interface specification.
      iii. Provide PTPAC estimates within a defined range of accuracy, expected to be 10% at the end of the program, compared to sign-off results.
      iv. Integration of infrastructure, constraints, and/or estimates developed by Objectives 2 and 3.
      v. Use of and requirements for the Process and Assembly Design Kit being developed by Objective 4.
   e. Constraint-aware automated and integrated design, implementation, optimization, verification, and validation capabilities for designing a package containing a system of chiplets. These capabilities include the following.

i. Mechanical design including substrate/package, bump or equivalent placement and assignment, connector integration, and any needed power and cooling structures.
ii. Floorplanning (3D distribution of chiplets and any other system components within package), intra-package chiplet, interposer, connector, bridge, thermal structure, and embedded passive placement, full ultrafine pitch substrate, interposer, bridge, embedded passive, through-substrate and inter-die routing, power and clock delivery, timing, ECO
iii. Package and system-of-chiplet simulation, Multiphysics analysis, verification, validation, visualization, layout versus schematic (LVS) and design rule checking (DRC).
iv. Provide sign-off quality PTPAC estimates within a defined range of accuracy, expected to be 2% at the end of the program, compared to sign-off results.
v. Integration of infrastructure developed by Objectives 2 and 3 and the Thermal Management and Power Delivery R&D area.

f. Automated sign-off capability including automated generation of all deliverables needed for manufacture at NAPPF or equivalent facility, including evidence that each design constraint has been met, analogous to tapeout in a system-on-chip flow.

3. **Demonstrations:** Applicants should describe plans for providing the following demonstrations suitable for evaluation by NAPMP or an independent evaluator. In providing demonstrations for evaluation, successful applicants will be expected to describe and provide any embedded chiplet design content required by their tool or demonstration as a standard commercial design deliverable (e.g. synthesizable RTL, implementation scripts, plus complete documentation).
    a. A complete end-to-end design flow using the proposed design platform, including descriptions of tools, models, and data used at each step, for a chiplet-based system covering a High-Performance Technology Demonstrator as described in the Chiplets R&D area of this NOFO in Section 1.6.4.
    b. A verification flow showing how each aspect of any design or data created by the design platform can be verified to be correct and any metrics by which correctness is defined.
    c. An open interchange format that provides a complete description of any Covered Design along with tools that read and write that format.
    d. Two or more demonstrations based on HPC and low power systems of an automated advanced package design exploration flow.
    e. Two or more demonstrations based on HPC and low power systems of an automated system of chiplets design exploration flow.
    f. Two or more demonstrations based on HPC and low power systems of an automated advanced package and system of chiplets design implementation flow.
    g. Two or more demonstrations based on HPC and low power systems of an automated advanced package and system of chiplets design sign-off flow.
    h. Demonstration based on an HPC system of automated generation of synthesizable Register Transfer Level (RTL) for on-chiplet voltage and temperature monitoring designs.

i. Demonstration based on circuit simulation for an implementation of on-chiplet voltage and temperature monitoring designs.

4. **Platform**: Successful applicants will be expected to build a cloud-based Design Platform system that enables exploration of tradeoffs and implementation optimization of designer-chosen parameters such as power, performance (latency and/or throughput), and/or cost (component, manufacturing/assembly, and/or operating) and design sign-off while operating within a set of designer-chosen and other constraints and limits, including the following:
    a. Use of information from existing chip-level EDA descriptions (e.g., netlist, LEF/DEF, GDS)
    b. Use of information from preexisting PDKs/ADKs
    c. Tool execution time
    d. Design cost (time, resources)
    e. System cost (component, manufacturing/assembly, operating)
    f. Communication standards
    g. Size/Weight
    h. Power (total, instantaneous, idle, dynamic)
    i. Timing
    j. Thermal (steady state and dynamic, local and global)
    k. Mechanical
    l. Noise, signal/power integrity
    m. Debuggability

1.6.5.4.1.2 Outputs for Objective 2: Security

Required R&D outputs under this Objective include: (1) a documented Security Platform architecture; (2) a set of tools developed in accordance with that architecture; (3) simulation-based and system-based demonstrations of functionality; and (4) a built Security Platform based on the architecture and integrating the tool set. Requirements for these outputs can be summarized as follows.

1. **Architecture:** Applicants should describe plans for developing:
    a. A documented hardware security design architecture, including a threat model and provisions for automated tools and flows, for scale-down and scale-out HPC and low power systems. The architecture must specify any root-of-trust assumptions or requirements and the proposed full lifecycle control approach (e.g., a special control chiplet, a distributed system of control chiplets, or circuitry that must reside on one or more other chiplets, such as utility chiplets for power or test control). The threat model description must enumerate which Common Attack Pattern Enumeration and Classification (CAPEC) threats are intended to be covered, not covered, or out of scope for the planned approach.
    b. A side-channel attack-resistant wiring structure, amenable to automated routing, for advanced packaging designs.
2. **Tools:** Proposals should describe R&D approaches for developing the following tools.

a. A design exploration tool using chiplets as an abstraction layer that enables automated evaluation of security tradeoffs in power, thermal, performance, area, and cost (PTPAC) metrics and other relevant metrics.
b. A tool for automated generation of synthesizable Register Transfer Level (RTL) security infrastructure designs, including PTPAC overhead estimates.
c. A tool for automated calculation of security metrics for advanced packaging designs.
d. A tool enabling automated identification, at system power-up, of malicious chiplets, defined as those chiplets exhibiting one or more threats from the applicant-specified threat model(s).
e. A tool for automated routing of side-channel attack-resistant wiring structures.

3. **Demonstrations:** Applicants should describe plans for providing the following demonstrations suitable for evaluation by NAPMP or an independent evaluator. In providing demonstrations for evaluation, successful applicants will be expected to describe and provide any embedded chiplet design content required by their tool or demonstration as a standard commercial design deliverable (e.g. synthesizable RTL, implementation scripts, plus complete documentation)
    a. Demonstration via logic simulation of the Security Platform architecture.
    b. Demonstration based on an HPC system of automated evaluation of tradeoffs for PTPAC metrics and other relevant, applicant-selected metrics.
    c. Demonstration based on an HPC system of automated generation of synthesizable Register Transfer Level (RTL) security infrastructure designs.
    d. Two or more demonstrations based on HPC and low power systems of automated calculation of security metrics for advanced packaging designs.
    e. Two or more demonstrations based on HPC and low power systems of identifying a malicious chiplet at system power-up.
    f. Two or more demonstrations based on HPC and low power systems of automated routing of side-channel attack-resistant wiring structures.
    g. Demonstration, via side-channel appropriate simulation, side-channel resistance of an advanced package design.
    h. Demonstration, via simulation, formal proof, or other appropriate means, of the mechanism by which each covered threat in the applicant-specified threat model is covered and what security metrics apply to this coverage.
4. **Platform:** Proposals should include plans for building an instance of a cloud-based Security Platform based on the system architecture and tools developed in the project. The platform should enable exploration of security design tradeoffs and implementation/optimization of designer-chosen parameters such as defined security metrics (evaluated during design, manufacturing and/or operating life) and/or cost (component, manufacturing/assembly, and/or operating). The platform should provide for use of a chiplet abstraction layer consistent with the provisions of Objective 1 above and work with any predefined system of chiplets, including those for HPC and low power systems.

1.6.5.4.1.3 Outputs for Objective 3: Resilience

Required R&D outputs under this Objective include: (1) a documented Resilience Platform architecture; (2) a set of tools developed in accordance with that architecture; (3) demonstrations of functionality for each tool; and (4) a built Resilience Platform system based on the proposed architecture and integrating the proposed tool set. Requirements for these outputs can be summarized as follows.

1) **Architecture:** Applicants should describe plans for developing a documented Resilience Platform architecture capable of enabling:
    a. Standard test access port designs, including TAP, Test Access Ports; PTAP, Primary Test Access Ports; and STAP, Secondary Test Access Ports designs.
    b. A reference design for a system including examples of stacked and non-stacked utility chiplets and associated test infrastructure, including Instrument Connectivity Language (ICL) and Procedural Description Language (PDL) examples as well as a reference instrument interface design including support for a timer, a temperature sensor, and a voltage sensor along with a scanned digital logic block and embedded memory built-in self-test (BIST). The reference design will include at least one analog, RF, and photonic interface.
    c. Tools to generate synthesizable RTL designs for controllers and other required infrastructure (IEEE 1364.1-2002)
    d. A tool flow to set up instruments, deliver test data to chiplets and read test data from chiplets using logic simulation and commercially available automatic test equipment (ATE)
2) **Tools:** Proposals should describe R&D approaches for developing the following tools.
    a. An automated generation tool producing synthesizable RTL designs for standard test access infrastructure.
    b. A design exploration tool using chiplets as an abstraction layer that enables evaluation of tradeoffs between manufacturing test, redundancy/repair/isolation capability, fault/error tolerance, and graceful degradation/failure for systems that may include digital, analog, RF and/or photonic components.
    c. An automated test generation and diagnosis tool for fault models including shorts, opens and stuck-at for inter-chiplet wiring at ultrafine pitches specified in the NAPMP Materials and Substrates NOFO, including wiring on any substrate, bridge, and/or interposer, including embedded passives, and wired connections between stacked chiplets.
    d. A tool for automatically generating design-for-redundancy, repair, or error tolerance capabilities for ultrafine pitch inter-chiplet wiring allowing for manufacturing time reconfiguration for yield and reliability maximization. Proposals including online or power-up test and repair capability are encouraged. Proposals must not require physical rework (e.g. chiplet replacement, Focused Ion Beam (FIB)) as part of manufacturing but may include e-fuses or similar technology.
    e. Extensible in-system measurement tool(s) and associated on-package or on-chiplet infrastructure for, at a minimum, voltage, temperature, power consumption, and timing that are usable throughout the system lifecycle.

f. A tool for automatically generating manufacturing test flow, stimulus, known-good die/stack test capabilities usable for utility chips, prototypes, and other demonstrators or test vehicles.
g. One or more tools for implementing a fault tolerance methodology usable for HPC and low power Chiplet exemplars tied to a Failures in Time (FIT) rate; this methodology may be demonstrated via simulation rather than hardware.
h. In coordination with projects in the Equipment, Tools, Processes and Process Integration R&D area (see Section 1.6.1), develop appropriate tools to provide defect diagnosis capability suitable for use at the chiplet and substrate interconnect level.

3) **Demonstrations:** Applicants should describe plans for providing the following demonstrations suitable for evaluation by NAPMP or an independent evaluator. In providing demonstrations for evaluation, successful applicants will be expected to describe and provide any embedded chiplet design content required by their tool or demonstration as a standard commercial design deliverable (e.g. synthesizable RTL, implementation scripts, plus complete documentation).
    a. Demonstration of an advanced packaging reference design implemented as synthesizable Register Transfer Level (RTL) suitable for training purposes and demonstrating resilience functionality.
    b. Three or more demonstrations based on the reference design of 3a plus HPC and low power systems of automated generation of synthesizable Register Transfer Level (RTL) on-chiplet test access infrastructure designs.
    c. Three or more demonstrations based on the reference design of 3a plus HPC and low power systems of test generation and diagnosis capability with signoff quality on fault metrics.
    d. Three or more demonstrations based on the reference design of 3a plus HPC and low power systems of design for redundancy, repair or error tolerance.
    e. Three or more demonstrations based on the reference design of 3a plus HPC and low power systems of synthesizable Register Transfer Level (RTL) in-system measurement capability.
    f. A demonstration using circuit simulation of an implementation of in-system measurement of each of a timing, temperature, and voltage sensor.
    g. Three or more demonstrations based on the reference design of 3a plus HPC and low power systems and using logic simulation of FIT-based error tolerance capability.
    h. A demonstration of a full manufacturing test flow for a product in the NAPPF.
4) **Platform:** Proposals should include plans for building an instance of a cloud-based Resilience Platform that enables exploration of tradeoffs and implementation optimization of user-chosen parameters such as yield (at design, manufacturing and/or operating life), resilience (reliability, fault/error tolerance, graceful failure), and/or cost (component, manufacturing/assembly, and/or operating). The platform should:
    a. Provide for use of a chiplet abstraction layer consistent with the provisions of Objective 1 above and be compatible with security solutions, including those developed under Objective 2 above.
    b. Work with the Process and Assembly Design Kit being developed under Objective 4 below.

c. Work with any predefined system of chiplets, including those for HPC and low power systems.
d. Optimize test application time, equipment costs, and power, thermal, performance, area, and cost (PTPAC) overhead and failures in time (FIT) rates.

1.6.5.4.1.4 Outputs for Objective 4: IV&V

Required R&D outputs under this Objective include: (1) a documented IV&V Platform architecture; (2) a set of tools developed in accordance with that architecture; (3) demonstrations of functionality for each tool; (4) a built IV&V Platform system based on the proposed architecture and integrating the proposed tool set; and (5) a set of IV&V evaluations for Objectives 1-3 using the Platform. Requirements for these outputs can be summarized as follows.

1) **Architecture**: Applicants should describe plans for developing a documented IV&V Platform architecture capable of enabling:
    a. An actively managed design-in-cloud portal featuring independent work areas for the Co-Design/Electronic Design Automation (CDEDA) R&D area and possibly other NAPMP performers, secure and monitored access, upload and storage, application hosting and versioning capability, and sufficient compute and storage capability to demonstrate all CDEDA research outputs and to provide hosting services for those outputs to other NAPMP performers and enable their use for technology demonstrator and other program designs.
    b. A hosted and complete Process and Assembly Design Kit for each process to be made available in the NAPPF, using standard formats where possible but developing new ones as needed, including substrate PDKs as defined in the NAPMP Packaging and Substrates NOFO, and describing all phase-dependent and relevant technical properties of solutions developed in the Chiplets, ETPI, PDTM, and Connector Technology R&D areas and providing all needed information for Objective 1-3 solutions. Properties will include, at minimum, 2D and 3D logical, physical, electrical, photonic, and thermal package properties, models, design and assembly rules, package and connector specifications including material properties and dimensions, device and interconnect models with physical and logical connectivity, supported Chiplet interface standards, reliability criteria, design-for-test, manufacturability, reliability, yield and similar rules, plus hooks and required properties of chiplet-level PDKs (e.g. foundry deliverables for a node PDK) and any additional information determined to be needed over the course of the program
2) **Tools**: Proposals should describe R&D approaches for developing the following tools:
    a. Tools enabling and implementing the cloud-based portal architecture hosted on a commercial cloud or equivalent.
    b. Tools required for validating the proposed PADK.
3) **Demonstrations**: Applicants should describe plans for providing the following demonstrations suitable for evaluation by NAPMP:
    a. A hosted cloud-based portal and platform implementing the architecture in Output 1a above.

b. An example of a Process and Assembly Design Kit implementing the architecture in Output 1b above.

4) **Platform**: Proposals should include plans for building an IV&V Platform capable of hosting and delivering architecture described above including:
    a. Managed releases of tools and other outputs developed under Objectives 1-3
    b. Managed and scheduled releases of the NAPPF PADK on at least an annual cadence, following industry standard nomenclature (e.g. v0.01, 0.1, 1.0)
5) **Evaluations**: Applicants should outline approaches, including relevant tools, design collateral, and evaluation criteria to measure performance and provide a detailed evaluation of each output milestone for Objectives 1-3 above, including generating a report assessing whether that milestone has been met together with the criteria, data, and any other relevant information used to make that assessment. Applicants should clearly explain their plans, definitions, and assumptions around maintaining independence and objectivity with respect to successful applicants working on Objectives 1-3.

1.6.5.4.2 Technical Targets

End-of-Program Project-Level Technical Targets fall into four categories: (1) Design; (2) Security; (3) Resilience, and (4) IV&V. The envisioned end states for the Technical Targets in each category can be summarized as follows.

1) Design
    a. A cloud-based design exploration framework using chiplets as an abstraction layer that enables evaluation of tradeoffs in PTPAC and other relevant metrics along with automated exploration of tradeoffs in advanced package design with PTPAC estimates within 10% of sign-off values at final release, with execution time of no more than 2 hours per cycle for a 1000 chiplet design and vCPU needs that scale linearly with the number of chiplets.
    b. A cloud-based design implementation framework including fully automated package and system-of-chiplet floorplanning, intra-package chiplet, connector, interposer, bridge, thermal structure, and embedded passive placement, full ultrafine pitch substrate, interposer, bridge, embedded passive, through-substrate and inter-die routing, power and clock delivery, timing, simulation, multiphysics analysis, verification, validation, visualization, LVS/DRC with PTPAC estimates within 2% of sign-off values at final release, execution time of no more than 8 hours per cycle for a 1000 chiplet design and vCPU needs that scale linearly with the number of chiplets.
    c. A cloud-based design sign-off framework including automated generation of all deliverables needed for manufacture at NAPPF or equivalent facility with execution time of no more than 24 hours per cycle for a 1000 chiplet design and vCPU needs that scale linearly with the number of chiplets.
    d. Automated generation of synthesizable on-chiplet management and monitoring infrastructure integrated compatible with IEEE standard access methods as described in the Resilience targets below, capable of monitoring on-chip voltage and temperature with at least 10,000 samples per second for a chosen chiplet with PTPAC overhead estimates within 2% of final implementation.

e. An open, standardizable format describing a chiplet-level abstraction layer that covers current and future advanced package designs of arbitrary size, complexity, and composition, including but not limited to analog, digital, RF, and photonic interconnects, with arbitrary numbers of chiplets arranged horizontally and vertically, together with tools that read and write this format.

2) Security
    a. A design exploration framework using chiplets as an abstraction layer that enables evaluation of tradeoffs in PTPAC and other relevant metrics along with automated exploration of security tradeoffs, with all estimated quantities within 10% of implementation at final release, on HPC prototype system or equivalent.
    b. Automated generation of synthesizable RTL for on-chiplet security control infrastructure compatible with IEEE standard access methods as described in the resilience targets below with PTPAC overhead estimates within 2% of final implementation.
3) Resilience
    a. A system for Resilient Design Exploration, including a demonstration on chiplets using each of digital, analog, RF and photonic connectors. All estimated quantities must be within 10% of implementation at final release.
    b. A Resilience Platform System working on an HPC design from Chiplets R&D areas. Estimates must be within 2% of implementation at final release. All other metrics must be sign-off quality. System must allow user selection of an agreed upon set of constraints which will include FIT requirements, software execution time and resources, test application time bounds, and PTPAC overhead limits (power, thermal, performance, area/cost)
    c. A reference design of an advanced package system, built on a substrate from the NAPMP Materials and Substrates NOFO, that includes examples of stacked and non-stacked utility chiplets and associated test infrastructure, including ICL and PDL examples as well as a power delivery network, cooling infrastructure, examples of analog, digital, RF and photonic interfaces, plus a reference instrument interface design including support for a timer, a temperature sensor, and a voltage sensor along with a scanned digital logic block and embedded memory BIST, and provides a supported methodology and flow for adding new instruments.
4) IV&V
    a. A complete Process and Assembly Design Kit for each process available in the NAPPF, using standard formats where possible but incorporating new ones as needed, including substrate PDKs as defined in the NAPMP Materials and Substrates NOFO, including at minimum, 2D and 3D logical, physical, electrical, mechanical, photonic, and thermal package design and assembly rules, package and connector specifications including material properties and dimensions, device and interconnect models with physical and logical connectivity, supported Chiplet interface standards, reliability criteria, design-for-test, manufacturability, reliability, yield and similar rules, plus any additional information determined to be needed over the course of the program.
    b. An actively managed design-on-cloud portal featuring independent work areas for a diverse set of users, secure and monitored access, upload and storage,

application hosting and versioning capability, and sufficient compute and storage capability to demonstrate all CDEDA research outputs and to provide hosting services for those outputs to other NAPMP performers.

1.6.5.5 Project Structure

1.6.5.5.1 Required Team Capabilities

CHIPS R&D strongly encourages applications from multi-disciplinary, multi-organization project teams that collectively demonstrate the full range of expertise, experience, and capabilities needed to achieve the technical objectives of this R&D area to innovate new breakthrough tools for advanced packaging design. For the purposes of this NOFO, a project team comprises all funded entities (the applicant and any proposed subrecipients) as well as unfunded collaborators planned for inclusion in a single application. Project team participation from academic and other research entities is strongly encouraged. To promote paths to commercial adoption, the program will connect projects funded under this NOFO with prototyping and piloting facilities capable of evaluating technologies for performance at commercial scale with a path to high volume manufacturing.

Project team leads for Objectives 1-3 are expected to be an entity with a demonstrated expertise in the core function of the technical area. Team leads must demonstrate a history of delivering and supporting complex EDA systems, either commercially or as part of a larger entity. The team must provide evidence of expertise in each portion of its proposal. Successful proposals must include plans to maintain open specifications, including but not limited to the chiplet-level layer of abstraction, on-chiplet infrastructure and data requirements, and Process and Assembly Design Kit architecture. Applicants will be expected to include community outreach and workforce development activities as part of their efforts.

Applicants should propose milestones that represent measurable steps toward achieving Project-Level Non-Technical Targets, as described in Sections 1.7.1 and 1.7.2. Applicants may also propose additional non-technical milestones.

1.6.5.5.2 Project Phases

1.6.5.5.2.1 Overview

Applicants must propose a detailed project plan for achieving Project-Level Technical Targets. Projects should be divided into four (4) phases over a five (5) year period of performance. Phase 1 should be 12 months, Phases 2 and 3 should be 18 months, and Phase 4 should be 12 months. Execution plans for each phase should describe key R&D activities and risk assessments, milestones within the phase and go/no-go checkpoints between the phases. Go/no-go checkpoints will be evaluated by the CHIPS team and will encompass a comprehensive review of progress toward achieving technical targets, risk assessment and mitigation plans. The focus for each of the four phases can be summarized as follows.

The discussion below uses standard software lifecycle terminology, where, an “alpha” release may be missing some features or capability, a “beta” release has a full set of features and capabilities but may contain bugs or miss corner cases. A “final” or “production quality” release has been fully tested and validated against all expected use cases. All deliverables across all phases must be made available for evaluation by NAPMP or an independent evaluator.

1.6.5.5.2.2 Phase 1

1) Design
    a. An initial (alpha) version of the chiplet-level layer of abstraction and its associated database
    b. An initial (alpha) version of the Design Platform architecture
    c. An initial (alpha) version of the design exploration framework
    d. An initial (alpha) version of the proposed open interchange format
    e. A revised (beta) version of the chiplet-level layer of abstraction and its associated database
    f. Initial (alpha) versions of the Design demonstrations in Section 1.6.5.4.1 above
2) Security
    a. An initial (alpha) version of the Security Platform architecture
    b. An initial (alpha) design of a side-channel attack-resistant wiring structure amenable for routing
    c. Initial (alpha) versions of the Security demonstrations in Section 1.6.5.4.1 above
3) Resilience
    a. An initial (alpha) version of the Resilience Platform architecture
    b. An initial (alpha) design of the test access infrastructure generator
    c. A revised (beta) design of the test access infrastructure generator
    d. An initial (alpha) version of the reference design
    e. Initial (alpha) versions of the Resilience demonstrations in Section 1.6.5.4.1 above
4) IV&V
    a. An initial (alpha) instance of the cloud-based portal
    b. An initial (alpha) version of the Process and Assembly Design Kit
    c. Reports for Phase 1 milestones in Design, Security and Resilience above
    d. Initial (alpha) versions of the IV&V demonstrations in Section 1.6.5.4.1 above

1.6.5.5.2.3 Phase 2

1) Design
    a. A revised (beta) version of the Design Platform architecture
    b. A revised (beta) version of the design exploration framework
    c. A revised (beta) version of the proposed open interchange format
    d. An initial (alpha) design of an on-chiplet monitoring structure.
    e. An initial (alpha) version of the design implementation and signoff frameworks
    f. Revised (beta) versions of the Design demonstrations in Section 1.6.5.4.1 above.
2) Security
    a. A revised (beta) version of the Security Platform architecture

b. A revised (beta) design of a side-channel attack-resistant wiring structure amenable for routing
c. Revised (beta) versions of the Security demonstrations in Section 1.6.5.4.1 above.

3) Resilience
   a. A revised (beta) version of the Resilience Platform architecture
   b. A built instance of the test access infrastructure generator
   c. A revised (beta) version of the reference design
   d. Revised (beta) versions of the Resilience demonstrations in Section 1.6.5.4.1above
4) IV&V
   a. A revised (beta) instance of the cloud-based portal
   b. A revised (beta) version of the Process and Assembly Design Kit
   c. Reports for Phase 2 milestones in Design, Security and Resilience above
   d. Revised (beta) versions of the IV&V demonstrations in Section 1.6.5.4.1 above

1.6.5.5.2.4 Phase 3

1) Design
   a. A final version of the Design Platform architecture
   b. A final version of the chiplet-level layer of abstraction and its associated database
   c. A revised (beta) design of an on-chiplet monitoring structure.
   d. A revised (beta) version of the design implementation and signoff frameworks
   e. Final versions of the Design demonstrations in Section 1.6.5.4.1 above
2) Security
   a. A final version of the Security Platform architecture
   b. A final design of a side-channel attack-resistant wiring structure amenable for routing
   c. Final versions of the Security demonstrations in Section 1.6.5.4.1 above
3) Resilience
   a. A final version of the Resilience Platform architecture
   b. A final version of the reference design
   c. Final versions of the Resilience demonstrations in Section 1.6.5.4.1 above
4) IV&V
   a. A built instance of the cloud-based portal based on the system architecture and tools developed in the project.
   b. Further revised (production) version of the Process and Assembly Design Kit
   c. Reports for Phase 3 milestones in Design, Security and Resilience above
   d. Further revised (production) versions of the IV&V demonstrations in Section 1.6.5.4.1 above

1.6.5.5.2.5 Phase 4

1) Design
   a. A built instance of the Design Platform based on the system architecture and tools developed in the project.

b. A built instance of an on-chiplet monitoring structure based on the design and infrastructure developed in the project.
c. A final version of the proposed open interchange format

2) Security
   a. A built instance of the Security Platform based on the system architecture and tools developed in the project.
3) Resilience
   a. A built instance of the Resilience Platform based on the system architecture and tools developed in the project.
4) IV&V
   a. A final version of the Process and Assembly Design Kit
   b. Reports for Phase 4 milestones in Design, Security and Resilience above

1.7 Project Level Non-Technical Plans

The following subsections provide contextual information applicable to all R&D areas and are intended to assist applicants in preparing responsive Concept Papers (see Section 4.5) and Full Applications (see Section 4.6). All applicants must comply with the requirements in this section.

1.7.1 Education and Workforce Development (EWD) Plans

Under this NOFO, NAPMP investments are intended to create innovation-driven domestic substrate manufacturing capability, which requires fostering a diverse and capable domestic workforce with access to good jobs, such as those consistent with the Good Jobs Principles. The combination of expertise, facilities, and equipment required to meet the technical targets described in Section 1.4 provide exceptional opportunities for tailored EWD programs. In developing an EWD plan, CHIPS R&D encourages applicants to consult the CHIPS R&D Education and Workforce Development (EWD) Plan Guidebook as well as the Department of Commerce Workforce Development Strategy Principles.

Applicants must provide an EWD plan that leverages capabilities supported through the proposed project to address domestic advanced packaging workforce needs, including educational opportunities to engage students in research. In the EWD plan, CHIPS R&D encourages applicants to describe any efforts to attract and retain a diverse student and trainee population and to demonstrate that the EWD efforts are worker-centered, industry-aligned, and promote high-quality jobs.

Examples of relevant activities in an EWD plan may include paid research internships and fellowships focused on project activities, paid research experiences for undergraduates, and training programs that take advantage of the project's facilities, including in-person and virtual programs, partnerships with employers, labor, and the public workforce system, as well as any other institutions key to the delivery of quality employment and training pathways, such as educational institutions, government agencies, industry organizations, and programs focused on training for underserved communities, as defined by Executive Order 13985, Advancing Racial Equity and Support for Underserved Communities Through the Federal Government (Jan. 20, 2021) and Executive Order 14091, Further Advancing Racial Equity and Support for

Underserved Communities Through the Federal Government (Feb. 16, 2023). Applicants must propose SMART EWD targets, such as the number of students trained or engaged in research and subsequently placed in good jobs in the domestic semiconductor industry, to be achieved under the EWD plan.

Educational and workforce activities that do not directly address areas specific to project technical needs, such as developing general curriculum or generic training program design, are not funded under this NOFO.

1.7.2 Commercial Viability and Domestic Production (CVDP) Plans

Consistent with promoting a robust, sustainable domestic capacity for substrate R&D, prototyping, and production, and in keeping with the provisions of Executive Order 14104 and the CHIPS Act domestic production requirements (15 U.S.C. § 4656(g)), CHIPS R&D requires applicants to develop and provide a CVDP plan that describes activities to be funded as part of the project. Applicants are encouraged to consult the CHIPS R&D Commercial Viability and Domestic Production (CVDP) Plan Guidebook in developing their CVDP plan.

The CVDP plan must include a realistic business model for the funded innovations (which may include software), include a technology transition plan, and describe pathways to benefitting national and economic security, such as through the domestic availability of the technology and successful adoption by commercial or defense partners. Applicants should propose measurable CVDP targets that demonstrate the viability of the proposed business model and of the domestic production. Where relevant, CVDP milestones should complement technical milestones.

Strong applications will present evidence of existing or potential demand for the funded innovations (which may include software); identify existing or potential customers, or categories of customers, at volumes necessary for commercial viability; provide an initial assessment of marketability in terms of cost and value proposition that can be updated as the project advances; describe existing or potential competitors and competing technologies; and demonstrate the potential to attract private capital such as venture capital.

CHIPS R&D strongly encourages applicants to identify approaches to maximizing market advantages of the funded innovation, such as by reducing manufacturing costs and improving yields (e.g., optimizing process times and achieving economies of scale through increasing volume). Other approaches could include addressing performance, availability, conformance to technical standards, and environmental sustainability.

CHIPS R&D further encourages applicants to outline mechanisms (which may include licensing strategies) to encourage domestic adoption, deployment, and integration of the funded innovation into domestic manufacturing processes and supply chains. Additionally, applicants should address any barriers or challenges that may impede U.S. manufacturer access or utilization of the funded innovation and propose strategies to overcome them.

Finally, CHIPS R&D recognizes the importance of preventing the illicit exfiltration of funded innovations, including software, in order to protect competitive advantage. Successful CVDP plans may therefore also consider security and compliance measures to mitigate risks associated with the unauthorized access to the funded innovation, which may include encryption, access controls, authentication mechanisms, and adherence to relevant cybersecurity standards and regulations.

1.8 BROADER IMPACTS

CHIPS R&D is committed to building strong communities that share in the prosperity of the semiconductor industry, as well as ensuring that taxpayer investments maximize benefits for the U.S. economy. CHIPS R&D also strongly supports inclusion, diversity, equity, and access and firmly believes that the semiconductor industry cannot succeed unless all Americans have an opportunity to participate, including individuals from underserved communities. In its concept paper and full application evaluation (Sections 5.1 and 5.3) and selection (Sections 5.2 and 5.4) processes, CHIPS R&D will consider how projects will create broader impacts across the dimensions discussed below.

1.8.1 Commitments to Future Investment

Ensuring U.S. leadership in semiconductor technology and the security and resilience of the domestic semiconductor supply chain will require sustained capital, R&D, and workforce investments. CHIPS R&D encourages applications that can induce larger-scale, private investments into domestic prototyping facilities and equipment that would not have occurred absent an award under this NOFO. CHIPS R&D encourages applications that demonstrate collaborations across the supply chain to clarify future demand, improve transparency and security, mitigate the risk of future chip shortages or oversupply, and support a more productive, efficient, and self-sustaining semiconductor ecosystem. In evaluating applications for award, CHIPS R&D will therefore prioritize applications that include credible commitments, from the applicant or other entities participating in the project, to investing in R&D or semiconductor substrate manufacturing in the United States, as evidenced by, for example, letters of commitment or interest.

1.8.2 Support for other R&D Programs

Strengthening the role of the United States in semiconductor technology requires a robust and collaborative innovation ecosystem. Applicants should help ensure that this innovation ecosystem – critical to the semiconductor industry's long-term success – can flourish. CHIPS R&D will favorably consider applications that demonstrate a commitment to participating in the NSTC, the NAPPF, and, if applicable, other semiconductor-related R&D initiatives established by the CHIPS Act[24] or the CHIPS and Science Act[25]. These initiatives may include but are not

[24] For the purposes of this NOFO, the term "CHIPS Act" refers to Title XCIX of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021, as amended (United States Code Title 15 Chapter 72A).
[25] For the purposes of this NOFO, the "CHIPS and Science Act" refers to Public Law 117-167 that provides funds to support the domestic production of semiconductors and authorizes various programs and activities of the Federal science agencies.

limited to the CHIPS Manufacturing USA Institute focused on digital twins for the semiconductor industry; NIST Metrology research for microelectronics; the NSTC Workforce Center of Excellence; the Department of Defense (DoD) National Network for Microelectronics Research and Development, also known as the Microelectronics Commons; semiconductor education activities led by the National Science Foundation (NSF); and other Federally-funded initiatives such as the DARPA Next Generation Microelectronics Manufacturing (NGMM) , DoD Strategic Transition of Microelectronics to Accelerate Modernization by Prototyping and Innovating in the Packaging Ecosystem (STEAM PIPE), and NSF Future of Semiconductors (FuSe2) programs. Further details will become available as these organizations develop their operational plans and membership programs.

Examples of possible collaborative activities include:

- Rotate project technical staff to the NSTC or train NSTC technical staff through exchanges;
- Provide process data to the NSTC to support aggregated large-scale datasets for training and manufacturing process optimization;
- Provide access to existing R&D facilities either as affiliated partners of the NSTC, the Microelectronics Commons, ongoing NSF programs, or independently;
- Provide the NSTC, NAPPF, CHIPS Manufacturing USA Institute, or Microelectronics Commons with donations of or access to equipment and/or design tools;
- Increase domestic public and industry access to process design kits to foster IP development, training and education, and improve foundry interoperability;
- Make data from design, metrology and process tools available for use in developing and evaluating digital twins;
- Make APIs from metrology and process tools available for use in developing and evaluating digital twins;
- Make data from the design, fabrication and testing of utility chiplets available for use in developing and evaluating digital twins;
- Make design and process models available for use in developing and evaluating digital twins;
- Design new data gathering systems and design and process models for use in parametric studies and capable of closed-loop iteration of design parameters to improve overall performance or yield;
- Work with other research teams to develop utility chiplet interfaces that are serialized and use a shared communications protocol and approach to streamline data gathering and facilitate data merging and comparisons; and
- Coordinate and collaborate to the fullest extent possible with the CHIPS Manufacturing USA Institute, which may include negotiating terms to share proprietary data.

1.8.3 Creating Inclusive Opportunities

The CHIPS for America program strives for the inclusion of a broad array of partners, such as educational institutions, small businesses, minority-owned businesses, veteran-owned

businesses, and women-owned businesses.[26] CHIPS R&D will favorably consider applications that, for instance:

- Outline robust outreach plans and demonstrate the inclusion of a broad array of partners in the funded activities proposed under this NOFO, such as the businesses described above, as well as educational institutions (public, private, Historically Black Colleges and Universities (HBCUs), Minority Serving Institutions (MSIs), tribal colleges, etc.);
- Include meaningful leadership opportunities for early career researchers, including individuals from underserved communities, and for emerging research institutions; and
- Provide specific plans for training programs that expand opportunities for participation, including for underserved communities, such as building recruitment partnerships with community-based organizations that have a track record of serving underserved communities, investing in pre-apprenticeship programs, investing in supportive services such as childcare, transportation, and housing where appropriate and feasible, and promoting a safe and respectful workforce culture that prevents harassment and discrimination.

1.8.4 Environmental Responsibility

CHIPS R&D understands that semiconductor companies can reduce their environmental impact, improve the potential for domestic production, and further their competitive advantage by helping their customers meet sustainability and environmental goals. CHIPS R&D will favorably consider applications that identify metrics and milestones that demonstrate the capability of funded technologies to improve upon environmental outcomes of current methodologies and minimize the potential for adverse impacts on health, the environment, and the local community, including communities with environmental justice concerns, such as by reducing or eliminating the use of PFAS. Applicants are encouraged to incorporate strategies for pollution prevention, energy efficiency, water efficiency, and renewable energy use in their project approach. More detailed information on sustainability principles is articulated in programs such as the OSTP AI Aspiration for Sustainable Materials, the OSTP Subcommittee for Microelectronics Leadership National Strategy on Microelectronics Research, technical papers generated by the SIA PFAS Consortium, industry commitments, and upcoming regulations. This focus is imperative for both national and economic security.

The Department expects applicants to design their projects so that they avoid, minimize, and mitigate the potential for significant effects on the human environment. While construction activities are not an eligible use of funds under this NOFO, certain activities may be subject to various Federal, state, and local environmental and permitting requirements, such as under the National Environmental Policy Act (NEPA), National Historic Preservation Act (NHPA), Endangered Species Act, Clean Water Act, Clean Air Act, Resource Conservation and Recovery Act, and related Executive Orders. Applicants must assist the Department with compliance with the above requirements and, where applicable, are responsible for obtaining and complying with Federal, state, and local permits.

[26] See Exec. Order No. 14080, 87 Fed. Reg. 52,847 (Aug. 25, 2022).

CHIPS R&D will review full applications to determine whether they provide sufficient information to support NEPA and NHPA reviews, and may, at its discretion, request the applicant to provide additional information. The Department may request that an applicant prepare draft environmental analyses, which it will review to determine the potential environmental impacts and consultation needs of proposed activities under consideration in connection with a Federal award made under this NOFO. CHIPS R&D may also request further supplementary written information or may ask questions during pre-selection interviews and/or site visits. CHIPS R&D will not issue an award until any environmental review required under NEPA for that award has been completed.

1.8.5 Community Impact and Support

CHIPS for America aims to ensure that its semiconductor manufacturing incentives build strong communities that participate in the prosperity of the semiconductor industry, grow the U.S. economy, and support the creation of good jobs, such as those with working conditions consistent with the Good Jobs Principles. CHIPS R&D efforts can complement these goals by further strengthening or expanding regional semiconductor manufacturing and innovation ecosystems, including by facilitating the development of new or existing regional semiconductor industry clusters.[27] CHIPS R&D will favorably consider applications that demonstrate the impact of the project on regional ecosystems—such as through their creation of Good Jobs, including for individuals from underserved communities—either as a direct consequence of the project or by virtue of the anticipated research results. Project activities do not necessarily need to be completed within a specific geographic area to demonstrate an impact on a regional semiconductor industry cluster.

Applicants or members of project teams seeking to demonstrate community impact and support, including impact on a new or existing regional semiconductor industry cluster, can do so in a variety of ways, as relevant to the objectives and funded activities proposed under this NOFO, including through:

(1) Letters of commitment or interest from community-based organizations and local officials;
(2) Letters of commitment or interest submitted by semiconductor and/or supply chain companies with operations or facilities in the selected region or in a relevant regional semiconductor industry cluster;
(3) Letters of commitment or interest submitted by potential customers and/or other stakeholders;
(4) Letters of commitment or interest submitted by labor organizations;
(5) Cost share from third parties and philanthropies;
(6) Partnerships with State, local, Tribal, and territorial governments and with institutions of higher education in the selected region;
(7) Partnerships with entities focused on innovation, entrepreneurship, access to capital, and technology commercialization in the selected region;

[27] See Executive Order 14080, 87 Fed. Reg. 52847 (Aug. 25, 2022).

(8) Partnerships with minority-owned businesses, veteran-owned businesses, women-owned businesses, Minority-serving Institutions (MSIs), including Historically Black Colleges and Universities (HBCUs), Tribal Colleges and Universities (TCUs), Hispanic Serving Institutions (HSIs), Asian American/Pacific Islander Institutions, and organizations that serve underserved communities; and
(9) Alignment with regional, state, or local economic development strategies, assets, resources, or capacities, such as relevant Comprehensive Economic Development Strategies,[28] regional or cluster-based growth efforts, or other complementary Federal investments under programs such as the DOC Build Back Better Regional Challenge (BBBRC).[29] DOC Regional Technology and Innovation Hub (Tech Hubs) program,[30] or NSF Regional Innovation Engines program,[31] including through strong, concrete commitments to such programs' consortia and participation in consortium/coalition governance.

1.9 PROJECT COORDINATION

CHIPS R&D intends that activities funded under this NOFO will help establish a vibrant, self-sustaining, profitable, domestic advanced packaging industry in the United States. This requires modular research outputs tailored for use in combinations that enable end-to-end advanced packaging flows. Successful research products are expected to contribute to the NAPPF through standardization and technology transfer into the NAPPF packaging fabrication flows. For example, chiplet designs by one research team must be compatible with the scale-down targets of other research teams creating substrates to which those chiplets are to be attached. New packaging equipment created by one set of research teams must not only be able to work together in integrated packaging flows, but also handle new power delivery and thermal management solutions created by other research teams to enable advanced 3D architectures. To achieve compatibility and interoperability across research outputs, close coordination across all funded projects is needed to ensure that:

- Individual projects are not conducted in isolation and are not producing siloed outputs incompatible with advances from others;
- Research is responsive to real industry needs, including addressing identified gaps in domestic packaging capabilities; and
- Information is shared among projects with known interdependencies with appropriate protection for the performers' intellectual property.

CHIPS R&D will work closely with successful applicants to coordinate activities across funded projects. Applicants must plan for participation in these coordination activities, including the following:

- Ongoing and frequent meetings between project participants and NAPMP staff to share information about project status, known interdependencies, and relationships with other ongoing work;

[28] https://www.eda.gov/resources/comprehensive-economic-development-strategy
[29] https://www.eda.gov/funding/programs/american-rescue-plan/build-back-better
[30] https://techhubs.gov
[31] https://new.nsf.gov/funding/initiatives/regional-innovation-engines

- Regular events bringing together all project teams to share information, coordinate efforts, and seek opportunities for cooperation and collaboration;
- Events convening the broader semiconductor community, including industry and academia, along with project teams to assess technology trends and the evolving needs of the community; and
- Research exchange opportunities in which experts from one project work for defined intervals in other projects to promote coordinated and well-integrated efforts, particularly where there are close interdependencies across the intended research outputs.

Planning for participation in these coordination activities must include prioritizing participation in coordination events, with appropriate protections under negotiated IP sharing and/or licensing agreements, and including in project budgets anticipated costs for participation in coordination activities.

1.10 PROJECT ASSESSMENTS

Throughout the program, CHIPS R&D retains sole discretion to determine whether a recipient has achieved phase-specific targets (including technical, education and workforce development, and commercial viability and domestic production targets). Similarly, CHIPS R&D has the sole discretion regarding whether the recipient has met the requirements for each project-level and phase-specific target.

In making this judgment, CHIPS R&D may, as appropriate to the project phase, consider information provided by the recipient, including an assessment of project outputs, including demonstration devices. Assessments of project outputs may be conducted, at CHIPS R&D's sole discretion, by CHIPS R&D or by an independent evaluator, with appropriate protections under negotiated IP sharing and/or licensing agreements.

Based on the results of CHIPS R&D assessments of project outputs, such as demonstration devices and systems, equipment and tools, and design documentation; evaluation of overall progress; availability of funding; and continued alignment with CHIPS R&D priorities, CHIPS R&D, at its sole discretion, may decide at the end of each phase to proceed with the next increment of funding, request a revised plan from the recipient (subject to the constraints of the approved award scope and budget and CHIPS R&D approval), or terminate funding for the project.

1.11 GOVERNMENT-FURNISHED PROPERTY (GFP) AND GOVERNMENT FURNISHED INFORMATION (GFI)

Under this NOFO, no GFP or GFI is identified to be provided at this time. Availability will be determined for each award on a case-by-case-basis.

2 FEDERAL AWARD INFORMATION

2.1 FUNDING INSTRUMENT

Awards in this program will be made as other transaction agreements (OT), as authorized by 15 U.S.C. § 4659(a)(1), which provide the Department the flexibility to create award agreements reflecting the unique, innovative nature of this program.

2.2 MULTI-YEAR FUNDING POLICY

When an application for a multi-year award is approved, funding will be provided only for the first phase of the project; additional phases will be funded incrementally. If a project is selected for funding, CHIPS R&D has no obligation to provide any additional funding in connection with that award. Funding for subsequent phases of a project will be contingent upon satisfactory performance of the terms and conditions of the award, as determined by CHIPS R&D, continued relevance to the mission, goals, and priorities of the CHIPS R&D, and the availability of funds.

2.3 FUNDING AVAILABILITY

CHIPS R&D anticipates making available up to approximately $1,550,000,000 for funding multiple awards of varying size and scope, with anticipated amounts ranging from approximately $10,000,000 to approximately $150,000,000 in Federal funds per award over a five (5) year period of performance. Anticipated maximum award sizes and total funding per R&D Area are as follows:

R&D Area	Total Funding	Anticipated Maximum Award
Equipment, Tools, Processes, and Process Integration	$450M	$150M
Power Delivery and Thermal Management	$250M	$50M
Connector Technology, Including Photonics and Radio Frequency	$250M	$100M
Chiplets Ecosystem	$300M	$75M
Co-design/Electronic Design Automation	$250M	$100M

CHIPS R&D anticipates reserving up to $50,000,000 to support recipients under this NOFO pursuing prototyping activities, to be awarded once the NAPMP NAPPF has established a baseline capability. Prototypes will focus on application areas such as high-performance computing and low-power systems needed for AI. Funding for prototyping activities will be executed as add-on projects to existing awards, based on information that will be requested by CHIPS R&D at a later date.

2.3.1 Eligible Uses of Funds

Eligible uses of funds include basic and applied research; systems, equipment, tools, and software systems development and production as appropriate to the R&D area; commercial viability analyses and domestic production preparation; integrated education and workforce

development; and prototype production. Where consistent with the objectives of this NOFO, applicants may also propose to expend limited funds to protect innovations developed under this NOFO, including to cover fees for patent protection or to enhance research security.

2.4 INDIRECT (F&A) COSTS

CHIPS R&D will reimburse applicants for proposed indirect costs, commonly referred to as Facilities & Administrative (F&A) Costs, in accordance with this subsection. Applicants with a current negotiated indirect cost rate may use up to their Federally approved indirect rate to budget indirect costs. Alternatively, applicants that do not have a current negotiated (including provisional) indirect cost rate may elect to charge a de minimis rate of 15 percent of modified total direct costs (MTDC). Applicants proposing indirect costs must follow the application requirements set forth in Sections 4.6.1.8 and 4.6.1.9 of this NOFO.

2.5 PUBLIC ACCESS TO CHIPS R&D RESEARCH

NIST is committed to the principle that the results of Federally funded research are a valuable national resource and a strategic asset. To the extent feasible and consistent with law, agency mission, resource constraints, and U.S. national, homeland, and economic security, NIST will promote the deposit of scientific data arising from unclassified research and programs, funded wholly or in part by NIST, except for Standard Reference Data, free of charge in publicly accessible databases. Subject to the same conditions and constraints listed above, NIST also intends to make freely available to the public, in publicly accessible repositories, all peer-reviewed scholarly publications arising from unclassified research and programs funded wholly or in part by CHIPS R&D.

All applications for activities that will generate research data (see 2 C.F.R. § 200.315(e)(3)) using Federal funds awarded under this NOFO are required to adhere to a Data Management Plan (DMP) or explain why data sharing and/or preservation are not within the scope of the project (see Section 4.6.1.12).

2.6 FUNDAMENTAL RESEARCH

National Security Decision Directive (NSDD) 189 defines "fundamental research" as follows:

> *'Fundamental research' means basic and applied research in science and engineering, the results of which ordinarily are published and shared broadly within the scientific community, as distinguished from proprietary research and from industrial development, design, production, and product utilization, the results of which ordinarily are restricted for proprietary or national security reasons.*[32]

Funded activities under this NOFO may include efforts categorized as fundamental research. In submitting an application, the applicant acknowledges that research activities considered to be

[32] National Security Decision Document 189, "National policy on the transfer of scientific, technical and engineering information." September 21, 1985.

fundamental research may include or produce IP with relevance to U.S. national or economic security and that requires protection against foreign interference and exploitation. As such, the applicant and any subrecipients agree to comply with the research security requirements described in Section 0 of this NOFO.

2.6.1 Fundamental Research Declaration

NIST/CHIPS reserves sole discretion to determine which elements of a proposed research project shall be considered fundamental research. However, applicants must indicate in the Project Narrative (see Section 4.6.1.6) whether, in the applicant's understanding, the proposed work includes fundamental research conducted either by the applicant or by subrecipient members of the project team.

2.6.2 On-Campus Research

Wherever feasible, NIST/CHIPS will seek to consider basic or applied research conducted on campus at a university as fundamental research.

2.6.3 Pre-Publication Reviews

Awards made under this NOFO that include fundamental research will include appropriate language reaffirming the ability of the applicant and members of the project team to publish and share broadly the results of such fundamental research.

Awards made under this NOFO that include research not deemed fundamental will prescribe publication requirements and other restrictions, as appropriate, for such research. This may include requirements for the applicant to submit publications describing work carried out under this program for an efficient pre-publication review by NIST/CHIPS. The pre-publication review may result in a request for revisions to address national security concerns. The pre-submission review may also include an assessment of and advice to the award recipient regarding whether information disclosed in the publication could negatively impact the patent interests of either the award recipient or the Government.

2.7 RESEARCH SECURITY

It is NIST policy to create a culture of personal and organizational responsibility where the practice and management of research and its products are free from undue influence and interference not essential to the practice of science, such as personal or social allegiances, beliefs, or interests. NIST adheres to the principle that U.S. research leadership benefits from mutually beneficial international collaborations, including welcoming international scientists, and that U.S. national and economic security depends on effective risk management practices for all research organizations to protect against foreign interference and exploitation.

Founded on NIST's core values of perseverance, integrity, inclusivity, and excellence, the NIST Research Security Team promotes mutually beneficial international engagement using a risk-based methodology to safeguard NIST research programs and intellectual property.

2.7.1 Research Security Definitions

Unless otherwise noted, the definitions for terms used in this section are found in the Appendix to Guidance for Implementing National Security Memorandum 33 (NSPM-33) on National Security Strategy for United States Government-Supported Research and Development issued by the National Science and Technology Council in January 2022 (NSPM-33 Guidance).

2.7.2 Authorities

In recent years, both Congress and the Executive Branch have focused on protecting R&D conducted or funded by Federal agencies from undue foreign influence. On January 14, 2021, National Security Presidential Memorandum-33 (NSPM-33) was issued to "strengthen protections of United States Government-supported R&D against foreign government interference and exploitation." NSPM-33 requires U.S. agencies that fund R&D to require the disclosure of information related to potential conflicts of interest and commitment from participants in the Federal R&D enterprise.

Under Section 223 of Division A, Title II of the William M. (Mac) Thornberry National Defense Authorization Act (NDAA) for Fiscal Year 2021 (FY21), (Pub. L. No 116–283, codified at 42 U.S.C. § 6605), "covered individuals" (see Section 2.7.4) must disclose the amount, type and source of all current and pending research support, which includes both monetary and non-monetary support, and certify that the disclosure is current, accurate, and complete as part of the application for an R&D award. In addition, covered individuals must agree to update disclosures, as required, before and during the term of the award.

Subtitle D of Title VI of the Research and Development, Competition, and Innovation Act, enacted along with the CHIPS and Science Act of 2022, codified at 42 U.S.C. § 19231-19237, also contains research security requirements. On February 14, 2024, the Office of Science and Technology Policy (OSTP) defined the term "foreign talent recruitment program" in issuing Guidelines for Federal Research Agencies Regarding Foreign Talent Recruitment Programs required under 42 U.S.C. § 19231(b). Also, on July 9, 2024, OSTP released Guidelines for Research Security Programs at Covered Institutions.

The research security provisions in this NOFO are consistent with all authorities cited in this section, as applicable.

2.7.3 Requirement for a Research Security Plan or Program

Applicants to this NOFO must submit a written plan (see Section 4.6.1.6)—

(1) identifying a member of applicant's leadership team to serve as the point of contact responsible for coordinating with NIST on research security issues;
(2) describing internal processes or procedures to address foreign talent recruitment programs (as referenced in Section 2.7.5), conflicts of commitment, conflicts of interest, research security training, and research integrity;

(3) describing measures taken to ensure that appropriate practices for cybersecurity, such as the NIST Cybersecurity Framework and Cybersecurity and Infrastructure Security Agency (CISA) Cybersecurity Performance Goals (CPGs), are incorporated in the project.
(4) listing any relevant certifications in place or plans to obtain such certifications (e.g., FCL, CMMC) and standards they follow (e.g. ISO/IEC 27001, ISO 8000-51).

Pursuant to the authorities described above, for any applicant that meets the definition of a "covered institution,"[33], the Research Security Plan must further describe its intent to establish and operate a Research Security Program (see Section 0). Applicants can refer to the CHIPS R&D Research Security and Technology Protection web page for additional information.

In August 2023, NIST published the Safeguarding International Science: Research Security Framework (NIST IR 8484), which provides (1) guidance on establishing a successful Research Security Program; (2) background information related to research security generally; and (3) methodologies and requirements for an integrated, mission-focused, risk-balanced approach for safeguarding international science and technology from undue foreign interference while protecting the openness and integrity of the U.S. research ecosystem. In addition, CHIPS R&D published a companion document, the CHIPS Technology Protection Guidebook, as a resource for implementing applicant and performer research security requirements.

Upon review of the applicant's Research Security Plan NIST may provide the applicant with feedback and an opportunity to refine the Plan, as described in Section 2.7.9.

By submitting an application under this NOFO, an applicant—regardless of its status as a "covered institution"—acknowledges that, if preliminarily selected for an award, it has the capacity to demonstrate, prior to receipt of the award, that CRDO-funded research and associated data products will be protected. The applicant further acknowledges that NIST/CHIPS may deem implementation of certain elements of a research security plan as a condition of the award.

2.7.4 Covered Individuals

For the purposes of this NOFO and as defined under 42 U.S.C. § 6605(d)(1), the term "covered individual" is defined as "an individual who (1) contributes in a substantive, meaningful way to the scientific development or execution of a research and development project proposed to be carried out with a research and development award from a Federal research agency; and (2) is designated as a covered individual by the Federal research agency concerned."

[33] The July 9, 2024, OSTP Guidance defines "covered institution" as an institution
(A) of higher education, a federally funded research and development center (FFRDC), or a nonprofit research institution; and
(B) that receives in excess of $50 million per year, in fiscal year 2022 constant dollars, under
(1) the three-year average of federal R&D obligations provided to participants in the U.S. R&D enterprise as reported in the most recent version of the Survey of Federal Science and Engineering Support to Universities, Colleges, and Nonprofit Institutions; or
(2) the three-year average of federal R&D obligations to FFRDCs as provided in the most recent versions of the Survey of Federal Funds for Research and Development.

In developing the Project Narrative required under Section 4.6.1.6, the applicant must determine and identify which individuals are covered individuals and provide a brief description (title or one-sentence summary) of the role to be served by each covered individual. Applicants must also complete the Current and Pending Support Forms required under Section 4.6.1.13.

Covered individuals should include the Project Director; any identified principal investigators, co-investigators, and associate investigators; and any individual listed under Section 4.6.1 by the applicant as "key personnel" or as a "Senior/Key Person" or for whom a resume or CV is included. Personnel who participate only through isolated tasks that are incidental to the research (for example, setting up equipment or performing administrative functions) and those individuals who support research by executing discrete tasks as directed are not covered individuals. Consistent with guidance for implementing NSPM-33, disclosures from broader classes of individuals (e.g., certain graduate students and undergraduate students) will generally be unnecessary, except when the activities of such an individual in a specific proposal rise to the level of meeting the definition of a "covered individual" under 42 U.S.C. § 6605(d)(1).

2.7.5 Foreign Entities of Concern

Pursuant to 15 U.S.C. § 4657, no Federal funds awarded under this NOFO may be provided to a foreign entity of concern, as defined in 15 U.S.C. § 4651(8) and implemented by the final rule entitled Preventing the Improper Use of CHIPS Act Funding, 88 FR 65600 (Sept. 25, 2023), codified at 15 C.F.R. § 231.104. Foreign entities of concern are also ineligible to participate in this NOFO as unfunded collaborators.

To ensure compliance with this requirement, applicants to this NOFO must submit a Written Summary of Certain Research Partnerships or Technology Transfer Commitments (See Section 4.6.1). This document should describe any research partnerships or technology transfer commitments in areas relevant to the activities within this NOFO or any other areas related to the mission and goals of CHIPS R&D (see Section 1.1.1) between the applicant entity and (a) any entities located in a foreign country of concern or (b) with any entities that are foreign entities of concern.[34]

2.7.6 Research Security Review and Risk Determination

The NIST Research Security Team will conduct a preliminary research security review and a risk determination of concept papers initially identified for invitation to full application and may conduct a subsequent review and risk determination of submitted full applications. During the review, NIST will use NIST IR 8484 as the basis for reviewing and assessing research security risks. In conducting this review, NIST will review available information (e.g., the Current and Pending Support Form and Resume or CV) to assess whether the applicant or any covered individuals, including foreign nationals who are not lawful permanent residents or protected persons as defined in 8 U.S.C. § 1324b(a)(3), are subject to any undue foreign influence or interference through conflicts of interest or conflicts of commitment. Undue foreign influence or interference may include, but is not limited to, associations or affiliations with foreign strategic

[34] Covered Individuals should separately detail potential research activities or technology transfer commitments within their Current and Pending Support forms

competitors or governments of countries that have a history of intellectual property theft, research misconduct, or targeting U.S. technology for unauthorized transfer. Affiliations include any past or present organization (foreign and domestic) with whom the applicant has a formal relationship or obligation (e.g., universities, scholarships, professional societies, foreign talent recruitment programs).[35] NIST will examine associations or affiliations during the ten-year period immediately preceding the application submission.

At the conclusion of the research security review for the application, NIST will issue a determination of low, medium, or high risk. NIST will base its risk determination of the proposal on the totality of information, which may include but is not limited to:

1. The ownership structure, subsidiaries, and obligations of the applicant, the project team (including subrecipients, contractors, and/or unfunded collaborators);
2. Conflicts of interest and conflicts of commitment of covered individuals;
3. Participation of covered individuals in a foreign talent recruitment programs; and
4. Any military-civil applications of the funded research, as applicable.

Regardless of the risk determination and at its sole discretion, NIST may request clarifying information, or work with the applicant to mitigate the assessed risks (see Section 2.7.8). NIST may contact the applicant at any time after submission of its concept paper or full application to seek relevant clarifications or risk mitigation including during the merit review or evaluation process.

2.7.7 Non-Discrimination

Consistent with Section 10637 of the CHIPS and Science Act of 2022 and Executive Orders 13985 and 14031, NIST activities that implement NSPM-33 and 42 U.S.C. § 6605 are carried out in a manner that does not inadvertently target, stigmatize, or discriminate against individuals on the basis of race, color, ethnicity, religion, sex (including pregnancy, sexual orientation, or gender identity), national origin, age (40 or older), disability, and genetic information (including family medical history), consistent with title VI of the Civil Rights Act of 1964 (42 U.S.C. § 2000d et seq.).

2.7.8 Potential for Mitigation

NIST may, at its sole discretion, provide the applicant an opportunity to mitigate any assessed risks prior to CHIPS R&D making a final determination to select either the concept paper or full application. NIST/CHIPS R&D reserves the right to request specific mitigation actions, including but not limited to requiring additional training for project participants or segmentation of certain tasks of the proposed work, and any follow-up information needed to assess risk or mitigation strategies. CHIPS R&D may determine not to make an award despite any proposed mitigation terms in connection with an application.

2.7.9 Requirement for Recipients to Update Research Security-Related Information

[35] See OSTP Guidelines for Federal Research Agencies Regarding Foreign Talent Recruitment Programs.

Pursuant to 42 U.S.C. § 6605(a)(1)(C), applicants have an ongoing duty to update the NIST Agreements Officer of any changes made to the list of covered individuals or to the foreign affiliations and research financial and in-kind support of such individuals or of the applicant and subrecipients. Prior to NIST making an award under this NOFO, applicants must update the NIST Agreements Officer of any such changes immediately; during a project's period of performance, award recipients must update the NIST Agreements Officer within five (5) business days of such changes being made or of becoming aware of such changes.

Applicants and subrecipients are expected to reasonably exercise due diligence to ensure that covered individuals involved in the subject award are not subject to foreign interference or exploitation.

2.8 Intellectual Property (IP) and Domestic Production

As set forth in 15 U.S.C. § 4656(g), the Department of Commerce must "develop policies to require domestic production, to the extent possible, for any intellectual property" resulting from R&D conducted using Federal funds awarded under this NOFO. Further, 15 U.S.C. § 4656(g) requires CHIPS R&D to develop domestic control requirements to protect any such IP (which may include software) from foreign adversaries. For the purposes of 15 U.S.C. § 4656(g), "intellectual property" means any invention that is or may be patentable under U.S. law; and "foreign adversaries" include any "foreign entity of concern" and "foreign country of concern," as those terms are defined in 15 U.S.C. § 4651(7)-(8) and 15 C.F.R. §§ 231.102, 231.104, as well as any entity whose actions, policies, or personnel decisions are controlled by a "foreign entity of concern" or "foreign country of concern."

2.8.1 Domestic Production

For the purposes of 15 U.S.C. § 4656(g), "production" includes the manufacture, integration, assembly, testing, and packaging of semiconductors, materials used to manufacture semiconductors, or semiconductor manufacturing equipment developed or improved as a result of CHIPS-funded intellectual property.

Applicants for an award under this NOFO should describe their intent to maximize domestic production in the CVDP and, as appropriate, Intellectual Property Rights Management Plan. CHIPS R&D does not require the covered production to occur exclusively within the United States. However, applicants that are unable to conduct certain production activities in the United States should explain within their CVDP, to the extent practicable at the current level of technology development, why such production may not be possible, considering the following factors:

- The availability or lack of availability of domestic production capabilities, which may consider:
    - Planned or previous efforts made to locate, develop, or contract for the production of the CHIPS R&D-funded technology, or relevant similar technologies, in the United States;
    - Access to resources and other material inputs required for production;

    - The expected additional product development time or cost required to make U.S. production of the CHIPS R&D-funded technology commercially feasible;
- The relative costs of domestic versus foreign production of the CHIPS R&D-funded technology at relevant production volumes;
- Commercial adoption risks and benefits, such as
    - Risks to the market acceptance and to the value proposition for the CHIPS-funded technology resulting from U.S. production;
    - Expected commercial, economic, or national security benefits to the United States resulting from distributed production among U.S. and overseas sites; and
- Any other factors that are important to the success of the CHIPS R&D-funded technology.

Applicants should be aware that this assessment of domestic production may be an initial assessment, with updates occurring across the award period.

2.8.2 Domestic Control

To meet the requirements of 15 U.S.C. § 4656(g), CHIPS R&D will include special award terms and conditions related to intellectual property and domestic control. The relevant terms and conditions will include, at a minimum, the following:

(1) At least one domestic entity must own or co-own any intellectual property resulting from R&D (e.g., applicant or sub-recipient) conducted under this NOFO ("resulting intellectual property") and must have full rights to enforce the applicable intellectual property rights, at least for a period of years to be determined prior to the final award.
(2) At the conclusion of the period of years, ownership of the resulting intellectual property may generally be sold, transferred, or assigned to a foreign entity that is not a foreign adversary.
(3) In the event a domestic entity sells, transfers, or assigns ownership of the resulting intellectual property, the entity must promptly disclose such transaction to NIST prior to such transaction.
(4) Any owner or co-owner of the resulting intellectual property (including successors in interest) may not sell, transfer, or assign ownership of such intellectual property to a foreign adversary.
(5) Any owner of the resulting intellectual property may not license such intellectual property to a foreign adversary, subject to the following specific exceptions.
    a. This restriction is not applicable to the following specific exceptions, provided that an owner or co-owner of any patent or patent application resulting from R&D conducted under this NOFO satisfies the notification requirement specified in 5.a.iii below.
        i. This restriction is not applicable to any patent(s) or published patent application(s) (i) declared and/or determined to be essential to a technical standard and (ii) under an obligation that the owner of the patent or published patent application license such rights pursuant to the terms of a standards development organization's Intellectual Property Rights policy.

ii. This restriction is not applicable to any license(s) of patent(s) or published patent application(s), including cross-licenses, resulting from settling an actual case or controversy, including patent infringement or validity disputes, whether part of a formal proceeding or not.
iii. In the event an owner or co-owner of the patent(s) resulting from R&D conducted under this NOFO determines that any of the specific exceptions above applies and plans to license such patent(s) to a foreign adversary pursuant to the exception(s), the owner or co-owner must promptly disclose such action for NIST review.

b. This restriction is not applicable to the sale of a product by a funding recipient (or any other lawful owner, assignee, transferee or licensee of the IP) and any accompanying implied or explicit intellectual property license relating to the use of the product that is sold.

3 ELIGIBILITY INFORMATION

3.1 ELIGIBLE APPLICANTS

Eligible applicants are domestic non-profit organizations; domestic accredited institutions of higher education; State, local, and Tribal governments; and domestic for-profit organizations. A domestic entity is one that is incorporated within the United States (including a U.S. territory) with its principal place of business in the United States (including a U.S. territory).

Eligible applicants (normally identified by having a separate unique entity identifier in SAM.gov) may submit only one concept paper per R&D area. Each concept paper may only include one R&D Area. Applicants may submit multiple concept papers on different R&D Areas. Following concept paper evaluation, CHIPS R&D will invite and accept full applications from selected applicants only.

Prospective applicants and subrecipients are required to have an active registration in SAM.gov and are encouraged to begin the process of registering as early as possible.

3.1.1 Federally Funded Research and Development Centers

Federally Funded Research and Development Centers (FFRDCs) may participate in awards as subrecipients or as contractors, to the extent allowed by law, based on the unique and specific needs of the project.

Applicants must identify the FFRDC(s) in the Project Narrative and provide documentation attached to the required letter of commitment (see Section 4.6.1.11) establishing that FFRDC subrecipients and contractors are able to participate in the proposed work, including:

1. Documentation demonstrating that the proposed work does not compete with the private sector; and
2. Documentation from the FFRDC's sponsoring institution citing the FFRDC's eligibility to participate in competitive Government funding opportunities, the FFRDC's

compliance with the sponsor agreement, and confirmation from the sponsoring agency that they can receive Federal funds from NIST.

FFRDCs interested in participating in this NOFO should first contact their sponsoring agency to discuss their eligibility to receive Federal funds under this NOFO.

3.1.2 Federal Entities

Federal entities (e.g., Federal departments and agencies, military services educational institutions, etc.) are eligible to participate in this NOFO as subrecipients or contractors, to the extent allowed by law and subject to applicable direct competition limitations. Federal entities must clearly demonstrate that the work is not otherwise available from the private sector and provide written documentation citing the specific statutory authority and contractual authority, if relevant, establishing their ability to receive Federal award funds and compete with industry.

Applicants must identify the Federal entity in the Project Narrative and provide documentation attached to the required letter of commitment (see Section 4.6.1.11) establishing that the Federal entity is able to participate in the proposed work.

3.1.3 Individuals and Unincorporated Sole Proprietors

Individuals and unincorporated sole proprietors are not eligible to receive funding under this NOFO.

3.1.4 Foreign Partners and Foreign Research Activities

Foreign organizations may participate as members of a project team, subrecipients, or contractors, provided that they are not a foreign entity of concern, subject to CHIPS R&D review and approval. In each case, the applicant leading a project must be a domestic entity. For the purposes of this section, a foreign entity is any entity that is not a domestic entity. A domestic entity includes the following: (1) a State, local, or Tribal government in the United States; or (2) any entity that is (a) organized under the laws of the United States or any jurisdiction within the United States and (b) has a principal place of business in the United States.

3.1.4.1 Foreign Partner Justification

Under this NOFO, CHIPS R&D must provide the applicant with written approval for a foreign partner's participation in a funded project prior to the foreign partner engaging in any project-related work. Such participation may include receipt of CHIPS funding, receipt of CHIPS-funded intellectual property, or research activities occurring outside of the United States. The applicant must provide CHIPS R&D with a written justification demonstrating:

1. The foreign partner's involvement is essential to advancing program objectives, such as by offering access to unique facilities, IP, or expertise that is otherwise not readily available in the United States;
2. The adequacy of any agreements and protocols between the applicant and foreign partner regarding IP protection and data protection;

3. The partnership does not jeopardize the soundness of the project's proposed pathway to domestic production;
4. As applicable, the foreign partner will comply with any necessary nondisclosure agreements, security regulations, export control laws, audit requirements, and other governing statutes, regulations, and policies;
5. The foreign partner is not based in a foreign country of concern as defined at 15 U.S.C. § 4651(7) and implemented by the final rule entitled Preventing the Improper Use of CHIPS Act Funding, 88 FR 65600 (Sept. 25, 2023), codified at 15 C.F.R. § 231.104; and
6. The foreign partner agrees to be subject to a security review by CHIPS R&D, which may include a risk assessment of IP leakage, if appropriate.

3.1.4.2 Location of funded activity

While the work funded under this NOFO is to be conducted within the United States, certain tasks outside the United States may be allowed based on the unique and specific capabilities available at the foreign location, their relevance to the project objectives, and the lack of comparable capabilities in the United States. CHIPS R&D's determination regarding the performance of project tasks outside the United States, whether by a domestic entity or by a foreign partner, will be based on information provided by the applicant and by other Federal agencies.

CHIPS R&D will approve work outside of the United States only if it is in the best interest of CHIPS R&D and the United States, including the domestic economy generally, U.S. national security, U.S. industry, and U.S. manufacturing competitiveness.

In making this determination, CHIPS R&D will consider whether the proposed non-domestic activity advances the economic or national security interests of the United States and the justification described in Section 3.1.4.1. CHIPS R&D will not approve the disbursement of funds to an entity in or under the control of a country of concern under any circumstances.

3.2 COST SHARE

3.2.1 Provisions.

Under this NOFO, a non-Federal cost share over the lifetime of an award is strongly encouraged but not required. The non-Federal cost share is that portion of the project costs not borne by the Federal government. Cost share may include cash, services, and third-party in-kind contributions, as described at 2 C.F.R. § 200.306. Applicants may propose other types of cost share, provided that the proposed cost share is necessary and reasonable for accomplishment of the project objectives and approved by NIST.

3.2.2 Allocation.

The source and detailed rationale of the cost share, including cash, full- and part-time personnel, and in-kind donations, must be documented in the Research and Related Budget (Total Fed +

Total Non-Fed) form and Budget Narrative and Justification submitted as part of the full application and may be considered as part of the review described in Section 5 of this NOFO. As with the Federal share, any cost share specifically pledged on a voluntary basis in the applicant's proposed budget will become a binding requirement of any Federal award. Cost share must be allowable/eligible costs under this program and under the applicable cost principles per Section 3.3. The value of any cost share to be provided by any subrecipients may be determined using Generally Acceptable Accounting Principles (GAAP). For instructions on incorporating cost share into the Research and Related Budget (Total Fed + Total Non-Fed) form and the Budget Narrative and Justification, see Section 4.6.1.8.

3.3 ALLOWABLE COSTS

For purposes of submitting an application, allowable costs are generally determined in accordance with cost principles similar to those identified at 2 C.F.R. Part 200 Subpart E. For final award costs, NIST may, in its sole discretion, accept costs that would not be allowable under 2 C.F.R. Part 200, Subpart E, provided that the proposed costs are allocable to and necessary for the success of the project and approved in writing by NIST.

4 APPLICATION AND SUBMISSION INFORMATION

4.1 OVERVIEW

The application process consists of a mandatory concept paper and a required full application. Full applications will be accepted only from applicants that are invited after the concept paper stage.

Eligible applicants may submit only one concept paper and one full application, where invited, per R&D area (see Section 1.4.3 for a list of R&D areas) under this NOFO. See Section 3 regarding eligibility requirements.

CHIPS R&D may make changes or additions to this NOFO at any time, including, for example, adjustments to submission dates, times, or other requirements. All changes will be communicated through Grants.gov. CHIPS R&D may also close the NOFO with at least 60 days' notice.

All submissions must be unclassified. The Government will not reimburse applicants for any costs associated with participation in this NOFO. Likewise, the cost of preparing concept papers and full applications in response to this NOFO is not an allowable charge (direct or indirect) under any Federal award.

4.2 ADDRESS TO REQUEST APPLICATIONS PACKAGE

The application package for concept papers and full proposals is available at Grants.gov under Funding Opportunity Number 2025-NIST-CHIPS-NAPMP-01.

4.3 PAGE COUNT GUIDANCE

This NOFO identifies strict limitations on page counts for the concept paper and full application. As part of its initial administrative review, CHIPS R&D will redact any pages received in excess of the stated page limits prior to beginning the merit review. The applicant should refer to Tables 16 and 17 to determine which documents and forms are included and excluded in page count limits for concept papers and full applications, respectively.

4.4 SUBMISSION FORMAT

Applicants should follow the guidance and information provided at Grants.gov and in Section 4.5 and Section 4.6 for concept paper and full application submissions, respectively, which includes requirements for uploading specific required forms and plans. A concept paper or full application received after the specified due date and time will NOT be considered for an award.

Applicants should carefully follow specific Grants.gov instructions to ensure that all attachments will be accepted by the Grants.gov system. A receipt from Grants.gov indicating that an application has been received does not provide information about whether attachments have been received. For information or questions regarding applying electronically for the 2025-NIST-CHIPS-NAPMP-01 NOFO, contact the Grants.gov Help Desk at 800-518-4726.

Document formatting requirements are specified to ensure the readability of the document by reviewers. Neither the concept paper nor full application should contain any hyperlink references used solely to circumvent any page restrictions. All information critical for the application must be contained within the specified page limits provided in Tables 16 and 17 below for the concept papers and full applications.

4.4.1 Amendments

Any amendments to this NOFO will be announced through https://www.grants.gov and https://www.chips.gov. Applicants may sign up on Grants.gov to receive notification of any amendments by e-mail.

4.4.2 Proprietary and Sensitive Business Information

Applicants must clearly identify proprietary information in their concept papers and full applications. Submissions containing proprietary or sensitive business information must have the cover page and each page containing such information clearly marked with a label such as “Proprietary” or “Sensitive Business Information” and provide an indication as to what specific information is proprietary or sensitive.

Applicants must not submit classified information.

4.5 CONCEPT PAPER INSTRUCTIONS

The required content and form of concept papers submitted pursuant to this NOFO are set forth below.

4.5.1 Required Forms and Documents

4.5.1.1 Standard Form (SF)-424 (R&R), Application for Federal Assistance.

Instructions for completing the SF-424 (R&R) can be found on www.grants.gov, as well as at the NIST Financial Assistance Agreements Management Office SF-424 Research & Related (R&R) Application Package Guidance.

The SF-424 (R&R) must be signed by an authorized representative of the applicant organization.

For SF-424 (R&R), Items 5, 14, and 19, use the Zip Code + 4 format (##### - ####) when addresses are called for.

The list of certifications and assurances referenced in Item 17 of the SF-424 (R&R) is contained in the Federal Financial Assistance Certifications and Representations (Certs and Reps) as part of the SAM.gov entity registration.

4.5.1.2 Cover sheet and additional items

Items a. through e. below must be completed and attached as a single document to Item 20. Pre-application on the SF-424 (R&R).

a. Cover Sheet – The cover sheet is a one-page document providing:

- NOFO Name and Reference Number (2025-NIST-CHIPS-NAPMP-01)
- Concept paper submission date
- Relevant R&D area
- Name of the applicant
- Name of the project director(s)/principal investigator(s)
- Any major subrecipients
- Proposal title – Title must begin with the header "*R&D Area 'n':*" where 'n' is the number from the following list for the corresponding R&D area covered in the proposal. Example for a proposal covering the Chiplets Ecosystem area: "*R&D Area 4: (applicant title text here)*."
    1. Equipment, Tools, Processes, and Process Integration
    2. Power Delivery and Thermal Management
    3. Connector Technology, Including Photonics and Radio Frequency (RF)
    4. Chiplets Ecosystem
    5. Co-design/Electronic Design Automation (EDA)
- Point of Contact for the applicant, to include name, address, telephone number, and business e-mail address
- Total funds requested and total proposed cost share (rough order of magnitude)

- Any statement regarding confidentiality, including proprietary or sensitive business information, if applicable

The cover sheet does not contribute to the concept paper narrative page limit.

Concept Paper Executive Summary – The executive summary is a one (1)-page summary/abstract suitable for dissemination to the public and must not include any classified information or proprietary or sensitive business information. It should be a self-contained document that identifies the name of the applicant, the project director(s)/principal investigator(s), the application title, the objectives of the proposed team, and the intended impacts (i.e., benefits, outcomes) of the proposed project, including both technical and education/workforce goals. The executive summary does not contribute to the concept paper narrative page limit.

Table of Contents (This does not contribute to the concept paper narrative page limit)

Concept Paper Narrative - The concept paper narrative is a word-processed document of no more than ten (10) pages. The concept paper must contain the following to be considered for initial review:

i. Project Impact Statement

- Provide a clear problem statement and well-defined project outcomes, explaining how both are relevant to the CHIPS R&D mission and goals (See Section 1.1.1) and the objectives of this NOFO, as expressed in Sections 1.1.2and 1.1.3.
- Provide a description of the project's contribution to economic and national security, as expressed in the evaluation criteria in Section 5.1.

ii. Project-Level Technical Plan

- Provide an overview of the project plan, including each of the following aspects:
- A description of how the planned project and proposed team contribute to U.S. advanced packaging needs and the objective of this NOFO (See Section 1.1.3).
- An outline of the proposed approach, including intended R&D area and their associated Technical Targets (see Section 1.4.3). The applicant should provide a rationale for selecting the Technical Target(s), address why the Target(s) represent a significant but achievable technical advance and describe the innovativeness of the approach to achieving the Target(s).

iii. Project-Level Non-Technical Plan

- An outline of plans for transitioning the proposed technology to commercial deployment.
- An outline of the overall education and workforce plan, including the targeted educational or professional levels and support mechanisms (e.g., internships and traineeships).

iv. Project Team – For purposes of this NOFO, a project team comprises all funded entities (the applicant and any proposed subrecipients), as well as unfunded

collaborators planned for inclusion in a single proposal. The lead institution will be the applicant for both concept paper and full application stages. The concept paper narrative must address each of the following topics:

- Describe the capabilities of the lead institution, including any required capabilities specified for the applicant-selected R&D area (see Section 1.4.3 for required applicant capabilities for each R&D area).
- Describe the planned role for additional team members (subrecipients and unfunded collaborators) and the capabilities each bring that are essential to the planned proposal. Examples of relevant capabilities include the following.
  - Advanced packaging capability.
  - Research and innovation capability, including innovation capabilities provided by academic research team members.
  - Education and workforce development capability
- As an appendix to the concept paper (not included in the concept paper narrative page limit), provide a letter of commitment from each planned team member (including both subrecipients and unfunded collaborators) indicating their intention to participate and the capabilities they expect to provide to the proposed project.

v. **Budget Estimate –** Provide a rough order of magnitude estimate of the total project budget, including the lead applicant and all subrecipients.

Letters of Interest - Letters of interest are optional and, where included, should indicate willingness from any third party to support this proposed effort. Note that Letters of Interest do not include subrecipients or unfunded collaborators, who must provide letters of commitment as described in Section 4.5.1.2 immediately above. Letters of Interest should outline the nature and importance of the support being offered. Letters of interest may also be from entities wishing to vouch for the applicant's knowledge, skills, or abilities to conduct the proposed work or to express interest as potential customers for or users of the technologies to be developed under the project plan, including those with commercial, national security, or critical infrastructure interests. Letters of interest do not contribute to the Concept Paper Narrative page limit.

4.5.2 Concept Paper Format and Guidelines

Table 16. Concept Paper Format and Guidelines	
Paper, Email, and Facsimile (fax) Submissions	Will not be accepted. All submissions must be submitted via Grants.gov.
Figures, Graphs, Images, and Pictures	Should be of a size that is easily readable or viewable and may be landscape orientation.

Font	Use one of the following fonts:
	• Preferred: Calibri at a font size of 11 points or larger;
	• Acceptable alternatives:
	  o Arial (not Arial Narrow), Courier New, or Palatino Linotype at a font size of 10 points or larger;
	  o Times New Roman at a font size of 11 points or larger; or

	o Computer Modern family of fonts at a font size of 11 points or larger.
Line Spacing	Single.
Margins	One (1) inch top, bottom, left, and right.
Page layout	Portrait orientation only except for figures, graphs, images, and pictures.
Page Limit	Ten (10) pages for concept paper narrative.
Page limit includes	Concept paper narrative including Project Impact Statement, Project Level Technical Plan, Project Level Non-Technical Plan, Project Team, Budget Estimate, and any figures, graphs, images, and pictures.
Page limit excludes	Cover Sheet; Table of Contents, Concept Paper Executive Summary; Letters of Interest.
Page numbering	Number all pages sequentially.
Paper size	21.6 cm by 27.9 cm (8 ½ inches by 11 inches) with 2.5 cm (1 inch) margins.
Application language	English.
Typed document	All applications, including forms, must be typed.

4.6 FULL APPLICATIONS

Full applications will be accepted only from applicants that are invited after the concept paper stage. Submissions from entities other than those specifically invited to submit a full application will not be reviewed or considered.

The required content and form of full applications submitted pursuant to this NOFO are set forth below.

4.6.1 Required Forms and Documents

The full application must contain the following:

4.6.1.1 Standard Form (SF)-424 (R&R), Application for Federal Assistance

The SF-424 (R&R) must be signed by an authorized representative of the applicant organization. For SF-424 (R&R), Items 5, 14, and 19, use the Zip Code + 4 format (##### - ####) when addresses are requested.

For SF-424 (R&R), Item 11, the descriptive title must begin with the header "R&D Area 'n':" where 'n' is the number from the following list for the corresponding R&D area covered in the application. Example for a proposal covering the Chiplets Ecosystem area: "R&D Area 4: (applicant title text here)."

1. Equipment, Tools, Processes, and Process Integration
2. Power Delivery and Thermal Management
3. Connector Technology, Including Photonics and Radio Frequency (RF)
4. Chiplets Ecosystem
5. Co-design/Electronic Design Automation (EDA)

The list of certifications and assurances referenced in Item 17 of the SF-424 (R&R) is contained in the Federal Financial Assistance Certifications and Representations (Certs and Reps) as part of the SAM.gov entity registration.

SF-424 (R&R), Item 18. If the SF-LLL, Disclosure of Lobbying Activities form (Section 4.6.1.5below) is applicable, attach it to field 18.

Instructions for completing the SF-424 (R&R) can be found on Grants.gov, as well as at the NIST Financial Assistance Agreements Management Office SF-424 Research & Related (R&R) Application Package Guidance.

4.6.1.2 Research and Related Budget (Total Fed + Non-Fed)

The budget should reflect anticipated expenses for the full term of the project, considering all potential cost increases, including cost of living adjustments.

The budget should be detailed in these categories:

A. Senior/Key Personnel;
B. Other Personnel;
C. Equipment Description;
D. Travel;
E. Participant/Trainee Support Costs;
F. Other Direct Costs;
G. Direct Costs (automatically generated);
H. Indirect Costs;
I. Total Direct and Indirect Costs (automatically generated);
J. Fee (not relevant to this competition);
K. Total Costs and Fee (automatically generated);
L. Budget Narrative and Justification document (item 4.6.1.8 below) should be attached to field L.

A separate detailed R&R Budget must be completed for each project phase during the proposed award. To add additional phases, click "Add Period" embedded at the end of the form. Information regarding the Research & Related Budget (Total Fed + Non-Fed) is available in the R&R Family Section of Grants.gov, as well as at the NIST Financial Assistance Agreements Management Office SF-424 Research & Related (R&R) Application Package Guidance.

4.6.1.3 CD-511, Certification Regarding Lobbying

Enter "2025-NIST-CHIPS-NAPMP-01" in the Award Number field. Enter the title of the application, or an abbreviation of that title, in the Project Name field.

4.6.1.4 Research and Related Other Project Information

Answer the highlighted questions and use this form to attach the Project Narrative (item d below), the Indirect Cost Rate Agreement (item 4.6.1.9), the Letters of Commitment and Interest, if applicable, (item 4.6.1.11 below), the Data Management Plan (item 4.6.1.12 below), and the Current and Pending Support Form (item 4.6.1.13 below). Instructions for completing the Research and Related Other Project Information form can be found in the Grants.gov R&R Forms Repository by scrolling down to Research And Related Other Project Information and clicking the Instructions link, as well as in the NIST Financial Assistance Agreements Management Office SF-424 Research & Related (R&R) Application Package Guidance. Research And Related Other Project Information and clicking the Instructions link, as well as in the NIST Financial Assistance Agreements Management Office SF-424 Research & Related (R&R) Application Package Guidance.

4.6.1.5 SF-LLL, Disclosure of Lobbying Activities

Complete this form if applicable.

4.6.1.6 Project Narrative

The project narrative is a word-processed document of no more than twenty-five (25) pages (single-spaced) that is responsive to the program description and the evaluation criteria in Sections 1.1 and 5.3 of this NOFO. The project narrative for the full application should contain the following information and required elements:

a. **Cover Sheet.** (This does not contribute to the project narrative page limit.) The cover sheet is limited to one (1) page and must provide the following:
   - NOFO Name and Reference Number (2025-NIST-CHIPS-NAPMP-01)
   - Full application submission date
   - Relevant R&D areas (see Section 1.4.3)
   - Name of the applicant organization
   - Name of the project director(s)/principal investigator(s)
   - Name of any subrecipient and contractor organizations
   - Application title – Title must begin with the header "*R&D Area 'n'*" where 'n' is the number from the following list for the corresponding R&D area covered in the proposal. Example: "*R&D Area 1: (applicant title text here)*."
     1. Equipment, Tools, Processes, and Process Integration
     2. Power Delivery and Thermal Management
     3. Connector Technology, Including Photonics and Radio Frequency (RF)
     4. Chiplets Ecosystem
     5. Co-design/Electronic Design Automation (EDA)
   - Point of Contact for the applicant, to include name, address, telephone number, and business e-mail address
   - Total funds requested and total proposed cost share (if applicable)
   - Any statement regarding confidentiality, including proprietary or sensitive business information, if applicable

b. **Executive Summary.** (This does not contribute to the project narrative page limit.) The executive summary is limited to two (2) pages and provides a concise summary/abstract of the proposed effort. The summary/abstract must contain a summary of the proposed activity suitable for dissemination to the public. It should be a self-contained document that identifies the name of the applicant, the project director(s)/principal investigator(s), the proposal title, the objectives of the proposed team, a description of the proposed team, methods to be employed, the potential impact of the proposed team (i.e., benefits, outcomes). This document must not include any classified information or proprietary or sensitive business information, as CHIPS R&D may make it available to the public after awards are issued.

c. **Table of Contents.** (This does not contribute to the project narrative page limit.)

d. **Project Description**. A description of the proposed project covering items i-v below and sufficient to permit evaluation of the application in accordance with the evaluation criteria (see Section 5.3).

   i. **Project Impact Statement**
      - Provide a clear problem statement and well-defined project outcomes, explaining how both are relevant to the CHIPS R&D mission and goals (see Section 1.1.1) and the objective of this NOFO, as expressed in Section 1.1.3.
      - Describe the project's contribution to economic and national security, as expressed in the evaluation criteria in Section 5.3.
      - Provide, if applicable, evidence of known or expected impacts to the U.S. Department of Defense, other government systems, critical infrastructure, and/or to advancing domestic production.

   ii. **Project Team**
      - For purposes of this NOFO, a team comprises all funded entities (applicants and subrecipients), as well as unfunded collaborators included in the application.
        - Describe the capabilities of the applicant that make it suitable to lead the proposed project, including any required capabilities specified for the applicant-selected R&D areas (see Section 1.4.3 for required capabilities for each R&D area). For each of the team members, provide a description where applicable or indicate 'no current capability.'
      - Describe the planned role for additional team members (subrecipients and unfunded collaborators) and the capabilities each bring that are essential to the planned proposal. Examples of relevant capabilities may include the following:
        - Advanced packaging capability.
        - Research and innovation capability, including innovation capabilities provided by academic research team members.
        - Education and workforce development capability.

iii. **Roles and Responsibilities**

- Provide an organizational chart showing key management positions.
- Describe the roles and responsibilities for each position in the organizational chart.
- Describe the reporting relationships among the positions in the organizational chart.
- Provide the names and roles of all key personnel who will contribute to the proposed project, including individuals not listed on the organizational chart.

iv. **Project-Level Technical Plan**

- Consistent with the overall scientific and technical merit evaluation criterion in Section 5.3, provide an assessment of the current technological state of the art and the projected state of art resulting from the project.
- Describe plans for meeting, exceeding, or not-meeting each of the Technical Targets listed for each R&D area addressed in the proposal (see Section 1.4.3for R&D Area Technical Targets). Describe plans for any additional technical targets selected by the applicant.
- Describe project Phases 1-4 in terms of measurable steps toward achieving project level goals, noting the feasibility and innovativeness of the required actions and any gaps, constraints, and challenges to be addressed.
- Describe the design of any proposed demonstration device(s) and explain how this design is suitable for demonstrating the ability to integrate project outputs into an advanced packaging flow.
- Describe plans for implementing project outputs into relevant baseline flows at the NAPPF or other NAPMP-designated research facility.
- Provide SMART (Specific, Measurable, Achievable, Relevant, and Time-Bound) milestones at approximately quarterly intervals and a corresponding Gantt Chart with timeline covering project Phases 1-4. Propose milestones suitable for go/revise/no-go checkpoints at each transition between project phases.

v. **Project-Level Non-Technical Plan**

- **Education and Workforce Development Plan**
    - Describe the overall education and workforce plan (see Section 1.7.1), including the targeted educational or professional levels, support mechanisms (e.g., internships, Registered Apprenticeships and pre-apprenticeships with direct links to Registered Apprenticeship Programs, and traineeships), and the roles and responsibilities of relevant participating organizations, such as accredited educational

institutions, labor organizations, or other workforce training organizations.
    - Provide SMART project-level targets (e.g., number of students trained, graduated, hired, and/or retained) and milestones for assessing progress toward targets at approximately semiannual intervals and a corresponding Gantt Chart with timeline covering project Phases 1-4. Propose milestones suitable for go/no-go checkpoints at each transition between project phases.
    - Provide evidence of alignment with U.S. industry needs, such as demonstrated linkages between the skills to be developed in the programs and available jobs or to industry-recognized credentials or certifications. Other evidence may include letters of interest from potential employers and labor organizations.
    - Describe any efforts to maximize access to and participation in the semiconductor workforce, including efforts to attract and retain a diverse student and trainee population such as supportive services and outreach to underserved communities.
    - Describe any physical or virtual infrastructure that will be made available to support education and workforce training programs.
- **Commercial Viability and Domestic Production Plan**
    - Provide a Commercial Viability and Domestic Production plan (See Section 1.7.2), including a timeline with SMART milestones at approximately semiannual intervals demonstrating the viability of the proposed business model (see below) and of the pathway to domestic production (see below), and a corresponding Gantt Chart with timeline covering project Phases 1-4. Where relevant, milestones should complement technical milestones. Propose milestones suitable for go/no-go checkpoints at each transition between project phases.
    - Describe the business model, including an initial assessment of the funded innovation's marketability, considering factors such as cost competitiveness, value proposition, and the impact of competitor products.
    - Describe the technology transition plan and pathway to domestic production and, if relevant, the potential for adoption for commercial or defense uses. If relevant, identify any mitigating factors, as described in Section 1.7.2. Identify any relevant approaches to maximizing the market advantages of the funded innovation, such as through improving cost-efficiency, performance, manufacturing yield, and process times.

- Provide an overview of current or expected customer demand at the volumes required for commercial viability, including examples of possible top customers or categories of customers, and plans for engaging with the customer ecosystem as the project advances.

- **Broader Impacts Statement**
  - Consistent with Section 1.8, provide an overview of the proposed project's broader impacts, such as commitments to future investment, support for other R&D programs, creating inclusive opportunities, climate and environmental responsibility, or community impact and support.
  - If relevant, identify impacts on a new or existing regional semiconductor industry cluster or alignment with regional, state, or local economic development strategies, assets, resources, or capacities.
  - If relevant, identify any known or potential collaborations across the supply chain, IP rights or licensing plans, or investments into domestic prototyping and manufacturing facilities that would result from this project.
  - If relevant, describe the potential for the funded innovation to attract private capital and induce larger-scale, private domestic investments into domestic prototyping. While construction activities are not an allowable cost under this program, costs related to internal modifications of existing buildings may be allowed, in NIST's sole discretion. Where such costs are proposed, a description of whether and how the applicant intends to utilize domestically produced iron, steel, and construction materials as part of their projects, including how any non-Federal entity[36] plans to meet any applicable legal requirements pursuant to the Build America, Buy America Act.

vi. **Fundamental Research Declaration** (Not to exceed two (2) pages. This does not contribute to the project narrative page limit.)

- Identify which of the proposed research activities, if any, the applicant believes NIST/CHIPS R&D should consider as fundamental research and the rationale for that determination.
- For any proposed fundamental research, identify the involved project team member. Note that NIST/CHIPS R&D reserves sole discretion to determine which elements of a proposed research project shall be considered fundamental.

vii. **Research Security Plan.** Provide a written plan that—

- Provides a point of contact on research security issues within the project leadership team.

[36] Non-Federal entity (NFE) means a State, local government, Indian tribe, Institution of Higher Education (IHE), for-profit, or nonprofit organization that carries out a Federal award as a recipient or subrecipient (see M-24-02).

- Describes, as applicable, any internal processes or procedures to address foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity.
- Describes measures taken to ensure that appropriate practices for cybersecurity, such as the NIST Cybersecurity Framework and Cybersecurity and Infrastructure Security Agency (CISA) Cybersecurity Performance Goals (CPGs), are incorporated in the project.[37]
- Lists any relevant certifications in place or plans to obtain such certifications (e.g., FCL, CMMC) and standards they follow (e.g. ISO/IEC 27001, ISO 8000-51).
- For "covered institutions", describes the applicant's intent to establish and operate a Research Security Program.

viii. **Intellectual Property Rights Management Plan** (Not to exceed five (5) pages. This does not contribute to the project narrative page limit.)

- Clearly identify (1) any pre-existing IP (which may include patents, proprietary information, etc.) that may be utilized or will need to be licensed to complete the project; (2) IP that may be developed with funding awarded under this NOFO; (3) the path through which any partners who may join later could access the above-referenced IP; and (4) consistent with Attachment A, the path through which any associate recipients may join later could access the above-referenced IP, where necessary.
- Describe any desired deviations from standard IP regulations and terms, such as 2 C.F.R. 200.315
- Describe how the proposed management and ownership of IP support the Commercial Viability and Domestic Production plan and any existing or planned protocols to ensure domestic control of CHIPS R&D-funded intellectual property, including to protect such intellectual property from foreign adversaries (see Section 2.8).
- Describe any additional desired licensing provisions, including provisions to protect IP rights, for providing project outputs (such as equipment, demonstration devices, or other project outputs, including documentation such as process assumptions, design manuals, process design kits, etc.) to the NAPPF, an independent evaluator, Associate Recipient, or other entities designated by CHIPS R&D.

ix. **Physical Infrastructure** (Not to exceed two (2) pages. This does not contribute to the project narrative page limit.)

[37] The CISA performance goals provide a baseline set of cybersecurity practices that are broadly applicable, with known risk-reduction value. They also allow applicants the ability to measure and improve their cybersecurity maturity, and a combination of recommended practices for IT and OT owners, including a prioritized set of security practices.

- Describe the physical location(s) of project team members and the associated physical infrastructure capabilities relevant to achieving project goals.
- Describe existing or planned facilities to be used for substrate and demonstration device production, including detailed plans and timelines for creating or modifying facilities within three (3) months of the initial award, if applicable.
- Include a description of the existing or planned testing and measurement infrastructure for use in assessing progress toward R&D Area Technical Targets and relevant milestones.

xii. **Table of Abbreviations and Acronyms**. (Not to exceed two (2) pages. This does not contribute to the project narrative page limit.) Provide an alphabetical list of all abbreviations, acronyms, and their meanings.

xiii. **Bibliographic List of References**. (Not to exceed five (5) pages. This does not contribute to the project narrative page limit.) Provide a complete bibliographic listing of all references used within the application.

xiv. **Compliance Matrix.** (Not to exceed two (2) pages. This does not contribute to the project narrative page limit.) Applicants must provide a compliance matrix in table format that explains how and where each evaluation criterion is addressed (see Section 5.3 for evaluation criteria). The table's format is at the discretion of the applicant.

xv. **Table of Funded Participants and Unfunded Collaborators.** (This does not contribute to the project narrative page limit.) A table that identifies all organizations that will participate in and collaborate with the awarded team, known at the time of the application submission. The table should consist of an alphabetically ordered list, by organization, of all team members, funded and unfunded, including any known contractors. Foreign partners should be identified.

xvi. **Written Summary of Certain Research Partnerships and Technology Transfer Commitments.** (This does not contribute to the project narrative page limit.) Applicants should provide a written summary that describes any research partnerships or technology transfer commitments in areas relevant to the activities within this NOFO or any other areas related to the mission and goals of CHIPS R&D (see Section 1.1.1) between the applicant entity and (a) any entities located in a foreign country of concern or (b) with any entities that are foreign entities of concern;[38] each foreign entity should be identified.

xvii. **Foreign Partner/Activity Justifications.** (This does not contribute to the project narrative page limit.) Applicants should provide concise initial justifications for the proposed involvement of any foreign partners or proposed execution of research activities overseas, consistent with Section 3.1.4).

xviii. **Table of Cost share Components and Contributors.** (Not to exceed two (2) pages. This does not contribute to the project narrative page limit.)

Where voluntary, committed cost share is offered, provide a table with details about all contributing sources of cost share, both cash and in-kind, including the rationale for selection of the contribution and the merits and risks associated with each known and anticipated contribution.

4.6.1.7 Resume(s) or CV(s)

Not to exceed two (2) pages per individual. These do not contribute to the project narrative page limit. Resumes or CVs are required for all key personnel, including the principal investigator(s) and anyone deemed a "covered individual" per Section 2.7.4 of this NOFO. For purposes of research security reviews, any individual whose resume is included will be deemed a covered individual. The resumes or CVs should highlight experience relevant to the proposed work and should provide sufficient detail for CHIPS R&D to make determinations regarding covered individuals in accordance with 42 U.S.C. § 6605.

4.6.1.8 Budget Narrative and Justification

Not to exceed five (5) pages. These pages do not count against the project narrative page limit. There is no set format for the Budget Narrative and Justification; however, the written justification should include the necessity and the basis for the cost, as described below. When cost share is included in the budget, the written justification must also identify the Federal and non-Federal portion of each cost, to include indirect costs, as applicable (see Section 3.2 of this NOFO for information regarding cost share). Proposed funding levels must be consistent with the project scope, and only allowable costs should be included in the budget.

The proposed budget will be evaluated in accordance with the evaluation criteria for Project Management, Resources, and Budget. Applicants must provide a detailed budget table[39] and budget narrative.[40] All budget tables will be reviewed to determine if all costs are allowable in accordance with Section 3.3 of this NOFO.

Information needed for each budget category is as follows (categories not listed are automatically generated by the form or are not relevant to this competition):

A. **Senior/Key Personnel** – At a minimum, the budget justification should include the following: name, job title, commitment of effort on the proposed project in terms of average number of hours per week or percentage of time, salary rate, total direct charges on the proposed project, description of the role of the individual on the proposed project and the work to be performed.

   Senior/Key Person Fringe Benefits – Fringe benefits should be identified separately from salaries and wages and based on rates determined by

[39] A budget table shows accounting information broken out by budget form object class categories in rows and summarized by project phase and Federal award total in the columns.
[40] The budget should reflect the total costs, composed of both the Federal funds that will be requested and the cost share or matching that is planned.

organizational policy. The items included in the fringe benefit rate (e.g., health insurance, parking, etc.) should not be charged under another cost category.

B. **Other Personnel** – Data is requested at the project role level, and not at the individual level for Other Personnel. The budget justification should include the following: job title, commitment of effort on the proposed project in terms of average number of hours per week or percentage of time, salary rate, total direct charges on the proposed project, description of the role of the position on the proposed project and the work to be performed.

   Other Personnel Fringe Benefits – Fringe benefits should be identified separately from salaries and wages and based on rates determined by organizational policy. The items included in the fringe benefit rate (e.g., health insurance, parking, etc.) should not be charged under another cost category.

C. **Equipment Description** – Equipment is defined as an item of property that has an acquisition cost of $10,000 or more (unless the organization has established lower levels) and an expected service life of more than one year. The budget justification should list each piece of equipment, the cost, and a description of how it will be used and why it is necessary to the successful completion of the proposed project. Please note that any general use equipment (computers, etc.) charged directly to the award should be allocated to the award according to expected usage on the project. Any items that do not meet the threshold for equipment can be included under the Materials and Supplies line item in Section F, Other Direct Costs (see below).

D. **Travel** – For all travel costs required by the applicant to complete the project, including attendance at any relevant conferences and/or meetings, the budget justification for travel should include the following: destination; names or number of people traveling; dates and/or duration; mode of transportation, lodging and subsistence rates; and description of how the travel is directly related to the proposed project. For travel that is yet to be determined, please provide best estimates based on prior experience. If a destination is not known, an approximate amount may be used with the assumptions given for the location of the meeting. Applicants should build into travel budgets anticipated travel and related costs for planned team meetings.

E. **Participant/Trainee Support Costs** – Participant support costs are stipends, subsistence allowances, travel, and registration fees paid to or on behalf of participants or trainees, who are not employees of your organization, for conferences or training projects. The budget justification

should indicate the names or number of participants or trainees, a description and calculation of costs per person, a description and date of the event, and a description of why the cost is necessary for the successful completion of the proposed project.

F. **Other Direct Costs** – For costs that do not easily fit into the other cost categories, please list the cost, and the breakdown of the total costs by quantity or unit of cost. Include the necessity of the cost for the completion of the proposed project. Only allowable costs can be charged to the award. Each subaward or contractual cost must be treated as a separate item in the Other Direct Costs category. Describe the services to be provided and the necessity of the subaward or contract to the successful performance of the proposed project. Contracts are for obtaining goods and services. Subrecipients perform part of the project scope of work. For each subaward, applicants must provide budget detail justifying the cost of the work performed on the project.

H. **Indirect Costs** – Commonly referred to as Facilities & Administrative (F&A) Costs, indirect costs are defined as costs incurred by the applicant organization that cannot otherwise be directly assigned or attributed to a specific project. For more details, see Section 4.6.1.9 of this NOFO.

4.6.1.9 Indirect Cost Rate Agreement

If indirect costs are included in the proposed budget, provide a copy of the approved negotiated agreement if this rate was negotiated with a cognizant Federal audit agency. If the rate was not established by a cognizant Federal audit agency provide a statement to this effect. If the successful applicant includes indirect costs in the budget and has not established an indirect cost rate with a cognizant Federal audit agency, the applicant may be required to obtain such a rate upon award.

Alternatively, applicants that do not have a current negotiated (including provisional) indirect cost rate may elect to charge a de minimis rate of fifteen (15) percent of modified total direct costs (MTDC). Applicants proposing fifteen (15) percent de minimis rate should note this election as part of the budget portion of the application.

4.6.1.10 Subaward Budget Form

The Research & Related Subaward Budget Attachment Form is required if subrecipients and contractors are included in the application budget.

Instructions for completing subaward budget forms are available by visiting the R & R Family section of the Grants.gov Forms Repository and scrolling down to the R & R Subaward Budget Attachment(s) Form and selecting “Instructions.”

4.6.1.11 Letters of Commitment and Interest

1. **Letters of Commitment** – (Letters of Commitment do not apply to the project narrative page limit.) Letters that commit specific resources or funding to the proposed project – in the event that the application is funded – are required from all of the following that apply.
   - If the application includes subawards or contracts to known third parties, a letter of commitment from an authorized organization representative of each known proposed subrecipient and unfunded collaborator must be included. Each letter should indicate the submitting organization's willingness to participate as a subrecipient or unfunded collaborator, as applicable, describe the work they will do in relation to the Project Narrative.
   - Letters of commitment from subrecipients that are operators of an FFRDC (see Section 3.1.1) or are Federal entities must include, in addition to the information above, documentation demonstrating that the proposed work does not compete with the private sector and documentation from the FFRDC's sponsoring institution citing the FFRDC's eligibility to participate in competitive Government funding opportunities, the FFRDC's compliance with the sponsor agreement, and confirmation from the sponsoring agency that they can receive Federal funds from NIST.
   - Letters of commitment from subrecipients that are Federal entities (see Section 3.1.2) must include, in addition to the information above, documentation demonstrating that the proposed work does not compete with the private sector and/or citing the specific statutory authority and contractual authority, if relevant, establishing their ability to receive Federal award funds and compete with industry
   - If key personnel who are willing to fill vacancies on the applicant's or subrecipient's staff are identified by the applicant, a letter of commitment from each of the relevant key-personnel individuals must be included. The letter from each such individual, or group of individuals, should indicate the relationship of the writer to the applicant and how the writer will help fulfill the efforts described in the Funding Opportunity Description (see Section 1.4).
   - Applicant and Third-Party Non-Federal Cost share: Letters of commitment for all sources of non-Federal cost share must be included.
     - Applicant Non-Federal Cost share (Cash and In-kind): A letter of commitment is required from an authorized representative of the applicant, stating the total amount of cost share to be contributed by the applicant towards the proposed team. This letter includes a per year break-out of cash cost share and in-kind (non-cash) contributions for the duration of the award.
     - Third Party Cost share (Cash and In-kind): The applicant must include a letter of commitment from an authorized representative of each third-party organization providing cash or in-kind contributions that are being committed to the proposed project, subject to the application being funded. Any such letter(s) should clearly state: whether the third-party contribution will consist of cash contributions, in-kind contributions, or a combination thereof; the total amount or value of the contribution, including a break-out of cash versus in-kind contributions (as applicable); the time period over which the third-party

contribution will be made; any interim performance requirements for phased contributions; and all contingencies or pre-conditions to which the contribution is subject.

- Letters of commitment should not be letters submitted by non-proposing entities wishing to vouch for the applicant's (or entities associated with the applicant) knowledge, skills, and abilities or entities to conduct the proposed work. These letters should be in the form of a letter of interest. Letters of Commitment from education and workforce development partners should describe the specific role of the partner.

2. **Letters of Interest** – (Letters of Interest do not apply to the project narrative page limit.) Letters of Interest are optional and, where included, should indicate willingness from any third party to support this proposed effort. Letters of Interest should outline the nature and importance of the collaboration or involvement being offered. Letters of interest may also be from non-proposing entities wishing to vouch for the applicant's knowledge, skills, or abilities to conduct the proposed work or to express interest as potential customers for or users of the technologies to be developed under the project plan, including those with commercial, national security, or critical infrastructure interests. CHIPS R&D encourages the applicant to limit the number of such letters to those absolutely required to strengthen the application and, where applicable, to consider consolidating letters of interest to include multiple entities.

4.6.1.12 Data Management Plan

The Data Management Plan does not apply to the project narrative page limit. Consistent with NIST Policy 5700.00,[41] Managing Public Access to Results of Federally Funded Research, and NIST Order 5701.00,[42] Managing Public Access to Results of Federally Funded Research, applicants must include a Data Management Plan (DMP).

All applications for activities that will generate scientific data using CHIPS R&D funding are required to adhere to a DMP or explain why data sharing and/or preservation are not within the scope of the proposed project. For the purposes of the DMP, NIST adopted the definition of "research data" at 2 C.F.R. § 200.315(e)(3).

The DMP must include, at a minimum, a summary of proposed activities that are expected to generate data; a summary of the types of data expected to be generated by the identified activities; a plan for storage and maintenance of the data expected to be generated by the identified activities, including after the end of the award's period of performance; and a plan describing whether and how data generated by the identified activities will be reviewed and made available to the public.

A template for the DMP, an example DMP, and the rubric against which the DMP will be evaluated for sufficiency is available online at Data Management Plan Template, Example, and

[41] https://www.nist.gov/system/files/documents/2018/06/19/final_p_5700.pdf
[42] https://www.nist.gov/system/files/documents/2019/11/08/final_o_5701_ver_2.pdf

Rubric. An applicant is not required to use the template as long as the DMP contains the required information.

If an application stands a reasonable chance of being funded and the DMP is determined during the review process to be insufficient, the program office may reach out to the applicant to resolve deficiencies in the DMP. If an award is issued prior to the deficiencies being fully rectified, the award will include a term and condition stating that no research activities shall be initiated or costs incurred for those activities under the award until the NIST Agreements Officer amends the award to indicate the term and condition has been satisfied. Reasonable costs for data preservation and access may be included in the application.

4.6.1.13 Current and Pending Support Form

Applicants must identify all sources of current and potential funding, including this award, for all covered individuals. Any current project support (e.g., Federal, state, local, public or private foundations, etc.) must be listed on this form. The proposed project and all other projects or activities requiring a portion of time of the Principal Investigator(s) (PI), co-PI (s), and key personnel must be included, even if no salary support is received. The total award amount for the entire award period covered, including indirect costs, must be shown, as well as the number of person-months per year to be devoted to the project, regardless of the source of support. Similar information must be provided for all proposals already submitted or that are being submitted concurrently to other potential funders.

Applicants must complete the Current and Pending Support Form, using multiple forms as necessary to account for all activity for each covered individual. A separate form should be used for each identified individual.

Applicants must download the Current and Pending Support Form from the NIST website and reference the guidance provided as it contains information to assist with accurately completing the form.

4.6.2 Attachment of Required Documents

Items 4.6.1.1 through 4.6.1.4 above are part of the standard application package in Grants.gov and can be completed through the download application process.

Item 4.6.1.5 the SF-LLL, Disclosure of Lobbying Activities form, is an optional application form which is part of the standard application package in Grants.gov. If item IV.2.a.(5), the SF-LLL, Disclosure of Lobbying Activities form is applicable to this proposal, attach it to field 18 of the SF-424 (R&R), Application for Federal Assistance.

Item 4.6.1.6, the Project Narrative, should be attached to field 8 (Project Narrative) of the Research and Related Other Project Information form by clicking on “Add Attachment”.

Item 4.6.1.8, the Budget Narrative and Justification, should be attached to field L (Budget Justification) of the Research and Related Budget (Total Fed + Total Non-Fed) form by clicking on "Add Attachment".

Items 4.6.1.7, Resume(s) or CV(s), 4.6.1.7, the Indirect Cost Rate Agreement, 4.6.1.9 Letters of Commitment if applicable to the submission, 4.6.1.12, the Data Management Plan, 4.6.1.13, the Current and Pending Support Form must be completed and attached by clicking on "Add Attachments" found in item 12 (Other Attachments) of the Research and Related Other Project Information form.

Item 4.6.1.10, the Subaward Budget Form(s), if applicable to the submission, should be attached to the Research & Related Subaward Budget (Total Fed + Non-Fed) Attachment(s) Form in the application package.

Following these directions will create zip files which permit transmittal of the documents electronically via Grants.gov.

Applicants must carefully follow specific Grants.gov instructions to ensure the attachments will be accepted by the Grants.gov system. A receipt from Grants.gov indicates only that an application was transferred to the system. It does not provide details concerning whether all attachments (or how many attachments) transferred successfully. Applicants will receive a series of e-mail messages over a period of up to two business days before learning whether a Federal agency's electronic system has received its application.

Applicants are strongly advised to access the "Download Submitted Forms and Applications" option at Grants.gov to check if all attachments were contained in their submitted application and to download a zip file of the full submitted application.

After submitting the application, check the status of your application here: CHECK APPLICATION STATUS. If any, or all, of the required attachments are absent from the submission, follow the attachment directions found above, resubmit the application, and check again for the presence of the required attachments.

If the directions found at the Grants.gov Get Started help page are not effective, please contact the Grants.gov Help Desk immediately. If calling from within the United States or from a U.S. territory, please call 800-518-4726. If calling from outside the United States or from a U.S. territory, please call 606-545-5035. Questions also may be e-mailed to support@grants.gov. Assistance from the Grants.gov Help Desk will be available around the clock every day, with the exception of Federal holidays. Help Desk service will resume at 7:00 a.m. Eastern Time the day after Federal holidays.

Applicants can track their submission in the Grants.gov system by following the procedures at the Grants.gov site (CHECK APPLICATION STATUS). It can take up to two business days for an application to fully move through the Grants.gov system to CHIPS R&D.

CHIPS R&D uses the Tracking Numbers assigned by Grants.gov and does not issue Agency Tracking Numbers.

4.6.3 Full Application Format and Guidelines

Table 17. Full Application Format and Guidelines	
Paper, Email, and Facsimile (fax) Submissions	Will not be accepted. All applications must be submitted through Grants.gov.
Figures, Graphs, Images, and Pictures	Should be of a size that is easily readable or viewable and may be displayed in landscape orientation. Any figures, graphs, images, or pictures will count toward the page limits for the project narrative.
Font	Use one of the following fonts: • Preferred: Calibri at a font size of 11 points or larger • Alternatives: o Arial (not Arial Narrow), Courier New, or Palatino Linotype at a font size of 10 points or larger; o Times New Roman at a font size of 11 points or larger; or o Computer Modern family of fonts at a font size of 11 points or larger
Project Narrative Page Limit	The project narrative is limited to twenty-five (25) pages.
Project Narrative Page Limit Exclusions	Portions of the project narrative are NOT included in the 25-page limit. A summary of those components not included in the page limit is listed below. Fundamental Research Declaration (5-page limit) Research Security plan (5-page limit) Intellectual Property Rights Management plan (5-page limit) Foreign Partner/Activity Justifications Physical Infrastructure (2-page limit) Table of Abbreviations and Acronyms (2-page limit) Bibliographic List of References (2-page limit) Compliance Matrix (2-page limit) Table of Funded Participants and Unfunded Collaborators Table of Cost Share Components and Contributors (2-page limit)
Other Page Limit Exclusions	Additional materials required in the full application that are not subject to the project narrative page limit are listed below. SF-424 (R&R), Application for Federal Assistance Research & Related Budget (Total Fed + Non-Fed) CD-511, Certification Regarding Lobbying Research and Related Other Project Information SF-LLL, Disclosure of Lobbying Activities

	Cover Sheet (1-page limit) Executive Summary (2-page limit) Table of Contents Table of Cost Share Components Resume(s) or CV(s) Budget Narrative and Justification Indirect Cost Rate Agreement Subaward Budget Form Letters of Commitment and/or Interest Data Management Plan Current and Pending Support Form Written Summary of Certain Research Partnerships/Technology Transfer Commitments
Page Layout	The project narrative must be in portrait orientation
Page size	21.6 centimeters by 27.9 centimeters (8 ½ inches by 11 inches) with 2.5-centimeter (1 inch) margins
Page numbering	Number all pages sequentially within each section of the application, in a format that is clear and consistent. CHIPS R&D suggests formatting such as 'Project Narrative page 1 of 10' for ease of reference
Application language	All documents must be in English, including but not limited to the initial application, any additional documents submitted in response to a CHIPS R&D request, all reports, and any correspondence with CHIPS R&D
Typed document	All applications, including forms, must be typed

4.7 APPLICATION REPLACEMENT PAGES

Applicants may not submit replacement pages and/or missing documents once a concept paper or full application has been submitted through Grants.gov. Any revisions must be made by submission of a new concept paper or full application that must be received by NIST by the submission deadline.

4.8 UNIQUE ENTITY IDENTIFIER AND SYSTEM FOR AWARD MANAGEMENT (SAM)

Pursuant to 2 C.F.R. part 25, an applicant is required to: (i) be registered in SAM (https://www.sam.gov) before submitting its concept paper and full application; (ii) provide a valid unique entity identifier in its application; and (iii) continue to maintain an active SAM registration with current information at all times during which it has an active Federal award or an application or plan under consideration by a Federal awarding agency, unless otherwise excepted from these requirements pursuant to 2 C.F.R. § 25.110.

NIST will not make a Federal award to an applicant until the applicant has complied with all applicable unique entity identifier and SAM registration requirements and, if an applicant has not

fully complied with the requirements by the time that NIST is ready to make a Federal award pursuant to this NOFO, NIST may determine that the applicant is not qualified to receive a Federal award and use that determination as a basis for making a Federal award to another applicant.

4.9 SUBMISSION DATES AND TIMES

CHIPS R&D strongly encourages applicants to begin the process of registering for SAM.gov as early as possible. While this process ordinarily takes between three days and two weeks, in some circumstances it can take six or more months to complete due to information verification requirements.

Applicants should be aware, and factor into their application submission planning, that the Grants.gov system closes periodically for routine maintenance. Applicants should visit Grants.gov for information on any scheduled closures.

Please note that an award cannot be issued if the designated recipient's registration at SAM.gov is not active at the time of the award.

4.9.1 Concept Papers

Concept papers must be received through Grants.gov no later than 11:59 p.m. Eastern Time, December 20, 2024. Concept papers received after the specified deadline will not be reviewed or considered.

Review of the concept papers, selection, and notification to applicants is expected to be completed on or about February 24, 2025. Changes to the expected completion date will be communicated on the CHIPS R&D Frequently Asked Questions page.

4.9.2 Full Applications

The full application deadline will be communicated to invited applicants at the time of invitation. CHIPS R&D will consider the date and time recorded by Grants.gov as the official submission time. Applications received after the specified deadline will not be reviewed or considered.

4.10 INTERGOVERNMENTAL REVIEW

Applications under this program are not subject to Executive Order 12372.

4.11 FUNDING RESTRICTIONS

Construction activities are not an allowable cost under this program. However, costs related to internal modifications of existing buildings that would be necessary to carry out the proposed research tasks may be allowed at NIST's sole discretion.

In addition, recipients and subrecipients may not charge any profits, fees, or other increments above cost to an award issued pursuant to this NOFO.

5 APPLICATION REVIEW INFORMATION

5.1 CONCEPT PAPER EVALUATION CRITERIA

The CHIPS R&D merit review process will assess concept papers against the following five criteria: (1) relevance to economic and national security; (2) overall scientific and technical merit; (3) project management; (4) transition and impact strategy; and (5) education and workforce development. The evaluation will be qualitative, not numerical.

5.1.1 Relevance to economic and national security

This criterion addresses relevance of the proposal to enhancing U.S. economic or national security competitiveness and to achieving the CHIPS R&D mission and goals (see Section 1.1.1). Reviewers will consider the extent to which the project is likely to:

1. Advance domestic semiconductor development capabilities;
2. Generate substantial economic benefits to the Nation that extend beyond the direct return to participants in the program; and
3. Support the development of semiconductors necessary to the U.S. Department of Defense, other government systems, or critical infrastructure.

5.1.2 Overall Scientific and Technical Merit

This criterion addresses the quality, innovativeness, and feasibility of the proposed Concept Paper Narrative and the potential for meeting the objectives of this NOFO, as expressed in Sections 1.1.2and 1.1.3. Reviewers will consider the extent to which the concept paper:

1. Describes activities that are innovative, original, or potentially transformative;
2. Demonstrates knowledge of the current state of the art in relevant fields and the feasibility of the proposed technologies to be advanced, including gaps, constraints, and significant challenges that must be addressed;
3. Addresses NAPMP program drivers (see Section 1.3.1) for scale down and scale out; heterogeneous integration, including chiplets; end-to-end advanced packaging; and prototypes for demonstrating functionality; and
4. Sets out goals for R&D Area Technical Targets (Section 1.6) and plans for implementation in an advanced packaging flow that represent a significant advance relative to the state of the art globally.

5.1.3 Project Management

This criterion addresses the degree to which applicants demonstrate that they have the appropriate personnel and access to required equipment and facilities. Reviewers will consider the extent to which the concept paper:

1. Identifies key staff, leadership, and technical experts with qualifications and experience appropriate to the proposed work, including prior experience and results in efforts similar in nature, purpose, or scope of proposed activities;
2. Identifies equipment and facilities required to support the project and demonstrates either access to or a clear plan to obtain access to such equipment and facilities;
3. Addresses the NAPMP program driver (see Section 1.3.1) for Aligned R&D efforts; and
4. Convincingly demonstrates existing or planned advanced packaging capability needed for the proposed activities by the applicant and/or other committed project participants.

5.1.4 Transition and Impact Strategy

This criterion addresses the project's potential for supporting the commercialization and domestic production of funded semiconductor innovations, as well as beneficial impacts to the broader domestic research, development, and innovation ecosystem. Reviewers will consider the extent to which the proposal provides:

1. Evidence of an understanding of relevant competing commercial and emerging technologies and how the proposed project would provide a significant, marketable improvement over these competing technologies;
2. A reasonable approach for transitioning the proposed technology to commercial deployment; and
3. Evidence of one or more team members with experience designing, developing, demonstrating, and delivering advanced packaging equipment and integrated processes for forward-looking technology nodes.

The evaluation may also consider the applicant's history of transitioning (or plans to transition) technologies to foreign governments or to companies that are foreign owned, controlled, or influenced.

5.1.5 Education and Workforce Development (EWD)

Concept papers will be evaluated for the quality, completeness, rationality, and feasibility of the proposed project's EWD models and plans. Reviewers will therefore evaluate the overall EWD approach and the extent to which the EWD plan:

1. Includes rational and feasible targets, milestones, and metrics (e.g., students trained, graduated, hired, and retained), appropriate to developing a diverse and skilled workforce;
2. Describes how EWD programs prepare participants good jobs as defined by the Department of Commerce and Department of Labor Good Jobs Principles;
3. Provides evidence of alignment with U.S. industry needs; and
4. Encourages participation by underserved communities, including the education and training of veterans and individuals with disabilities.

5.2 CONCEPT PAPER SELECTION FACTORS

The selection factors for concept papers in this competition are:

1. Merit Review. Results of the merit reviewers' evaluations, including technical comments, and the evaluation panel's evaluations and adjectival ratings.
2. Relevance to Program and Mission. Alignment with the objectives of this NOFO as well as the objectives and priorities of the NAPMP and the mission, goals, and priorities of CHIPS R&D.
3. Non-Duplication. The degree to which the proposed project duplicates other projects funded by NIST or other Federal sources.
4. Diversity of Projects and Participants. The degree to which the proposed team and project provides for a diversity of proposed project topics, regional diversity, and institutional diversity (including small and medium enterprises, universities, non-profit research organizations, etc.) in the overall NAPMP portfolio.
5. Broader Impacts and Workforce Development. The potential for the proposed project to contribute to broader U.S. research, development, innovation, manufacturing, education, workforce development, environmental responsibility, and regional economic development goals, including plans for broader impact consistent with Sections 1.7.1 and 1.8 of this NOFO.

5.3 FULL APPLICATION EVALUATION CRITERIA

The CHIPS R&D merit review process will assess full applications against the following five criteria: (1) relevance to economic and national security; (2) overall scientific and technical merit; (3) project management, resources, and budget; (4) transition and impact strategy; and (5) education and workforce development. The first two criteria—economic and national security and overall scientific and technical merit—will receive the greatest and approximately equal weight. The remaining three criteria will receive approximately equal weight to each other. The evaluation will be qualitative, not numerical. Applications will be recommended for award only if CHIPS R&D determines that each criterion is adequately addressed in the application materials.

5.3.1 Relevance to Economic and National Security

This criterion addresses relevance of the proposal to enhancing U.S. economic or national security competitiveness and to achieving the CHIPS R&D mission and goals (See Section 1.1.1.) Specifically, the applicant must clearly demonstrate its plans and capabilities to enable domestic invention, development, prototyping, manufacture, and deployment of advanced packaging technologies. Reviewers will therefore evaluate the extent to which the project is likely to:

1. Advance domestic semiconductor research and development capabilities;
2. Create a more resilient U.S. semiconductor supply chain, such as by addressing the risks associated with geographic concentration of current semiconductor production;
3. Generate substantial economic benefits to the Nation that extend beyond the direct return to participants in the program;
4. Support the packaging of semiconductors necessary to the U.S. Department of Defense, other government systems, or critical infrastructure; and
5. Increase non-Federal investment in advanced packaging research and manufacturing capabilities in the United States.

5.3.2 Overall Scientific and Technical Merit

This criterion addresses the quality, innovativeness, and feasibility of the proposed project and the potential for meeting the objectives of this NOFO, as expressed in Sections 1.1.2 and 1.1.3. Specifically, the application must be clear and concise and identify the core innovation, technical approach, and major technical hurdles and risks, as well as clearly establish the feasibility of the project through adequately detailed plans linked to major technical barriers. Reviewers will therefore evaluate the extent to which the application:

1. Describes activities that are innovative, original, or potentially transformative;
2. Includes activities, goals, objectives, and strategies that are well-reasoned, well-organized, and presented in sufficient technical detail;
3. Demonstrates knowledge of the current state of the art in relevant fields and the feasibility of the proposed technologies to be advanced, including gaps, constraints, and significant challenges that must be addressed;
4. Addresses NAPMP program drivers (see Section 1.3.1) for scale down and scale out; heterogeneous integration, including chiplets; end-to-end advanced packaging; and prototypes for demonstrating functionality;
5. Incorporates effective mechanisms to assess success, including meaningful milestones and effective demonstration device design and packaging flow implementation; and
6. Sets out goals for R&D Area Technical Targets (Section1.6) and plans for implementation in an advanced packaging flow that represent a significant advance relative to the state of the art globally.

5.3.3 Project Management, Resources, and Budget

This criterion addresses the reasonableness, appropriateness, and cost-effectiveness of the proposed budget, management strategy, and resources, relative to the work and objectives of the proposed project. Applicants must demonstrate that they have the appropriate personnel and management structure to complete the work, access to the required equipment/facilities, and that the budget requested matches the need. Reviewers will therefore evaluate the extent to which the proposal:

1. Provides a clear picture of annual expenditures and a budget that is cost-effective, reasonable, and consistent with the proposed scope of work;
2. Clearly describes targets, milestones, and a project management approach that supports the objectives of this NOFO, including schedule and budget risk and mitigation strategies;
3. Addresses the NAPMP program driver (see Section 1.3.1) for Aligned R&D efforts;
4. Identifies key staff, leadership, and technical experts with qualifications and experience appropriate to the proposed work, including prior experience and results in efforts similar in nature, purpose, or scope of proposed activities;
5. Identifies equipment and facilities required to support the project and demonstrates either access to or a clear plan to obtain access to advanced packaging equipment and facilities required for the proposed work; and
6. Convincingly demonstrates existing or planned advanced packaging capability by the applicant and/or other committed project participants.

5.3.4 Transition and Impact Strategy

This criterion addresses the project's potential for supporting the commercialization and domestic production of funded semiconductor innovations, as well as beneficial impacts to the broader domestic research, development, and innovation ecosystem. Reviewers will therefore evaluate the extent to which the proposal:

1. Includes a Commercial Viability and Domestic Production plan that demonstrates an understanding of competing commercial and emerging technologies and how the proposed innovation would provide a significant, marketable improvement over these competing technologies, as applicable;
2. Provides a reasonable approach for transitioning the proposed technology to commercial deployment, including an Intellectual Property Rights Management plan;
3. Includes a Broader Impacts Statement that, in combination with the Commercial Viability and Domestic Production plan, demonstrates a credible commitment to future investment, support for other R&D programs, creating inclusive opportunities, environmental responsibility, and community impact and support;
4. Describes the potential for the proposed work to contribute to establishing sustainable domestic advanced packaging innovation and manufacturing capability such as contributions to the development of new or existing regional semiconductor industry clusters; and
5. Provides evidence of one or more team members with experience designing, developing, demonstrating, and delivering advanced packaging equipment and integrated processes for forward-looking technology nodes.

The evaluation may also consider the applicant's history of transitioning (or plans to transition) technologies to foreign governments or to companies that are foreign owned, controlled, or influenced.

5.3.5 Education and Workforce Development (EWD)

This criterion addresses the quality, completeness, rationality, and feasibility of the proposed project's EWD models and plans. Reviewers will therefore evaluate the extent to which the proposal's EWD plan:

1. Includes rational and feasible targets, milestones, and metrics (e.g., students trained, graduated, hired, and retained), appropriate to developing a diverse and skilled workforce;
2. Demonstrates how the applicant will support the hiring of participants that have successfully completed EWD programs by specific industry partners, into good jobs as defined by the Department of Commerce and Department of Labor Good Jobs Principles;
3. Provides evidence of alignment with U.S. industry needs, such as demonstrated linkages between the skills to be developed and in-demand high-quality jobs or to industry-recognized curriculum, credentials, or certifications; and

4. Encourages participation by underserved communities, including the education, training, of veterans and individuals with disabilities.

5.4 SELECTION FACTORS

The selection factors for this competition are:

1) Merit Review. Results of the merit reviewers' evaluations, including technical comments, and the evaluation panel's evaluations and adjectival ratings.
2) Relevance to Program and Mission. Alignment with the objectives of the NOFO as well as the objectives and priorities of the NAPMP program and the mission, goals, and priorities of the CHIPS Research and Development Office, which may include considerations related to domestic economic and national security, research security, domestic production, and domestic control of intellectual property.
3) Funding. The availability of funding and the reasonableness and reliability of cost share from specific, known, and anticipated non-Federal sources.
4) Non-Duplication. The degree to which the proposed project duplicates other projects funded by NIST or other Federal sources.
5) Diversity of Projects and Participants. The degree to which the proposed team and project provides for a diversity of proposed project topics, regional diversity, and institutional diversity (including small and medium enterprises, universities, nonprofit research organizations, etc.) in the overall NAPMP portfolio.
6) Broader Impacts and Workforce Development. The potential for the proposed project to contribute to broader U.S. research, development, innovation, manufacturing, education, workforce development, environmental responsibility, and regional economic development goals — including plans for broader impact consistent with Sections 1.7.1 and 1.8 of this NOFO — in addition to any commitment to cost share from specific, known and anticipated non-Federal sources.

5.5 REVIEW AND SELECTION PROCESS

Proposals, reports, documents, and other information related to applications submitted to CHIPS R&D and/or relating to awards issued by CHIPS R&D will be reviewed and considered by Federal employees or non-Federal personnel who have entered into conflict of interest and confidentiality agreements covering such information, as applicable.

5.5.1 Initial Review of Applications

Concept papers and full applications received by the respective deadlines will be reviewed to determine eligibility, completeness, and responsiveness to this NOFO and stated program objectives. Concept papers and full applications determined to be ineligible, incomplete, and/or nonresponsive may be eliminated from further review. However, CHIPS R&D, in its sole discretion, may continue the review process for any concept paper or full application that is missing non-substantive information, the absence of which may easily be rectified during the review process.

Applicants are reminded that it is a crime to knowingly make false statements to a Federal agency. Misrepresentation of material facts may be the basis for denial of an application. Penalties upon conviction may include fine and imprisonment. For details, please refer to 18 U.S.C. § 1001.

5.5.2 Review of Concept Papers

Concept papers that are determined to be eligible, complete, and responsive will proceed for full reviews in accordance with the review and selection process below:

5.5.2.1 Merit Review

At least three (3) independent, objective reviewers, who may be Federal employees or non-Federal personnel, with appropriate expertise relating to the topics covered in this NOFO, will each provide a written evaluation and adjectival ratings (see Section 5.5.2.3) based on the evaluation criteria (see Section 5.1). While every concept paper will have at least three (3) reviewers, concept papers may have more than three (3) reviewers if specialized expertise is needed. During the review process, the reviewers may discuss concept papers with each other, but ratings will be determined on an individual basis, not a consensus.

5.5.2.2 Evaluation Panel

Following the merit review, an evaluation panel consisting of CHIPS R&D staff and/or other Federal employees with the appropriate expertise will conduct a panel review of the concept papers. The evaluation panel may contact applicants via e-mail to clarify the contents of a concept paper.

5.5.2.3 Adjectival Rating

The evaluation panel will provide a final adjectival rating and written evaluation of each concept paper to the Selecting Official for further deliberation, considering:

- All concept paper materials.
- Results of the merit reviewers' evaluations, including written assessments.
- Any relevant publicly available information.
- Any clarifying information obtained from the applicants.

The adjectival ratings that will be assigned are:

- Outstanding
- Very Good
- Average
- Deficient

For decision-making purposes, concept papers receiving the same adjectival rating will be considered to have an equivalent ranking.

5.5.2.4 Selection of Successful Concept Papers and Invitations to Submit Full Applications

The NIST Director or designee will serve as the Selecting Official and will make final determinations regarding which concept papers to invite to submit full applications. The Selecting Official shall generally select the most meritorious concept papers for invitation based upon the adjectival ratings and one or more of the Selection Factors. The Selecting Official retains the discretion to select concept papers from a lower adjectival category based on one or more of the Selection Factors. The decisions of the Selecting Official regarding the selection of concept papers are final and may not be appealed. CHIPS R&D may publicly release or publish successful concept paper applicant names and concept paper executive summaries.

5.5.3 Review of Full Applications

Applications that are determined to be eligible, complete, and responsive will proceed for full reviews in accordance with the review and selection process below:

5.5.3.1 Merit Review

At least three (3) independent, objective reviewers, who may be Federal employees or non-Federal personnel, with appropriate expertise relating to the topics covered in this NOFO, will each provide a written evaluation and adjectival ratings (see Section 5.5.3.4 based on the evaluation criteria (see Section 5.3). While every application will have at least three (3) reviewers, applications may have more than three (3) reviewers if specialized expertise is needed to evaluate an application. During the review process, the reviewers may discuss the applications with each other, but evaluations will be determined on an individual basis, not a consensus.

5.5.3.2 Evaluation Panel

Following the merit review, an evaluation panel consisting of CHIPS R&D staff and/or other Federal employees with the appropriate expertise will conduct a panel review of the ranked applications. The evaluation panel may contact applicants via e-mail to clarify contents of an application.

5.5.3.3 Pre-selection Interviews and Site Visits

At CHIPS R&D's discretion, applicants may be requested to participate in Pre-Selection Interviews and/or Site Visits during the evaluation panel phase, either at CHIPS R&D, the applicant's site, or a mutually agreed upon location, or via conference call or webinar. The interviews and site visits are intended to allow the applicant to provide clarifications on the contents of the application and to provide CHIPS R&D an opportunity to ask questions and collect relevant information. Information provided during the interview and/or site visit will contribute to CHIPS R&D's evaluation of the applications.

5.5.3.4 Adjectival Rating

The evaluation panel will provide a final adjectival rating and written evaluation of each full application to the Selecting Official for further deliberation, considering:

- All application materials.
- Results of the merit reviewers' evaluations, including written assessments.
- Any relevant publicly available information.
- Any clarifying information obtained from the applicants.

The adjectival ratings that will be assigned are:

- Outstanding
- Very Good
- Average
- Deficient

For decision-making purposes, applications receiving the same adjectival rating will be considered to have an equivalent ranking.

5.5.3.5 Selection

The Selecting Official, the NIST Director or designee, will make final award recommendations to the NIST Agreements Officer. The Selecting Official shall generally select and recommend the most meritorious applications for an award based upon the adjectival ratings and one or more of the Selection Factors. The Selecting Official retains the discretion to select and recommend an application from a lower adjectival category based on one or more of the Selection Factors.

CHIPS R&D reserves the right to negotiate the budget costs with any applicant selected to receive an award, which may include requesting that the applicant remove certain costs. Additionally, CHIPS R&D may request that successful applicants modify objectives, work plans, or team composition and provide supplemental information required by the agency prior to award.

CHIPS R&D also reserves the right to reject an application where information is uncovered that raises a reasonable doubt as to the responsibility of the applicant. CHIPS R&D may select some, all, or none of the applications, or part(s) of any application. The final approval of selected applications and issuance of awards will be by the NIST Agreements Officer. The award decisions of the NIST Agreements Officer are final and may not be appealed.

5.5.3.6 Federal Awarding Agency Review of Risk Posed by Applicants

To inform the review by the Selecting Official, NIST will also conduct the research security review described in Section 2.7.6 and the results will be provided to the Selecting Official. Applicants with proposals that have been assessed as having medium or high risk may be given an opportunity to mitigate the risk, as described in Section 2.7.8.

After applications are proposed for funding by the Selecting Official, the NIST Financial Assistance Agreements Management Office (FAAMO) performs pre-award risk assessments, which may include a review of the financial stability of an applicant, the quality of the

applicant's management systems, the history of performance, and/or the applicant's ability to effectively implement statutory, regulatory, or other requirements imposed on award recipients.

In addition, prior to making an award where the total Federal share is expected to exceed the simplified acquisition threshold (currently $250,000), NIST FAAMO will review and consider the publicly available Responsibility/Qualification records about that applicant available in SAM.gov (formerly available via the Federal Awardee Performance and Integrity Information System (FAPIIS)). An applicant may, at its discretion, review and comment on information about itself previously entered into SAM.gov by a Federal awarding agency. As part of its review of risk posed by applicants, NIST FAAMO will consider any comments made by the applicant in SAM.gov in making its determination about the applicant's integrity, business ethics, and record of performance under Federal awards. Upon completion of the pre-award risk assessment, the NIST Agreements Officer will make a responsibility determination concerning whether the applicant is qualified to receive the subject award and, if so, whether appropriate specific conditions that correspond to the degree of risk posed by the applicant should be applied to an award.

5.6 ADDITIONAL INFORMATION

5.6.1 Safety

Safety is a top priority at NIST. Employees and affiliates of award recipients who conduct project work at NIST will be expected to be safety-conscious, to attend NIST safety training, and to comply with all NIST safety policies and procedures and all applicable terms of their guest research agreement.

5.6.2 Notification to Unsuccessful Applicants

Unsuccessful applicants will be notified by e-mail and will have the opportunity to receive a debriefing after the funding opportunity has officially closed. Applicants must request, within 10 business days of the email notification, a debriefing from CHIPS R&D. CHIPS R&D will then work with the applicant in arranging a date and time for the debriefing.

5.6.3 Retention of Unsuccessful Applications

Unsuccessful applications will be retained in accordance with the General Record Schedule 1.2/021.

6 Federal Award Administration Information

6.1 FEDERAL AWARD NOTICES

Successful applicants will receive an award package electronically from the NIST Agreements Officer.

6.2 ADMINISTRATIVE AND NATIONAL POLICY REQUIREMENTS

6.2.1 Terms and Conditions

The complete terms and conditions of each award will be contained in the award package signed by the NIST Agreements Officer.

6.2.1.1 NIST/CHIPS R&D Discretion

Awards in this program require significant ongoing involvement from CHIPS R&D staff and provides NIST the flexibility to alter the course of the project in real-time to meet the overarching goals. This will generally include collaboration with the recipient organization in developing and implementing the approved scope of work.

6.2.1.2 Management Systems and Procedures

Recipient organizations are expected to have systems, policies, and procedures in place by which they manage funds and activities. Recipients may use their existing systems to manage Federal award funds and activities as long as they are consistently applied regardless of the source of funds and across their business functions. To ensure that an organization is committed to compliance, recipient organizations are expected to have in place written policies and procedures that provide for: clearly delineated roles and responsibilities for their organization's staff, both programmatic and administrative; training; management controls and other internal controls; performance assessment; administrative simplifications; and information sharing.

6.2.1.3 Financial Management System Standards

Recipients must have in place accounting and internal control systems that provide for appropriate monitoring of other transaction accounts to ensure that obligations and expenditures are congruent with programmatic needs and are reasonable, allocable, and allowable. In addition, the systems must be able to identify unobligated balances, accelerated expenditures, inappropriate cost transfers, and other inappropriate obligation and expenditure of funds, and recipients must notify CHIPS R&D when problems are identified. A recipient's failure to establish adequate control systems constitutes a material violation of the terms of the award.

6.2.2 Funding Availability and Limitation of Liability

Funding for the program listed in this NOFO is contingent upon the availability of appropriations. The U.S. Department of Commerce or NIST will not be responsible for application preparation costs, including but not limited to if this program fails to receive funding or is cancelled because of agency priorities. Publication of this NOFO does not oblige the U.S. Department of Commerce or NIST to award any specific project or to obligate any available funds.

As specified in Section 2.2 of this NOFO, when a proposal for a multi-year award is approved, funding will be provided for only the first phase of the project and incrementally thereafter. If a

project is selected for funding, NIST has no obligation to provide any additional funding in connection with that award. Continued funding of an award will be contingent upon factors including, but not necessarily limited to, satisfactory performance and the availability of funds.

6.2.3 Collaborations with CHIPS R&D and Other Federal Agencies

CHIPS R&D employees may not participate in the preparation of any application in response to this funding opportunity. After award, the team is expected to interact with CHIPS R&D and with Federal government organizations and FFRDCs as appropriate and consistent with their respective missions, objectives, and operational structures.

The award recipient is encouraged to collaborate with Federal entities to support the program goals and to ensure that the Federal investment in this team can be leveraged to the extent appropriate for national priorities.

If an applicant proposes collaboration with NIST, the statement of work should include a statement of this intention, a description of the collaboration, and prominently identify the NIST employee(s) involved, if known. Any collaboration by a NIST employee must be approved by appropriate NIST management and is at the sole discretion of NIST. Prior to beginning the merit review process, NIST will verify the approval of the proposed collaboration. Any unapproved collaboration will be stricken from the application prior to the merit review. Any collaboration with an identified NIST employee that is approved by appropriate NIST management will not make an application more or less favorable in the competitive process.

6.2.4 Use of Federal Government-Owned Intellectual Property

If the applicant anticipates using any Federal government-owned intellectual property in the custody of CHIPS R&D or another Federal agency to carry out the work proposed, the applicant should clearly identify such intellectual property in its proposal. This information will be used to ensure that no Federal employee involved in the development of the intellectual property will participate in the review process for that competition. In addition, if the applicant intends to use the Federal Government-owned intellectual property, the applicant must comply with all statutes and regulations governing the licensing of Federal government patents and inventions, described in 35 U.S.C. § 200-212, 37 C.F.R. Part 401, 2 C.F.R. § 200.315. Questions about these requirements may be directed to the Chief Counsel for NIST at (301) 975-2803 and via e-mail at nistcounsel@nist.gov.

Any use of Federal government-owned intellectual property by a recipient of an award under this announcement is at the sole discretion of the Federal government and will need to be negotiated on a case-by-case basis by the recipient and the Federal agency having custody of the intellectual property if a project is deemed meritorious. The applicant should indicate within the statement of work whether it already has a license to use such intellectual property or whether it intends to seek a license from the applicable Federal agency.

If any inventions made in whole or in part by a NIST employee arise in the course of an award made pursuant to this NOFO, the United States Government may retain its ownership rights in any such invention.

Licensing or other disposition of the Federal government's rights in such inventions will be determined solely by the Federal government, through CHIPS R&D as custodian of such inventions and include the possibility of the Federal government putting the intellectual property into the public domain.

6.2.5 Export Controls

Some activities may require access to export-controlled items and therefore be subject to export control laws and regulations. If an applicant is selected for award, the applicant and all subrecipients agree to comply with United States export laws and regulations, including, but not limited to, the International Traffic in Arms Regulations and the U.S. Department of Commerce Export Administration Regulations. Under no circumstances may foreign entities (organizations, companies, or persons) obtain access to export-controlled items unless proper procedures have been satisfied and such access is authorized pursuant to law or regulation. If involvement of foreign entities is approved by CHIPS R&D under Section 6.2.4, recipients must develop measures to properly protect export-controlled information, as appropriate. Approval of foreign entity involvement by CHIPS R&D does not constitute approval or waiver of any export licensing requirements that may apply.

Regarding any project-funded innovation (which may include software), recipients remain responsible for complying with all applicable laws, regulations, and policies governing intellectual property rights, licensing, and export control.

CHIPS R&D reserves the right to seek and consider additional information, including from applicants regarding their current compliance with export laws and regulations, or any pending investigations thereof, at any point in the selection process.

6.2.6 Post-Award Negotiation and Modification

Any changes or requirements that may arise during the period of performance regarding governance, scientific or programmatic matters, or reporting or legal requirements (within the scope of the award) may be negotiated between award recipients and NIST and resolved through an award modification as necessary.

6.3 REPORTING

6.3.1 Reporting Requirements

The following reporting requirements apply to awards made in this program:

6.3.1.1 Financial Reports

Each award recipient will be required to submit financial reports. Financial reporting requirements will be outlined in the terms and conditions of award.

6.3.1.2 Research Performance Monitoring and Reporting

Award recipients will be required to submit quarterly progress reports within 30 days of the close of the reporting period. CHIPS R&D expects the recipient to include similar content to that requested in the Research Performance Progress Report (see 2 C.F.R. § 200.329). However, CHIPS R&D may approve the use of a different format at the request of the recipient. Detailed progress reporting requirements will be outlined in the terms of the award.

A final consolidated report must be submitted within 120 days after the expiration date of the award. The recipient is required to submit publication citation information, links to publicly available data, and other public outputs as soon as they become available.

In addition to the formal quarterly progress reports, the award recipient will be expected to meet quarterly with the Federal Program Officer to discuss operational, technical, and strategic plans. It is expected that the recipient will additionally establish regular and ongoing cadence of informal communication with the Federal program team to ensure timely awareness of issues and achievements.

The recipient is also expected to report progress against specific NIST-issued activity metrics at the end of each phase period and to contribute data for the NAPMP annual report on a Federal fiscal year basis. NIST will work with the recipient in the start-up phase of the award to implement activity metrics.

Information submitted in the course of applying for funding under this program or provided in the course of its grant management activities will be subject to analysis and evaluation for official Government or statistical purposes, including but not limited to assessing performance and evaluating program outcomes.

6.3.1.3 Patent and Property Reports

In accordance with the terms and conditions governing the award, the recipient may need to submit property and patent reports. The award recipient is required to notify CHIPS R&D of any patents or other intellectual property issuing from work performed within this award. CHIPS R&D requires periodic reporting on the utilization or efforts at obtaining utilization that are being made by the recipient or its licensees or assignees, provided that any such information as well as any information on utilization or efforts at obtaining utilization shall be treated by the Federal agency as commercial and financial information obtained from a person and privileged, confidential, and not subject to disclosure.

6.3.1.4 Recipient Integrity and Performance Matters

In accordance with section 872 of Public Law 110-417 (as amended; see 41 U.S.C. § 2313), if the total value of a recipient's currently active grants, cooperative agreements, and procurement

contracts from all Federal awarding agencies exceeds $10,000,000 for any period of time during the period of performance of an award made under this NOFO, then the recipient shall be subject to maintaining the currency of information reported to SAM that is made available in FAPIIS about certain civil, criminal, or administrative proceedings involving the recipient.

6.3.2 Audit Requirements

Any recipient that expends Federal awards of $1,000,000 or more in the recipient's fiscal year must conduct a single or program specific audit similar to the requirements set out in the 2 C.F.R. Part 200, Subpart F. Additionally, unless otherwise specified in the terms and conditions of the award, entities that are not subject to Subpart F of 2 C.F.R. Part 200 (e.g., for-profit commercial entities) that expend $1,000,000 or more in DOC funds during their fiscal year must submit to the assigned NIST Agreements Officer either (1) a financial related audit of each DOC award or subaward in accordance with Generally Accepted Government Auditing Standards or (2) a project specific audit for each award or subaward with similar content to that requested in 2 C.F.R. § 200.507. Applicants are reminded that CHIPS R&D, the U.S. Department of Commerce Office of Inspector General, or another authorized Federal agency may conduct an audit of an award at any time.

6.3.3 Federal Funding and Accountability Transparency Act of 2006

In accordance with 2 C.F.R. Part 170, all recipients of a Federal award made on or after October 1, 2010, are required to comply with reporting requirements under the Federal Funding Accountability and Transparency Act of 2006 (Public Law No. 109-282). In general, all recipients are responsible for reporting sub-awards of $25,000 or more. In addition, recipients that meet certain criteria are responsible for reporting executive compensation. Applicants must ensure they have the necessary processes and systems in place to comply with the reporting requirements should they receive funding. Also see the Federal Register Notice published September 14, 2010, at 75 FR 55663.

7 AGENCY CONTACTS

Applicants must submit all questions pertaining to this funding opportunity in writing to the following:

Subject Area	Point of Contact
Programmatic and Technical Questions	E-mail: research@chips.gov with "2025-NIST-CHIPS-NAPMP-01 Questions" in the subject line
Technical Assistance with Grants.gov Submissions	www.grants.gov Phone: 800-518-4726 E-mail: support@grants.gov
Award Management Inquiries	Lisa Ko

Subject Area	Point of Contact
	E-mail: NOFO@nist.gov with "2025-NIST-CHIPS-NAPMP-01 Questions" in the subject line

8 OTHER INFORMATION

8.1 PERSONAL AND BUSINESS INFORMATION

The applicant acknowledges and understands that information and data contained in applications for other transactions, as well as information and data contained in financial, performance and other reports submitted by applicants, may be used by CHIPS R&D in conducting reviews and evaluations of its financial assistance programs. For this purpose, applicant information and data may be accessed, reviewed, and evaluated by U.S. Department of Commerce employees, other Federal employees, and also by Federal agents and contractors, and/or by non-Federal personnel, who enter into conflict of interest and confidentiality agreements covering the use of such information as appropriate. As may be provided in the terms and conditions of a specific other transaction award, applicants are expected to support program reviews and evaluations by submitting required financial and performance information and data in an accurate and timely manner, and by cooperating with U.S. Department of Commerce and external program evaluators. Applicants must safeguard protected personally identifiable information and other confidential or sensitive personal or business information created or obtained in connection with a U.S. Department of Commerce financial assistance award consistent with information security requirements under applicable standards, this NOFO, and the terms of the award agreement.

In addition, U.S. Department of Commerce regulations implementing the Freedom of Information Act (FOIA), 5 U.S.C. § 552, are found at 15 C.F.R. Part 4, Disclosure of Government Information. These regulations set forth rules for the U.S. Department of Commerce regarding making requested materials, information, and records publicly available under the FOIA. Applications submitted in response to this Federal Funding Opportunity may be subject to requests for release under the FOIA. If an application contains information or data that the applicant deems to be confidential commercial information that should be exempt from disclosure under FOIA, that information should be marked as "Proprietary," "Sensitive Business Information," or similar markings as specified in Section 4.2 of this NOFO. In accordance with 15 C.F.R. § 4.9, CHIPS R&D and the U.S. Department of Commerce will protect from disclosure confidential business information contained in other transaction applications and other documentation provided by applicants to the extent permitted by law.

8.2 PUBLIC WEBSITE

CHIPS R&D has a public website that includes a Frequently Asked Questions page and other information pertaining to this funding opportunity. Any amendments to this NOFO will be announced through Grants.gov.

Applicants must submit all questions pertaining to this funding opportunity in writing to research@chips.gov with "2025-NIST-CHIPS-NAPMP-01 Questions" in the subject line.

8.3 ATTACHMENT A – ASSOCIATE RECIPIENT AGREEMENTS

It is recognized that the success of the NAPMP research effort depends in part upon the open exchange of information between the various recipients involved in the effort. Therefore, any resultant award instrument stemming from this Notice of Funding Opportunity will include a term/condition classifying recipients as "Associate Recipients" and requiring them to enter into an Associate Recipient Agreement with all other NAPMP recipients, with each recipient then assuming the responsibilities of an Associate Recipient. The paragraphs below outline the general verbiage pertaining to Associate Recipient Agreements applicants can expect in a resultant NAPMP award. All terms of Associate Recipient Agreements must be consistent with the terms of this NOFO and of each award agreement.

(a) Work under this agreement may involve access to proprietary or confidential data from an Associate Recipient. To the extent that such data is received by the Recipient from any Associate Recipient for the performance of this agreement, the Recipient hereby agrees that any proprietary information received shall remain the property of the Associate Recipient and shall be used solely for the purpose of the NAPMP research effort. Only that information which is received from another recipient in writing and which is clearly identified as proprietary or confidential shall be protected in accordance with this requirement. The obligation to retain such information in confidence will be satisfied if the Recipient receiving such information utilizes the same controls as it employs to avoid disclosure, publication, or dissemination of its own proprietary information. The receiving Recipient agrees to hold such information in confidence as provided herein so long as such information is of a proprietary/confidential or limited rights nature.

(b) The Recipient hereby agrees to closely cooperate as an Associate Recipient with the other Associate Recipients on this research effort. This involves as a minimum:

(1) maintenance of a close liaison and working relationship;

(2) maintenance of free and open information exchange with all Government-identified Associate Recipients;

(3) delineation of detailed interface responsibilities;

(4) entering into a written agreement with the other Associate Recipients setting forth the substance and procedures relating to the foregoing, and promptly providing the NIST Agreements Officer with a copy of same; and,

(5) receipt of proprietary information from the Associate Recipient and transmittal of Recipient proprietary information to the Associate Recipients subject to any applicable proprietary information exchange agreements between associate recipient when, in either case, those actions are necessary for the performance of either.

(c) In the event that the Recipient and the Associate Recipient are unable to agree upon any such interface matter of substance, or if the technical data identified is not provided as scheduled, the

Recipient must promptly notify the CHIPS Research and Development Office. NIST will determine the appropriate corrective action and will issue guidance to the affected Recipient.

(d) The Recipient agrees to insert in all subawards which require access to proprietary information belonging to the Associate Recipient, a requirement which shall conform substantially to the language of this requirement, including this paragraph (d).

(e) Associate Recipients for this research effort include:

Recipient	R&D Area